INTEGRATED CIRCUITS

DATA SHEET

74LVC08AQuad 2-input AND gate

Product specification IC24 Data Handbook

1997 Jun 30





Quad 2-input AND gate

74LVC08A

FEATURES

- Wide supply voltage range of 1.2 V to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels

DESCRIPTION

The 74LVC08A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V

The 74LVC08A provides the 2-input AND function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; t_{f} = t_{f} \leq 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t _{PHL} /t _{PLH}	Propagation delay nA, nB to nY	$C_L = 50 \text{ pF};$ $V_{CC} = 3.3 \text{ V}$	2.6	ns
C _I	Input capacitance		5.0	pF
C _{PD}	Power dissipation capacitance per gate	Notes 1 and 2	28	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation $(P_D \text{ in } \mu W)$

 $P_D = C_{PD} \times V_{CC}{}^2 \times f_i + \sum{(C_L \times V_{CC}{}^2 \times f_o)}$ where:

 f_i = input frequency in MHz; C_L = output load capacity in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V;

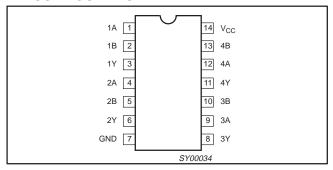
 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of the outputs.}$

2. The condition is $V_I = GND$ to V_{CC} .

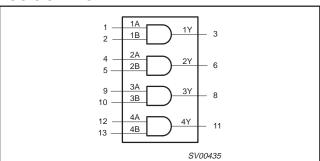
ORDERING INFORMATION

<u> </u>				
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	-40°C to +85°C	74LVC08A D	74LVC08A D	SOT108-1
14-Pin Plastic SSOP Type II	-40°C to +85°C	74LVC08A DB	74LVC08A DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40°C to +85°C	74LVC08A PW	74LVC08APW DH	SOT402-1

PIN CONFIGURATION



LOGIC SYMBOL



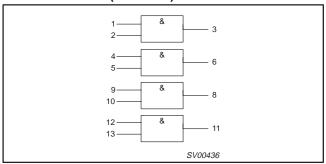
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A – 4A	Data inputa
2, 5, 10, 13	1B – 4B	Data inputs
3, 6, 8, 11	1Y – 4Y	Data outputs
7	GND	Ground (0 V)
14	V _{CC}	Positive supply voltage

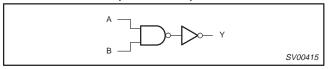
Quad 2-input AND gate

74LVC08A

LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (ONE GATE)



FUNCTION TABLE

INP	OUTPUTS	
nA	nB	nY
L	L	L
L	Н	L
Н	L	L
Н	Н	Н

NOTES:

H = HIGH voltage level L = LOW voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIM	UNIT	
STWIBOL	PARAMETER	CONDITIONS	MIN	MAX	UNII
V _{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V _{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
VI	DC input voltage range		0	5.5	V
V _O	DC output voltage range; output HIGH or LOW state		0	V _{CC}	V
T _{amb}	Operating ambient temperature range in free-air		-40	+85	°C
t _r , t _f	Input rise and fall times	$V_{CC} = 1.2 \text{ to } 2.7V$ $V_{CC} = 2.7 \text{ to } 3.6V$	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
Vcc	DC supply voltage		-0.5 to +6.5	V
I _{IK}	DC input diode current	$V_I < 0$	-50	mA
VI	DC input voltage	Note 2	-0.5 to +6.5	V
I _{OK}	DC output diode current	$V_{O} > V_{CC}$ or $V_{O} < 0$	±50	mA
Vo	DC output voltage; output HIGH or LOW state	Note 2	-0.5 to V _{CC} +0.5	V
I _O	DC output source or sink current	$V_O = 0$ to V_{CC}	±50	mA
I _{GND} , I _{CC}	DC V _{CC} or GND current		±100	mA
T _{stg}	Storage temperature range		-65 to +150	°C
P _{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the
 device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to
 absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

1997 Jun 30

Quad 2-input AND gate

74LVC08A

DC CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

			L	LIMITS					
SYMBOL	PARAMETER	TEST CONDITIONS	Temp = -	40°C to	+85°C	UNIT			
			MIN	TYP ¹	MAX				
V	HICH level Input veltage	V _{CC} = 1.2V	V _{CC}			V			
V _{IH}	HIGH level Input voltage	V _{CC} = 2.7 to 3.6V	2.0]			
	LOW lovel Input voltage	V _{CC} = 1.2V			GND	\ \			
V _{IL}	LOW level Input voltage	V _{CC} = 2.7 to 3.6V			0.8	1 °			
		$V_{CC} = 2.7V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = -12mA$	V _{CC} -0.5						
	LUCLUS STATE AND ASSESSED TO	$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = -100\mu A$	V _{CC} -0.2	V _{CC}					
V _{OH}	HIGH level output voltage	$V_{CC} = 3.0V; V_I = V_{IH} \text{ or } V_{IL;} I_O = -18\text{mA}$	V _{CC} -0.6			1 °			
		$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = -24$ mA	V _{CC} -0.8			1			
		$V_{CC} = 2.7V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = 12mA$			0.40				
V _{OL}	LOW level output voltage	$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = 100\mu A$			0.20	V			
		$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = 24mA$			0.55	1			
I _I	Input leakage current	V _{CC} = 3.6V; V _I = 5.5V or GND		±0.1	±5	μΑ			
I _{CC}	Quiescent supply current	$V_{CC} = 3.6V; V_I = V_{CC} \text{ or GND}; I_O = 0$		0.1	10	μΑ			
Δl _{CC}	Additional quiescent supply current per input pin	$V_{CC} = 2.7 \text{V to } 3.6 \text{V}; V_{I} = V_{CC} - 0.6 \text{V}; I_{O} = 0$		5	500	μА			

NOTE:

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \le 2.5 \text{ ns}$; $C_L = 50 \text{ pF}$

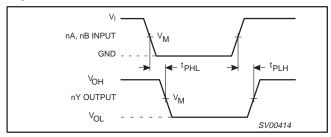
				LIMITS							
SYMBOL	PARAMETER	WAVEFORM	VEFORM V _{CC} =		$V_{CC} = 3.3V \pm 0.3V$			′	V _{CC} = 1.2V	UNIT	
			MIN	TYP ¹	MAX	MIN	TYP	MAX	TYP		
t _{PHL} /	Propagation delay nA, nB to nY	1, 2	1.5	2.6	5.1	1.5	3.0	6.1	16	ns	

NOTE:

AC WAVEFORMS

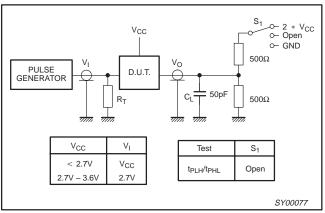
 V_M = 1.5 V at $V_{CC} \ge 2.7$ V V_M = 0.5 • V_{CC} at $V_{CC} < 2.7$ V

 $V_{\mbox{\scriptsize OL}}$ and $V_{\mbox{\scriptsize OH}}$ are the typical output voltage drop that occur with the output load.



Waveform 1. Input (nA, nB) to output (nY) propagation delays.

TEST CIRCUIT



Waveform 2. Load circuitry for switching times.

1997 Jun 30

^{1.} All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

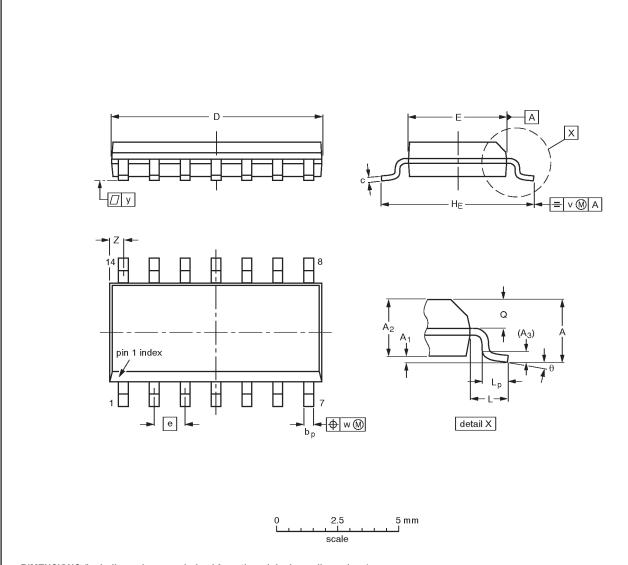
^{1.} These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

Quad 2-input AND gate

74LVC08A

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	Α1	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Ø	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01		0.0098 0.0075	0.35 0.34	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016		0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE			EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE	
SOT108-1	076E06\$	MS-012AB				91-08-13 95-01-23

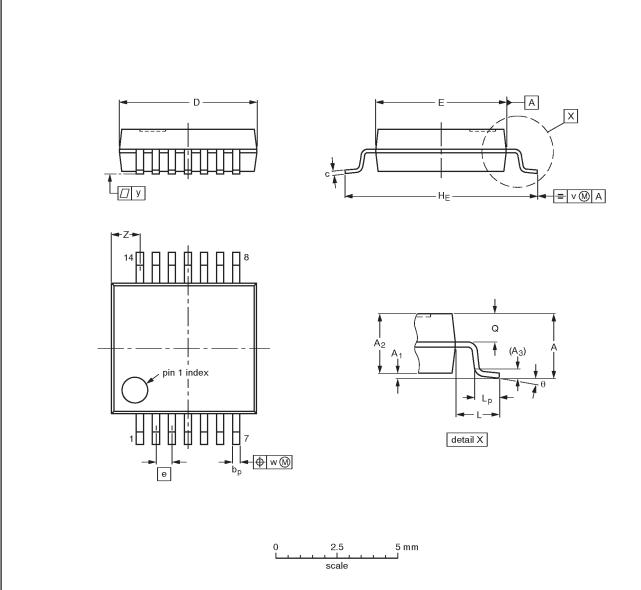
1997 Jun 30 5

Quad 2-input AND gate

74LVC08A

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	bp	c	D ⁽¹⁾	E ⁽¹⁾	e	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT337-1		MO-150AB				-95-02-04 96-01-18	

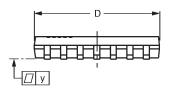
1997 Jun 30 6

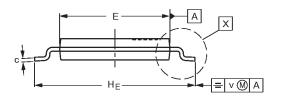
Quad 2-input AND gate

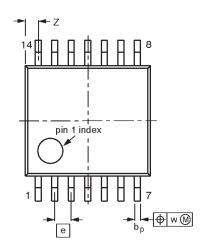
74LVC08A

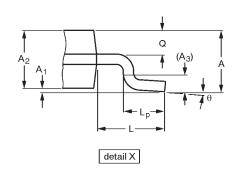
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

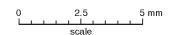
SOT402-1











DIMENSIONS (mm are the original dimensions)

UNIT	A max.	Α1	A ₂	A ₃	bр	c	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	1550E DATE	
SOT402-1		MO-153				94-07-12 95-04-04	

1997 Jun 30 7

Quad 2-input AND gate

74LVC08A

DEFINITIONS							
Data Sheet Identification	Product Status	Definition					
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.					
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.					
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.					

Philips Semiconductors and Philips Electronics North America Corporation reserve the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

LIFE SUPPORT APPLICATIONS

Philips Semiconductors and Philips Electronics North America Corporation Products are not designed for use in life support appliances, devices, or systems where malfunction of a Philips Semiconductors and Philips Electronics North America Corporation Product can reasonably be expected to result in a personal injury. Philips Semiconductors and Philips Electronics North America Corporation customers using or selling Philips Semiconductors and Philips Electronics North America Corporation Products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors and Philips Electronics North America Corporation for any damages resulting from such improper use or sale.

Philips Semiconductors 811 East Arques Avenue P.O. Box 3409 Sunnyvale, California 94088–3409 Telephone 800-234-7381 © Copyright Philips Electronics North America Corporation 1997 All rights reserved. Printed in U.S.A.

print code Date of release: 05-96

Document order number: 9397-750-04481

Let's make things better.

Philips Semiconductors



