

DATA SHEET

74LVC126A

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

Product specification
Supersedes data of 2002 Mar 8

2003 Feb 28

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC126A

FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard no. 8-1A
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from -40 to $+85$ °C and -40 to $+125$ °C.

DESCRIPTION

The 74LVC126A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V.

The 74LVC126A consists of four non-inverting buffers/line drivers with 3-state outputs (nY) which are controlled by the output enable input (nOE). A LOW at nOE causes the outputs to assume a high-impedance OFF-state.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nA to nY	$C_L = 50$ pF; $V_{CC} = 3.3$ V	2.4	ns
C_I	input capacitance		4.0	pF
C_{PD}	power dissipation capacitance per gate	$V_{CC} = 3.3$ V; notes 1 and 2	12	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2. The condition is $V_I = \text{GND to } V_{CC}$.

ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74LVC126AD	-40 to $+125$ °C	14	SO14	plastic	SOT108-1
74LVC126ADB	-40 to $+125$ °C	14	SSOP14	plastic	SOT337-1
74LVC126APW	-40 to $+125$ °C	14	TSSOP14	plastic	SOT402-1
74LVC126ABQ	-40 to $+125$ °C	14	DHVQFN14	plastic	SOT762-1

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC126A

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

Note

1. H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

PINNING

PIN	SYMBOL	DESCRIPTION
1	1OE	data enable input (active HIGH)
2	1A	data input
3	1Y	data output
4	2OE	data enable input (active HIGH)
5	2A	data input
6	2Y	data output
7	GND	ground (0 V)
8	3Y	data output
9	3A	data input
10	3OE	data enable input (active HIGH)
11	4Y	data output
12	4A	data input
13	4OE	data enable input (active HIGH)
14	V _{CC}	supply voltage

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC126A

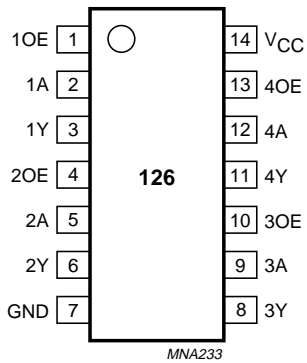
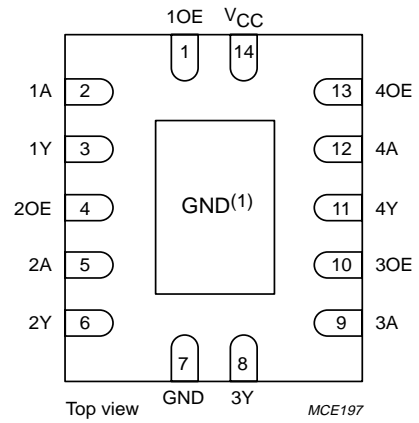


Fig.1 Pin configuration SO14 and (T)SSOP14.



* The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

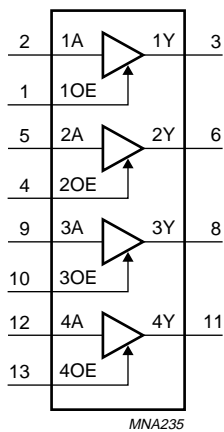


Fig.3 Logic symbol.

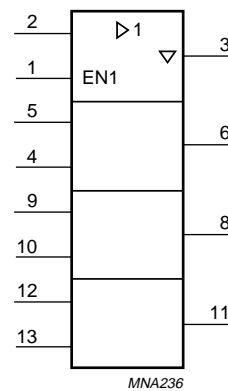


Fig.4 Logic symbol (IEEE/IEC).

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC126A

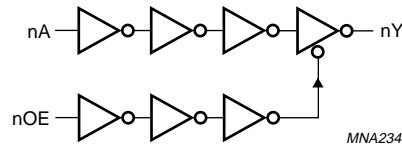


Fig.5 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	5.5	V
T_{amb}	operating ambient temperature		-40	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 1.2$ to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$	-	-50	mA
V_I	input voltage	note 1	-0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
V_O	output voltage	output HIGH or LOW state; note 1	-0.5	$V_{CC} + 0.5$	V
		output 3-state; note 1	-0.5	+6.5	V
I_O	output source or sink current	$V_O = 0$ to V_{CC}	-	±50	mA
I_{GND}, I_{CC}	V_{CC} or GND current		-	±100	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	power dissipation per package	$T_{amb} = -40$ to $+125$ °C; note 2	-	500	mW

Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For (T)SSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC126A

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +85 °C							
V _{IH}	HIGH-level input voltage		1.2	V _{CC}	-	-	V
			2.7 to 3.6	2.0	-	-	V
V _{IL}	LOW-level input voltage		1.2	-	-	GND	V
			2.7 to 3.6	-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -100 μA	2.7 to 3.6	V _{CC} - 0.2	V _{CC}	-	V
		I _O = -12 mA	2.7	V _{CC} - 0.5	-	-	V
		I _O = -18 mA	3.0	V _{CC} - 0.6	-	-	V
		I _O = -24 mA	3.0	V _{CC} - 0.8	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 μA	2.7 to 3.6	-	GND	0.2	V
		I _O = 12 mA	2.7	-	-	0.4	V
		I _O = 24 mA	3.0	-	-	0.55	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	3.6	-	±0.1	±5	μA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; note 2	3.6	-	±0.1	±5	μA
I _{off}	power off leakage supply	V _I or V _O = 5.5 V	0	-	±0.1	±10	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	3.6	-	0.1	10	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} - 0.6 V; I _O = 0	2.7 to 3.6	-	5	500	μA

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC126A

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +125 °C							
V _{IH}	HIGH-level input voltage		1.2	V _{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V _{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -100 µA	2.7 to 3.6	V _{CC} - 0.3	–	–	V
		I _O = -12 mA	2.7	V _{CC} - 0.65	–	–	V
		I _O = -18 mA	3.0	V _{CC} - 0.75	–	–	V
		I _O = -24 mA	3.0	V _{CC} - 1	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 µA	2.7 to 3.6	–	–	0.3	V
		I _O = 12 mA	2.7	–	–	0.6	V
		I _O = 24 mA	3.0	–	–	0.8	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	3.6	–	–	±20	µA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND; note 2	3.6	–	–	±20	µA
I _{off}	power off leakage supply	V _I or V _O = 5.5 V	0.0	–	–	±20	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	3.6	–	–	40	µA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} - 0.6 V; I _O = 0	2.7 to 3.6	–	–	5000	µA

Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. For I/O ports the parameter I_{OZ} includes the input leakage current.

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC126A

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 to +85 °C							
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 6 and 8	1.2	–	11	–	ns
			2.7	1.5	2.7	5.2	ns
			3.0 to 3.6	1.0	2.4 ⁽²⁾	4.7	ns
t _{PZH} /t _{PZL}	3-state output enable time nOE to nY	see Figs 7 and 8	1.2	–	15	–	ns
			2.7	1.5	3.1	6.3	ns
			3.0 to 3.6	1.0	2.9 ⁽²⁾	5.7	ns
t _{PHZ} /t _{PLZ}	3-state output disable time nOE to nY	see Figs 7 and 8	1.2	–	8.0	–	ns
			2.7	1.5	3.8	6.7	ns
			3.0 to 3.6	1.3	2.8 ⁽²⁾	6.0	ns
t _{sk(0)}	skew	note 3	3.0 to 3.6	–	–	1.0	ns
T_{amb} = -40 to +125 °C							
t _{PHL} /t _{PLH}	propagation delay nA to nY	see Figs 6 and 8	1.2	–	–	–	ns
			2.7	1.5	–	6.5	ns
			3.0 to 3.6	1.0	–	6.0	ns
t _{PZH} /t _{PZL}	3-state output enable time nOE to nY	see Figs 7 and 8	1.2	–	–	–	ns
			2.7	1.5	–	8.0	ns
			3.0 to 3.6	1.0	–	7.5	ns
t _{PHZ} /t _{PLZ}	3-state output disable time nOE to nY	see Figs 7 and 8	1.2	–	–	–	ns
			2.7	1.5	–	8.5	ns
			3.0 to 3.6	1.3	–	7.5	ns
t _{sk(0)}	skew	note 3	3.0 to 3.6	–	–	1.5	ns

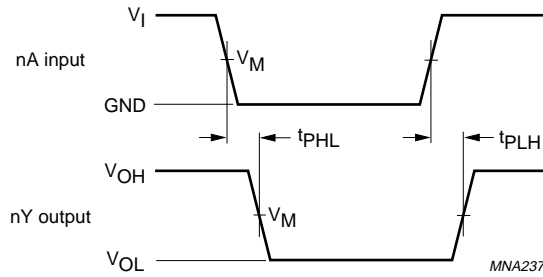
Notes

1. Typical values are measured at T_{amb} = 25 °C.
2. Typical values are measured at V_{CC} = 3.3 V.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

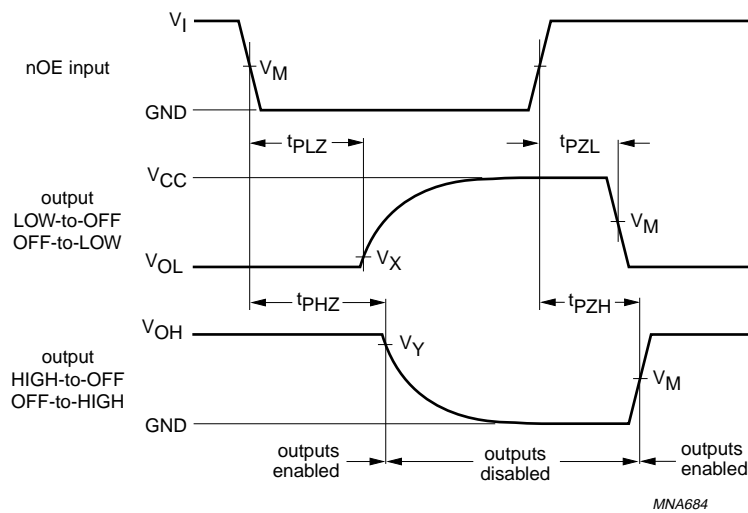
74LVC126A

AC WAVEFORMS



$V_M = 1.5\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$;
 $V_M = 0.5V_{CC}$ at $V_{CC} < 2.7\text{ V}$;
 V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 The input nA to output nY propagation delays.



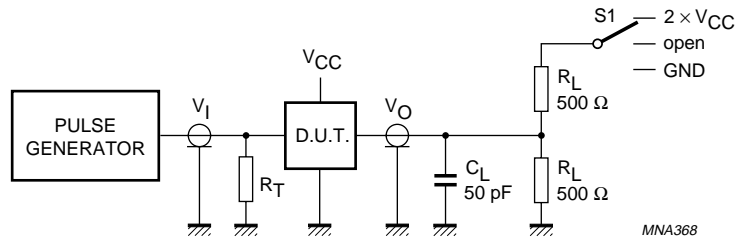
$V_M = 1.5\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$;
 $V_M = 0.5V_{CC}$ at $V_{CC} < 2.7\text{ V}$;
 $V_X = V_{OL} + 0.3\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$;
 $V_X = V_{OL} + 0.1\text{ V}$ at $V_{CC} < 2.7\text{ V}$;
 $V_Y = V_{OH} + 0.3\text{ V}$ at $V_{CC} \geq 2.7\text{ V}$;
 $V_Y = V_{OH} + 0.1\text{ V}$ at $V_{CC} < 2.7\text{ V}$.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 3-state enable and disable times.

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC126A



SWITCH POSITION	
TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
$< 2.7 V$	V_{CC}
2.7 to 3.6 V	2.7 V

Definitions for test circuits:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.8 Load circuitry for switching times.

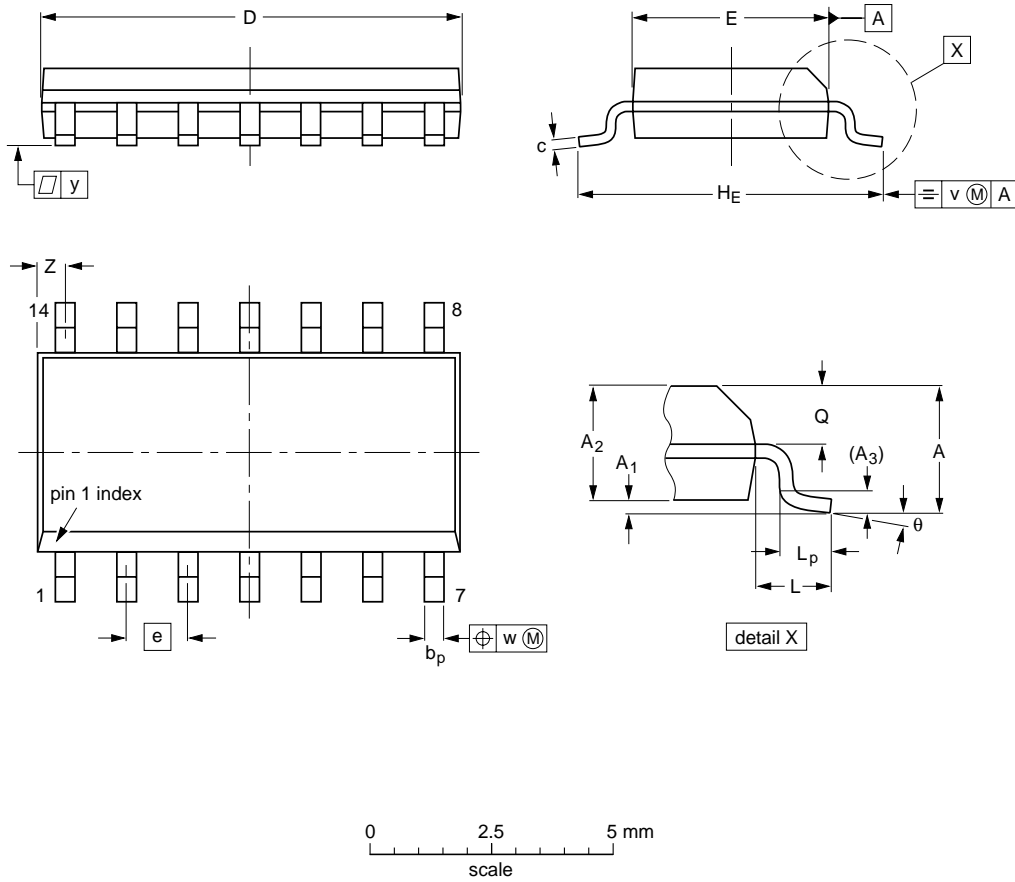
Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC126A

PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

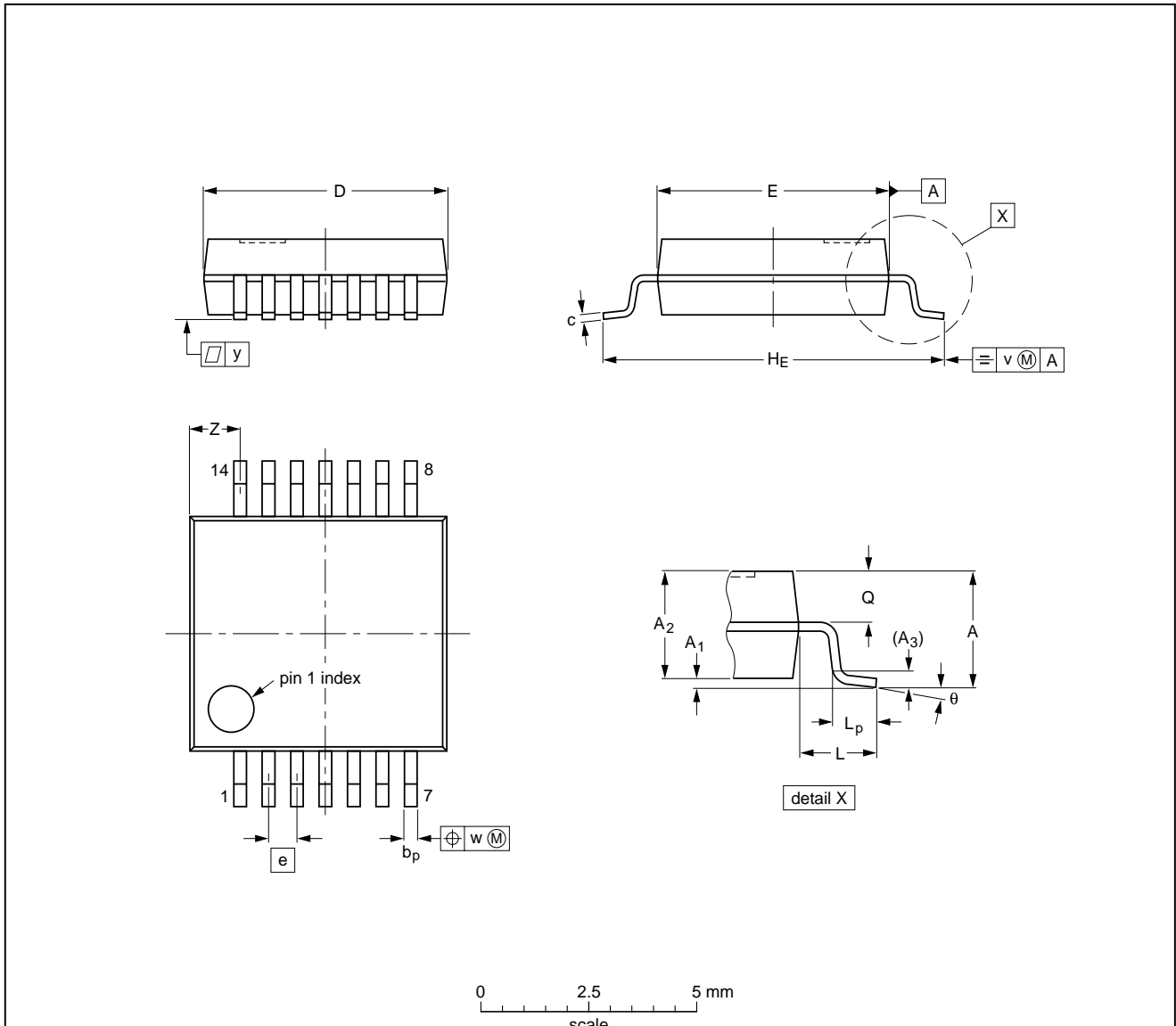
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				99-12-27 03-02-19

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC126A

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

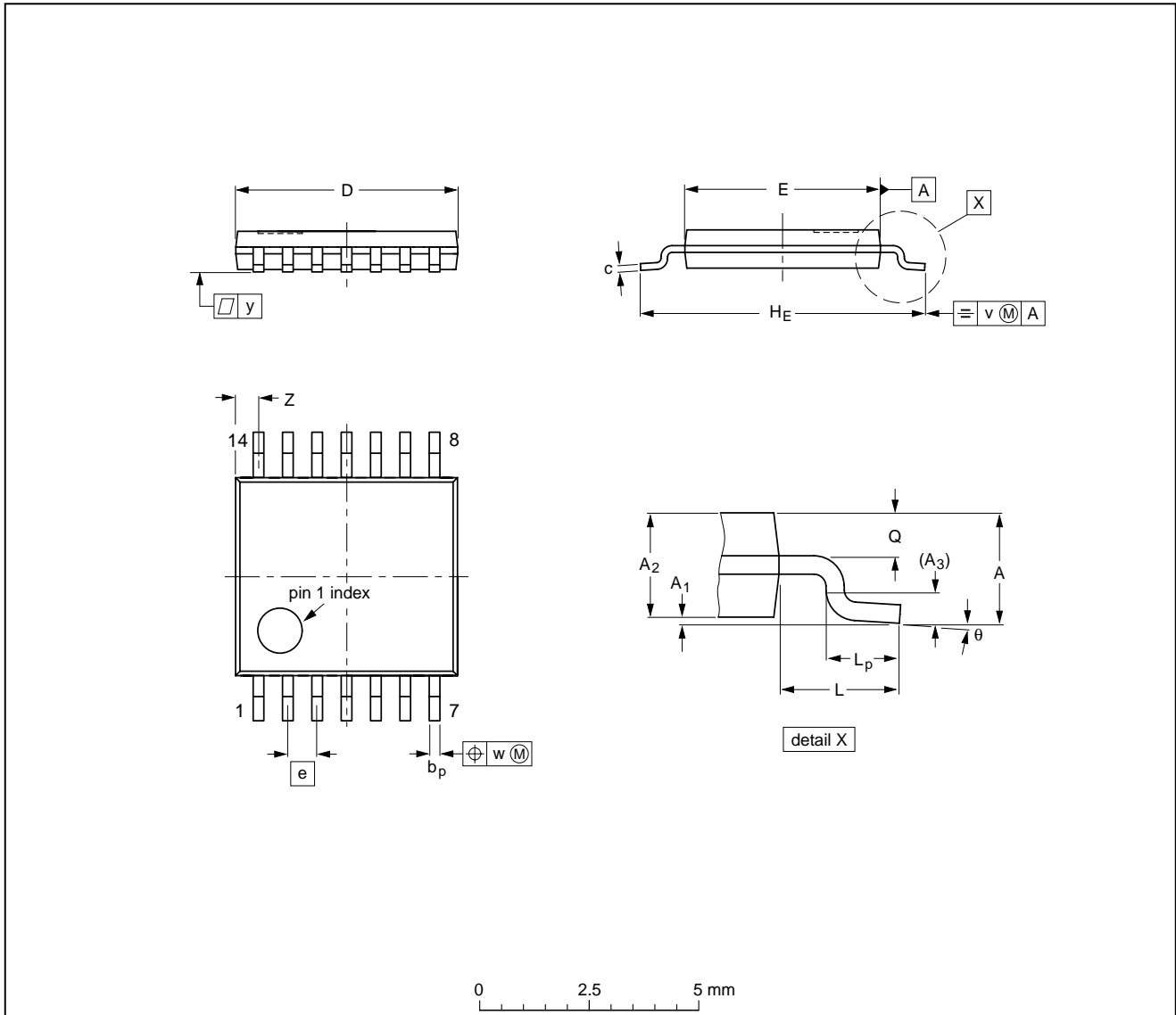
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				99-12-27 03-02-19

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC126A

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

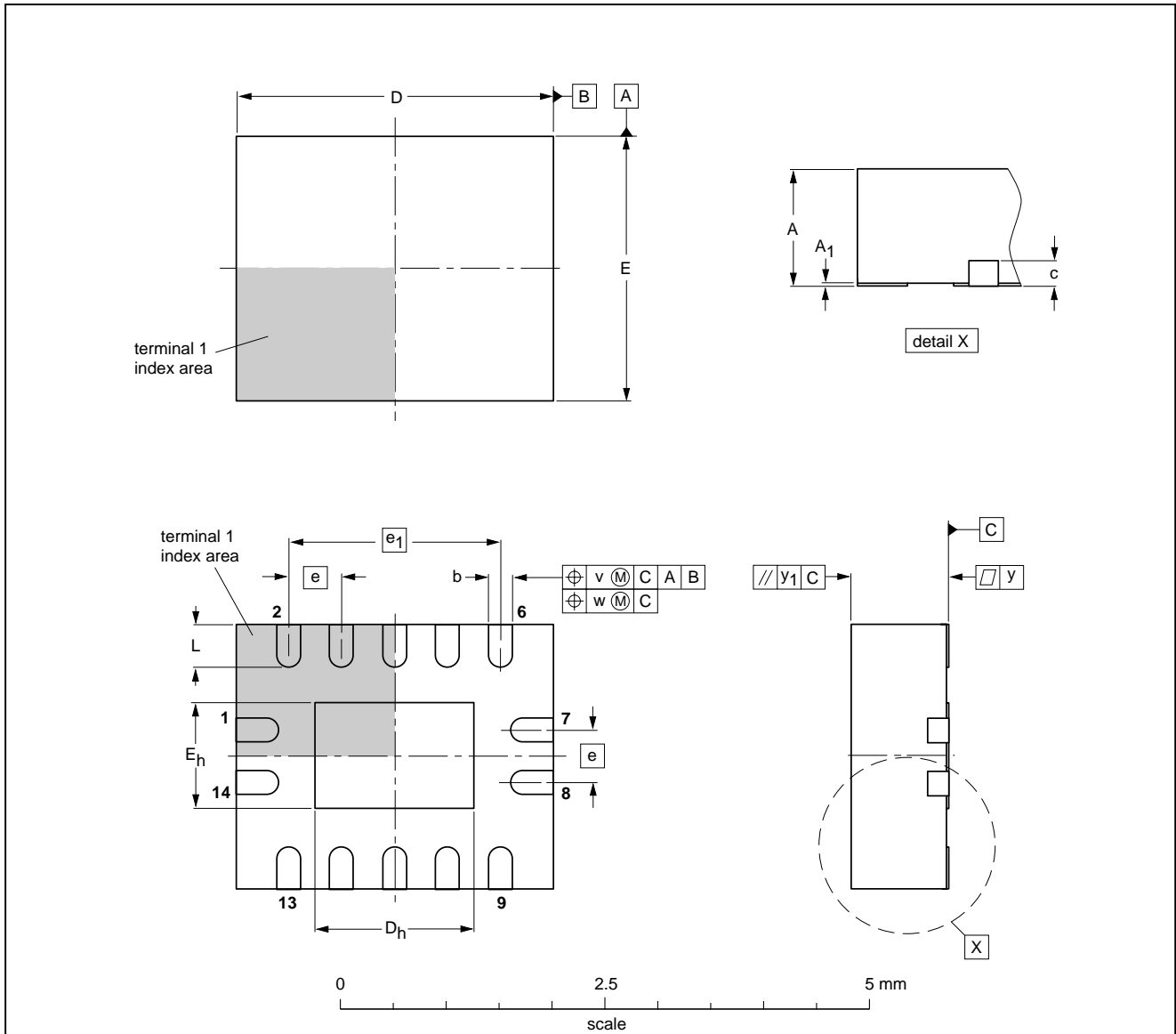
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				99-12-27 03-02-18

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC126A

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max.	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	L	v	w	y	y ₁
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	---	MO-241	---			02-10-17 03-01-27

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC126A

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept:

- below 220 °C for all the BGA packages and packages with a thickness ≥ 2.5 mm and packages with a thickness < 2.5 mm and a volume ≥ 350 mm³ so called thick/large packages
- below 235 °C for packages with a thickness < 2.5 mm and a volume < 350 mm³ so called small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC126A

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE ⁽¹⁾	SOLDERING METHOD	
	WAVE	REFLOW ⁽²⁾
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable ⁽³⁾	suitable
PLCC ⁽⁴⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽⁴⁾⁽⁵⁾	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended ⁽⁶⁾	suitable

Notes

- For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
- These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

Quad buffer/line driver with 5 Volt tolerant input/outputs; 3-state

74LVC126A

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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74LVC126A

NOTES

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