



## VND5025AK-E

### Double channel high side driver with analog current sense for automotive applications

#### Features

Max transient supply voltage	$V_{CC}$	41V
Operating voltage range	$V_{CC}$	4.5 to 36V
Max On-State resistance (per ch.)	$R_{ON}$	25 m $\Omega$
Current limitation (typ)	$I_{LIMH}$	41 A
Off state supply current	$I_S$	2 $\mu$ A <sup>(1)</sup>

1. Typical value with all loads connected

#### ■ Main

- In-rush current active management by power limitation
- Very low stand-by current
- 3.0V CMOS compatible input
- Optimized electromagnetic emission
- Very low electromagnetic susceptibility
- In compliance with the 2002/95/EC European directive
- Package: ECOPACK®

#### ■ Diagnostic functions

- Proportional load current sense
- High current sense precision for wide range currents
- Current sense disable
- Thermal shutdown indication
- Very low current sense leakage

#### ■ Protection

- Undervoltage shut-down
- Overvoltage clamp
- Load current limitation
- Self-limiting of fast thermal transients
- Protection against loss of ground and loss of  $V_{CC}$
- Thermal shut down
- Reverse battery protection
- Electrostatic discharge protection



#### Description

The VND5025AK-E is a monolithic device made using STMicroelectronics VIPower M0-5 technology, intended for driving resistive or inductive loads with one side connected to ground, and suitable for driving LEDs.

Active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS\_DIS is driven low or left open.

When CS\_DIS is driven high, the CURRENT SENSE pin is in a high impedance condition.

Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

**Table 1. Device summary**

Package	Tube	Tape and Reel
PowerSSO-24™	VND5025AK-E	VND5025AKTR-E

# Contents

<b>1</b>	<b>Block diagram and pin description</b> .....	<b>6</b>
<b>2</b>	<b>Electrical specification</b> .....	<b>8</b>
2.1	Absolute maximum ratings .....	8
2.2	Thermal data .....	9
2.3	Electrical characteristics .....	9
<b>3</b>	<b>Application information</b> .....	<b>23</b>
3.1	GND protection network against reverse battery .....	23
3.1.1	Solution 1: resistor in the ground line (RGND only) .....	23
3.1.2	Solution 2: diode (DGND) in the ground line .....	24
3.2	Load dump protection .....	24
3.3	$\mu$ C I/Os protection .....	24
3.4	Maximum demagnetization energy (VCC = 13.5V) .....	25
<b>4</b>	<b>Package and thermal data</b> .....	<b>26</b>
4.1	PowerSSO-24™ thermal data .....	26
<b>5</b>	<b>Package and packing information</b> .....	<b>29</b>
5.1	ECOPACK® packages .....	29
5.2	Package mechanical data .....	29
5.3	Packing information .....	31
<b>6</b>	<b>Revision history</b> .....	<b>32</b>

## List of tables

Table 1.	Device summary . . . . .	1
Table 2.	Pin functions . . . . .	6
Table 3.	Suggested connections for unused and N.C. pins . . . . .	7
Table 4.	Absolute maximum ratings . . . . .	8
Table 5.	Thermal data . . . . .	9
Table 6.	Power section . . . . .	9
Table 7.	Switching ( $V_{CC} = 13V$ ; $T_j = 25^{\circ}C$ ) . . . . .	10
Table 8.	Logic input . . . . .	11
Table 9.	Protection and diagnostics . . . . .	11
Table 10.	Current sense ( $8V < V_{CC} < 16V$ ) . . . . .	12
Table 11.	Truth table. . . . .	16
Table 12.	Electrical transient requirements . . . . .	18
Table 13.	Thermal parameters . . . . .	28
Table 14.	PowerSSO-24™ mechanical data . . . . .	29
Table 15.	Document revision history . . . . .	32

## List of figures

Figure 1.	Block diagram . . . . .	6
Figure 2.	Configuration diagram (top view) . . . . .	7
Figure 3.	Current and voltage conventions . . . . .	8
Figure 4.	Current sense delay characteristics . . . . .	13
Figure 5.	Delay response time between rising edge of output current and rising edge of current sense (CS enabled)14	
Figure 6.	IOUT/ISENSE vs IOUT (see <a href="#">Table 10</a> for details) . . . . .	15
Figure 7.	Maximum current sense ratio drift vs load current . . . . .	15
Figure 8.	Switching characteristics . . . . .	17
Figure 9.	Output voltage drop limitation . . . . .	17
Figure 10.	Waveforms . . . . .	19
Figure 11.	Off state output current . . . . .	20
Figure 12.	High level input current . . . . .	20
Figure 13.	Input clamp voltage . . . . .	20
Figure 14.	Input high level . . . . .	20
Figure 15.	Input low level . . . . .	20
Figure 16.	Input hysteresis voltage . . . . .	20
Figure 17.	On state resistance vs Tcase . . . . .	21
Figure 18.	On state resistance vs VCC . . . . .	21
Figure 19.	Undervoltage shutdown . . . . .	21
Figure 20.	ILIMH vs Tcase . . . . .	21
Figure 21.	Turn-on voltage slope . . . . .	21
Figure 22.	Turn-off voltage slope . . . . .	21
Figure 23.	CS_DIS high level voltage . . . . .	22
Figure 24.	CS_DIS low level voltage . . . . .	22
Figure 25.	CS_DIS clamp voltage . . . . .	22
Figure 26.	Application schematic . . . . .	23
Figure 27.	Maximum turn off current versus inductance (for each channel) . . . . .	25
Figure 28.	PowerSSO-24™ PC board . . . . .	26
Figure 29.	Rthj-amb vs PCB copper area in open box free air condition ( one channel ON) . . . . .	26
Figure 30.	PowerSSO-24™ thermal impedance junction to ambient single pulse (one channel ON) . . . . .	27
Figure 31.	Thermal fitting model of a double channel HSD in PowerSSO-24™ . . . . .	27
Figure 32.	PowerSSO-24™ package dimensions . . . . .	29
Figure 33.	PowerSSO-24™ tube shipment (no suffix) . . . . .	31
Figure 34.	PowerSSO-24™ tape and reel shipment (suffix “TR”) . . . . .	31

# 1 Block diagram and pin description

Figure 1. Block diagram

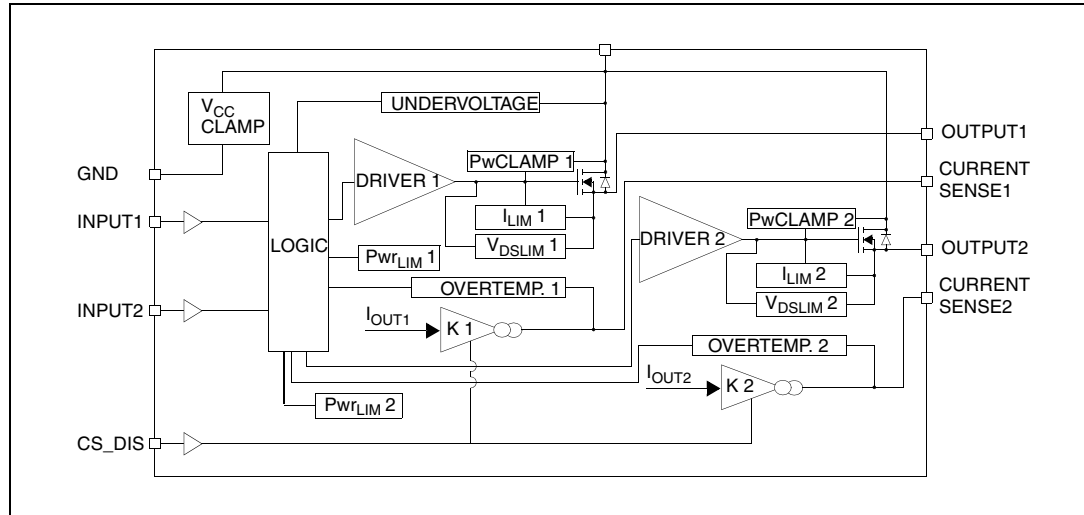
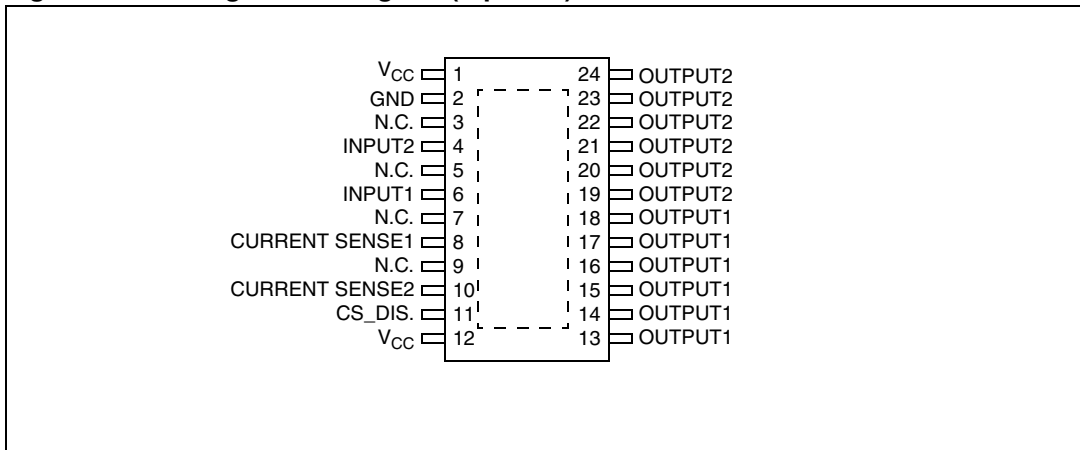


Table 2. Pin functions

Name	Function
V <sub>CC</sub>	Battery connection
OUTPUT <sub>1,2</sub>	Power output
GND	Ground connection; must be reverse battery protected by an external diode/resistor network
INPUT <sub>1,2</sub>	Voltage controlled input pin with hysteresis, CMOS compatible; controls output switch state
CURRENT SENSE <sub>1,2</sub>	Analog current sense pin; delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin to disable the current sense pin

**Figure 2. Configuration diagram (top view)**



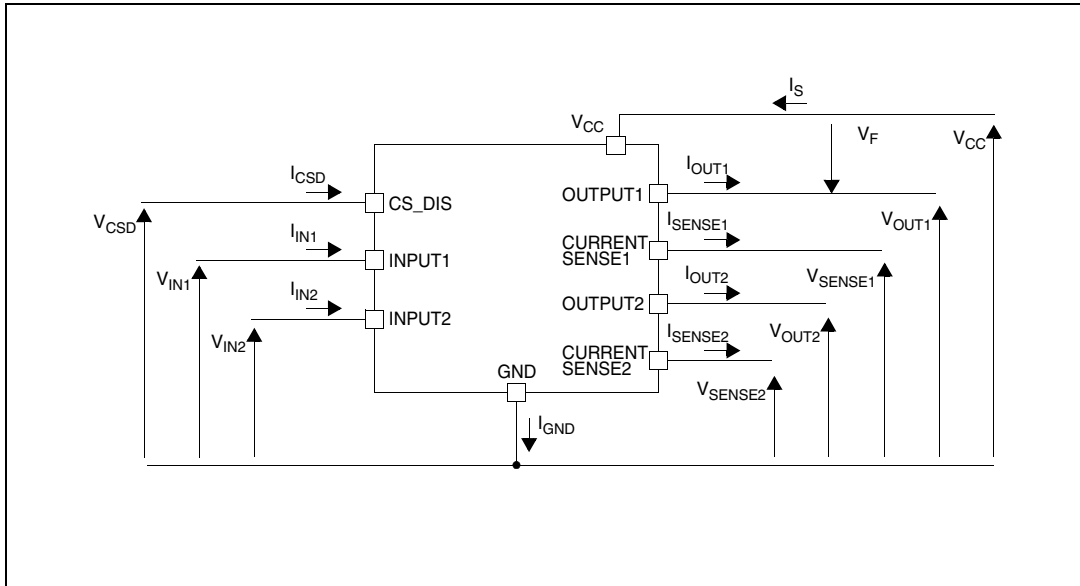
**Table 3. Suggested connections for unused and N.C. pins**

Connection / Pin	Current Sense	N.C.	Output	Input	CS_DIS
Floating	N.R. <sup>(1)</sup>	X	X	X	X
To Ground	Through 1kΩ resistor	X	N.R.	Through 10kΩ resistor	Through 10kΩ resistor

1. Not recommended

## 2 Electrical specification

Figure 3. Current and voltage conventions



Note:  $V_{Fn} = V_{OUTn} - V_{CC}$  during reverse battery condition

### 2.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	
$-I_{GND}$	DC reverse ground pin current	200	mA
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	24	
$I_{IN}$	DC input current	-1 to 10	mA
$I_{CS_D}$	DC current sense disable input current		
$-I_{CS_{SENSE}}$	DC reverse CS pin current		
$V_{CS_{SENSE}}$	Current sense maximum voltage	$V_{CC} - 41$ to $+V_{CC}$	V
$E_{MAX}^{(1)}$	Maximum switching energy (single pulse) ( $L = 0.8mH$ ; $R_L = 0\Omega$ ; $V_{bat} = 13.5V$ ; $T_{jstart} = 150^\circ C$ ; $I_{OUT} = I_{limL}(Typ.)$ )	140	mJ

**Table 4. Absolute maximum ratings (continued)**

Symbol	Parameter	Value	Unit
V <sub>ESD</sub>	Electrostatic Discharge (Human Body Model: R = 1.5kΩ; C = 100pF)		
	- Input	4000	V
	- Current sense	2000	V
	- CS_DIS	4000	V
	- Output	5000	V
	- V <sub>CC</sub>	5000	V
V <sub>ESD</sub>	Charge device model (CDM-AEC-Q100-011)	750	V
T <sub>j</sub>	Junction operating temperature	-40 to 150	°C
T <sub>stg</sub>	Storage temperature	-55 to 150	

1. See [Section 3.4](#) for details.

## 2.2 Thermal data

**Table 5. Thermal data**

Symbol	Parameter	Max Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case (MAX) (with one channel ON)	1.35	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient (MAX)	See <a href="#">Figure 29</a>	

## 2.3 Electrical characteristics

8V < V<sub>CC</sub> < 36V; -40°C < T<sub>j</sub> < 150°C, unless otherwise specified.

**Table 6. Power section**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	Operating supply voltage		4.5	13	36	V
V <sub>USD</sub>	Undervoltage shutdown			3.5	4.5	
V <sub>USDhyst</sub>	Undervoltage shut-down hysteresis			0.5		
R <sub>ON</sub>	On state resistance <sup>(1)</sup>	I <sub>OUT</sub> = 3A; T <sub>j</sub> = 25°C			25	mΩ
		I <sub>OUT</sub> = 3A; T <sub>j</sub> = 150°C			50	
		I <sub>OUT</sub> = 3A; V <sub>CC</sub> = 5V; T <sub>j</sub> = 25°C			35	
V <sub>clamp</sub>	Clamp voltage	I <sub>S</sub> = 20 mA	41	46	52	V
I <sub>S</sub>	Supply current	Off State; V <sub>CC</sub> = 13V; T <sub>j</sub> = 25°C; V <sub>IN</sub> = V <sub>OUT</sub> = V <sub>SENSE</sub> = V <sub>CSD</sub> = 0V		2 <sup>(2)</sup>	5 <sup>(2)</sup>	μA
		On State; V <sub>CC</sub> = 13V; V <sub>IN</sub> = 5V; I <sub>OUT</sub> = 0A		3	6	mA



**Table 6. Power section (continued)**

$I_{L(off)}$	Off state output current <sup>(1)</sup>	$V_{IN} = V_{OUT} = 0V; V_{CC} = 13V; T_j = 25^\circ C$	0	0.01	3	$\mu A$
		$V_{IN} = V_{OUT} = 0V; V_{CC} = 13V; T_j = 125^\circ C$	0		5	
$V_F$	Output - $V_{CC}$ diode voltage <sup>(1)</sup>	$-I_{OUT} = 4A; T_j = 150^\circ C$			0.7	V

1. For each channel
2. PowerMOS leakage included

**Table 7. Switching ( $V_{CC} = 13V; T_j = 25^\circ C$ )**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 4.3\Omega$ (see <a href="#">Figure 8</a> )		35		$\mu s$
$t_{d(off)}$	Turn-off delay time			50		
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L = 4.3\Omega$		(see <a href="#">Figure 21</a> )		V/ $\mu s$
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope			(see <a href="#">Figure 22</a> )		
$W_{ON}$	Switching energy losses during $t_{WON}$	$R_L = 4.3\Omega$ (see <a href="#">Figure 8</a> )		0.45		mJ
$W_{OFF}$	Switching energy losses during $t_{WOFF}$			0.35		

**Table 8. Logic input**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{IL}$	Input low level voltage				0.9	V
$I_{IL}$	Low level input current	$V_{IN} = 0.9V$	1			$\mu A$
$V_{IH}$	Input high level voltage		2.1			V
$I_{IH}$	High level input current	$V_{IN} = 2.1V$			10	$\mu A$
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1mA$	5.5		7	
		$I_{IN} = -1mA$		-0.7		
$V_{CSDL}$	CS_DIS low level voltage				0.9	$\mu A$
$I_{CSDL}$	Low level CS_DIS current	$V_{CSD} = 0.9V$	1			
$V_{CSDH}$	CS_DIS high level voltage		2.1			V
$I_{CSDH}$	High level CS_DIS current	$V_{CSD} = 2.1V$			10	$\mu A$
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
$V_{CSCL}$	CS_DIS clamp voltage	$I_{CSD} = 1mA$	5.5		7	
		$I_{CSD} = -1mA$		-0.7		

**Table 9. Protection and diagnostics<sup>(1)</sup>**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$I_{LIMH}$	DC short circuit current	$V_{CC} = 13V$	29	41	57	A
		$5V < V_{CC} < 36V$				
$I_{LIML}$	Short circuit current during thermal cycling	$V_{CC} = 13V$ ; $T_R < T_j < T_{TSD}$		16		
$T_{TSD}$	Shutdown temperature		150	175	200	°C
$T_R$	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		
$T_{RS}$	Thermal reset of STATUS		135			
$T_{HYST}$	Thermal hysteresis ( $T_{TSD} - T_R$ )			7		
$V_{DEMAG}$	Turn-off output voltage clamp	$I_{OUT} = 2A$ ; $V_{IN} = 0$ ; $L = 6mH$	$V_{CC} - 41$	$V_{CC} - 46$	$V_{CC} - 52$	V
$V_{ON}$	Output voltage drop limitation	$I_{OUT} = 0.20.1A$ ; $T_j = -40^\circ C$ to $+150^\circ C$ (see <a href="#">Figure 9</a> )		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Current sense (8V < V<sub>CC</sub> < 16V)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
K <sub>LED</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 0.05A; V <sub>SENSE</sub> = 0.5V; V <sub>CSD</sub> = 0V; T <sub>j</sub> = -40°C to 150°C	1450	3300	5180	
K <sub>0</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 0.5A; V <sub>SENSE</sub> = 0.5V; V <sub>CSD</sub> = 0V; T <sub>j</sub> = -40°C to 150°C	1720	3020	4360	
K <sub>1</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 2A; V <sub>SENSE</sub> = 4V; V <sub>CSD</sub> = 0V; T <sub>j</sub> = -40°C T <sub>j</sub> = 25°C to 150°C	1940 2230	2810 2810	3740 3390	
dK <sub>1</sub> /K <sub>1</sub> <sup>(1)</sup>	Current sense ratio drift	I <sub>OUT</sub> = 2A; V <sub>SENSE</sub> = 4V; V <sub>CSD</sub> = 0V; T <sub>j</sub> = -40°C to 150°C	-10		+10	%
K <sub>2</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 3A; V <sub>SENSE</sub> = 4V; V <sub>CSD</sub> = 0V; T <sub>j</sub> = -40°C T <sub>j</sub> = 25°C to 150°C	2250 2400	2790 2790	3450 3180	
dK <sub>2</sub> /K <sub>2</sub> <sup>(1)</sup>	Current sense ratio drift	I <sub>OUT</sub> = 3A; V <sub>SENSE</sub> = 4V; V <sub>CSD</sub> = 0V; T <sub>j</sub> = -40°C to 150°C	-7		+7	%
K <sub>3</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 10A; V <sub>SENSE</sub> = 4V; V <sub>CSD</sub> = 0V; T <sub>j</sub> = -40°C T <sub>j</sub> = 25°C to 150°C	2610 2650	2760 2760	2970 2870	
dK <sub>3</sub> /K <sub>3</sub> <sup>(1)</sup>	Current sense ratio drift	I <sub>OUT</sub> = 10A; V <sub>SENSE</sub> = 4V; V <sub>CSD</sub> = 0V; T <sub>j</sub> = -40°C to 150°C	-3		+3	%
I <sub>SENSE0</sub>	Analog sense leakage current	I <sub>OUT</sub> = 0A; V <sub>SENSE</sub> = 0V; V <sub>CSD</sub> = 5V; V <sub>IN</sub> = 0V; T <sub>j</sub> = -40°C to 150°C	0		1	μA
		V <sub>CSD</sub> = 0V; V <sub>IN</sub> = 5V; T <sub>j</sub> = -40°C to 150°C	0		2	μA
		I <sub>OUT</sub> = 2A; V <sub>SENSE</sub> = 0V; V <sub>CSD</sub> = 5V; V <sub>IN</sub> = 5V; T <sub>j</sub> = -40°C to 150°C	0		1	μA
V <sub>SENSE</sub>	Max analog sense output voltage	I <sub>OUT</sub> = 3A; V <sub>CSD</sub> = 0V	5			V
V <sub>SENSEH</sub>	Analog sense output voltage in overtemperature condition	V <sub>CC</sub> = 13V; R <sub>SENSE</sub> = 3.9kΩ		9		
I <sub>SENSEH</sub>	Analog sense output current in overtemperature condition	V <sub>CC</sub> = 13V; V <sub>SENSE</sub> = 5V		8		mA

**Table 10. Current sense (8V < V<sub>CC</sub> < 16V) (continued)**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t <sub>DSENSE1H</sub>	Delay response time from falling edge of CS_DIS pin	V <sub>SENSE</sub> < 4V, 0.5 < I <sub>OUT</sub> < 10A I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub> (see Figure 4)		50	100	μs
t <sub>DSENSE1L</sub>	Delay response time from rising edge of CS_DIS pin	V <sub>SENSE</sub> < 4V, 0.5 < I <sub>OUT</sub> < 10A I <sub>SENSE</sub> = 10% of I <sub>SENSEMAX</sub> (see Figure 4)		5	20	
t <sub>DSENSE2H</sub>	Delay response time from rising edge of INPUT pin	V <sub>SENSE</sub> < 4V, 0.5 < I <sub>OUT</sub> < 10A I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub> (see Figure 4)		70	300	
Δt <sub>DSENSE2H</sub>	Delay response time between rising edge of output current and rising edge of current sense	V <sub>SENSE</sub> < 4V, I <sub>SENSE</sub> = 90% of I <sub>SENSEMAX</sub> , I <sub>OUT</sub> = 90% of I <sub>OUTMAX</sub> , I <sub>OUTMAX</sub> = 3A (see Figure 5)			110	
t <sub>DSENSE2L</sub>	Delay response time from falling edge of INPUT pin	V <sub>SENSE</sub> < 4V, 0.5 < I <sub>OUT</sub> < 10A I <sub>SENSE</sub> = 10% of I <sub>SENSEMAX</sub> (see Figure 4)		100	250	

1. Parameter guaranteed by design; it is not tested.

**Figure 4. Current sense delay characteristics**

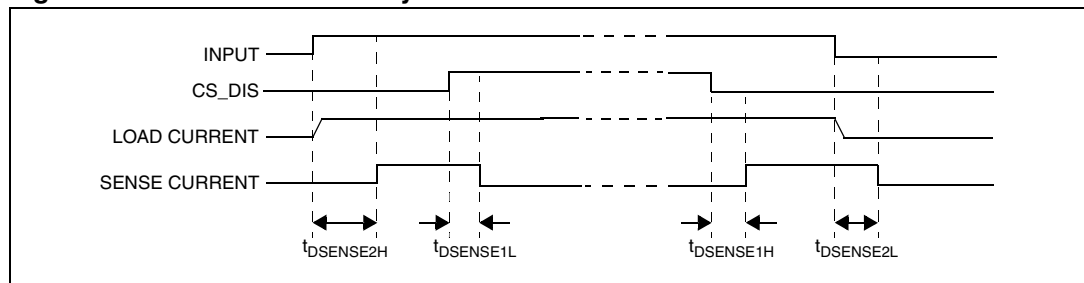


Figure 5. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)

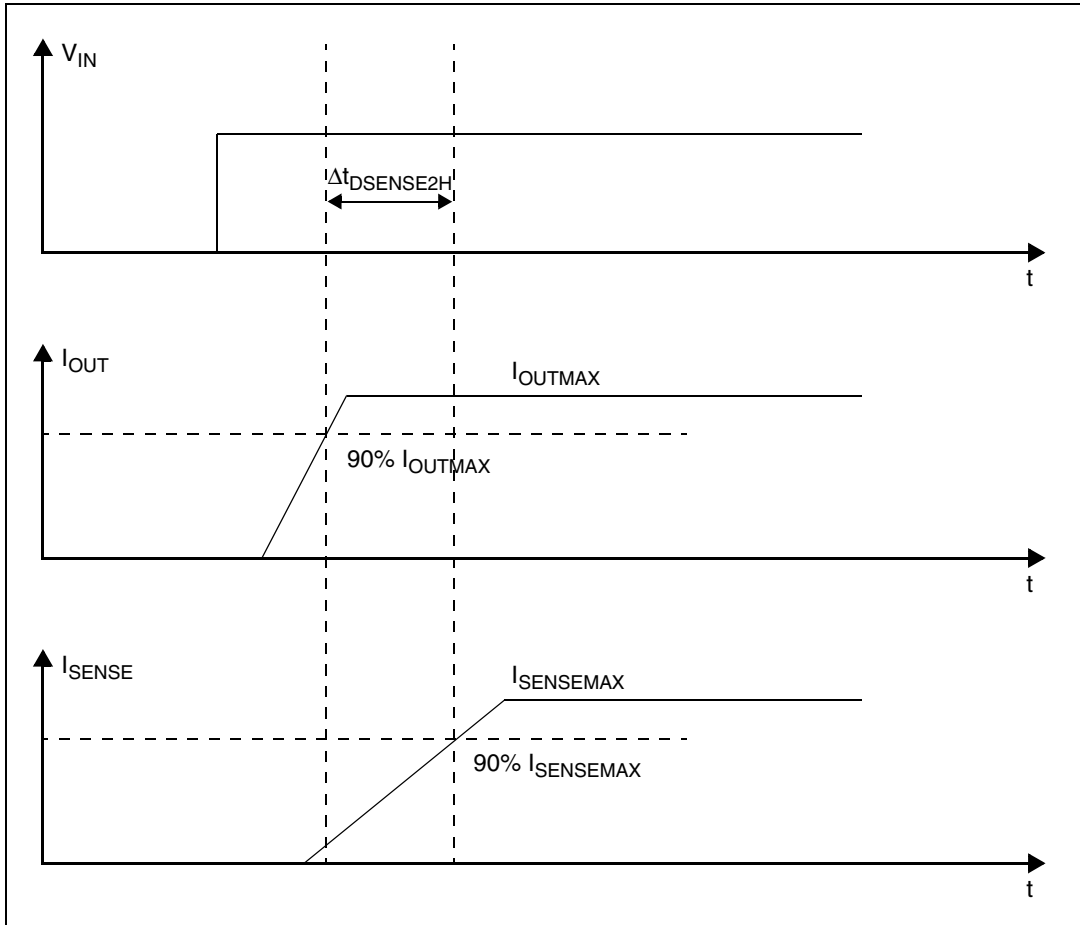


Figure 6.  $I_{OUT}/I_{SENSE}$  vs  $I_{OUT}$  (see Table 10 for details)

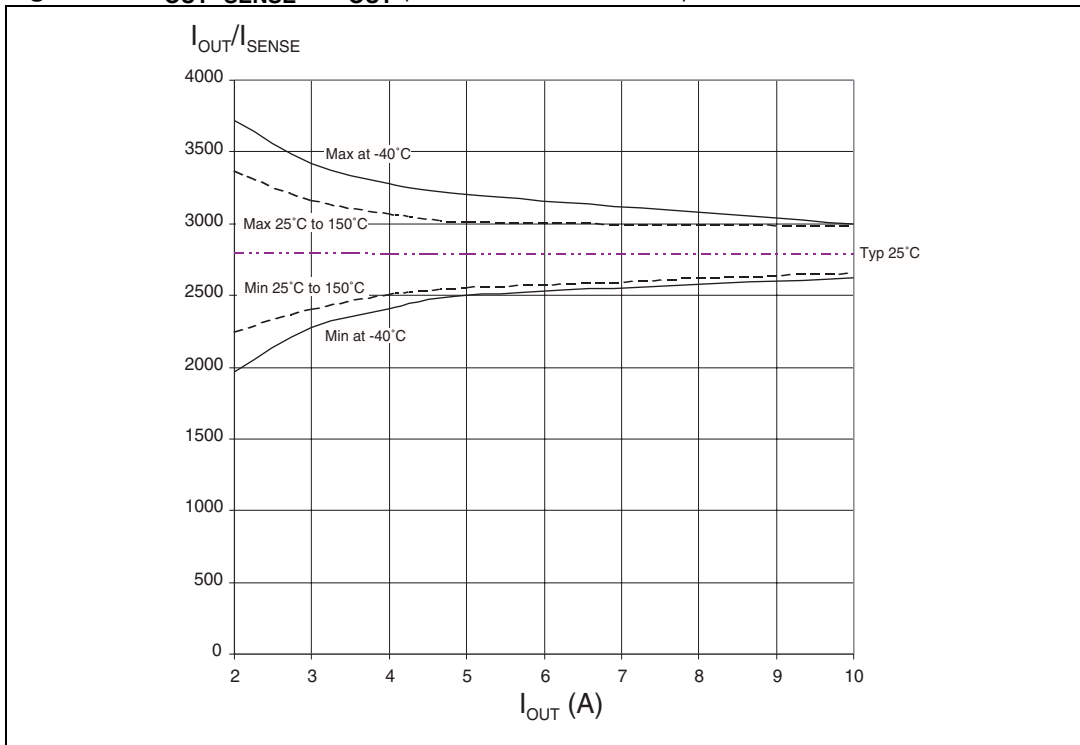
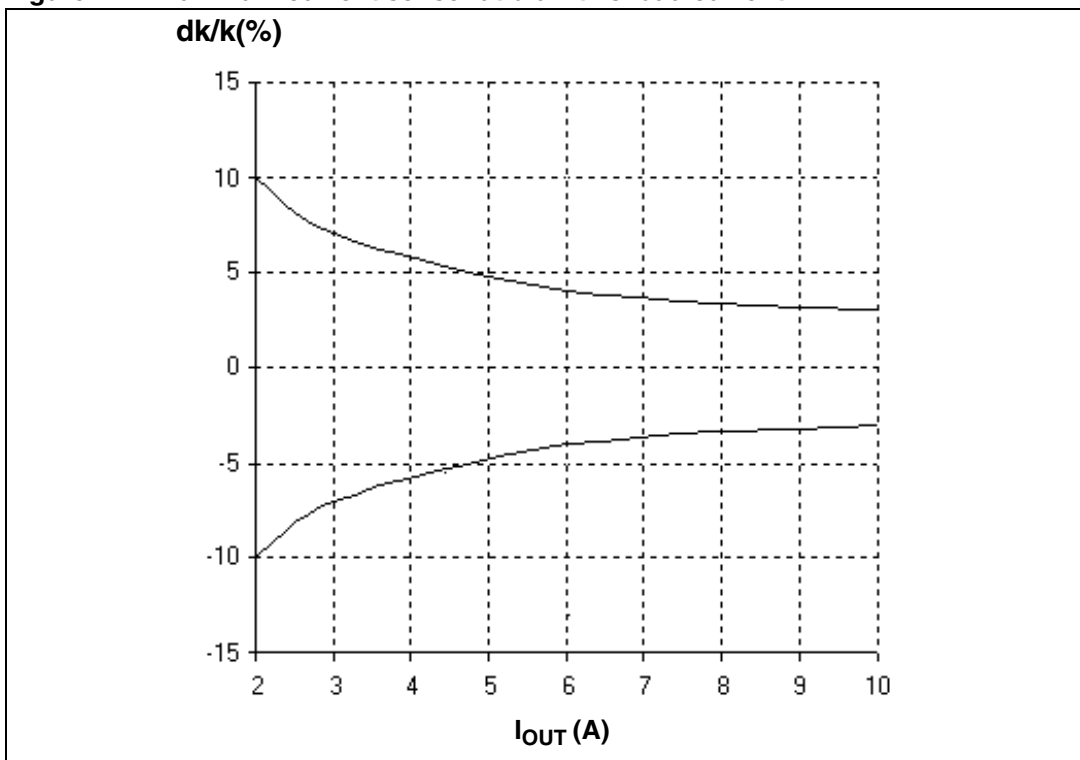


Figure 7. Maximum current sense ratio drift vs load current<sup>(a)</sup>



a. Parameter guaranteed by design; it is not tested

Table 11. Truth table

Conditions	Input	Output	Sense ( $V_{CSD} = 0V$ ) <sup>(1)</sup>
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H		$V_{SENSEH}$
Undervoltage	L	L	0
	H		
Short circuit to GND ( $R_{SC} \leq 10m\Omega$ )	L	L	0
	H		0 if $T_j < T_{TSD}$ $V_{SENSEH}$ if $T_j > T_{TSD}$
Short circuit to $V_{CC}$	L	H	0
	H		< Nominal
Negative output voltage clamp	L	L	0

1. If the  $V_{CSD}$  is high, the SENSE output is at a high impedance; its potential depends on leakage currents and external circuit.

Figure 8. Switching characteristics

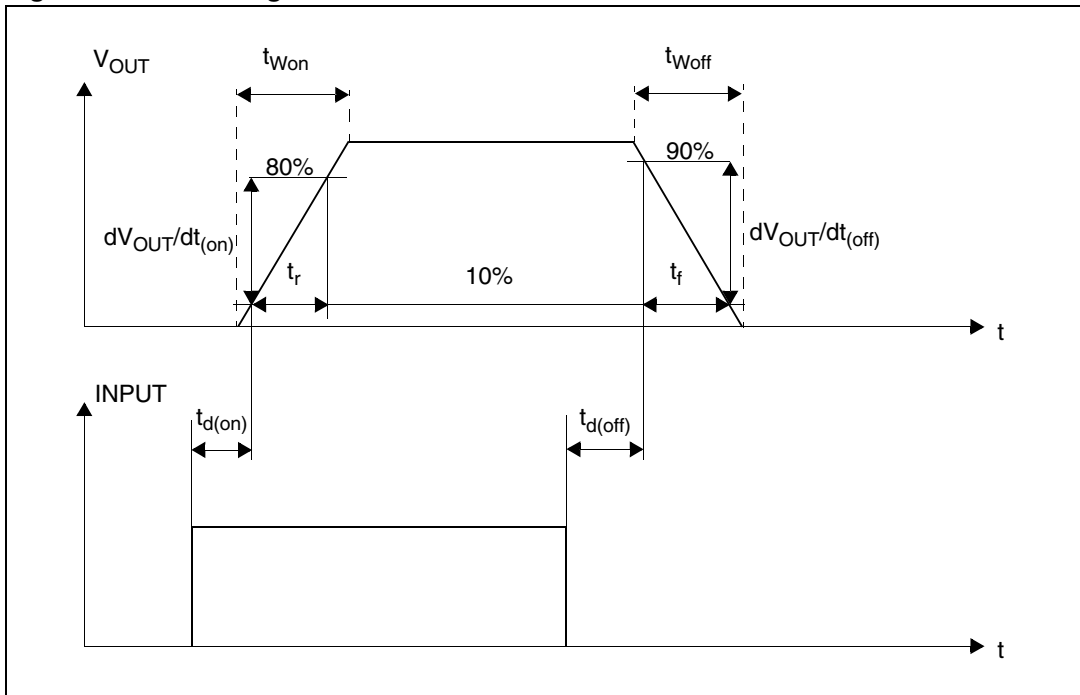
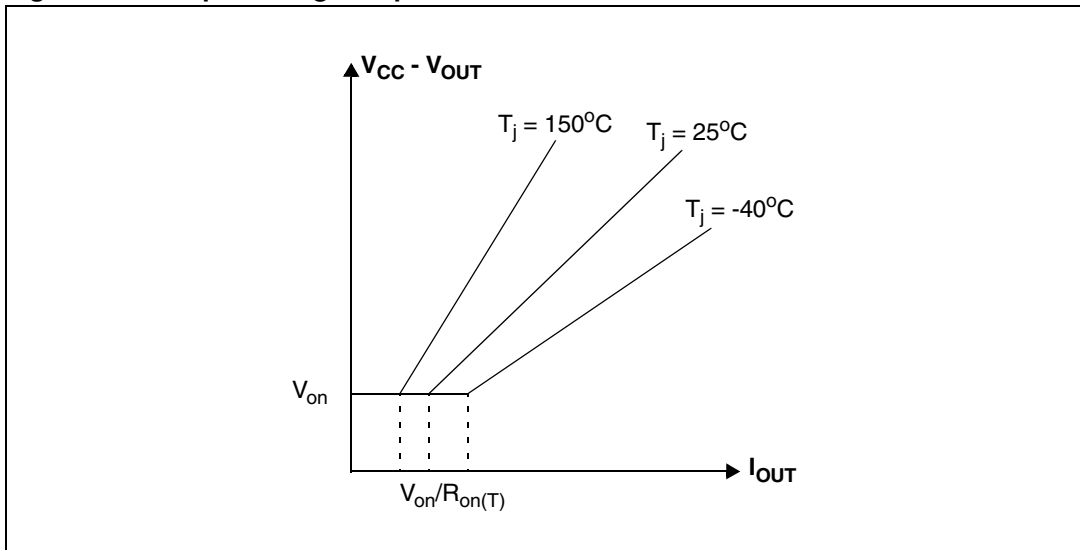


Figure 9. Output voltage drop limitation





**Table 12. Electrical transient requirements**

ISO 7637-2: 2004(E) Test pulse	Test levels <sup>(1)</sup>		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV		Min	Max	
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50μs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1μs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1μs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b <sup>(2)</sup>	+65V	+87V	1 pulse			400ms, 2Ω

ISO 7637-2: 2004E Test pulse	Test level results	
	III	VI
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b <sup>(2)</sup>	C	C

Class	Contents
C	All functions of the device <b>performed</b> as designed after exposure to disturbance.
E	One or more functions of the device <b>did not</b> perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

1. The above test levels must be considered referred to V<sub>CC</sub> = 13.5V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

Figure 10. Waveforms

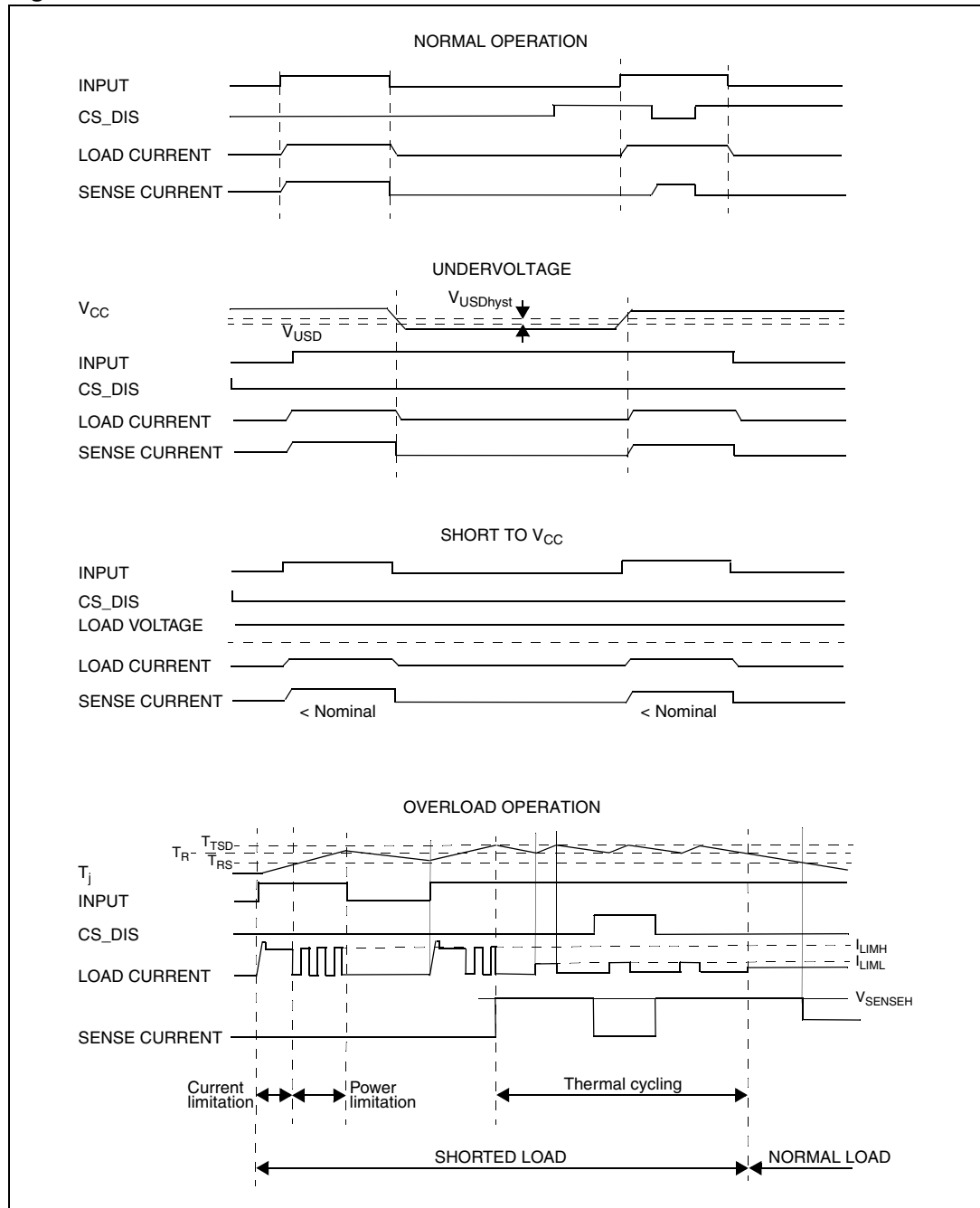


Figure 11. Off state output current

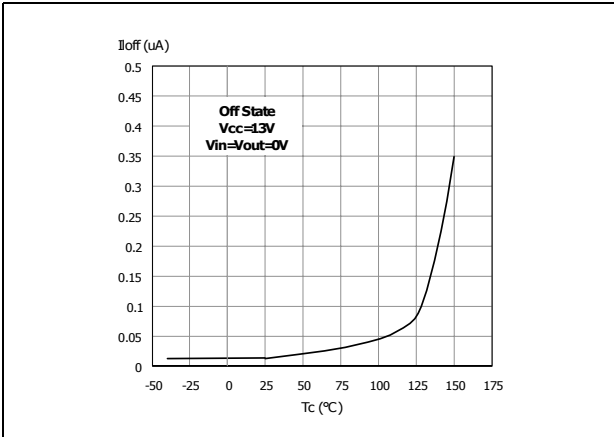


Figure 12. High level input current

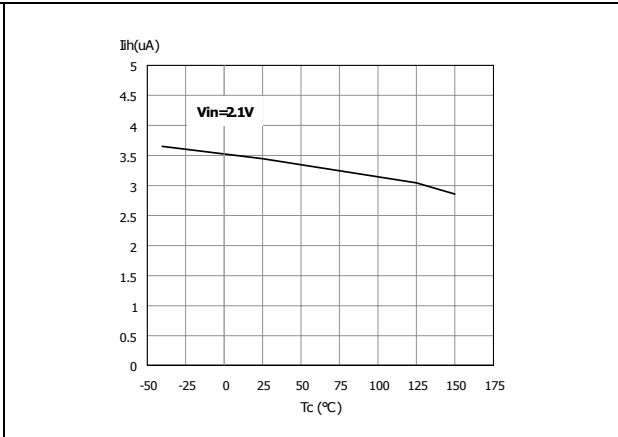


Figure 13. Input clamp voltage

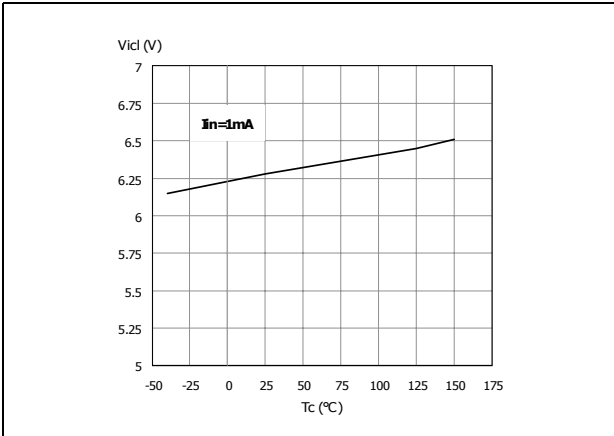


Figure 14. Input high level

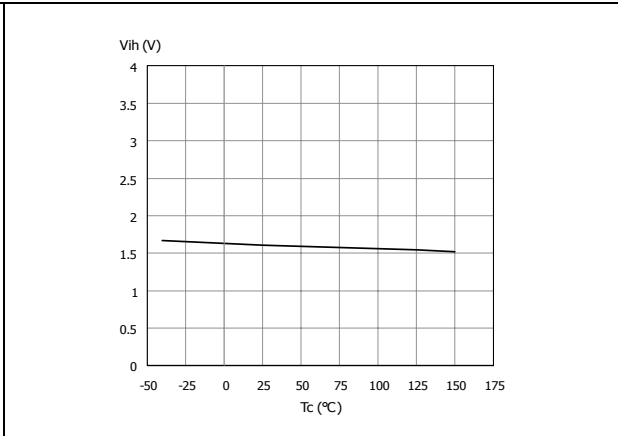


Figure 15. Input low level

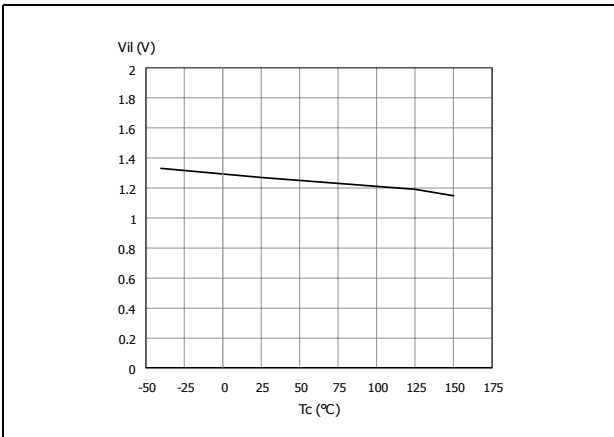


Figure 16. Input hysteresis voltage

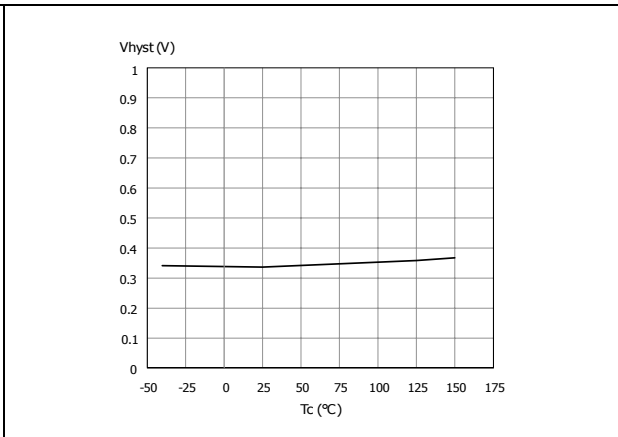


Figure 17. On state resistance vs  $T_{case}$

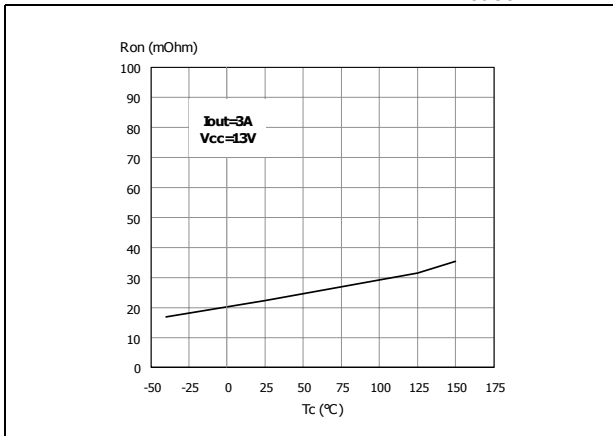


Figure 18. On state resistance vs  $V_{CC}$

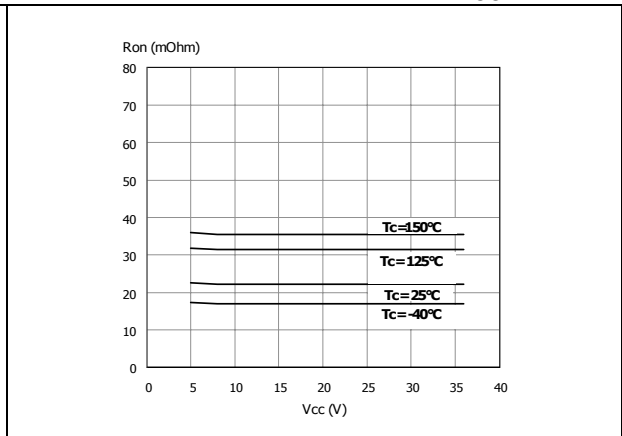


Figure 19. Undervoltage shutdown

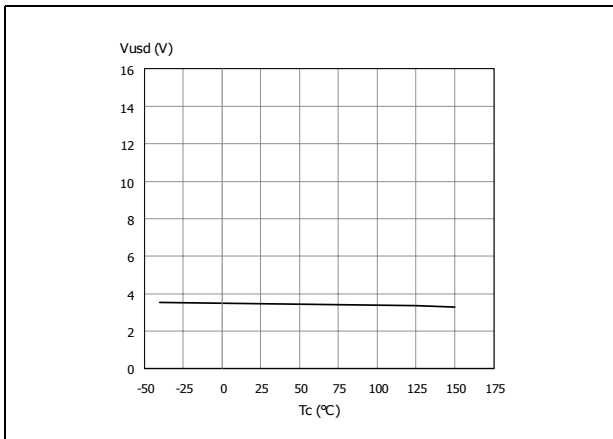


Figure 20.  $I_{LIMH}$  vs  $T_{case}$

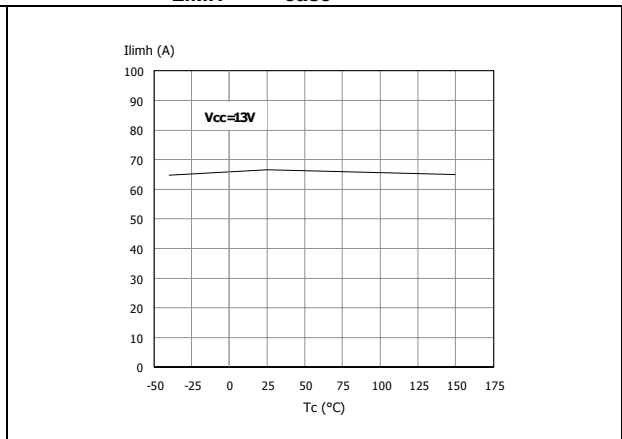


Figure 21. Turn-on voltage slope

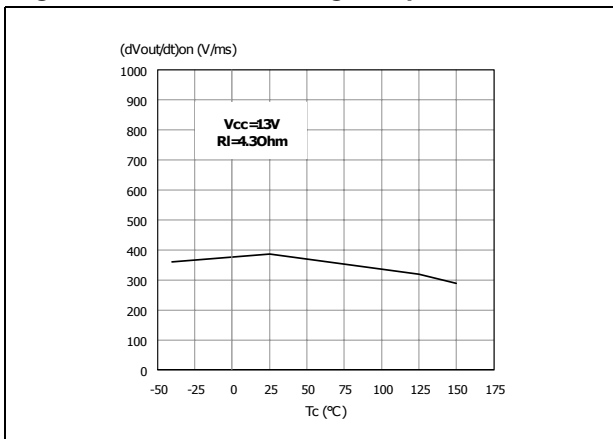


Figure 22. Turn-off voltage slope

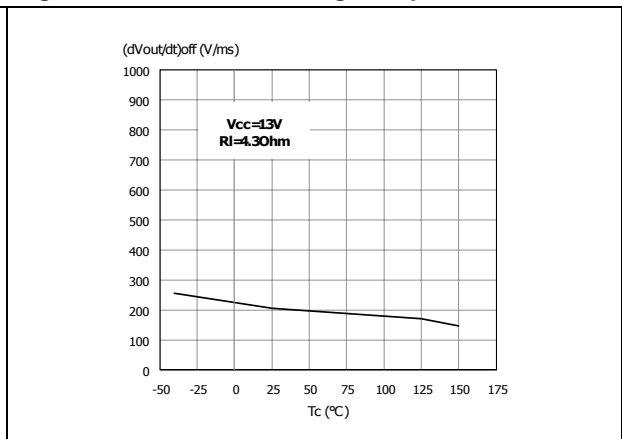


Figure 23. CS\_DIS high level voltage

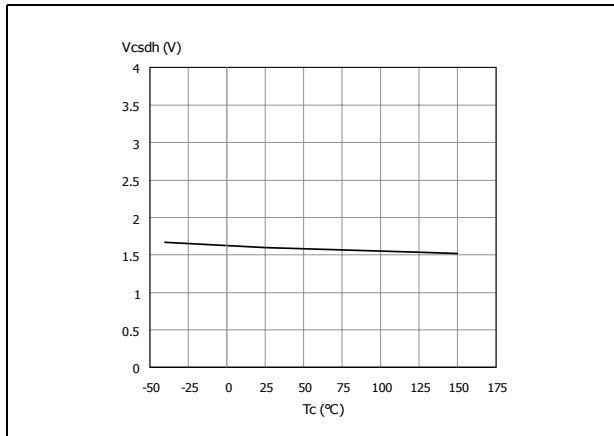


Figure 24. CS\_DIS low level voltage

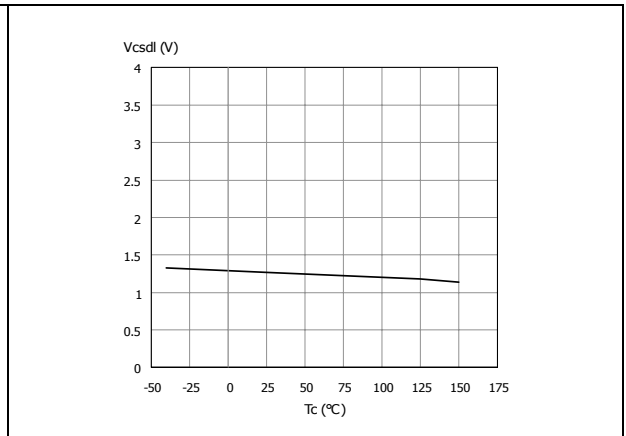
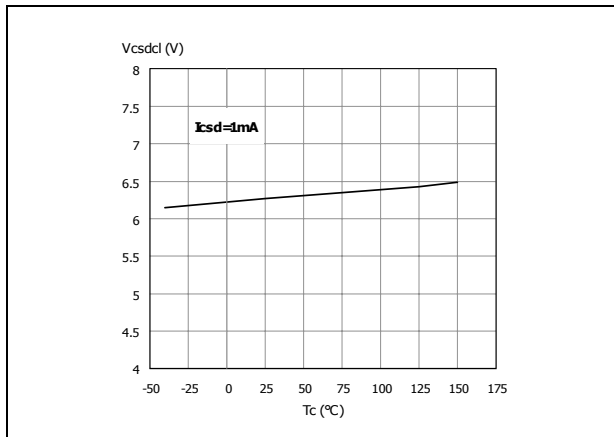
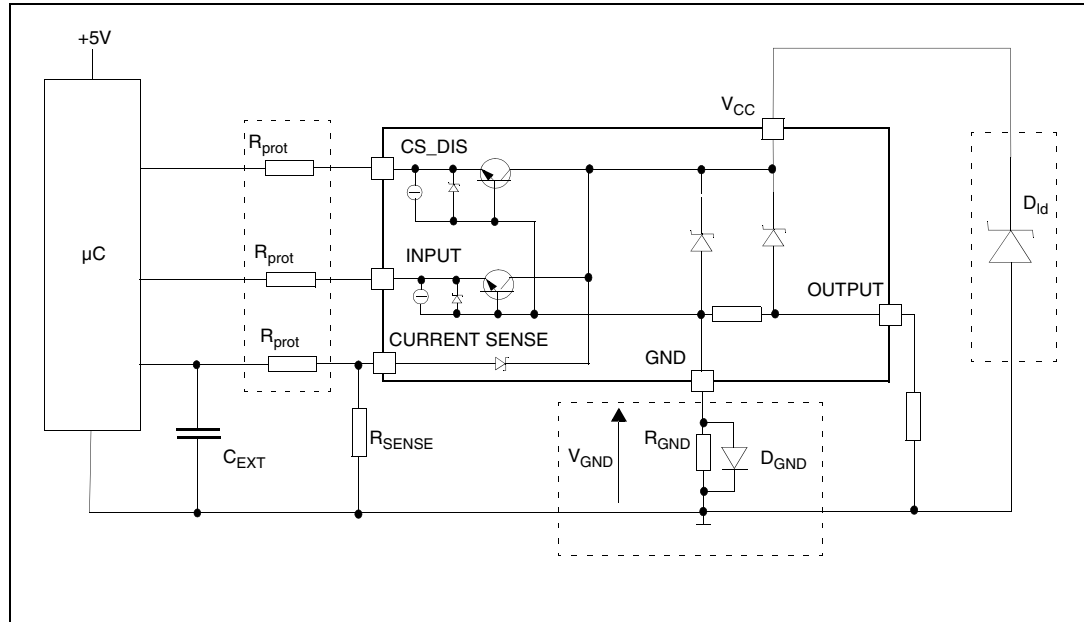


Figure 25. CS\_DIS clamp voltage



### 3 Application information

Figure 26. Application schematic



Note: Channel 2 has the same internal circuit as channel 1.

#### 3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

##### 3.1.1 Solution 1: resistor in the ground line (R<sub>GND</sub> only)

This first solution can be used with any type of load.

The following formulas indicate how to dimension the R<sub>GND</sub> resistor:

1.  $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R<sub>GND</sub> (when V<sub>CC</sub> < 0 during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared among several different HSDs. Please note that the value of this resistor is calculated with formula (1), where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground, the R<sub>GND</sub> produces a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This

shift varies depending on how many devices are ON in the case of several high-side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor, then ST suggests to utilize the following Solution 2.

### 3.1.2 Solution 2: diode ( $D_{GND}$ ) in the ground line

If the device drives an inductive load, insert a resistor ( $R_{GND} = 1k\Omega$ ) in parallel to  $D_{GND}$ .

This small signal diode can be safely shared among several different HSDs. Also in this case, the presence of the ground network produces a shift (j600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

## 3.2 Load dump protection

$D_{ld}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  maximum DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO 7637-2:2004E table.

## 3.3 $\mu C$ I/Os protection

If a ground protection network is used and negative transients are present on the  $V_{CC}$  line, the control pins are pulled negative. ST suggests to insert an in-line resistor ( $R_{prot}$ ) to prevent the  $\mu C$  I/Os pins from latch-up.

The value of these resistors is a compromise between the leakage current of  $\mu C$  and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of  $\mu C$  I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

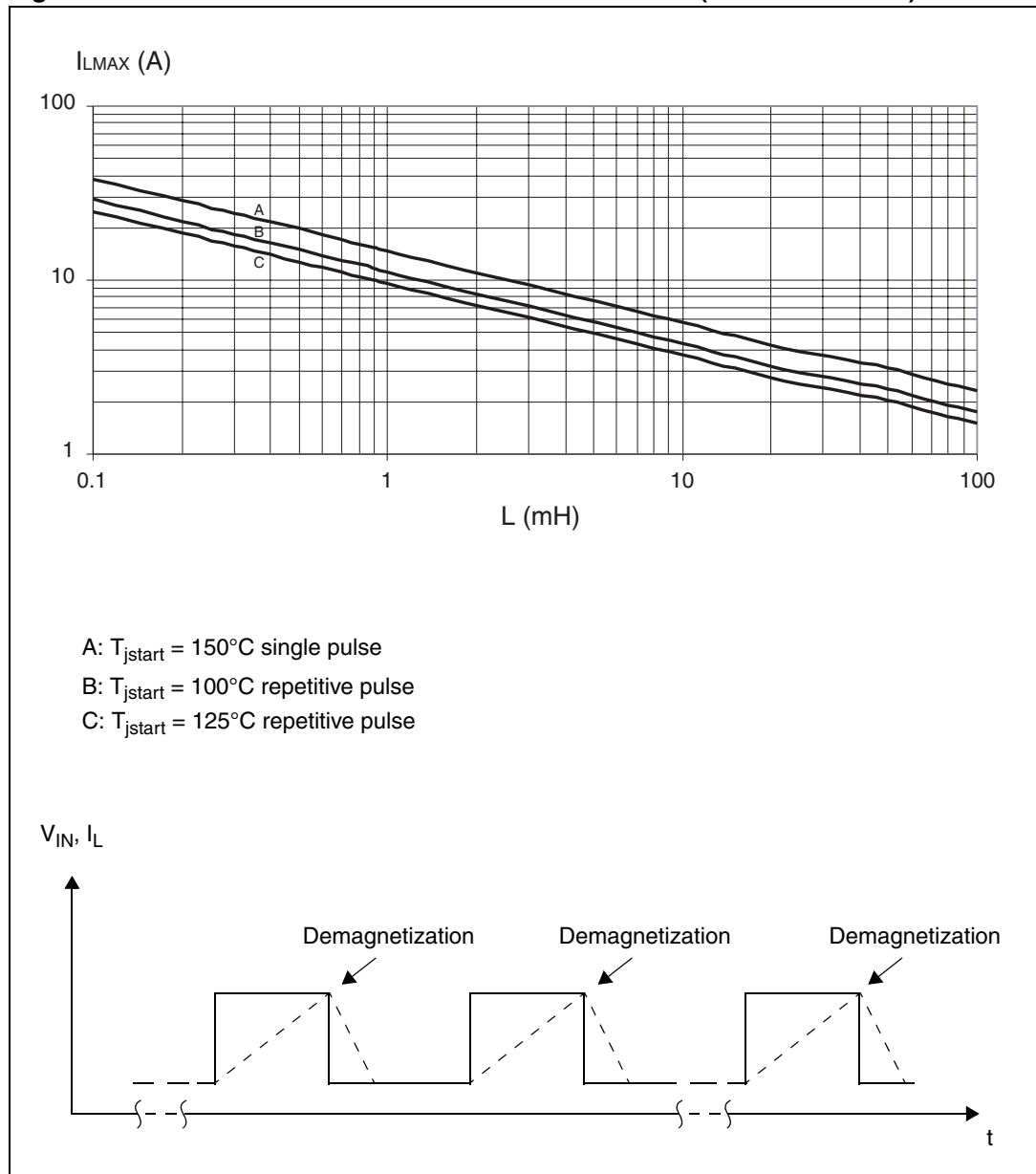
For  $V_{CCpeak} = -100V$  and  $I_{latchup} \geq 20mA$ ;  $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 65k\Omega$$

Recommended values:  $R_{prot} = 10k\Omega$ ,  $C_{EXT} = 10nF$

### 3.4 Maximum demagnetization energy ( $V_{CC} = 13.5V$ )

Figure 27. Maximum turn off current versus inductance (for each channel)



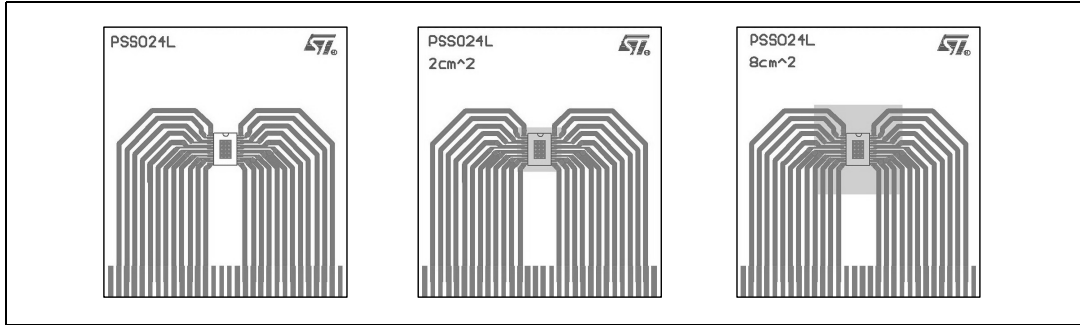
Note: Values are generated with  $R_L = 0\Omega$   
 In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.



## 4 Package and thermal data

### 4.1 PowerSSO-24™ thermal data

Figure 28. PowerSSO-24™ PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: Double layer, Thermal Vias, FR4 area = 77mm x 86mm, PCB thickness = 1.6mm, Cu thickness = 70µm (front and back side), Copper areas: from minimum pad layout to 8cm²).

Figure 29.  $R_{thj-amb}$  vs PCB copper area in open box free air condition ( one channel ON)

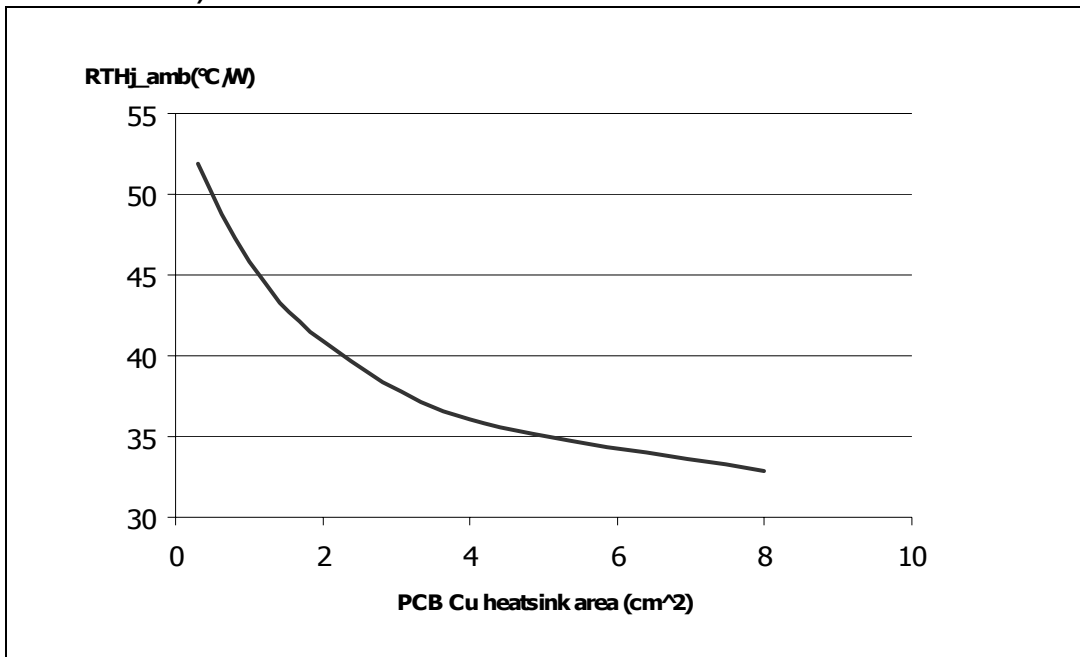
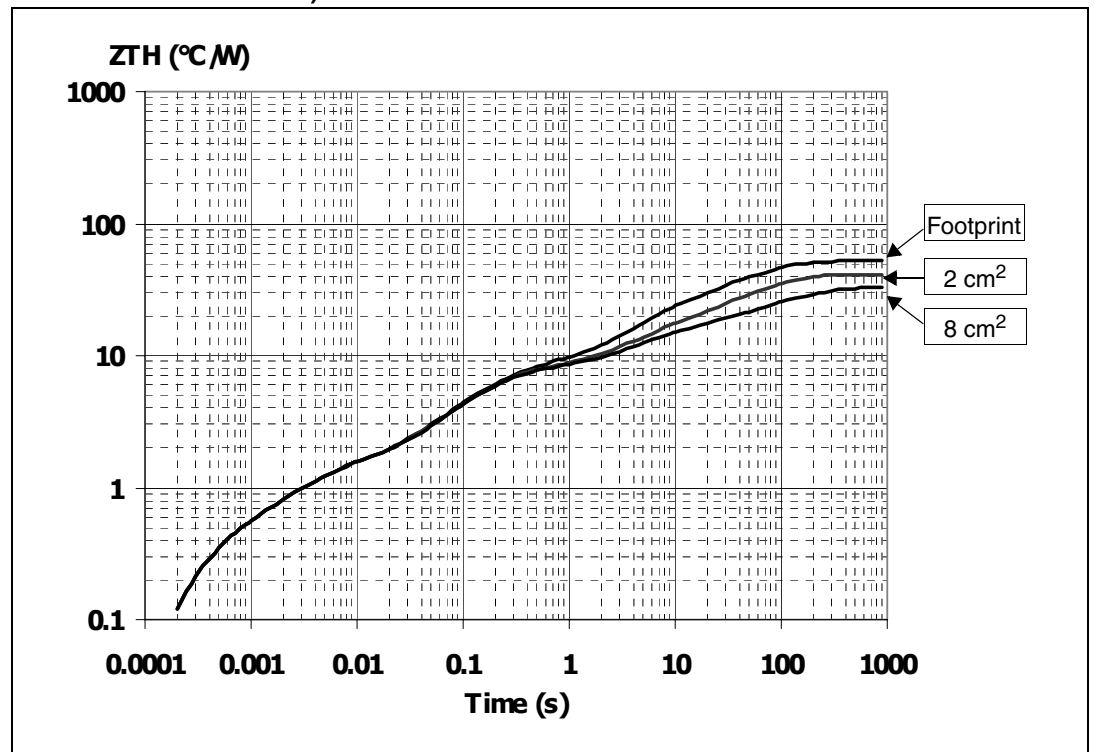


Figure 30. PowerSSO-24™ thermal impedance junction to ambient single pulse (one channel ON)

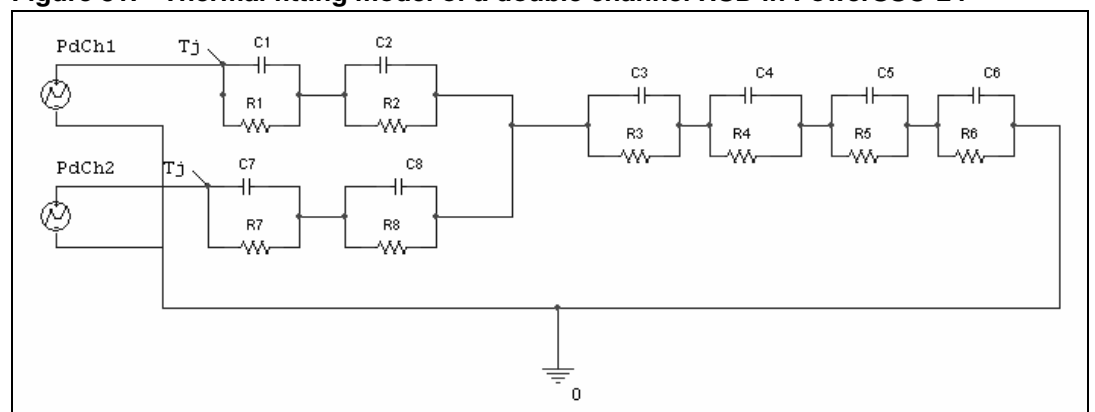


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p / T$

Figure 31. Thermal fitting model of a double channel HSD in PowerSSO-24™(b)



b. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered

Table 13. Thermal parameters

Area/Island (cm <sup>2</sup> )	Footprint	2	8
R1 (°C/W)	0.28		
R2 (°C/W)	0.9		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
R7 (°C/W)	0.28		
R8 (°C/W)	0.9		
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.003		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17
C7 (W.s/°C)	0.001		
C8 (W.s/°C)	0.003		

## 5 Package and packing information

### 5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of Second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at [www.st.com](http://www.st.com).

### 5.2 Package mechanical data

Figure 32. PowerSSO-24™ package dimensions

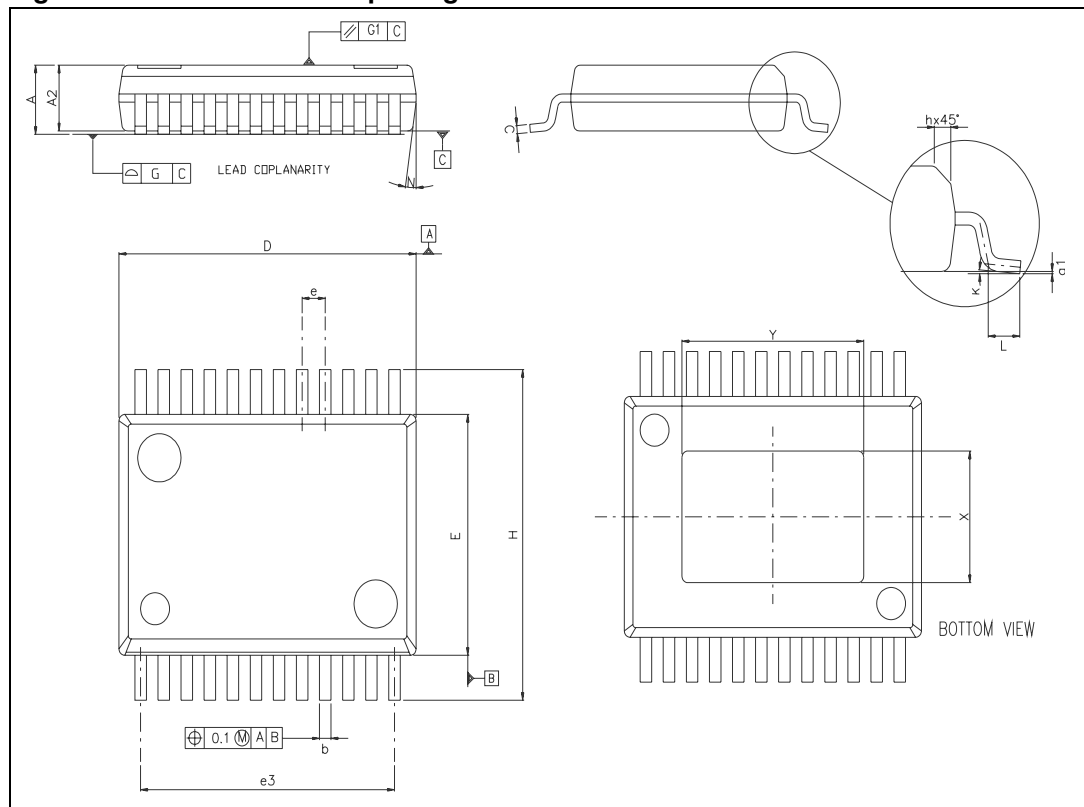


Table 14. PowerSSO-24™ mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	1.9		2.22
A2	1.9		2.15

Table 14. PowerSSO-24™ mechanical data

Symbol	Millimeters		
	Min	Typ	Max
a1	0		0.07
b	0.34	0.4	0.46
c	0.23		0.32
D	10.2		10.4
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10°
X	3.9		4.3
Y	6.1		6.5

### 5.3 Packing information

Figure 33. PowerSSO-24™ tube shipment (no suffix)

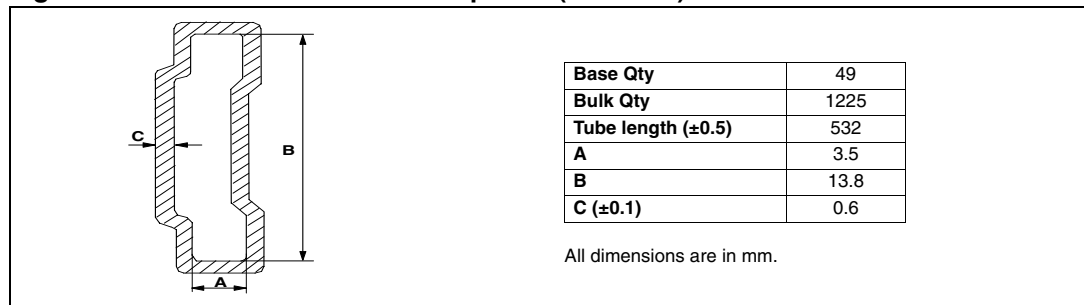
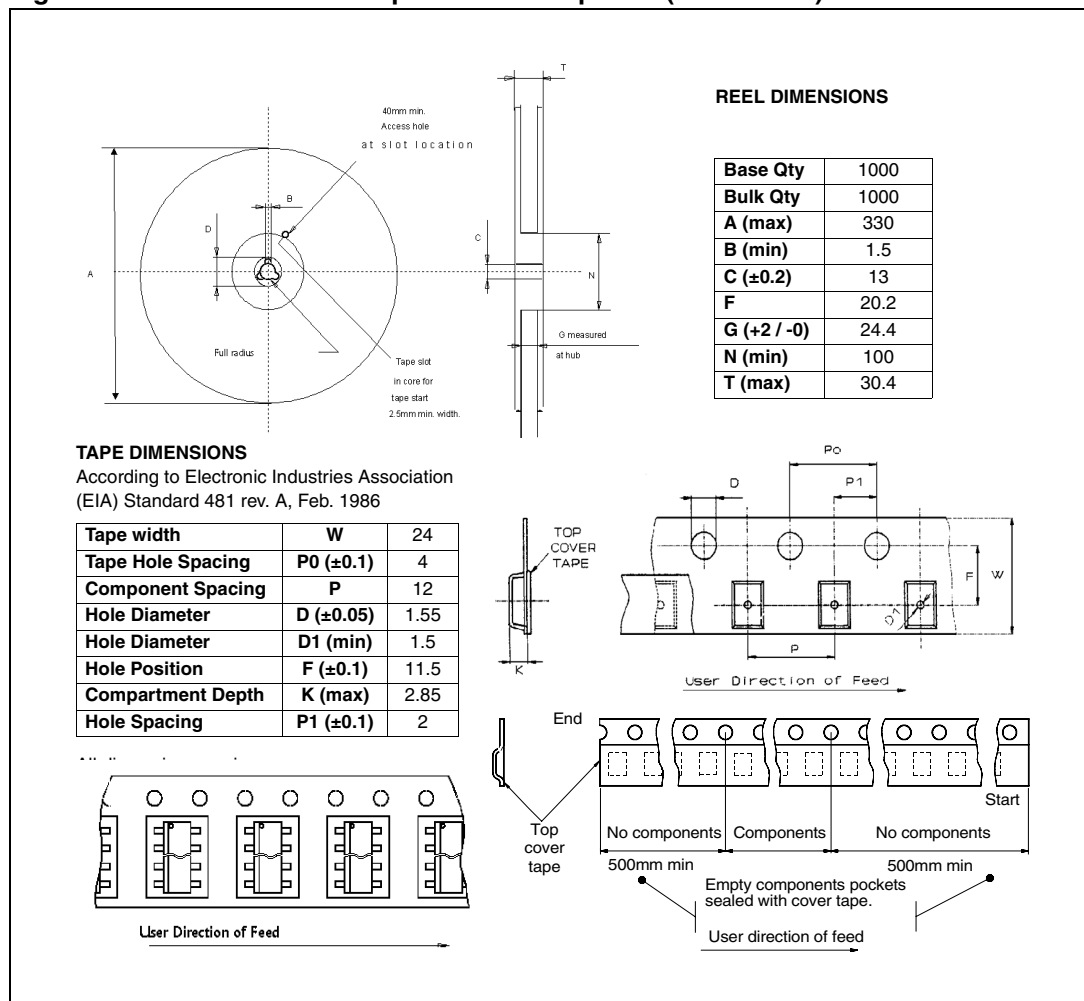


Figure 34. PowerSSO-24™ tape and reel shipment (suffix “TR”)



## 6 Revision history

**Table 15. Document revision history**

Date	Revision	Changes
11-Apr-2006	1	Initial release
30-Mar-2007	2	Reformatted. <i>Table 4 on page 8</i> : $E_{MAX}$ entries updated. <i>Table 6 on page 9</i> : $V_F$ test conditions updated. <i>Table 7 on page 10</i> : $T_j$ condition set to 25°C <i>Table 10 on page 12</i> : $dK_1/K_1$ , $dK_2/K_2$ and $dK_3/K_3$ , $\Delta t_{DSENSE2H}$ added, $t_{DSENSE2H}$ values updated and note added. <i>Figure 5: Delay response time between rising edge of output current and rising edge of current sense (CS enabled) on page 14</i> added. <i>Figure 6: IOOUT/ISENSE vs IOOUT (see Table 10 for details) on page 15</i> updated. <i>Figure 7: Maximum current sense ratio drift vs load current on page 15</i> added. <i>Table 12 on page 18</i> : Test Level values III and IV for test pulse 5b in and notes updated. <i>Section 3.4: Maximum demagnetization energy (VCC = 13.5V) on page 25</i> added. ECOPACK® packages information added. Table in <i>Figure 2 on page 7</i> updated. <i>Section 3.2 on page 24</i> : ISO T/R 7637/1 updated to ISO 7637-2:2004E. <i>Figure 30 on page 27</i> : Pulse calculation formula added. Disclaimer replaced.
01-Jun-2007	3	<i>Figure 31: Thermal fitting model of a double channel HSD in PowerSSO-24™</i> : note added

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2007 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)