

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER WITH FIFOs

DESCRIPTION

The ST16C2552 is a dual asynchronous receiver and transmitter with 16 byte transmit and receive FIFOs. Independent programmable baud rate generators are provided to select transmit and receive clock rates from 50Hz to 1.5 MHz for each UART.

The on board status registers of the ST16C2552 provide the error conditions, type and status of the transfer operation being performed. Complete MODEM control capability and a processor interrupt system that may be software tailored to the user's requirements are included. The ST16C2552 provides internal loop-back capability for on board diagnostic testing.

Signalling for DMA transfers is done through two pins per channel (TXRDY*, RXRDY*). The RXRDY* function is multiplexed on one pin with the OP2* and BAUDOUT functions. CPU can select these functions through the Alternate Function Register.

The ST16C2552 is fabricated in an advanced 0.6µ CMOS process to achieve low power and high speed requirements.

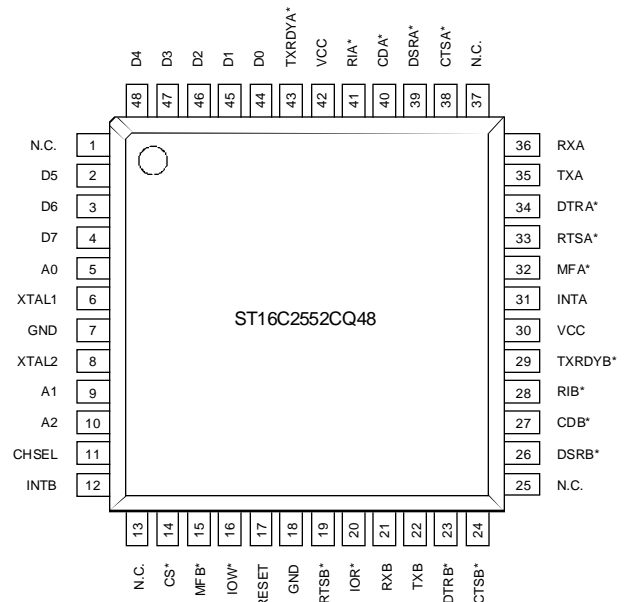
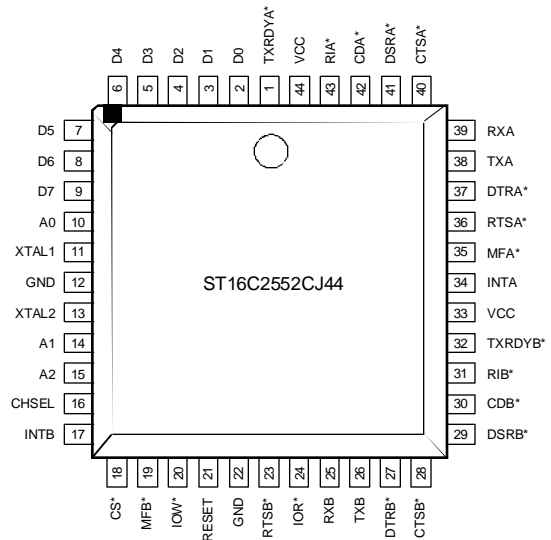
FEATURES

- Pin to pin and functional compatible to National NS16C552
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Modem control signals (CTS*, RTS*, DSR*, DTR*, RI*, CD*)
- Programmable character lengths (5, 6, 7, 8) bits
- Even, odd, or no parity bit generation and detection
- Status report register
- TTL compatible inputs, outputs
- Independent transmit and receive control
- Software compatible with INS8250, NS16C550
- 460.8 kHz transmit/receive operation with 7.372 MHz crystal or external clock source

ORDERING INFORMATION

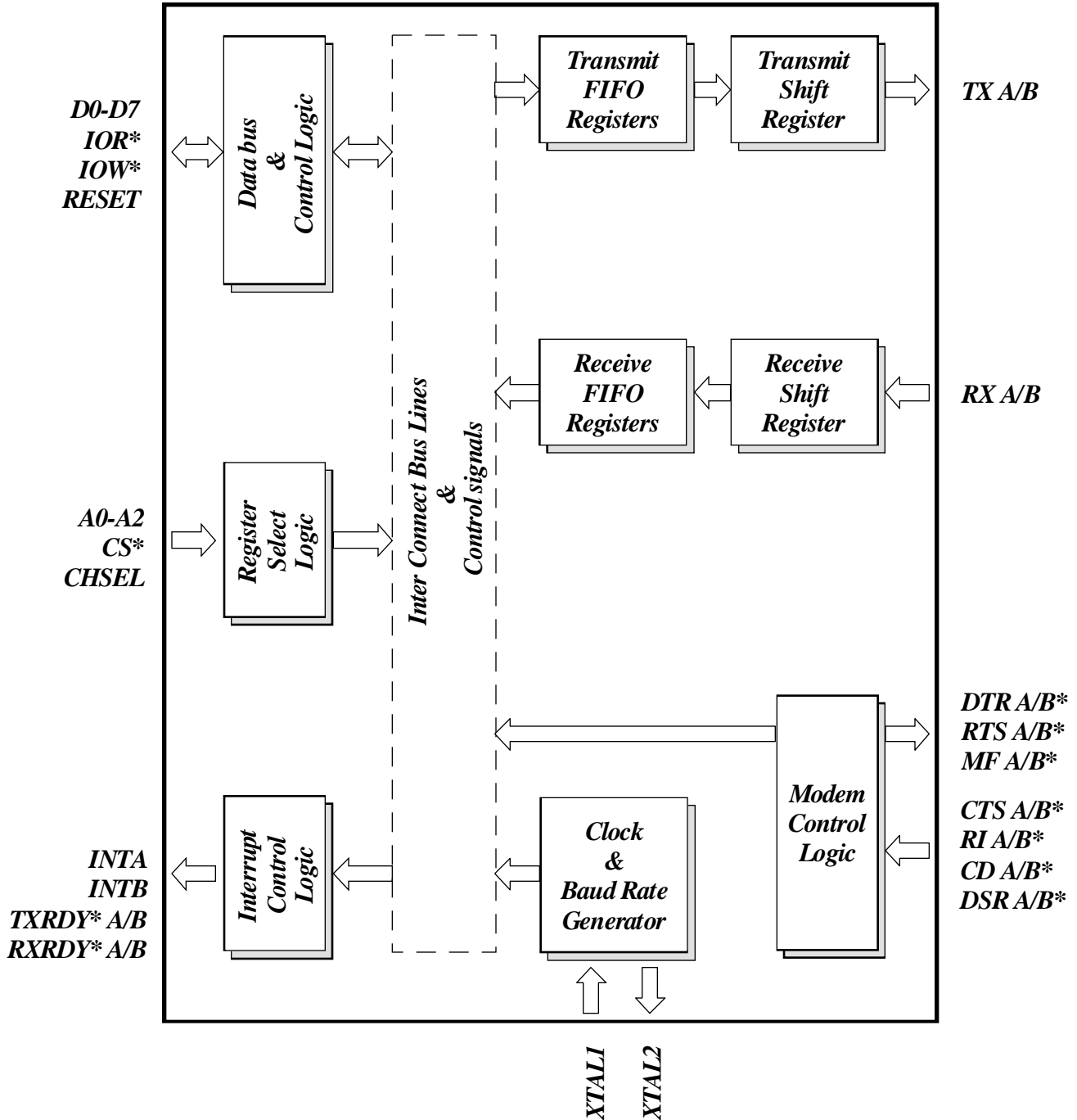
Part number	Package	Operating temperature
ST16C2552CJ44	PLCC	0° C to + 70° C
ST16C2552IJ44	PLCC	-40° C to + 85° C

PLCC Package



ST16C2552

BLOCK DIAGRAM



SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
D0-D7	2-9	I/O	Bi-directional data bus. Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit of the data bus and the first serial data bit to be received or transmitted.
RX A/B	39,25	I	Serial data input A/B. The serial information (data) received from serial port to ST16C2552 receive input circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RX input is disabled from external connection and connected to the TX output internally.
TX A/B	38,26	O	Serial data output A/B. The serial data is transmitted via this pin with additional start, stop and parity bits. The TX will be held in mark (high) state during reset, local loopback mode or when the transmitter is disabled.
CS*	18	I	Chip select. (active low) A low at this pin enables the ST16C2552 / CPU data transfer operation.
CHSEL	16	I	UART A/B select. UART A or B can be selected by changing the state of this pin when CS* is active. Low on this pin, selects the UART B and high on this pin selects UART A section.
XTAL1	11	I	Crystal input 1 or external clock input. A crystal can be connected to this pin and XTAL2 pin to utilize the internal oscillator circuit. An external clock can be used to clock internal circuit and baud rate generator for custom transmission rates.
XTAL2	13	O	Crystal input 2 or buffered clock output. See XTAL1. Should be left open if a clock is connected to XTAL1.
IOW*	20	I	Write strobe. (active low) A low on this pin will transfer the contents of the CPU data bus to the addressed register.
IOR*	24	I	Read strobe. (active low) A low level on this pin transfers the contents of the ST16C2552 data bus to the CPU.
A0-A2	10,14,15	I	Address select lines. To select internal registers.

ST16C2552

ST16C2552

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
INT A/B	34,17	O	Interrupt output A/B. (active high) This pin goes high (when enabled by the interrupt enable register) whenever a receiver error, receiver data available, transmitter empty, or modem status condition flag is detected.
MF* A/B	35,19	O	OP2* (interrupt enable), BAUDOUT* and RXRDY* outputs. These outputs are multiplexed via Alternate Function Register. When output enable function is selected the MF* pin stays high when INT out pin is set to three state mode and goes low when INT pin is enabled. See bit-3 modem control register (MCR bit-3). When BAUDOUT function is selected, the 16 X TX/RX Baud rate clock output is generated. RXRDY function can be selected to use to request a DMA transfer of data from the Receive data FIFO. OP2* is the default signal and it is selected immediately after master reset or power-up.
TXRDY* A/B	1,32	O	Transmit ready. (active low) This pin goes high when the transmit FIFO of the ST16C2552 is full. It can be used as a single or multi-transfer.
RTS* A/B	36,23	O	Request to send A/B (active low). To indicate that the transmitter has data ready to send. Writing a "1" in the modem control register (MCR bit-1) will set this pin to a low state. After the reset this pin will be set to high. Note that this pin does not have any effect on the transmit or receive operation.
DTR* A/B	37,27	O	Data terminal ready A/B (active low). To indicate that ST16C2552 is ready to receive data. This pin can be controlled via the modem control register (MCR bit-0). Writing a "1" at the MCR bit-0 will set the DTR* output to low. This pin will be set to high state after writing a "0" to that register or after the reset . Note that this pin does not have any effect on the transmit or receive operation.
RESET	21	I	Master reset. (active high) A high on this pin will reset all the outputs and internal registers. The transmitter output and the receiver input will be disabled during reset time.

SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
CTS* A/B	40,28	I	Clear to send A/B (active low). The CTS* signal is a MODEM control function input whose conditions can be tested by reading the MSR BIT-4. CTS* has no effect on the transmit or receive operation.
DSR* A/B	41,29	I	Data set ready A/B (active low). A low on this pin indicates the MODEM is ready to exchange data with UART. This pin does not have any effect on the transmit or receive operation.
CD* A/B	42,30	I	Carrier detect A/B (active low). A low on this pin indicates the carrier has been detected by the modem.
RI* A/B	43,31	I	Ring detect indicator A/B (active low). A low on this pin indicates the modem has received a ringing signal from telephone line.
VCC	33,44	I	Power supply input.
GND	12,22	O	Signal and power ground.

PROGRAMMING TABLE

A2	A1	A0	READ MODE	WRITE MODE
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
0	0	0		LSB of Divisor Latch
0	0	1		MSB of Divisor Latch
0	1	0	Alternate Function Register	Alternate Function Register

ST16C2552

ST16C2552 ACCESSIBLE REGISTERS A/B

A2 A1 A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0 0 0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER	0	0	0	0	modem status interrupt	receive line status interrupt	transmit holding register	receive holding register
0 1 0	FCR	RCVR trigger MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR	0/ FIFOs enabled	0/ FIFOs enabled	0	0	int priority bit-2	int priority bit-1	int priority bit-0	int status
0 1 1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR	0	0	0	loop back	OP2*	OP1*	RTS*	DTR*
1 0 1	LSR	0/ FIFO error	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR	CD	RI	DSR	CTS	delta CD*	delta RI*	delta DSR*	delta CTS*
1 1 1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8
0 1 0	AFR	0	0	0	0	0	MF* sel-1	MF* sel-0	SP write

These registers are accessible only when LCR bit-7 is set to "1".

REGISTER FUNCTIONAL DESCRIPTIONS

TRANSMIT AND RECEIVE HOLDING REGISTER

The serial transmitter section consists of a Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the transmit hold register is provided in the Line Status Register (LSR). Writing to this register (THR) will transfer the contents of data bus (D7-D0) to the Transmit holding register whenever the transmitter holding register or transmitter shift register is empty. The transmit holding register empty flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RX is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RX input. Receiver status codes will be posted in the Line Status Register.

FIFO INTERRUPT MODE OPERATION

When the receive FIFO (FCR BIT-0=1) and receive interrupts (IER BIT-0=1) are enabled, receiver interrupt will occur as follows:

- A) The receive data available interrupts will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.
- B) The ISR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.
- C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receiver FIFO. It is reset when the FIFO is empty.

FIFO POLLED MODE OPERATION

When FCR BIT-0=1; resetting IER BIT 3-0 to zero puts the ST16C2552 in the FIFO polled mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode operation by utilizing the Line Status Register.

- A) LSR BIT-0 will be set as long as there is one byte in the receive FIFO.
- B) LSR BIT4-1 will specify which error(s) has occurred.
- C) LSR BIT-5 will indicate when the transmit FIFO is empty.
- D) LSR BIT-6 will indicate when both transmit FIFO and transmit shift register are empty.
- E) LSR BIT-7 will indicate when there are any errors in the receive FIFO.

PROGRAMMABLE BAUD RATE GENERATOR

Each UART section of the ST16C2552 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC-24 MHz and dividing it by any divisor from 1 to $2^{16}-1$. The output frequency of the Baudout* is equal to 16X of transmission baud rate (Baudout*=16 x Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

INTERRUPT ENABLE REGISTER (IER)

The Interrupt Enable Register (IER) masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INT output pin.

IER BIT-0:

- 0=disable the receiver ready interrupt.
- 1=enable the receiver ready interrupt.

ST16C2552

IER BIT-1:

0=disable the transmitter empty interrupt.
1=enable the transmitter empty interrupt.

IER BIT-2:

0=disable the receiver line status interrupt.
1=enable the receiver line status interrupt.

IER BIT-3:

0=disable the modem status register interrupt.
1=enable the modem status register interrupt.

IER BIT 4-7:

All these bits are set to logic zero.

INTERRUPT STATUS REGISTER (ISR)

The ST16C2552 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register (ISR) provides the source of the interrupt in prioritized matter. During the read cycle the ST16C2552 provides the highest interrupt level to be serviced by CPU. No other interrupts are acknowledged until the particular interrupt is serviced. The following are the prioritized interrupt levels:

Priority level

P	D3	D2	D1	D0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2*	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY(Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

*RECEIVE TIME-OUT:

This mode is enabled when STARTECH UART is operating in FIFO mode. Receive time out will not occur if the receive FIFO is empty. The time out counter will be reset at the center of each stop bit received or each time receive holding register is read. The actual time out value is T (Time out length in bits)= $4 \times P$ (Programmed word length) + 12. To convert time out value to a character value, user has to divide this number to its complete word length + parity (if used) + number of stop bits and start bit.

Example -A: If user programs the word length = 7, and no parity and one stop bit, Time out will be:

$$T = 4 \times 7(\text{programmed word length}) + 12 = 40 \text{ bits}$$

$$\text{Character time} = 40 / 9 [(\text{programmed word length} = 7) + (\text{stop bit} = 1) + (\text{start bit} = 1)] = 4.4 \text{ characters.}$$

Example -B: If user programs the word length = 7, with parity and one stop bit, the time out will be:

$$T = 4 \times 7(\text{programmed word length}) + 12 = 40 \text{ bits}$$

$$\text{Character time} = 40 / 10 [(\text{programmed word length} = 7) + (\text{parity} = 1) + (\text{stop bit} = 1) + (\text{start bit} = 1)] = 4 \text{ characters.}$$

ISR BIT-0:

0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.

1=no interrupt pending.

ISR BIT 1-3:

Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 4-7:

These bits are not used and are set to zero if the FIFOs are not enabled. **BIT 6-7:** are set to "1" when the FIFOs are enabled.

FIFO CONTROL REGISTER (FCR)

This register is used to enable the FIFOs, clear the FIFOs, set the receiver FIFO trigger level, and select the type of DMA signaling.

FCR BIT-0:

0=Disable the transmit and receive FIFO.
1=Enable the transmit and receive FIFO.

FCR BIT-1:

0=No change.

1=Clears the contents of the receive FIFO and resets its counter logic to 0 (the receive shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-2:

0=No change.

1=Clears the contents of the transmit FIFO and resets its counter logic to 0 (the transmit shift register is not cleared or altered). This bit will return to zero after clearing the FIFOs.

FCR BIT-3:

0=No change.

1=Changes RXRDY and TXRDY pins from mode “0” to mode “1”.

Transmit operation in mode “0”:

When ST16C2552 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) when there are no characters in the transmit FIFO or transmit holding register, the TXRDY* pin will go low. Once active the TXRDY* pin will go high (inactive) after the first character is loaded into the transmit holding register.

Receive operation in mode “0”:

When ST16C2552 is in ST16C450 mode (FCR bit-0=0) or in the FIFO mode (FCR bit-0=1, FCR bit-3=0) and there is at least 1 character in the receive FIFO, the RXRDY* pin will go low. Once active the RXRDY* pin will go high (inactive) when there are no more characters in the receiver.

Transmit operation in mode “1”:

When ST16C2552 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) the TXRDY* pin will become high (inactive) when the transmit FIFO is completely full. It will be low if one or more FIFO locations are empty.

Receive operation in mode “1”:

When ST16C2552 is in ST16C550 mode (FCR bit-0=1, FCR bit-3=1) and the trigger level or the timeout has been reached, the RXRDY* pin will go low. Once it is activated it will go high (inactive) when there are

no more characters in the FIFO.

FCR BIT 4-5:

Not used.

FCR BIT 6-7:

These bits are used to set the trigger level for the receiver FIFO interrupt.

BIT-7	BIT-6	FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

ALTERNATE FUNCTION REGISTER (AFR)

This is a read/write register used to select specific modes of MF* operation and to allow both UART registers sets to be written concurrently.

AFR BIT-0:

When this bit is set, CPU can write concurrently to the same register in both UARTs. This function is intended to reduce the dual UART initialization time. It can be used by CPU when both channels are initialized to the same state. CPU can set or clear this bit by accessing either register set. When this bit is set the channel select pin still selects the channel to be accessed during read operation. Setting or clearing this bit has no effect on read operations.

The user should ensure that LCR Bit-7 of both channels are in the same state before executing a concurrent write to the registers at address 0,1, or 2.

AFR BIT 1-2:

Combinations of these bits selects one of the MF* functions.

ST16C2552

BIT-2	BIT-1	MF* Function
0	0	OP2*
0	1	BAUDOUT*
1	0	RXRDY*
1	1	Reserved

AFR BIT 3-7:

Not used. All these bits are set to logic zero.

LINE CONTROL REGISTER (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:

These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2:

The number of stop bits can be specified by this bit.

BIT-2	Word length	Stop bit(s)
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:

Parity or no parity can be selected via this bit.
0=no parity

1=a parity bit is generated during the transmission, receiver also checks for received parity.

LCR BIT-4:

If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.

0=ODD parity is generated by forcing an odd number of 1's in the transmitted data, receiver also checks for same format.

1= EVEN parity bit is generated by forcing an even number of 1's in the transmitted data, receiver also checks for same format.

LCR BIT-5:

If the parity bit is enabled, LCR BIT-5 selects the forced parity format.

LCR BIT-5=1 and LCR BIT-4=0, parity bit is forced to "1" in the transmitted and received data.

LCR BIT-5=1 and LCR BIT-4=1, parity bit is forced to "0" in the transmitted and received data.

LCR BIT-6:

Break control bit. It causes a break condition to be transmitted (the TX is forced to low state).

0=normal operating condition.

1=forces the transmitter output (TX) to go low to alert the communication terminal.

LCR BIT-7:

The internal baud rate counter latch enable (DLAB).

0=normal operation.

1=select Divisor Latch Register and Alternate Function Register.

MODEM CONTROL REGISTER (MCR)

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:

0=force DTR* output to high.

1=force DTR* output to low.

MCR BIT-1:

0=force RTS* output to high.

1=force RTS* output to low.

MCR BIT-2:

Not used except in local loop-back mode.

MCR BIT-3:

0=force OP2* output to high.
1=force OP2* output to low.

MCR BIT-4:

0=normal operating mode.
1=enable local loop-back mode (diagnostics). The transmitter output (TX) is set high (Mark condition), the receiver input (RX), CTS*, DSR*, CD*, and RI* are disabled. Internally the transmitter output is connected to the receiver input and DTR*, RTS*, OP1* and OP2* are connected to modem control inputs. In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the IER.

MCR BIT 5-7:

Not used. Are set to zero permanently.

LINE STATUS REGISTER (LSR)

This register provides the status of data transfer to CPU.

LSR BIT-0:

0=no data in receive holding register or FIFO.
1=data has been received and saved in the receive holding register or FIFO.

LSR BIT-1:

0=no overrun error (normal).
1=overrun error, next character arrived before receive holding register was emptied or if FIFOs are enabled, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. Note that character in the shift register is overwritten, but it is not transferred to the FIFO.

LSR BIT-2:

0=no parity error (normal).
1=parity error, received data does not have correct parity information. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-3:

0=no framing error (normal).
1=framing error received, received data did not have a valid stop bit. In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:

0=no break condition (normal).
1=receiver received a break signal (RX was low for one character time frame). In FIFO mode, only one zero character is loaded into the FIFO.

LSR BIT-5:

0=transmit holding register is full. ST16C2552 will not accept any data for transmission.
1=transmit holding register (or FIFO) is empty. CPU can load the next character.

LSR BIT-6:

0=transmitter holding and shift registers are full.
1=transmitter holding and shift registers are empty. In FIFO mode this bit is set to one whenever the transmitter FIFO and transmit shift register are empty.

LSR BIT-7:

0=Normal.
1=At least one parity error, framing error or break indication in the FIFO. This bit is cleared when LSR is read.

MODEM STATUS REGISTER (MSR)

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

ST16C2552

MSR BIT-0:

Indicates that the CTS* input to the ST16C2552 has changed state since the last time it was read.

MSR BIT-1:

Indicates that the DSR* input to the ST16C2552 has changed state since the last time it was read.

MSR BIT-2:

Indicates that the RI* input to the ST16C2552 has changed from a low to a high state.

MSR BIT-3:

Indicates that the CD* input to the ST16C2552 has changed state since the last time it was read.

MSR BIT-4:

This bit is equivalent to RTS in the MCR during local loop-back mode. It is the compliment of the CTS* input.

MSR BIT-5:

This bit is equivalent to DTR in the MCR during local loop-back mode. It is the compliment of the DSR* input.

MSR BIT-6:

This bit is equivalent to OP1 in the MCR during local loop-back mode. It is the compliment of the RI* input.

MSR BIT-7:

This bit is equivalent to OP2 in the MCR during local loop-back mode. It is the compliment to the CD* input.

Note: Whenever MSR BIT3-0: is set to logic "1", a MODEM Status Interrupt is generated.

SCRATCHPAD REGISTER (SR)

ST16C2552 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
150	768	
300	384	
600	192	
1200	96	
2400	48	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.77
115.2K	1	

ST16C2552 EXTERNAL RESET CONDITION

REGISTERS	RESET STATE
IER	IER BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0
MFR	AFR BITS 0-7=0

SIGNALS	RESET STATE
TX	High
OP2*	High
RTS*	High
DTR*	High
INT	Low
TXRDY*	Low

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

$T_A=0^\circ - 70^\circ \text{ C}$, $V_{CC}=5.0 \text{ V} \pm 10\%$ unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
V_{ILCK}	Clock input low level	-0.5		0.6	V	$I_{OL}= 6 \text{ mA}$ $I_{OH}= -6 \text{ mA}$
V_{IHCK}	Clock input high level	3.0		VCC	V	
V_{IL}	Input low level	-0.5		0.8	V	
V_{IH}	Input high level	2.2		VCC	V	
V_{OL}	Output low level on all outputs			0.4	V	
V_{OH}	Output high level	2.4			V	
I_{CC}	Avg. power supply current		2	2.5	mA	
I_{IL}	Input leakage			± 10	μA	
I_{CL}	Clock leakage			± 10	μA	

This product can operate in 3.0 Volts environment. Please consult with factory for additional information.

ST16C2552

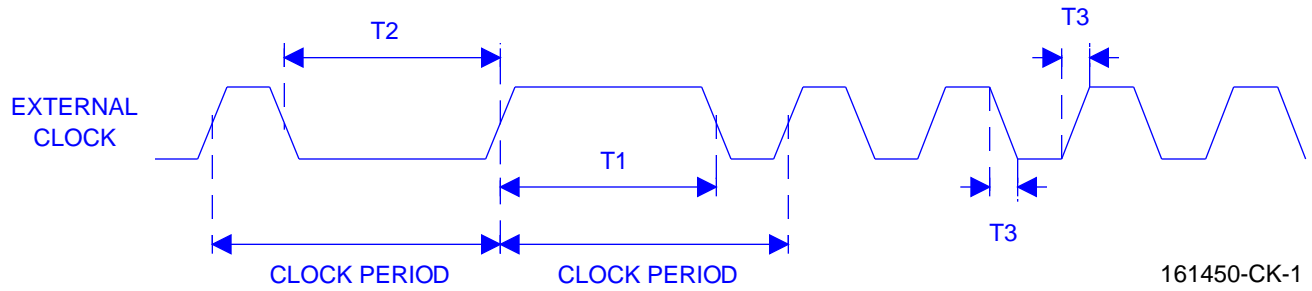
AC ELECTRICAL CHARACTERISTICS

$T_A=0^\circ - 70^\circ \text{ C}$, $V_{CC}=5.0 \text{ V} \pm 10\%$ unless otherwise specified.

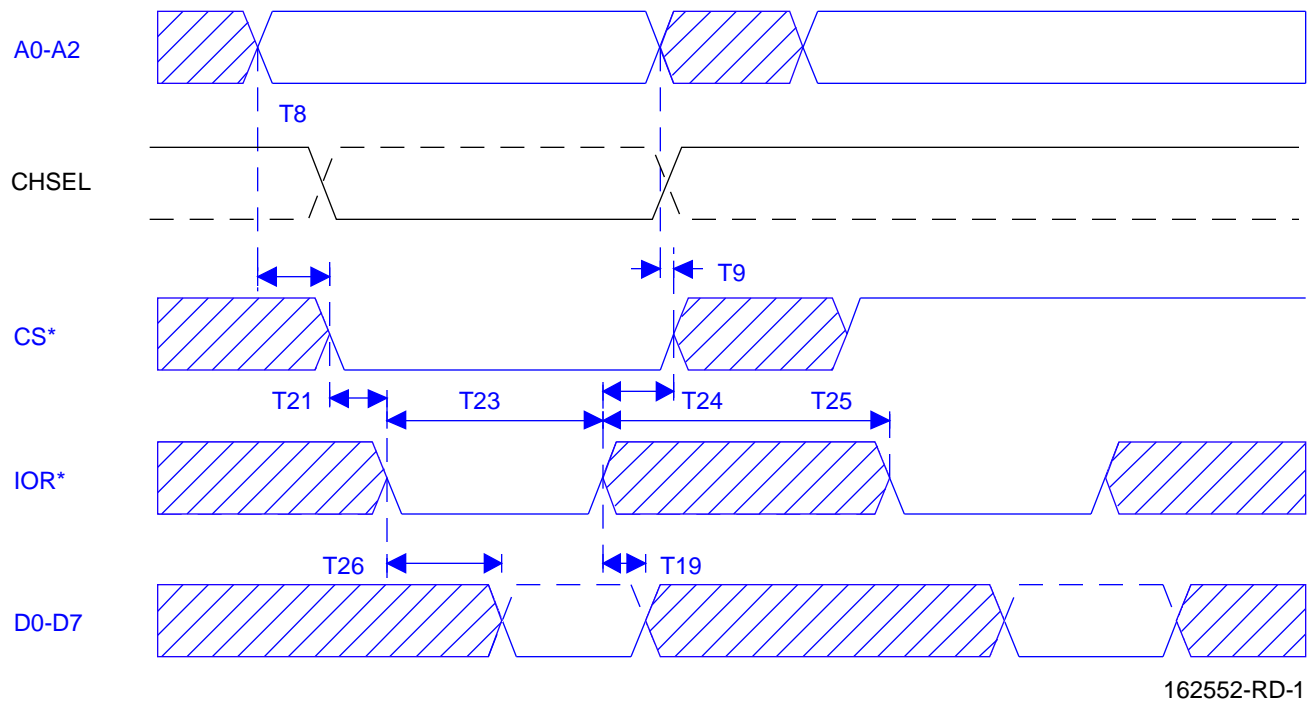
Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
T_1	Clock high pulse duration	20			ns	
T_2	Clock low pulse duration	20			ns	
T_3	Clock rise/fall time			10	ns	
T_8	Chip select setup time	0			ns	
T_9	Chip select hold time	0			ns	
T_{12}	Data set up time	15			ns	
T_{13}	Data hold time	15			ns	
T_{14}	IOW* delay from chip select	10			ns	
T_{15}	IOW* strobe width	50			ns	
T_{16}	Chip select hold time from IOW*	0			ns	
T_{17}	Write cycle delay	55			ns	
T_w	Write cycle= $T_{15}+T_{17}$	105			ns	
T_{19}	Data hold time	15			ns	
T_{21}	IOR* delay from chip select	10			ns	
T_{23}	IOR* strobe width	65			ns	
T_{24}	Chip select hold time from IOR*	0			ns	
T_{25}	Read cycle delay	55			ns	
T_r	Read cycle= $T_{23}+T_{25}$	115			ns	
T_{26}	Delay from IOR* to data			35	ns	100 pF load
T_{28}	Delay from IOW* to output			50	ns	100 pF load
T_{29}	Delay to set interrupt from MODEM input			70	ns	100 pF load
T_{30}	Delay to reset interrupt from IOR*			70	ns	100 pF load
T_{31}	Delay from stop to set interrupt			1_{RCLK}	ns	100 pF load
T_{32}	Delay from IOR* to reset interrupt			200	ns	100 pF load
T_{33}	Delay from initial INT reset to transmit start	8		24	*	
T_{34}	Delay from stop to interrupt			100	ns	
T_{35}	Delay from IOW* to reset interrupt			175	ns	
T_{36}	Delay from initial Write to interrupt	16		24	*	
T_{44}	Delay from stop to set RxRdy			1_{RCLK}		
T_{45}	Delay from IOR* to reset RxRdy			100	ns	
T_{46}	Delay from IOW* to set TxRdy			195	ns	
T_{47}	Delay from start to reset TxRdy			8	*	
T_R	Reset pulse width	10			ns	
N	Baud rate divisor	1		$2^{16}-1$		

Note 1: * = Baudout* cycle

CLOCK TIMING

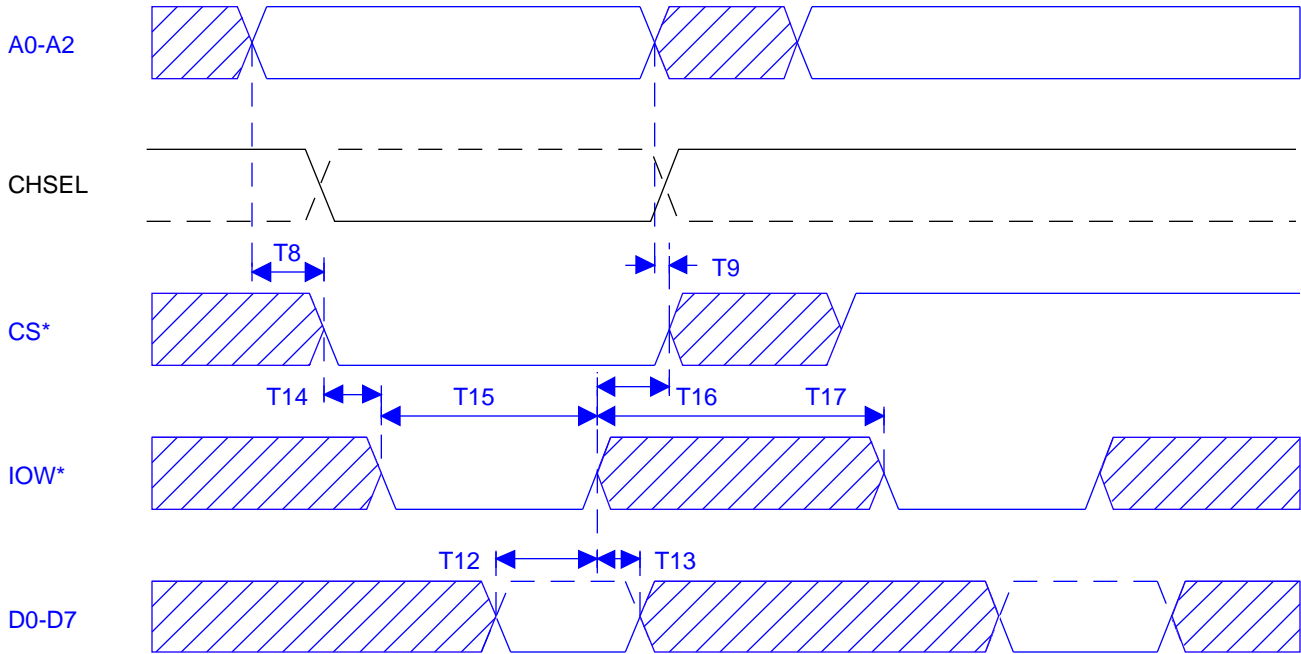


GENERAL READ TIMING



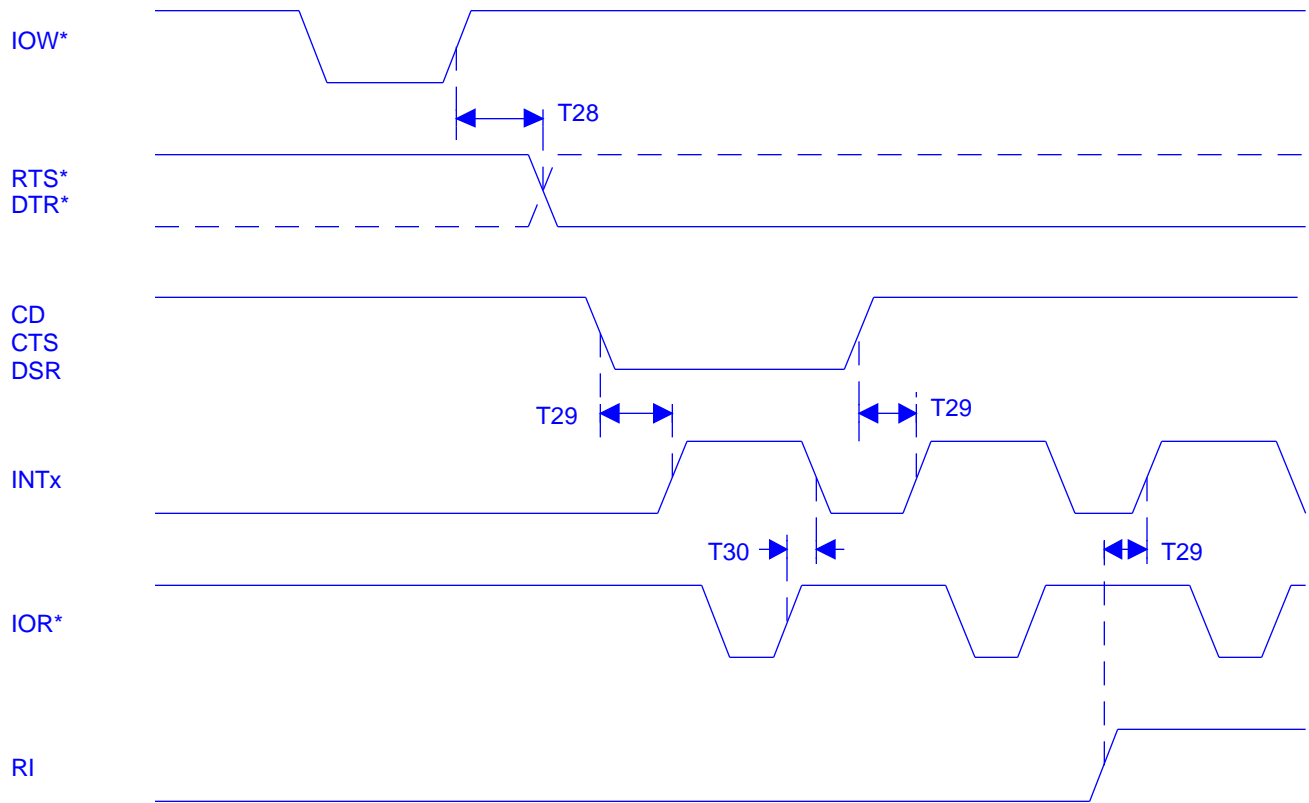
ST16C2552

GENERAL WRITE TIMING



162552-WD-1

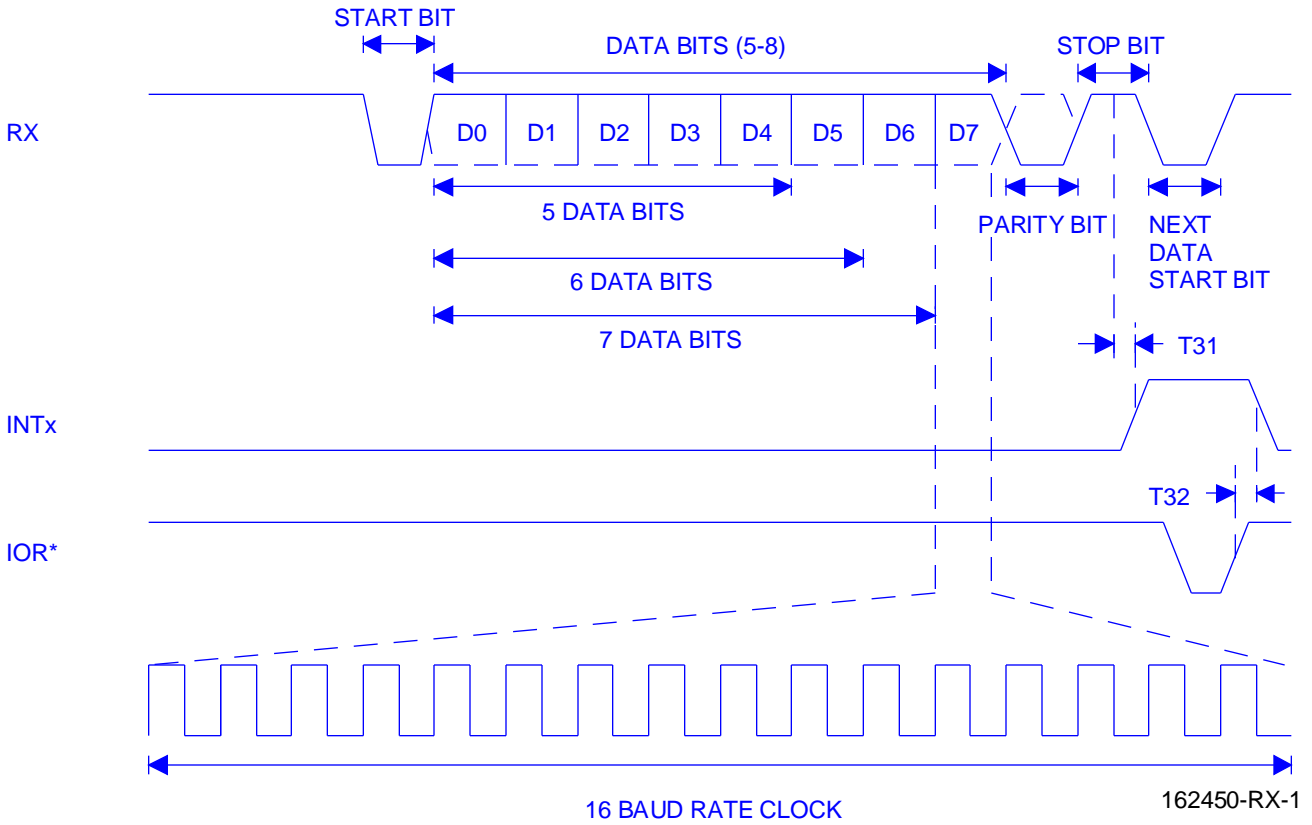
MODEM TIMING



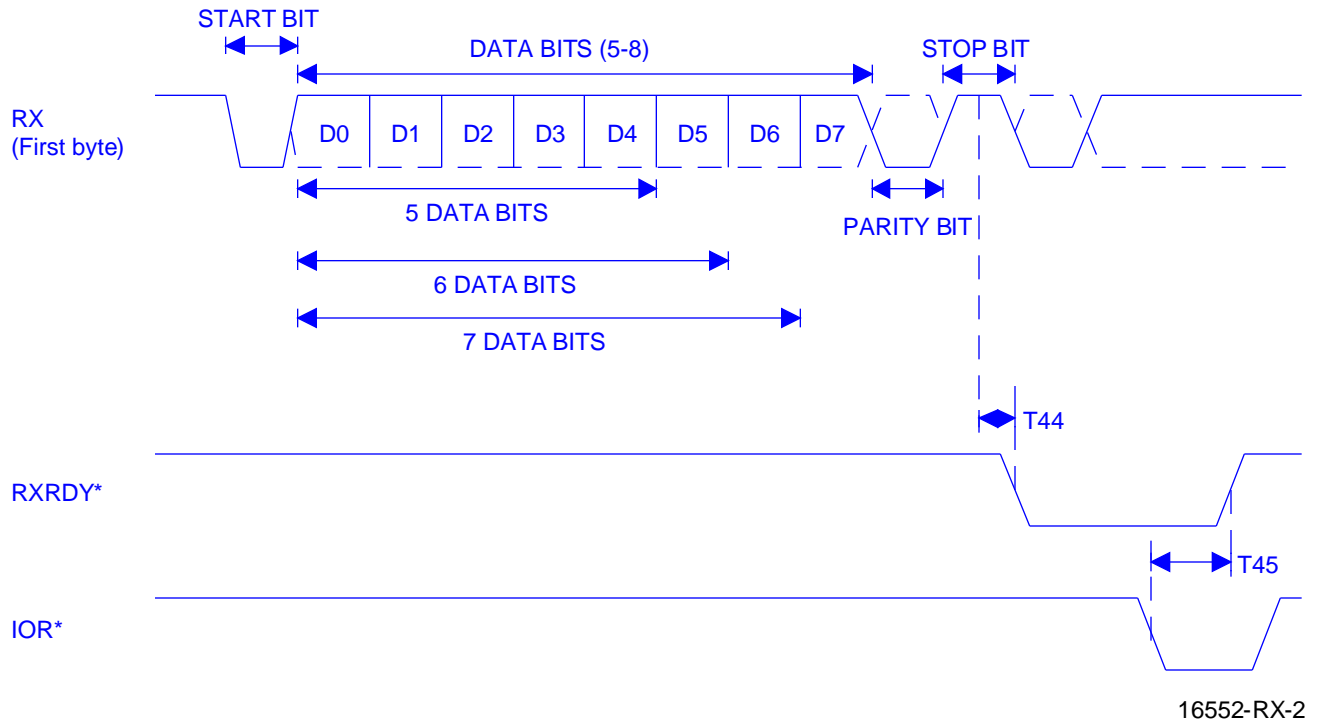
162450-MD-1

ST16C2552

RECEIVE TIMING

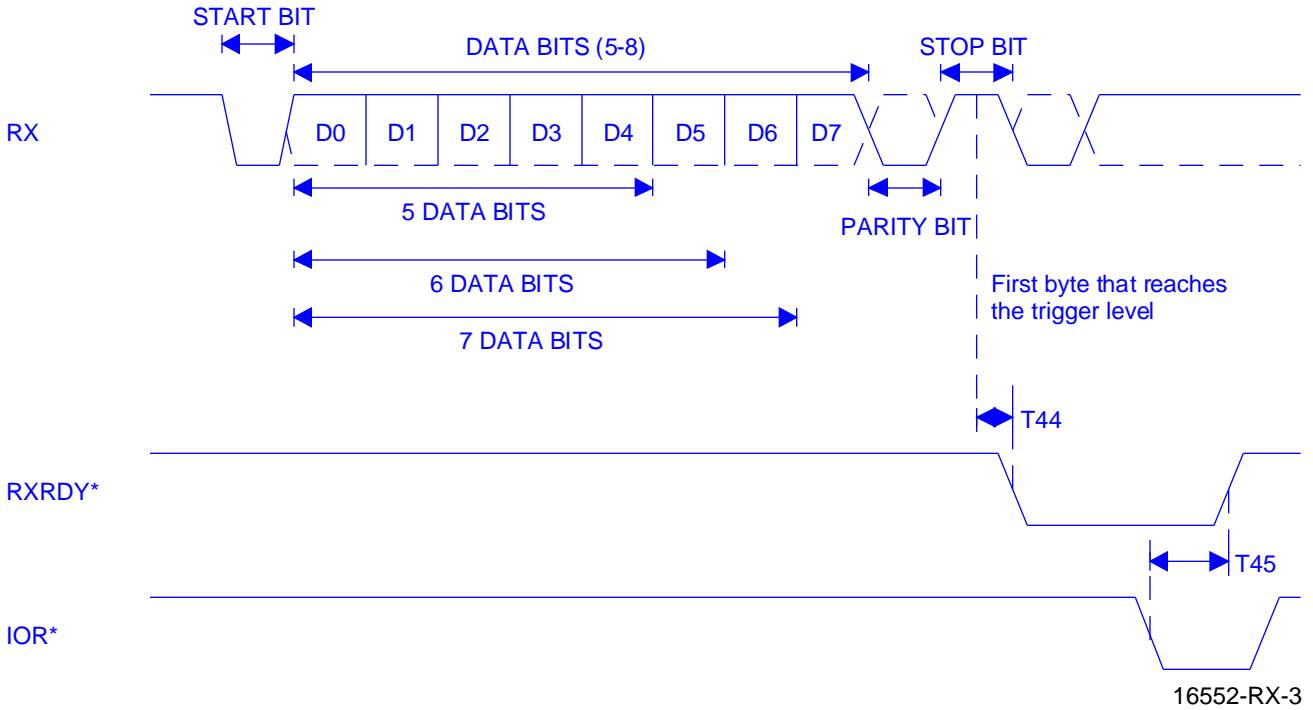


RXRDY TIMING FOR MODE "0"

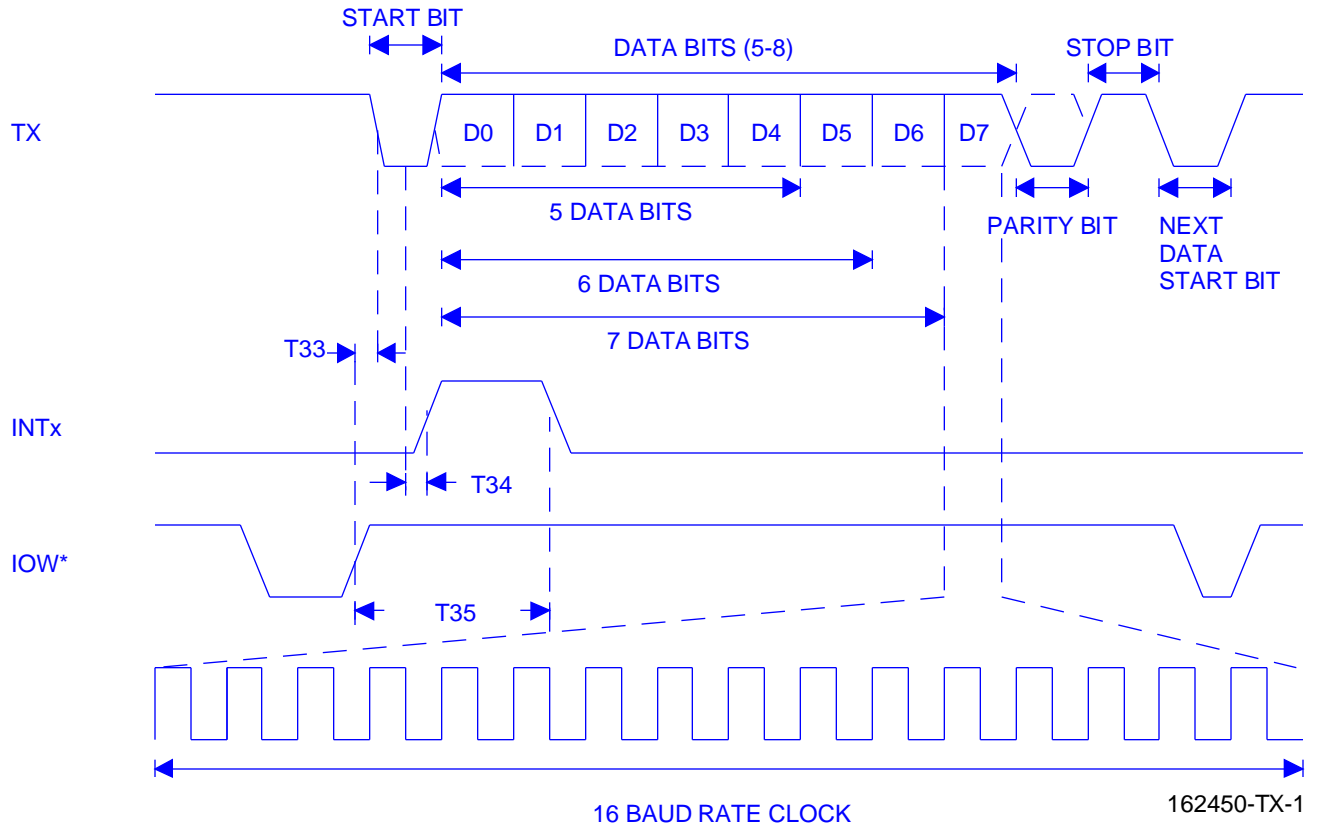


ST16C2552

RXRDY TIMING FOR MODE "1"

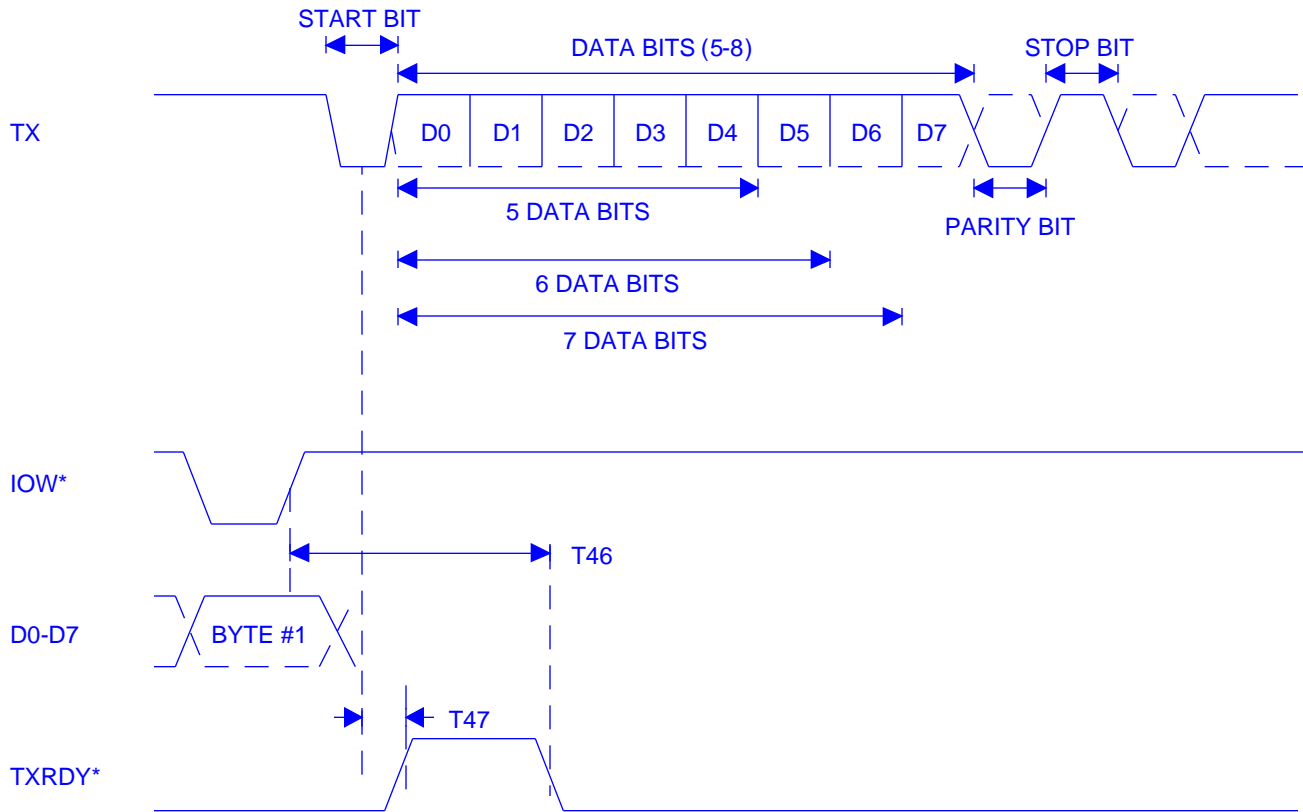


TRANSMIT TIMING



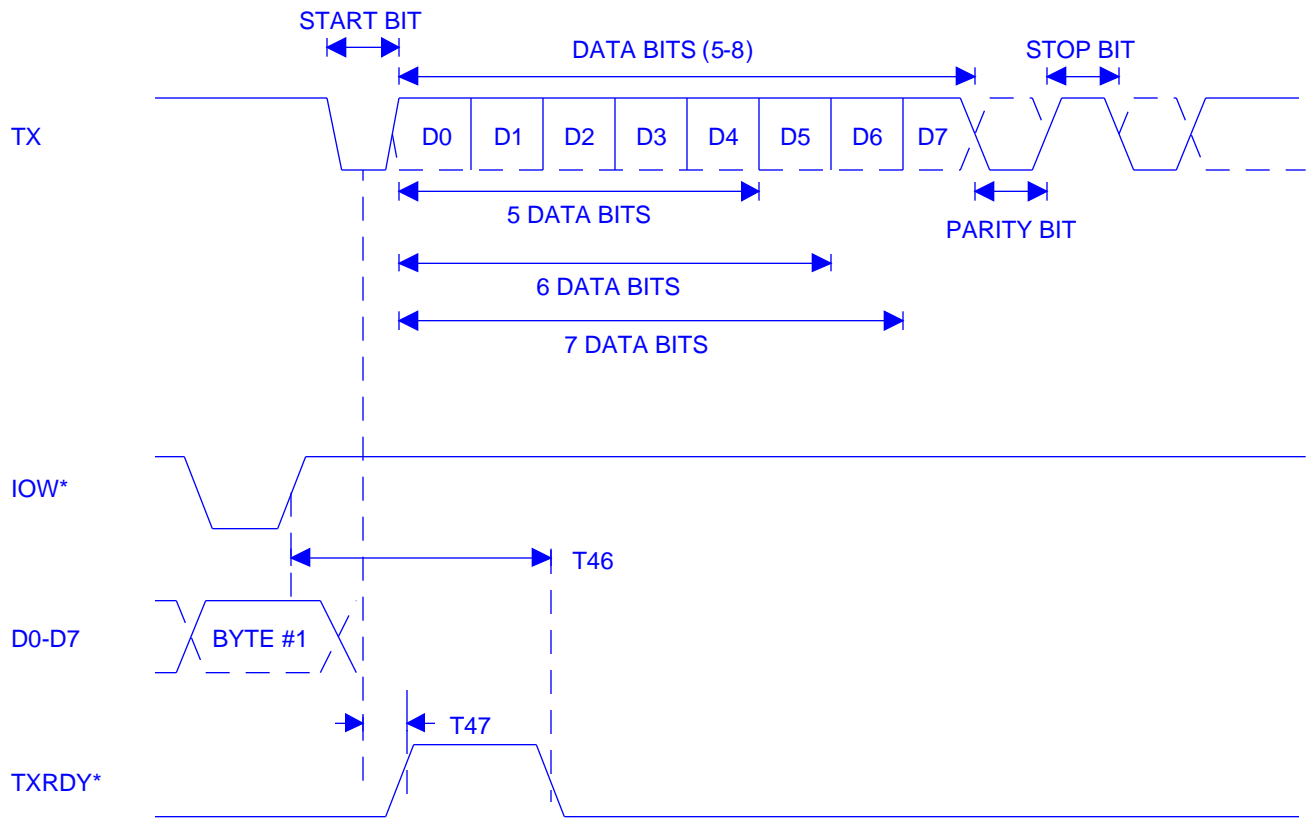
ST16C2552

TXRDY TIMING FOR MODE "0"



162550-TX-2

TXRDY TIMING FOR MODE "0"



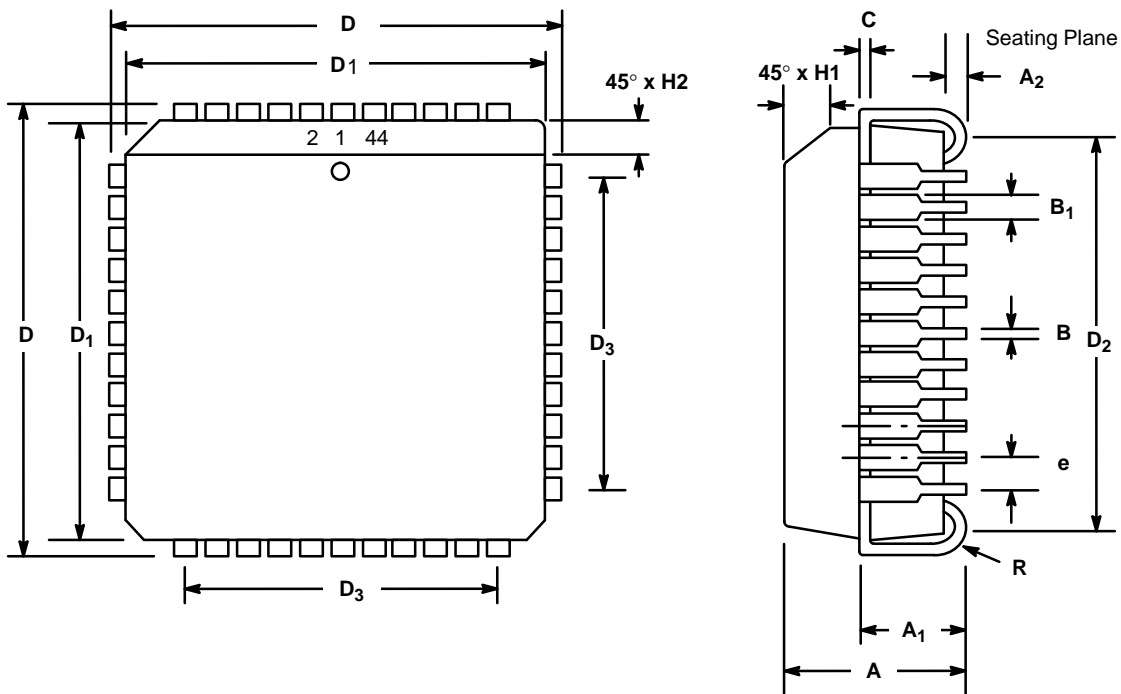
162550-TX-2

ST16C2552

Package Dimensions

44 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A ₁	0.090	0.120	2.29	3.05
A ₂	0.020	—	0.51	—
B	0.013	0.021	0.33	0.53
B ₁	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.685	0.695	17.40	17.65
D ₁	0.650	0.656	16.51	16.66
D ₂	0.590	0.630	14.99	16.00
D ₃	0.500 typ.		12.70 typ.	
e	0.050 BSC		1.27 BSC	
H ₁	0.042	0.056	1.07	1.42
H ₂	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

Note: The control dimension is the inch column

Notes

Notes



NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Copyright 1993 EXAR Corporation

Reproduction, in part or whole, without the prior written consent of EXAR Corporation is prohibited.

