



# 1.8V, *micro*POWER CMOS OPERATIONAL AMPLIFIERS Zero-Drift Series

## FEATURES

- **LOW OFFSET VOLTAGE:** 10 $\mu$ V (max)
- **ZERO DRIFT:** 0.05 $\mu$ V/ $^{\circ}$ C (max)
- **0.01Hz to 10Hz NOISE:** 1.1 $\mu$ V<sub>PP</sub>
- **QUIESCENT CURRENT:** 17 $\mu$ A
- **SINGLE-SUPPLY OPERATION**
- **SUPPLY VOLTAGE:** 1.8V to 5.5V
- **RAIL-TO-RAIL INPUT/OUTPUT**
- ***micro*SIZE PACKAGES:** SC70 and SOT23

## APPLICATIONS

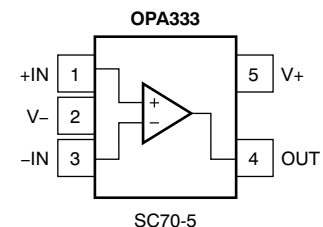
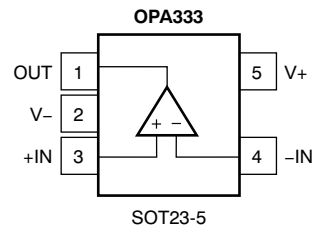
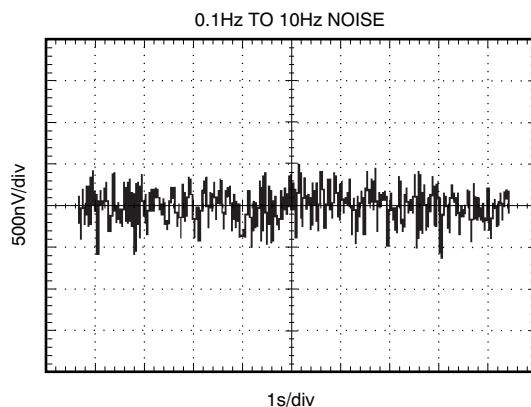
- **TRANSDUCER APPLICATIONS**
- **TEMPERATURE MEASUREMENTS**
- **ELECTRONIC SCALES**
- **MEDICAL INSTRUMENTATION**
- **BATTERY-POWERED INSTRUMENTS**
- **HANDHELD TEST EQUIPMENT**

## DESCRIPTION

The OPA333 series of CMOS operational amplifiers uses a proprietary auto-calibration technique to simultaneously provide very low offset voltage (10 $\mu$ V max) and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100mV beyond the rails and rail-to-rail output that swings within 50mV of the rails. Single or dual supplies as low as +1.8V ( $\pm$ 0.9V) and up to +5.5V ( $\pm$ 2.75V) may be used. They are optimized for low-voltage, single-supply operation.

The OPA333 family offers excellent CMRR without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity.

The OPA333 (single version) is available in the SC70-5, SOT23-5, and SO-8 packages. The OPA2333 (dual version) is offered in DFN-8 (3mm  $\times$  3mm), MSOP-8, and SO-8 packages. All versions are specified for operation from  $-40^{\circ}$ C to  $+125^{\circ}$ C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA333	SOT23-5	DBV	OAXQ
	SC70-5	DCK	BQY
	SO-8	D	O333A
OPA2333	SO-8	D	O2333A
	DFN-8	DRB	BQZ
	MSOP-8	DGK	OBAQ

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

	OPA333, OPA2333	UNIT
Supply Voltage	+7	V
Signal Input Terminals, Voltage <sup>(2)</sup>	−0.3 to (V+) + 0.3	V
Signal Input Terminals, Voltage <sup>(2)</sup>	±10	mA
Output Short-Circuit <sup>(3)</sup>	Continuous	
Operating Temperature	−40 to +150	°C
Storage Temperature	−65 to +150	°C
Junction Temperature	+150	°C
ESD Ratings:		
Human Body Model (HBM)	4000	V
Charged Device Model (CDM)	1000	V
Machine Model (MM)	400	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current limited to 10mA or less.
- (3) Short-circuit to ground, one amplifier per package.

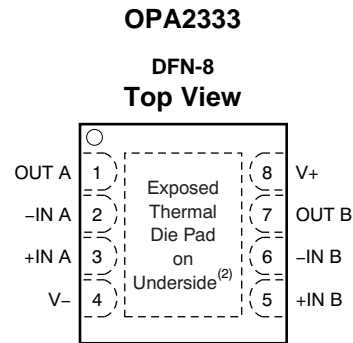
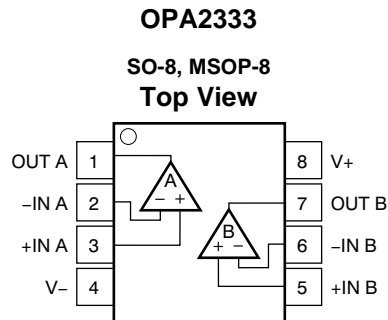
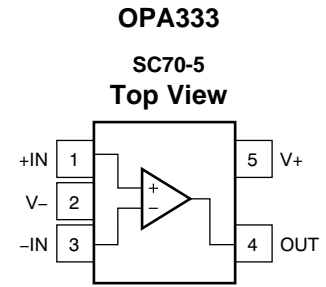
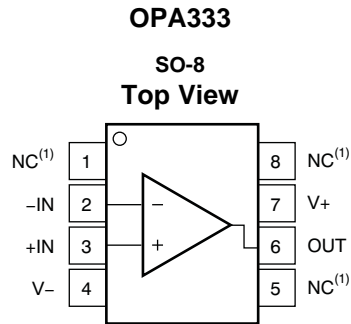
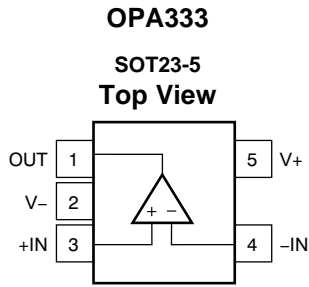
**ELECTRICAL CHARACTERISTICS:  $V_S = +1.8V$  to  $+5.5V$** 
**Boldface** limits apply over the specified temperature range,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ .

 At  $T_A = +25^{\circ}C$ ,  $R_L = 10k\Omega$  connected to  $V_S/2$ ,  $V_{CM} = V_S/2$ , and  $V_{OUT} = V_S/2$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	OPA333, OPA2333			UNIT
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b>					
Input Offset Voltage	$V_{OS}$ $V_S = +5V$		2	10	$\mu V$
<b>vs Temperature</b>	$dV_{OS}/dT$		<b>0.02</b>	<b>0.05</b>	$\mu V/^{\circ}C$
<b>vs Power Supply</b>	PSRR $V_S = +1.8V$ to $+5.5V$		<b>1</b>	<b>5</b>	$\mu V/V$
Long-Term Stability <sup>(1)</sup>			See <sup>(1)</sup>		
Channel Separation, dc			0.1		$\mu V/V$
<b>INPUT BIAS CURRENT</b>					
Input Bias Current	$I_B$		$\pm 70$	$\pm 200$	pA
<b>over Temperature</b>			<b><math>\pm 150</math></b>		<b>pA</b>
Input Offset Current	$I_{OS}$		$\pm 140$	$\pm 400$	pA
<b>NOISE</b>					
Input Voltage Noise, $f = 0.01Hz$ to $1Hz$			0.3		$\mu V_{PP}$
Input Voltage Noise, $f = 0.1Hz$ to $10Hz$			1.1		$\mu V_{PP}$
Input Current Noise, $f = 10Hz$	$i_n$		100		fA/ $\sqrt{Hz}$
<b>INPUT VOLTAGE RANGE</b>					
Common-Mode Voltage Range	$V_{CM}$		$(V-) - 0.1$	$(V+) + 0.1$	V
<b>Common-Mode Rejection Ratio</b>	CMRR $(V-) - 0.1V < V_{CM} < (V+) + 0.1V$		<b>106</b>	<b>130</b>	<b>dB</b>
<b>INPUT CAPACITANCE</b>					
Differential			2		pF
Common-Mode			4		pF
<b>OPEN-LOOP GAIN</b>					
<b>Open-Loop Voltage Gain</b>	$A_{OL}$ $(V-) + 100mV < V_O < (V+) - 100mV, R_L = 10k\Omega$		<b>106</b>	<b>130</b>	<b>dB</b>
<b>FREQUENCY RESPONSE</b>					
Gain-Bandwidth Product	GBW $C_L = 100pF$		350		kHz
Slew Rate	SR $G = +1$		0.16		V/ $\mu s$
<b>OUTPUT</b>					
Voltage Output Swing from Rail		$R_L = 10k\Omega$	30	50	mV
<b>over Temperature</b>		$R_L = 10k\Omega$		<b>70</b>	<b>mV</b>
Short-Circuit Current	$I_{SC}$		$\pm 5$		mA
Capacitive Load Drive	$C_L$		See <a href="#">Typical Characteristics</a>		
Open-Loop Output Impedance		$f = 350kHz, I_O = 0$	2		k $\Omega$
<b>POWER SUPPLY</b>					
Specified Voltage Range	$V_S$		1.8	5.5	V
Quiescent Current Per Amplifier	$I_Q$	$I_O = 0$	17	25	$\mu A$
<b>over Temperature</b>				<b>28</b>	<b><math>\mu A</math></b>
Turn-On Time		$V_S = +5V$	100		$\mu s$
<b>TEMPERATURE RANGE</b>					
Specified Range			-40	+125	$^{\circ}C$
Operating Range			-40	+150	$^{\circ}C$
Storage Range			-65	+150	$^{\circ}C$
Thermal Resistance	$\theta_{JA}$				$^{\circ}C/W$
SOT23-5			200		$^{\circ}C/W$
MSOP-8, SO-8			150		$^{\circ}C/W$
DFN-8			50		$^{\circ}C/W$
SC70-5			250		$^{\circ}C/W$

 (1) 300-hour life test at  $+150^{\circ}C$  demonstrated randomly distributed variation of approximately  $1\mu V$ .

**PIN CONFIGURATIONS**

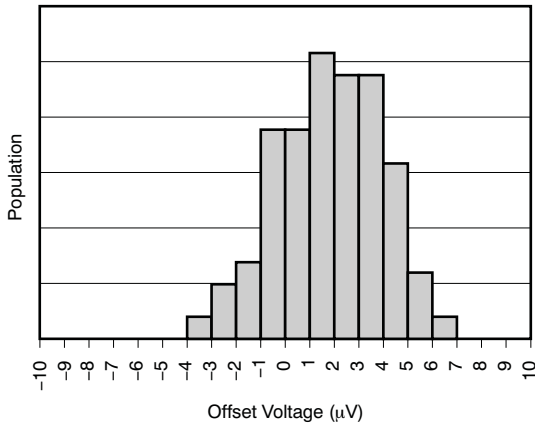


1. NC denotes no internal connection.
2. Connect thermal die pad to V-.

**TYPICAL CHARACTERISTICS**

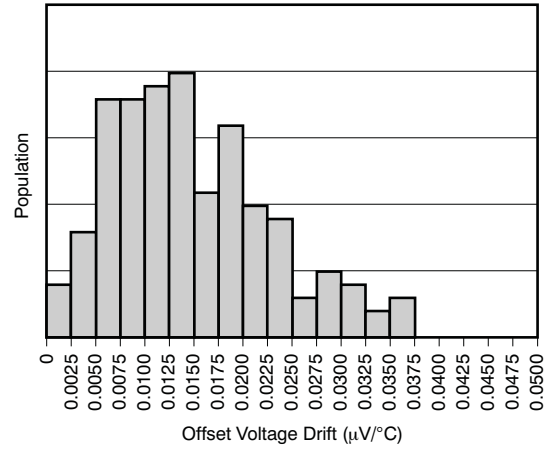
At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $C_L = 0\text{pF}$ , unless otherwise noted.

**OFFSET VOLTAGE PRODUCTION DISTRIBUTION**



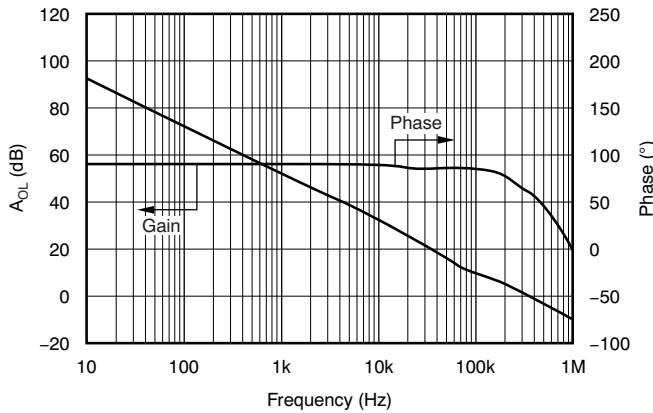
**Figure 1.**

**OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION**



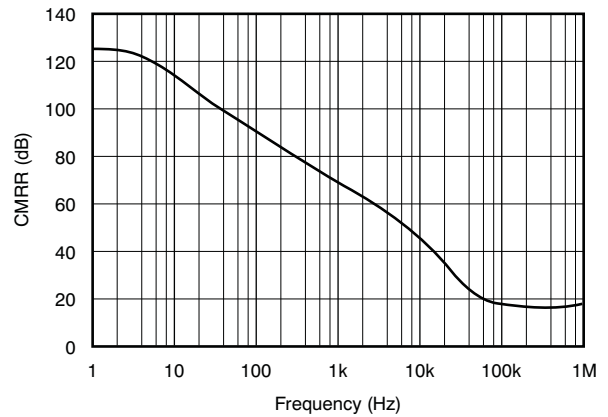
**Figure 2.**

**OPEN-LOOP GAIN vs FREQUENCY**



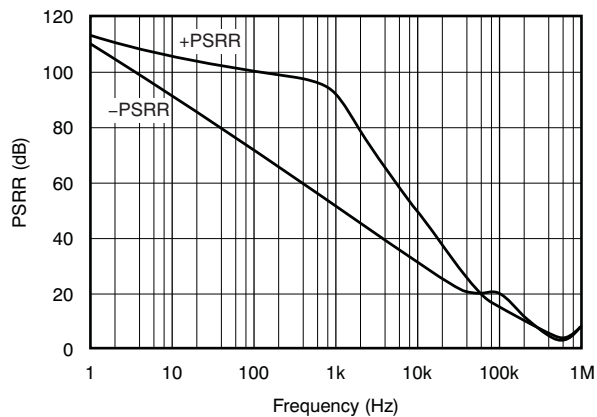
**Figure 3.**

**COMMON-MODE REJECTION RATIO vs FREQUENCY**



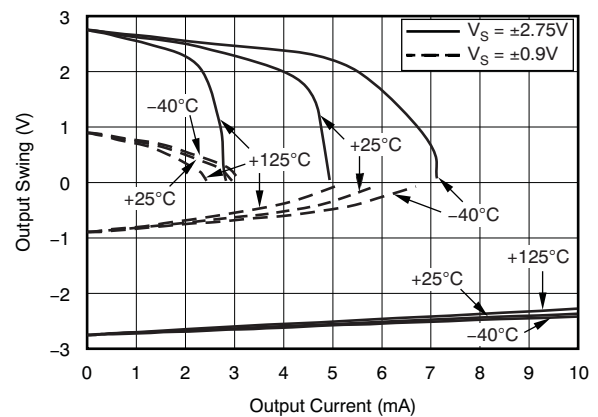
**Figure 4.**

**POWER-SUPPLY REJECTION RATIO vs FREQUENCY**



**Figure 5.**

**OUTPUT VOLTAGE SWING vs OUTPUT CURRENT**



**Figure 6.**

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $C_L = 0\text{pF}$ , unless otherwise noted.

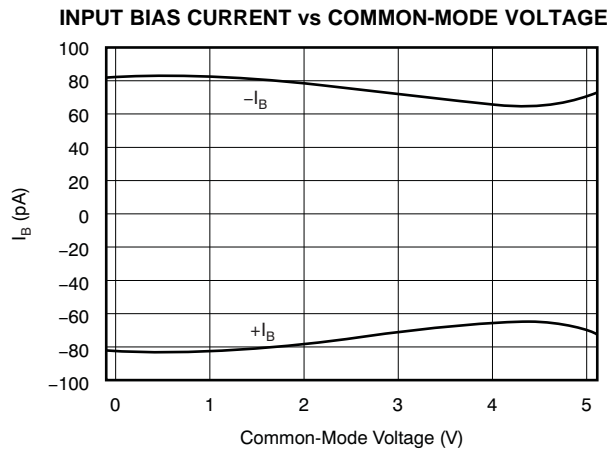


Figure 7.

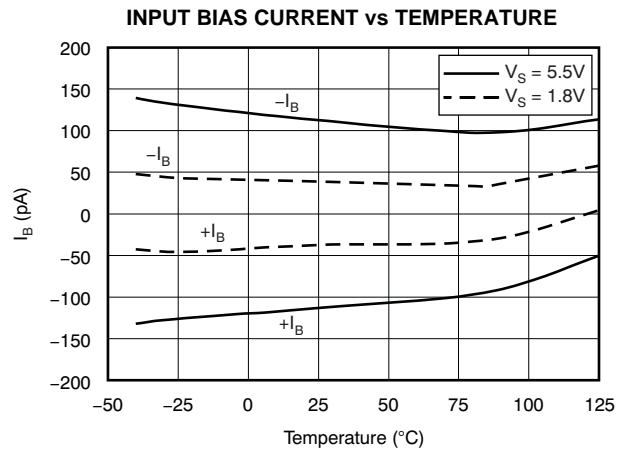


Figure 8.

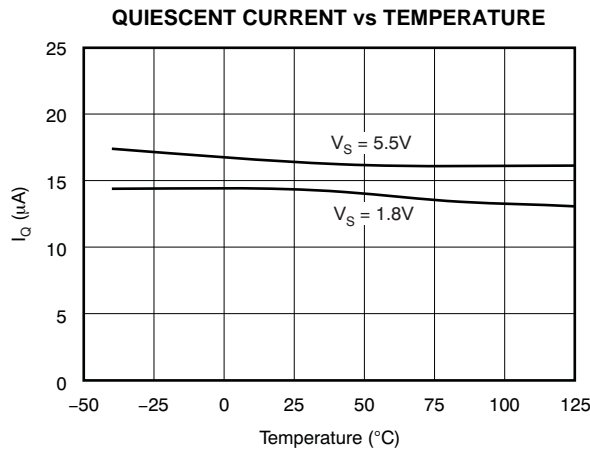


Figure 9.

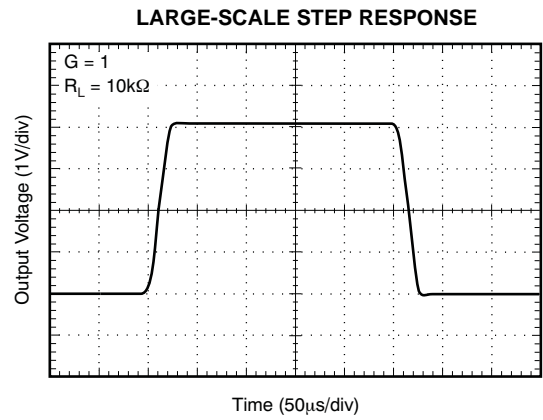


Figure 10.

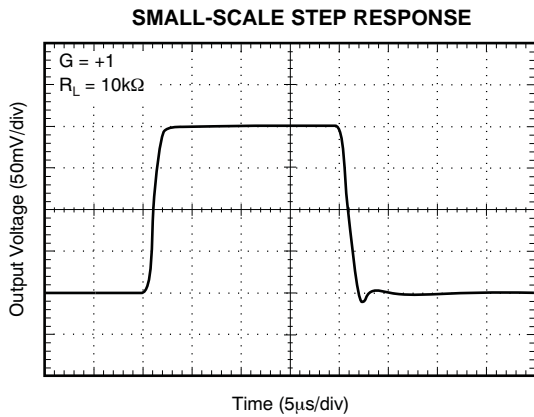


Figure 11.

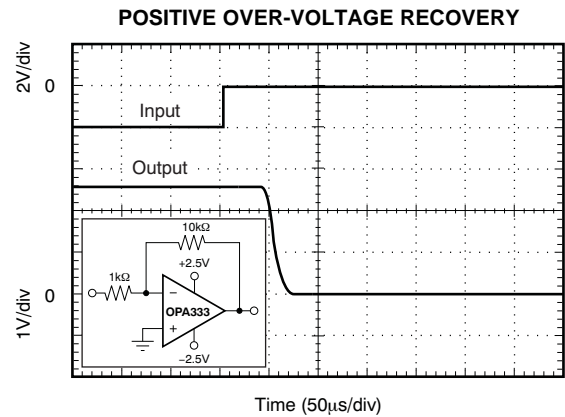


Figure 12.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +5\text{V}$ , and  $C_L = 0\text{pF}$ , unless otherwise noted.

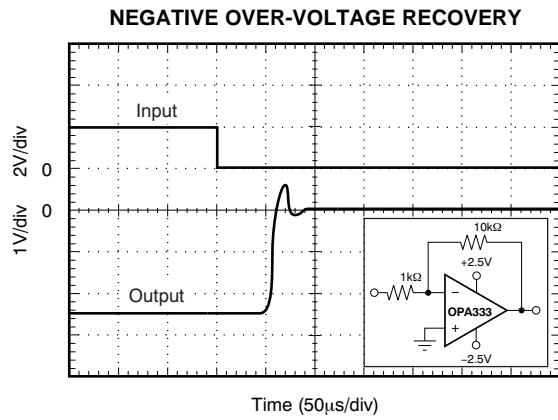


Figure 13.

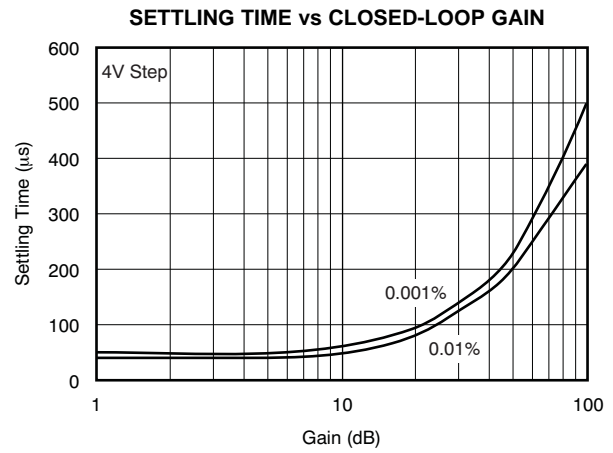


Figure 14.

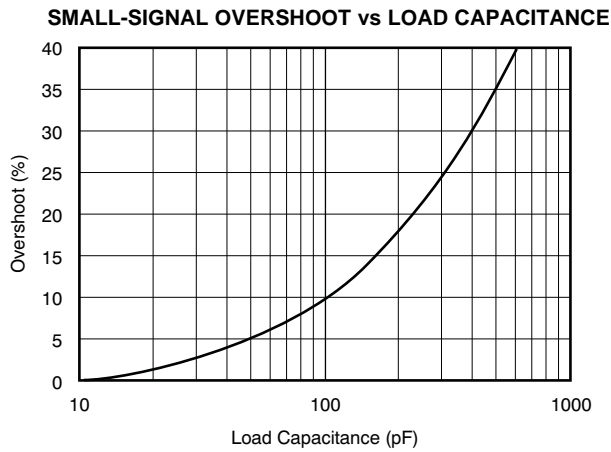


Figure 15.

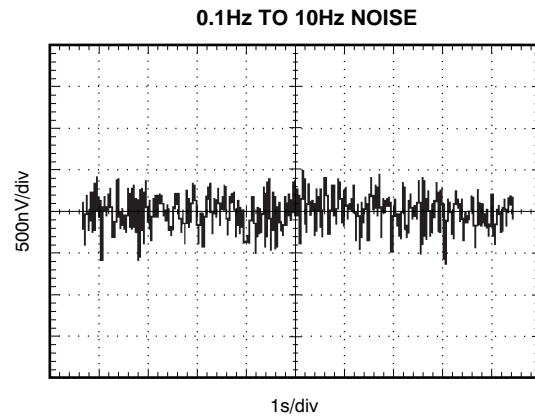


Figure 16.

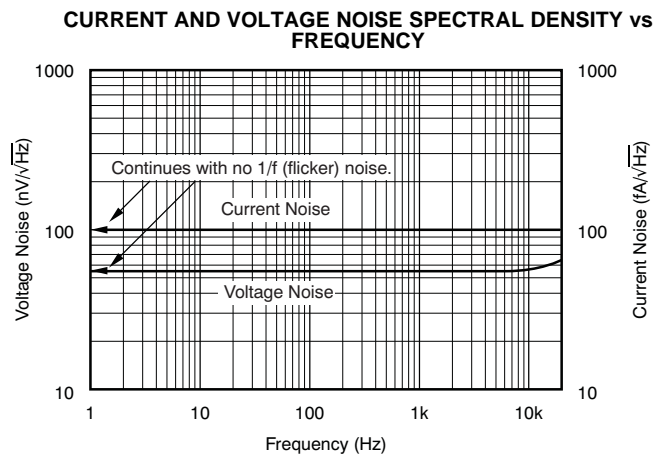


Figure 17.

## APPLICATIONS INFORMATION

The OPA333 and OPA2333 are unity-gain stable and free from unexpected output phase reversal. They use a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of  $0.1\mu\text{V}/^\circ\text{C}$  or higher, depending on materials used.

### OPERATING VOLTAGE

The OPA333 and OPA2333 op amps operate over a power-supply range of +1.8V to +5.5V ( $\pm 0.9\text{V}$  to  $\pm 2.75\text{V}$ ). Supply voltages higher than +7V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the [Typical Characteristics](#) section of this data sheet.

### INPUT VOLTAGE

The OPA333 and OPA2333 input common-mode voltage range extends 0.1V beyond the supply rails. The OPA333 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Normally, input bias current is about 70pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10mA. This limitation is easily accomplished with an input resistor, as shown in [Figure 18](#).

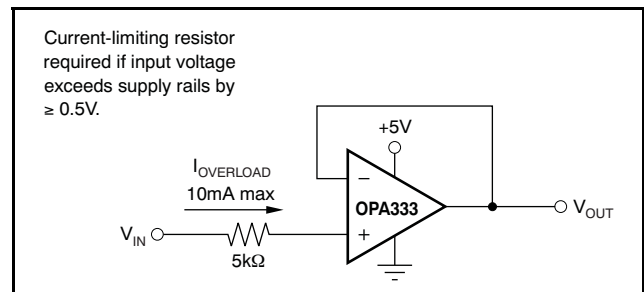


Figure 18. Input Current Protection

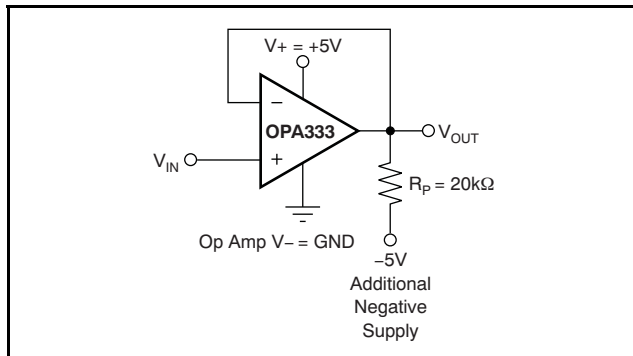
### INTERNAL OFFSET CORRECTION

The OPA333 and OPA2333 op amps use an auto-calibration technique with a time-continuous 350kHz op amp in the signal path. This amplifier is zero-corrected every  $8\mu\text{s}$  using a proprietary technique. Upon power-up, the amplifier requires approximately  $100\mu\text{s}$  to achieve specified  $V_{OS}$  accuracy. This design has no aliasing or flicker noise.



## ACHIEVING OUTPUT SWING TO THE OP AMP NEGATIVE RAIL

Some applications require output voltage swings from 0V to a positive full-scale voltage (such as +2.5V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA333 and OPA2333 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires the use of another resistor and an additional, more negative, power supply than the op amp negative supply. A pull-down resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 19.



**Figure 19. For  $V_{OUT}$  Range to Ground**

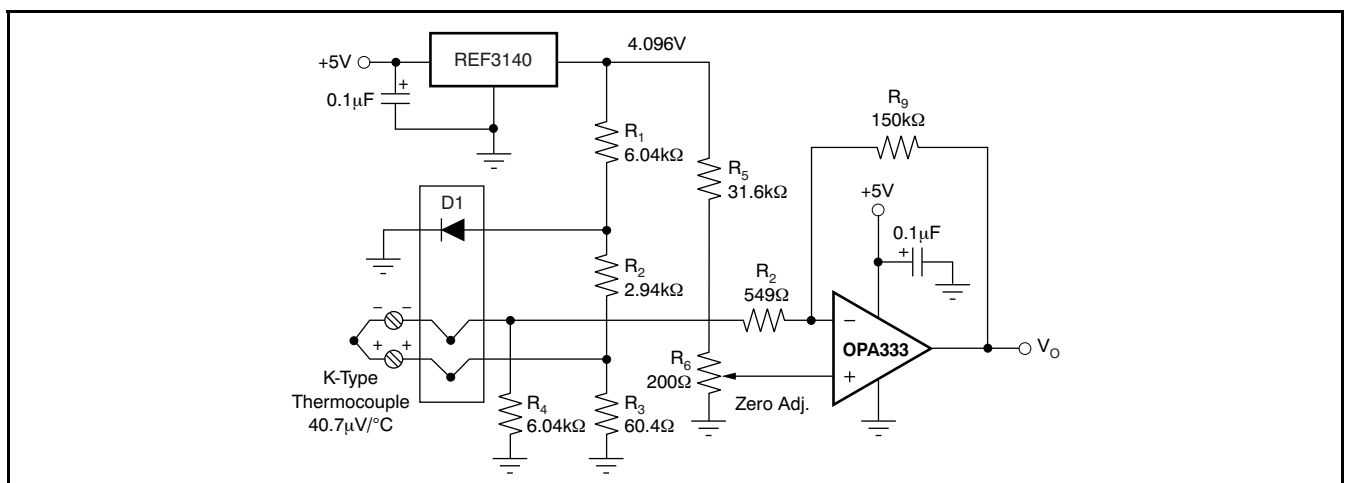
The OPA333 and OPA2333 have an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only

works with some types of output stages. The OPA333 and OPA2333 have been characterized to perform with this technique; the recommended resistor value is approximately 20kΩ. Note that this configuration will increase the current consumption by several hundreds of microamps. Accuracy is excellent down to 0V and as low as -2mV. Limiting and nonlinearity occurs below -2mV, but excellent accuracy returns as the output is again driven above -2mV. Lowering the resistance of the pull-down resistor will allow the op amp to swing even further below the negative rail. Resistances as low as 10kΩ can be used to achieve excellent accuracy down to -10mV.

## GENERAL LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI (electromagnetic-interference) susceptibility.

Operational amplifiers vary in their susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The OPA333 has been specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may still cause varying offset levels.



**Figure 20. Temperature Measurement**

Figure 21 shows the basic configuration for a bridge amplifier.

A low-side current shunt monitor is shown in Figure 22.  $R_N$  are operational resistors used to isolate the ADS1100 from the noise of the digital I<sup>2</sup>C bus. Since the ADS1100 is a 16-bit converter, a precise reference is essential for maximum accuracy. If absolute accuracy is not required, and the 5V power supply is sufficiently stable, the REF3130 may be omitted.

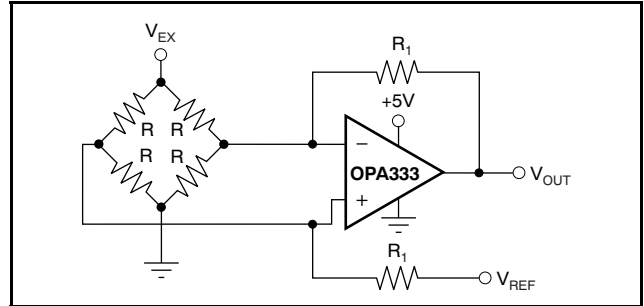


Figure 21. Single Op Amp Bridge Amplifier

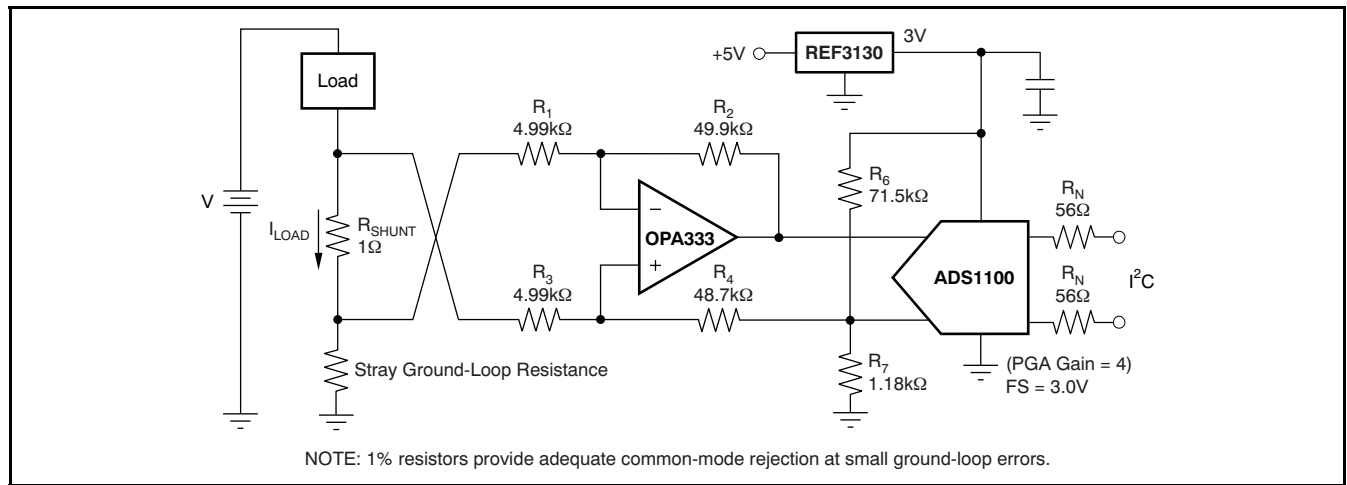


Figure 22. Low-Side Current Monitor

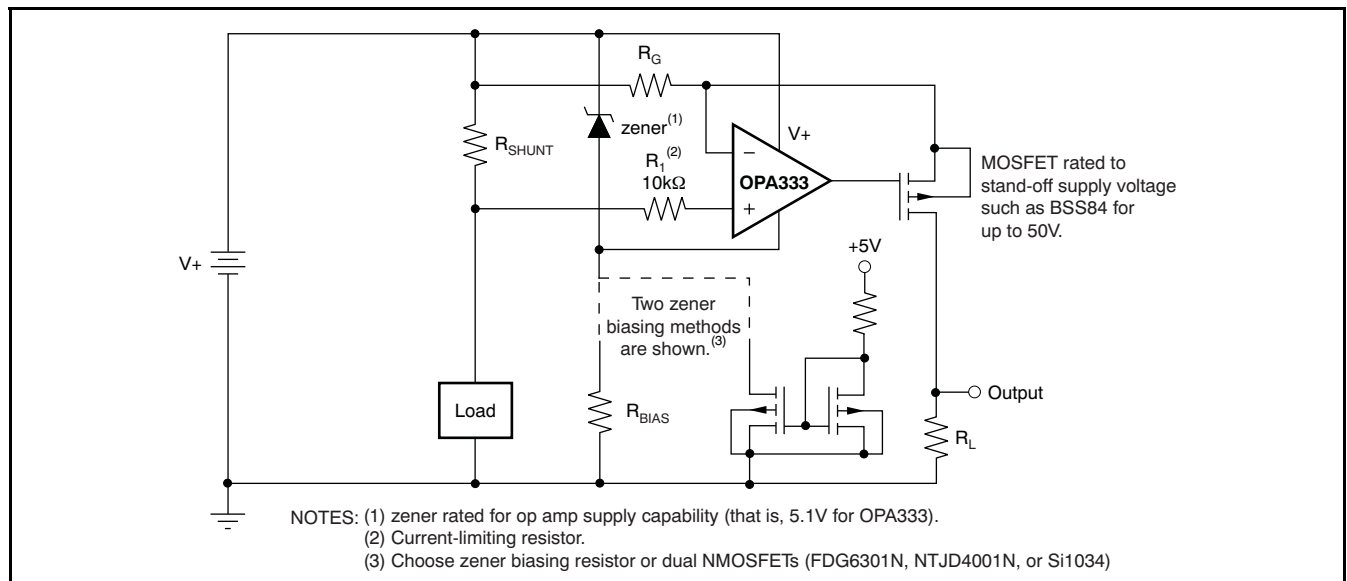


Figure 23. High-Side Current Monitor

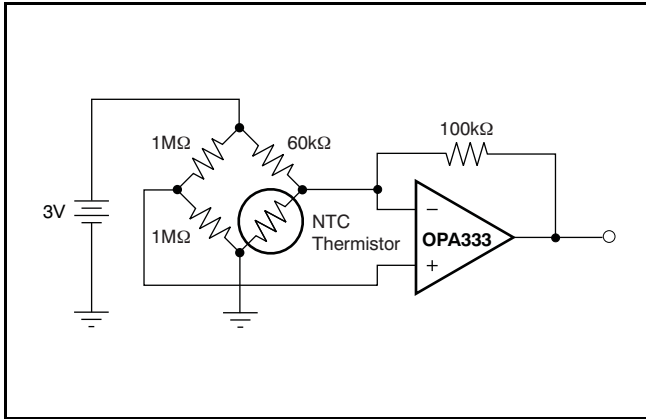


Figure 24. Thermistor Measurement

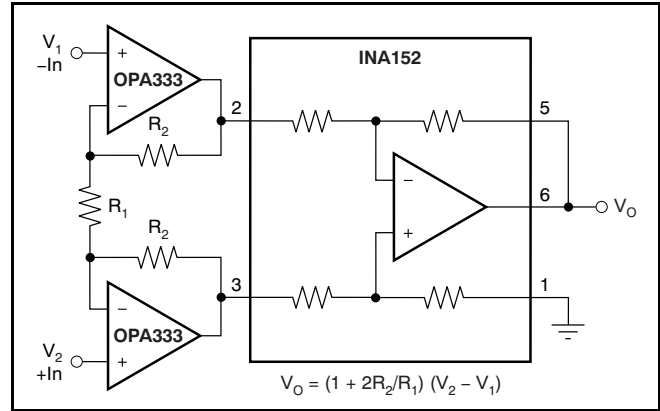


Figure 25. Precision Instrumentation Amplifier

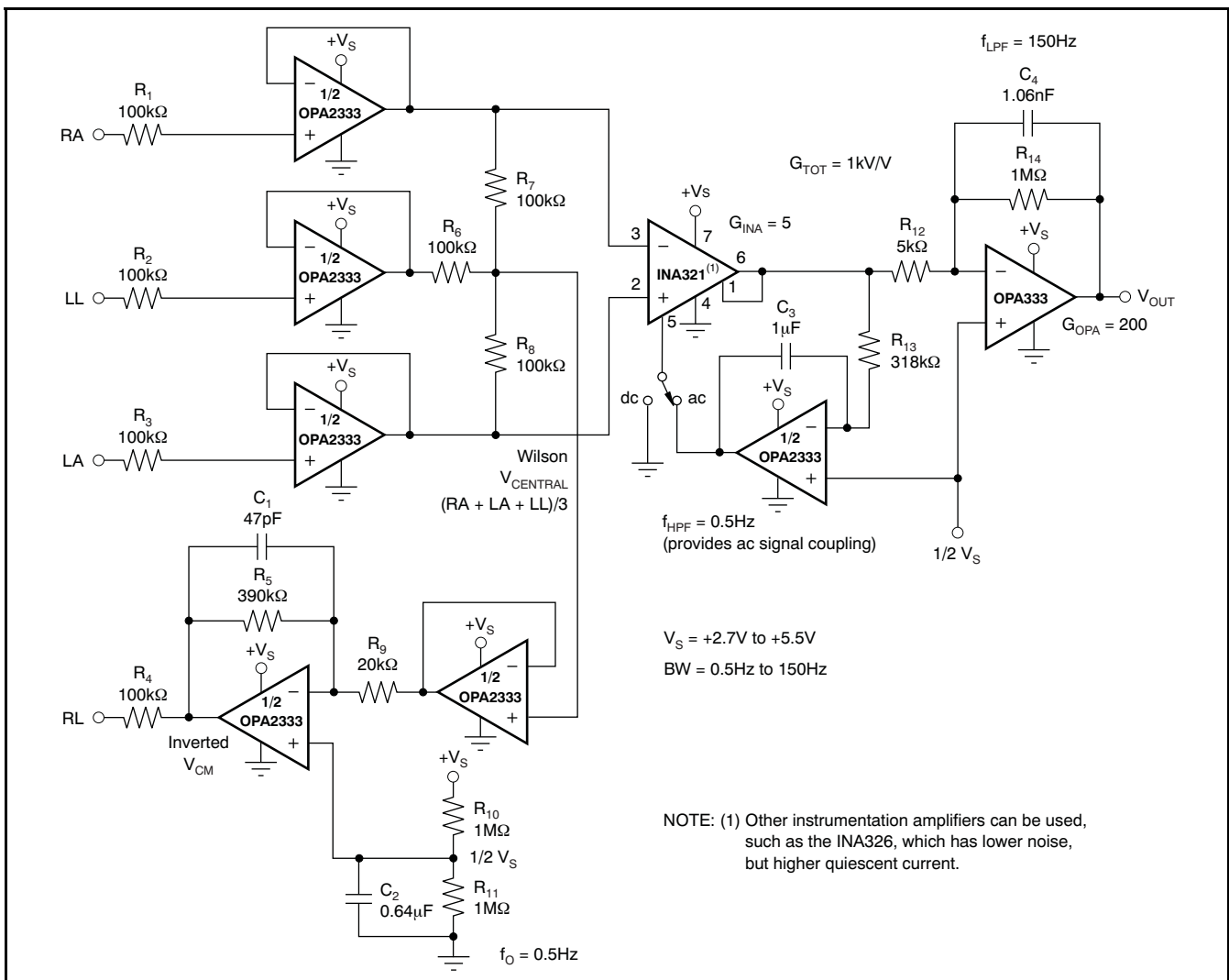


Figure 26. Single-Supply, Very Low Power, ECG Circuit

## DFN PACKAGE

The OPA2333 is offered in an DFN-8 package (also known as SON). The DFN is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See Application Note *QFN/SON PCB Attachment* (SLUA271) and Application Report *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at [www.ti.com](http://www.ti.com).

**The exposed leadframe die pad on the bottom of the package should be connected to V– or left unconnected.**

## DFN LAYOUT GUIDELINES

The exposed leadframe die pad on the DFN package should be soldered to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout may be necessary based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2333AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A	<a href="#">Samples</a>
OPA2333AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A	<a href="#">Samples</a>
OPA2333AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OBAQ	<a href="#">Samples</a>
OPA2333AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OBAQ	<a href="#">Samples</a>
OPA2333AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OBAQ	<a href="#">Samples</a>
OPA2333AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OBAQ	<a href="#">Samples</a>
OPA2333AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A	<a href="#">Samples</a>
OPA2333AIDRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ	<a href="#">Samples</a>
OPA2333AIDRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ	<a href="#">Samples</a>
OPA2333AIDRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ	<a href="#">Samples</a>
OPA2333AIDRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ	<a href="#">Samples</a>
OPA2333AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A	<a href="#">Samples</a>
OPA333AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 0	O333A	<a href="#">Samples</a>
OPA333AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ	<a href="#">Samples</a>
OPA333AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ	<a href="#">Samples</a>
OPA333AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ	<a href="#">Samples</a>
OPA333AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA333AIDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BQY	<a href="#">Samples</a>
OPA333AIDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BQY	<a href="#">Samples</a>
OPA333AIDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BQY	<a href="#">Samples</a>
OPA333AIDCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BQY	<a href="#">Samples</a>
OPA333AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A	<a href="#">Samples</a>
OPA333AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A	<a href="#">Samples</a>
OPA333AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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**OTHER QUALIFIED VERSIONS OF OPA2333, OPA333 :**

- Automotive: [OPA2333-Q1](#), [OPA333-Q1](#)

**NOTE: Qualified Version Definitions:**

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2333AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2333AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2333AIDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2333AIDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA333AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA333AIDCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA333AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



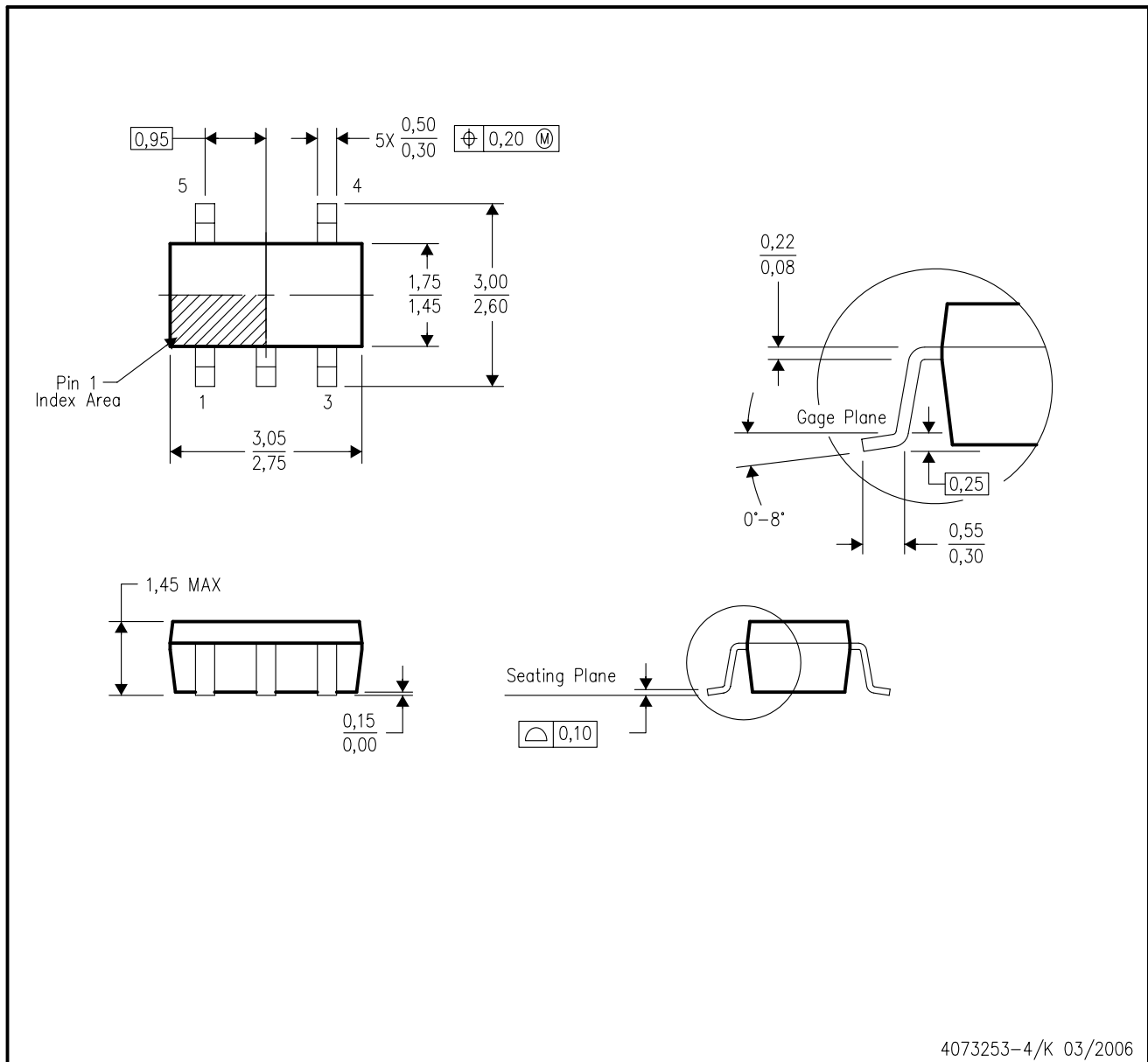
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2333AIDGKT	VSSOP	DGK	8	250	364.0	364.0	27.0
OPA2333AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA2333AIDRBR	SON	DRB	8	3000	367.0	367.0	35.0
OPA2333AIDRBT	SON	DRB	8	250	210.0	185.0	35.0
OPA333AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA333AIDCKR	SC70	DCK	5	3000	203.0	203.0	35.0
OPA333AIDR	SOIC	D	8	2500	367.0	367.0	35.0

DBV (R-PDSO-G5)

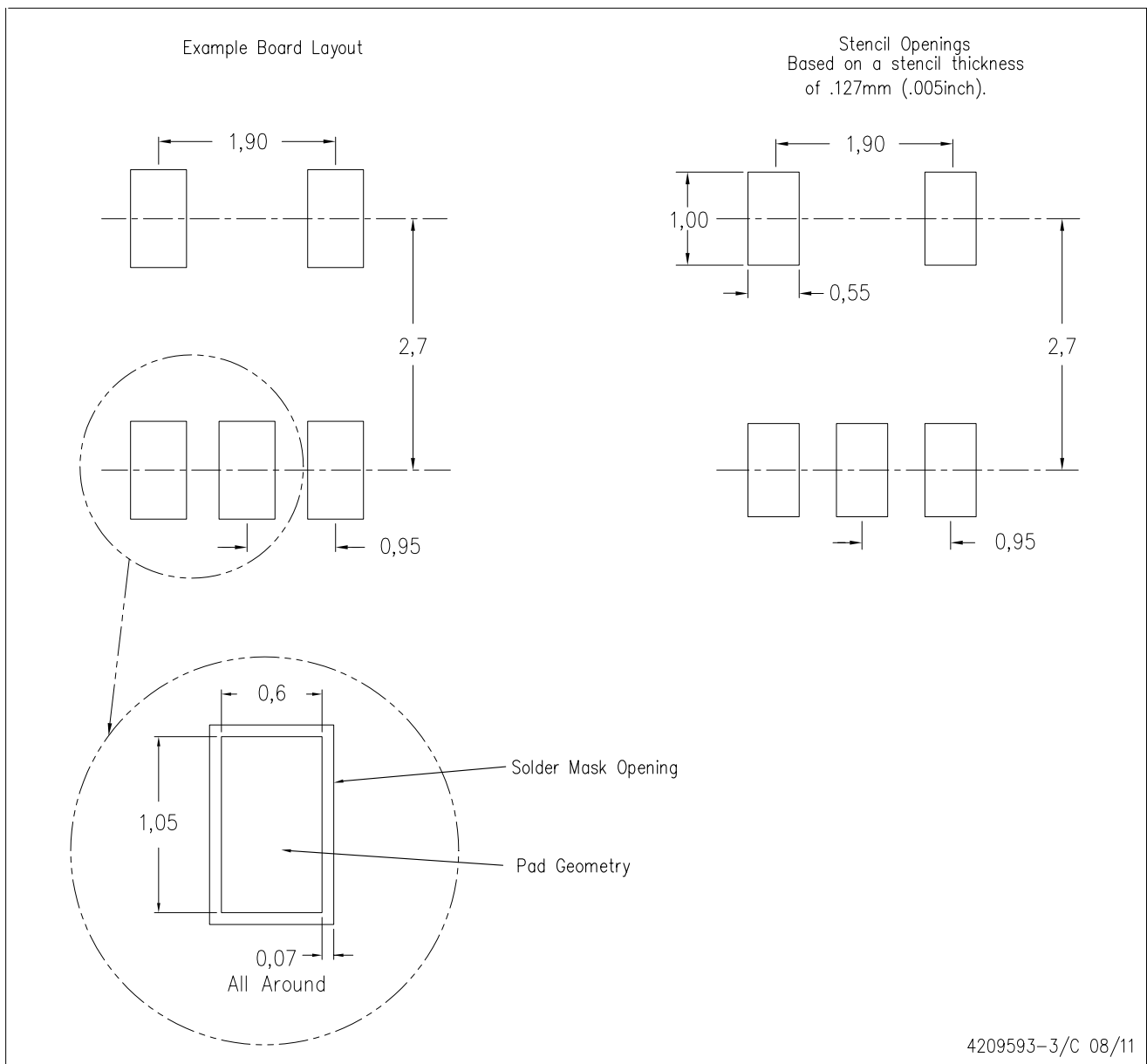
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE

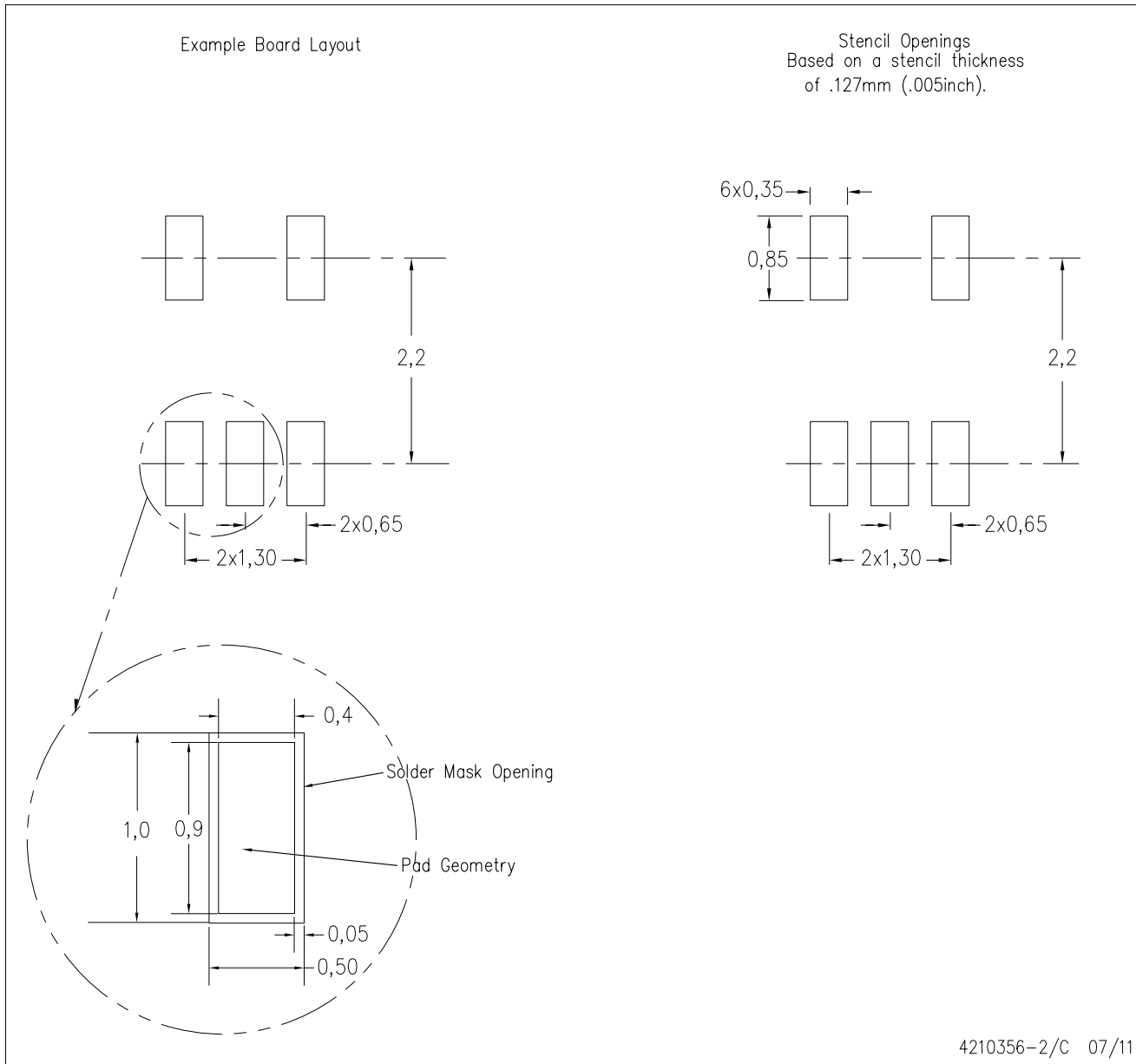


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G5)

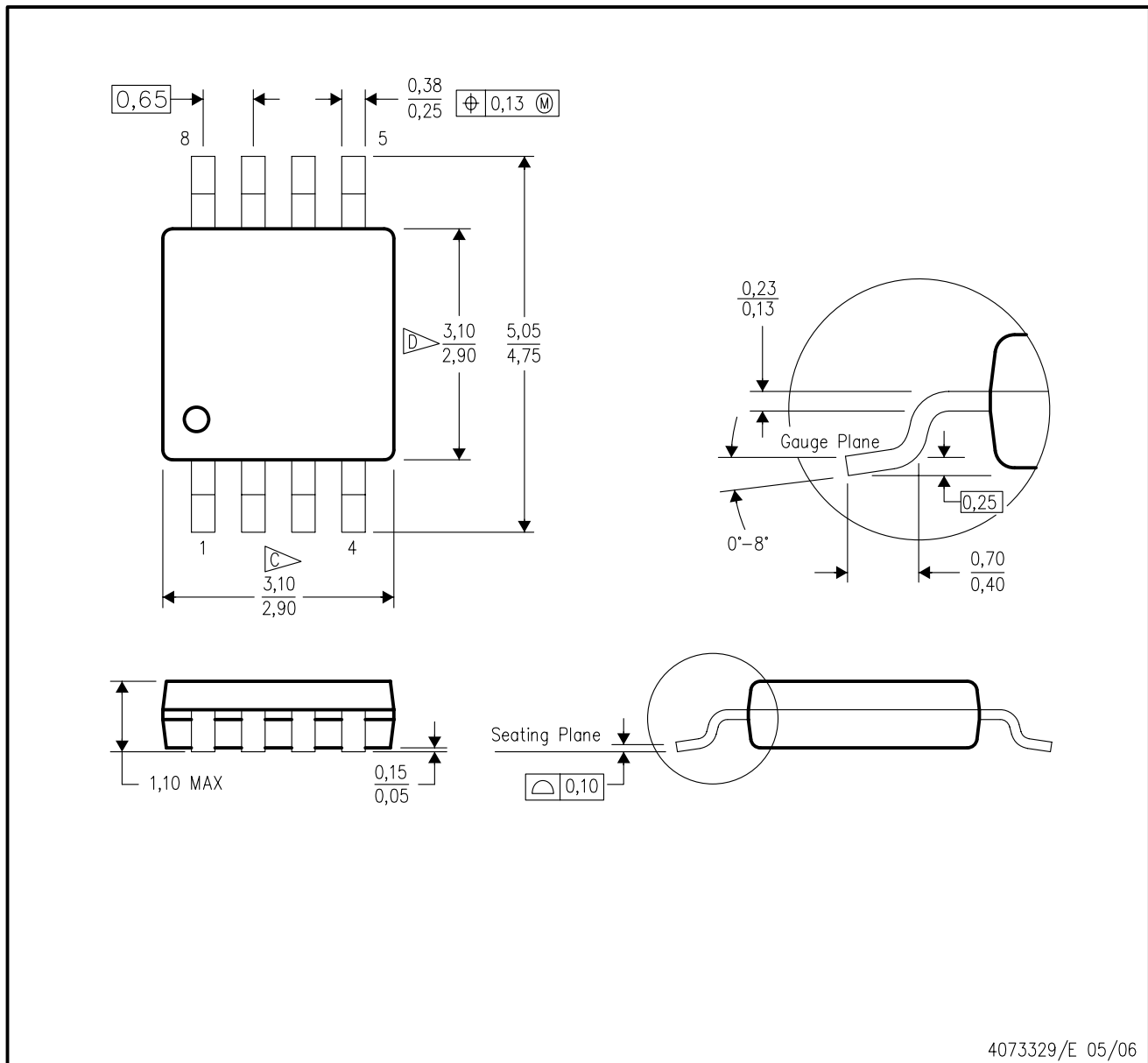
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

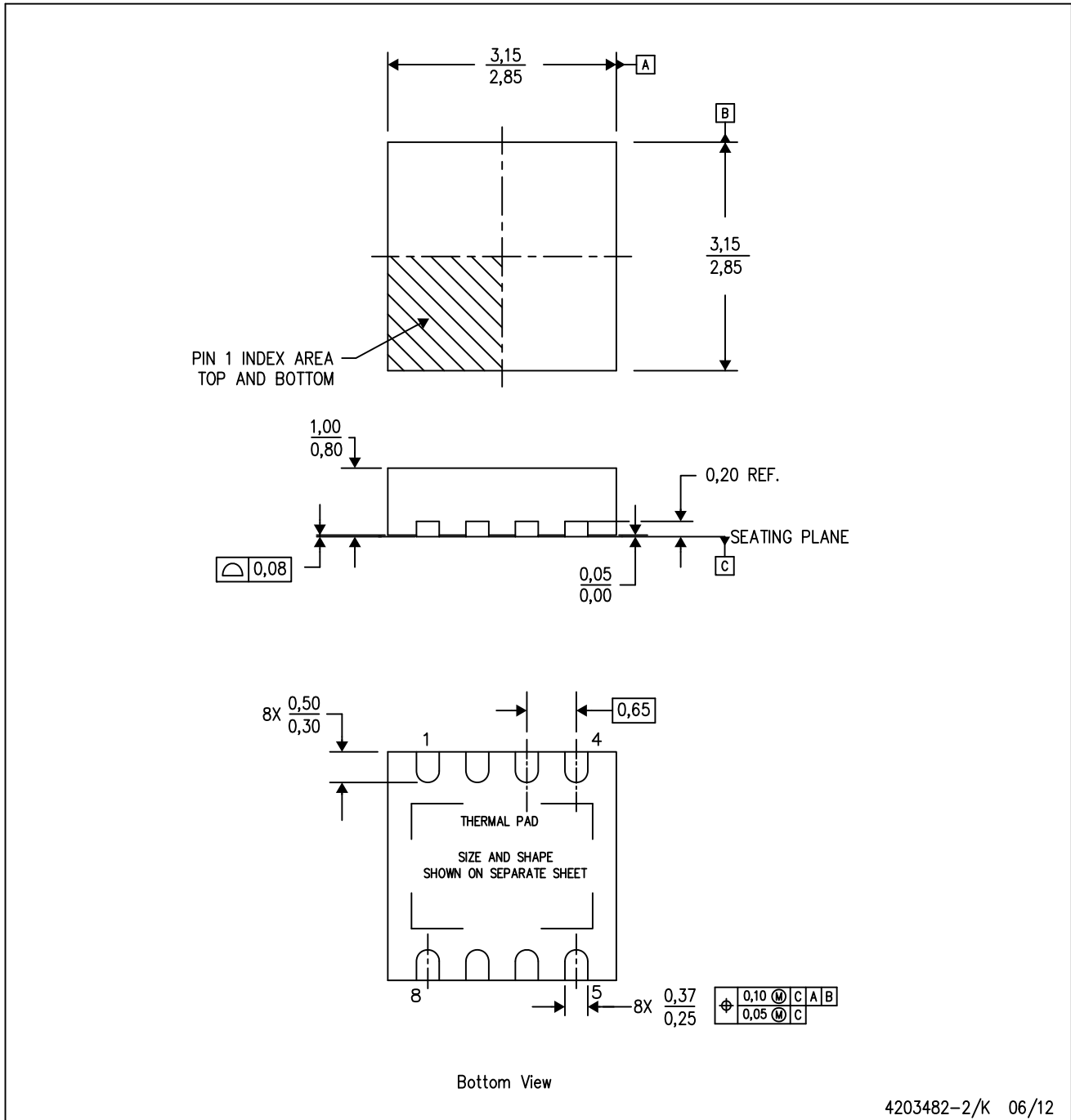
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DRB (S-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

# THERMAL PAD MECHANICAL DATA

DRB (S-PVSON-N8)

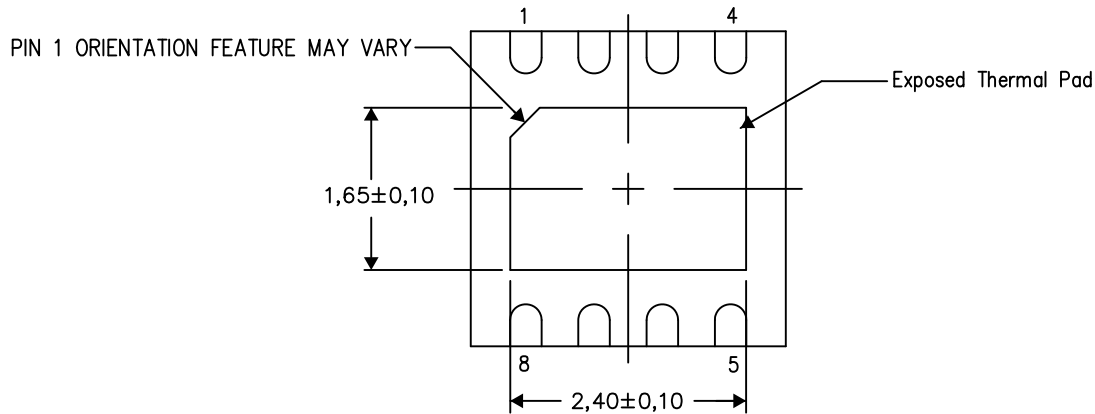
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206340-3/N 09/12

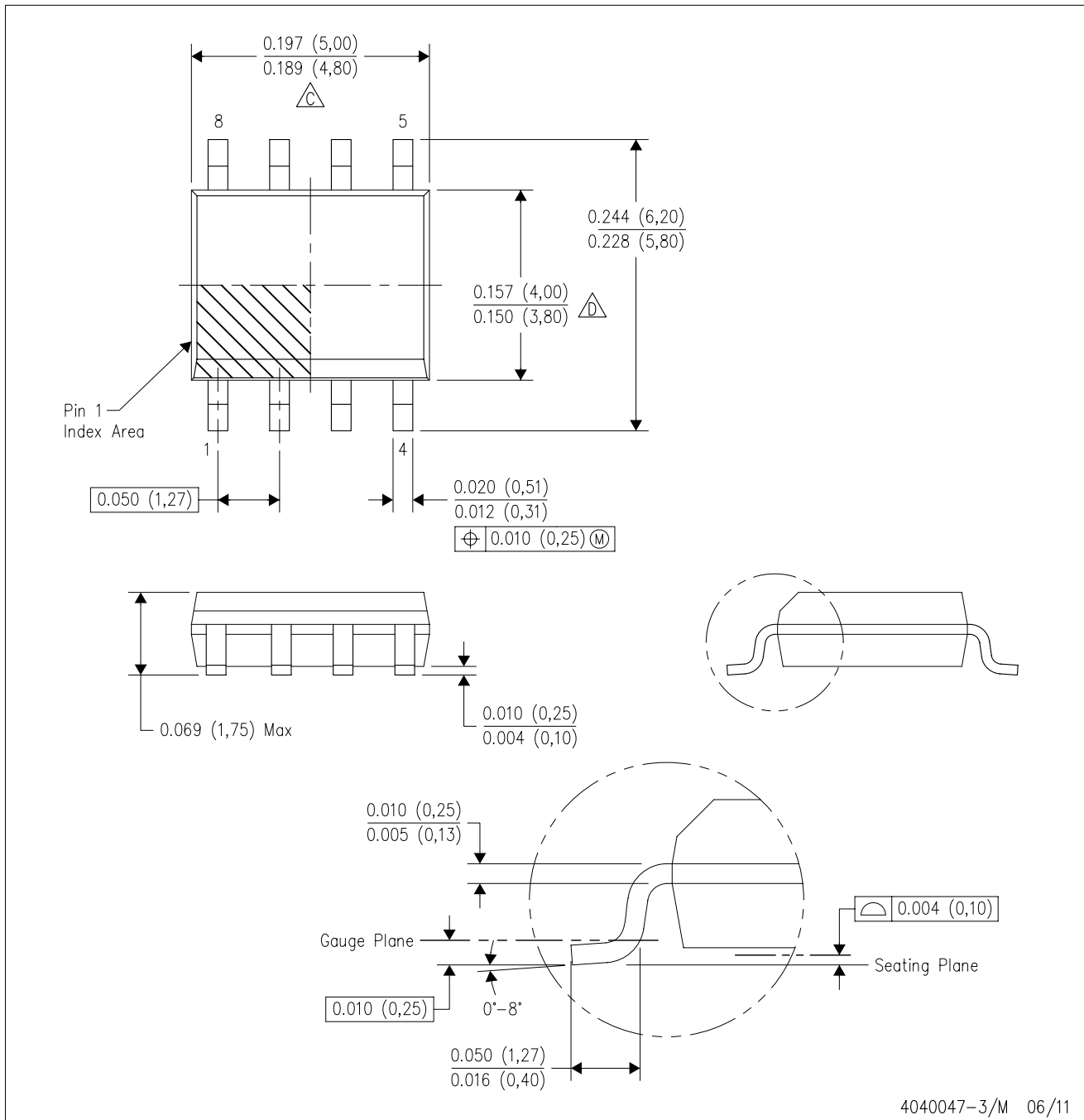
NOTE: All linear dimensions are in millimeters





D (R-PDSO-G8)

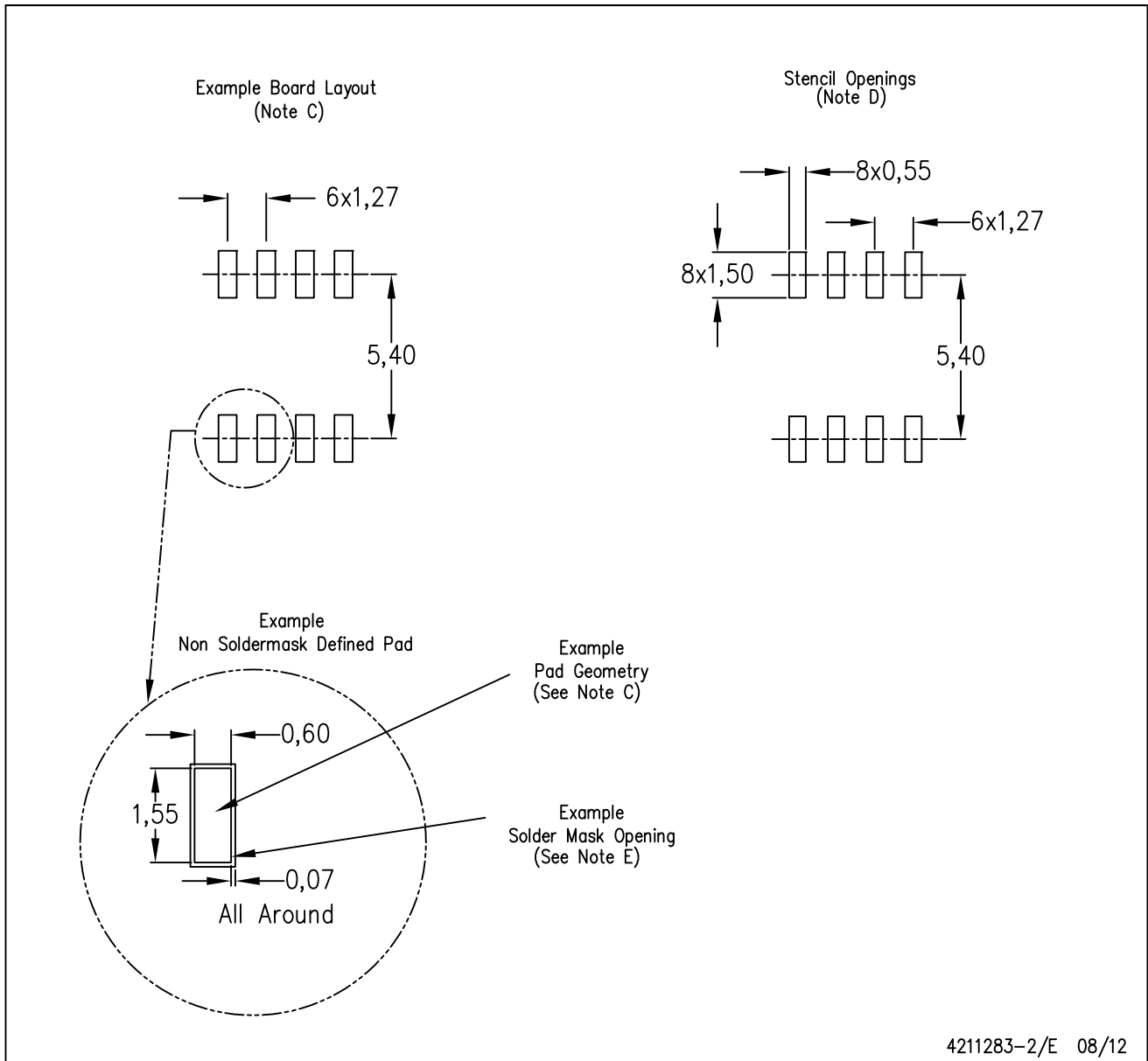
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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