LP38690，LP38692

1A 低压降 CMOS 线性稳压器

在使用陶瓷输出电容器时保持稳定

查询样品: LP38690, LP38692

特性

- **2.5%** 输出精度 **(25°C)**
- 低压降：**1A**（典型值，**5V** 输出）时为 **450mV**
- 宽输入电压范围（**2.7V** 至 **10V**）
- 精密（已调整）带隙基准
- 确保了 **-40°C** 至 **+125°C** 温度范围内的技术规格
- **1μA** 关闭状态静态电流
- 热过载保护
- 折返电流限制
- **PFM**，小外形尺寸晶体管 **(SOT)-223** 封装和 **6** 引线晶圆级小外形尺寸封装 **(WSON)** 封装
- 使能引脚 **(LP38692)**

应用范围

- 硬盘驱动器
- 笔记本电脑
- 电池供电类器件
- 便携式仪表

说明

LP38690/2 低压降 CMOS 线性稳压器提供严密的输出耐受（典型值 2.5%），极低压降（在负载电流为 1A，$V_{输出}$=5V 时为 450mV），并在采用超低等效串联电阻 (ESR) 陶瓷输出电容器时所提供出色的 AC 性能。

WSON，SON-223 以及 PFM 封装所具有的的低热阻可在周围温度较高的环境中实现满运行电流。

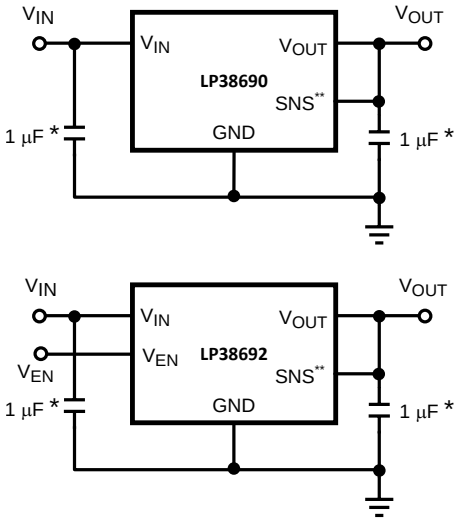
PMOS 功率晶体管的使用意味着无需 DC 基驱动电流对其进行偏置，从而无论负载电流、输入电压或者运行温度是多少时均可将接地引脚电流保持在低于 100μA 的水平上。

压降电压：450mV（典型值），这是在电流为 1A（典型值5V 输出）时的值。

接地引脚电流：满负载时为 55μA（典型值）。

精密输出电压：精度 2.5% (25°C)。

典型应用电路



* 稳定所需的最小值。
**只适用于 WSON 封装器件。

连接图

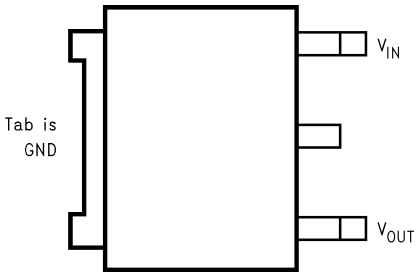


图 **1. PFM (LP38690DT-X.X) -** 顶视图
请见封装编号 **NDP0003B**

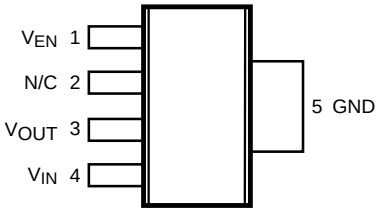


图 **2. SOT-223 (LP38692MP-X.X) -** 顶视图
请见封装编号 **NDC0005A**

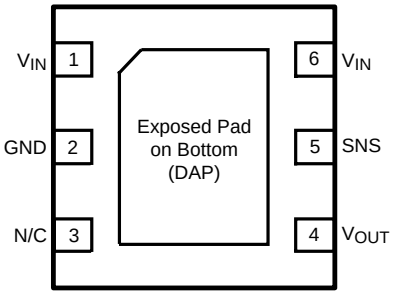


图 **3. 6** 引线 **WSON (LP38690SD-X.X) -** 顶视图
请见封装编号 **NGG0006A**

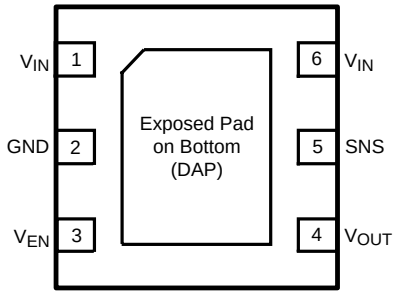


图 **4. 6** 引线 **WSON (LP38692SD-X.X)**，顶视图
请见封装编号 **NGG**

引脚说明

引脚	说明
$V_{输入}$	这是到稳压器的输入电源电压。 对于 WSON 器件，两个 $V_{输入}$引脚必须被接在一起以实现满电流运行（每引脚最大电流 500mA）。
GND	针对稳压器的电路接地。 对于 PFM 和 SOT-223 封装，它接至裸片并在被焊接到一个较大铜覆区下面时用作散热片。
SNS	输出感测引脚可实现负载上的遥感，这将消除由压降（由稳压器和负载间的引线电阻导致）引起的输出电压误差。 这个引脚必须被接至 $V_{输出}$。
V_{EN}	可通过将使能引脚拉至高电平或低电平来打开和关闭此部件。
$V_{输出}$	经稳压调节的输出电压。
DAP	只适用于 WSON 封装 - DAP（外露垫）在焊接到铜覆区时被用作散热连接。 更多信息请见WSON MOUNTING部分，此部分在APPLICATION HINTS中。

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 5 seconds)	260°C
ESD Rating(3)	2 kV
Power Dissipation(4)	Internally Limited
V(max) All pins (with respect to GND)	-0.3V to 12V
I_{OUT}(5)	Internally Limited
Junction Temperature	−40°C to +150°C

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) ESD is tested using the human body model which is a 100pF capacitor discharged through a 1.5k resistor into each pin.
(4) At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink values (if a heatsink is used). The junction-to-ambient thermal resistance (θ_{J-A}) for the PFM is approximately 90°C/W for a PC board mounting with the device soldered down to minimum copper area (less than 0.1 square inch). If one square inch of copper is used as a heat dissipator for the PFM, the θ_{J-A} drops to approximately 50°C/W. The SOT-223 package has a θ_{J-A} of approximately 125°C/W when soldered down to a minimum sized pattern (less than 0.1 square inch) and approximately 70°C/W when soldered to a copper area of one square inch. The θ_{J-A} values for the WSON package are also dependent on trace area, copper thickness, and the number of thermal vias used (refer to the TI AN-1187 Application Report and the WSON MOUNTING section in this datasheet). If power dissipation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.
(5) If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground.

OPERATING RATINGS

V_{IN} Supply Voltage	2.7V to 10V
Operating Junction Temperature Range	−40°C to +125°C

ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_{OUT}$ + 1V, $C_{IN} = C_{OUT}$ = 10 µF, I_{LOAD} = 10mA. Min/Max limits are specified through testing, statistical correlation, or design.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
V_O	Output Voltage Tolerance		-2.5		2.5	$\%V_{OUT}$
		100 µA < I_L < 1A V_O + 1V ≤ V_{IN} ≤ 10V	**-5.0**		**5.0**	
$\Delta V_O/\Delta V_{IN}$	Output Voltage Line Regulation(2)	V_O + 0.5V ≤ V_{IN} ≤ 10V I_L = 25mA		0.03	**0.1**	%/V
$\Delta V_O/\Delta I_L$	Output Voltage Load Regulation(3)	1 mA < I_L < 1A $V_{IN} = V_O$ + 1V		1.8	**5**	%/A
$V_{IN} - V_{OUT}$	Dropout Voltage(4)	(V_O = 1.8V) I_L = 1A		950	**1600**	mV
		(V_O = 2.5V) I_L = 0.1A I_L = 1A		80 800	**145** **1300**	
		(V_O = 3.3V) I_L = 0.1A I_L = 1A		65 650	**110** **1000**	
		(V_O = 5V) I_L = 0.1A I_L = 1A		45 450	**100** **800**	

(1) Typical numbers represent the most likely parametric norm for 25°C operation.
(2) Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.
(3) Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from 1mA to full load.
(4) Dropout voltage is defined as the minimum input to output differential required to maintain the output within 100mV of nominal value.

ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_{OUT}$ + 1V, $C_{IN} = C_{OUT}$ = 10 µF, I_{LOAD} = 10mA. Min/Max limits are specified through testing, statistical correlation, or design.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
I_Q	Quiescent Current	$V_{IN} \le$ 10V, I_L =100 µA - 1A		55	**100**	µA
		$V_{EN} \le$ 0.4V, (LP38692 Only)		0.001	1	
I_L(MIN)	Minimum Load Current	$V_{IN} - V_O \le$ 4V			**100**	
I_{FB}	Foldback Current Limit	$V_{IN} - V_O >$ 5V		450		mA
		$V_{IN} - V_O <$ 4V		1500		
PSRR	Ripple Rejection	$V_{IN} = V_O$ + 2V(DC), with 1V(p-p) / 120Hz Ripple		55		dB
T_{SD}	Thermal Shutdown Activation (Junction Temp)			160		°C
T_{SD} (HYST)	Thermal Shutdown Hysteresis (Junction Temp)			10		
e_n	Output Noise	BW = 10Hz to 10kHz V_O = 3.3V		0.7		µV/√Hz
V_O (LEAK)	Output Leakage Current	$V_O = V_O$(NOM) + 1V @ 10V_{IN}		0.5	12	µA
V_{EN}	Enable Voltage (LP38692 Only)	Output = OFF			**0.4**	V
		Output = ON, V_{IN} = 4V	**1.8**			
		Output = ON, V_{IN} = 6V	**3.0**			
		Output = ON, V_{IN} = 10V	**4.0**			
I_{EN}	Enable Pin Leakage	V_{EN} = 0V or 10V, V_{IN} = 10V	-1	0.001	1	µA

BLOCK DIAGRAMS

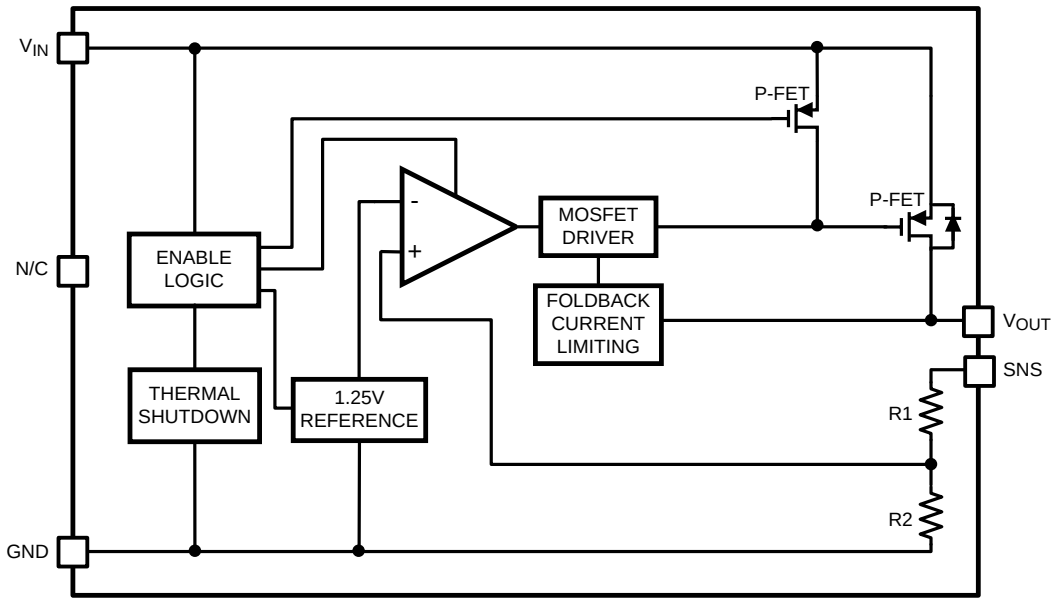


Figure 5. LP38690 Functional Diagram (WSON)

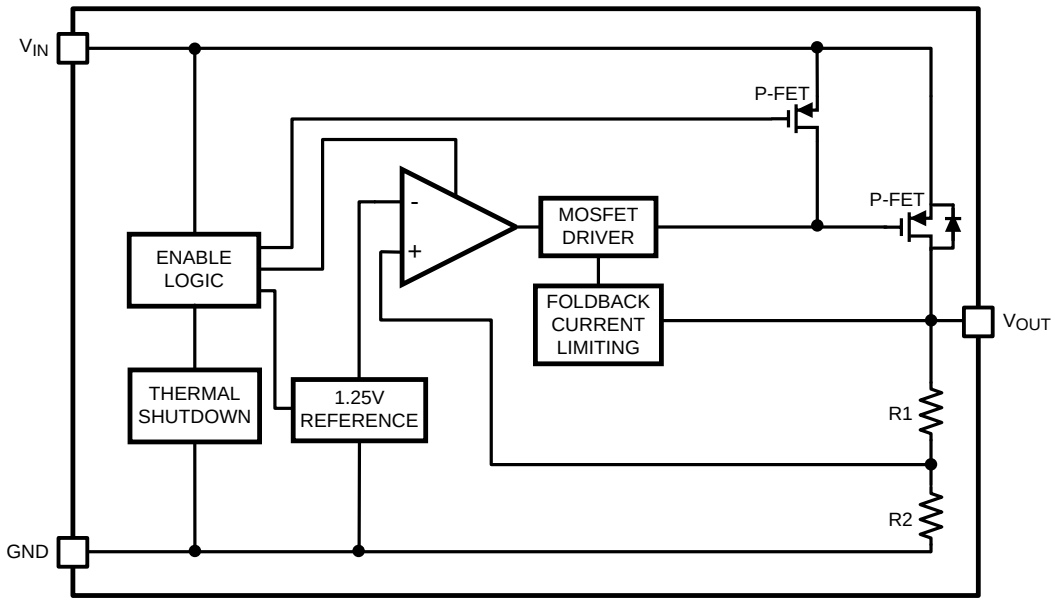


Figure 6. LP38690 Functional Diagram (PFM)

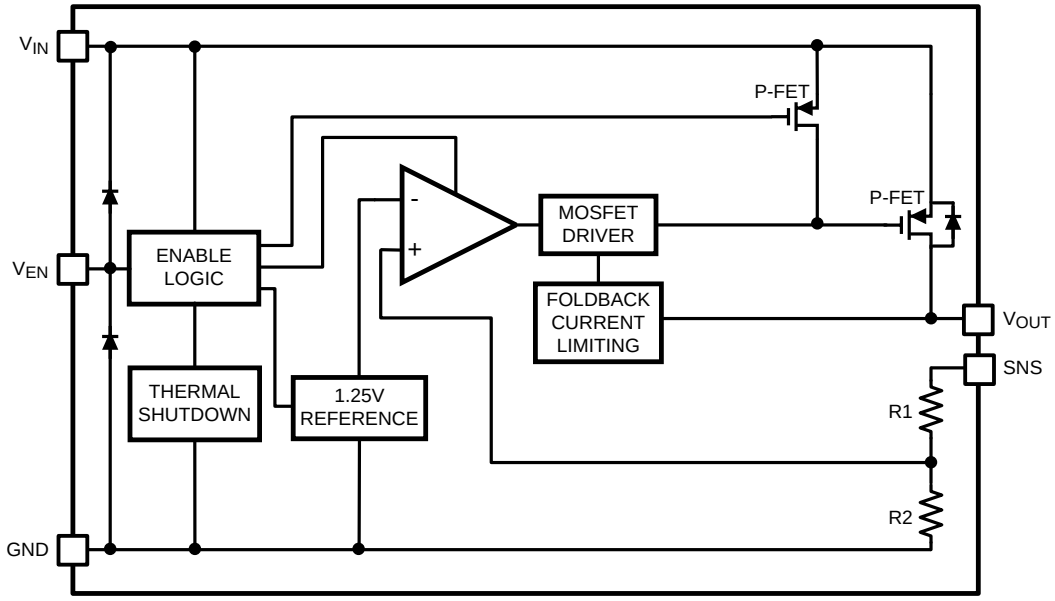


Figure 7. LP38692 Functional Diagram (WSON)

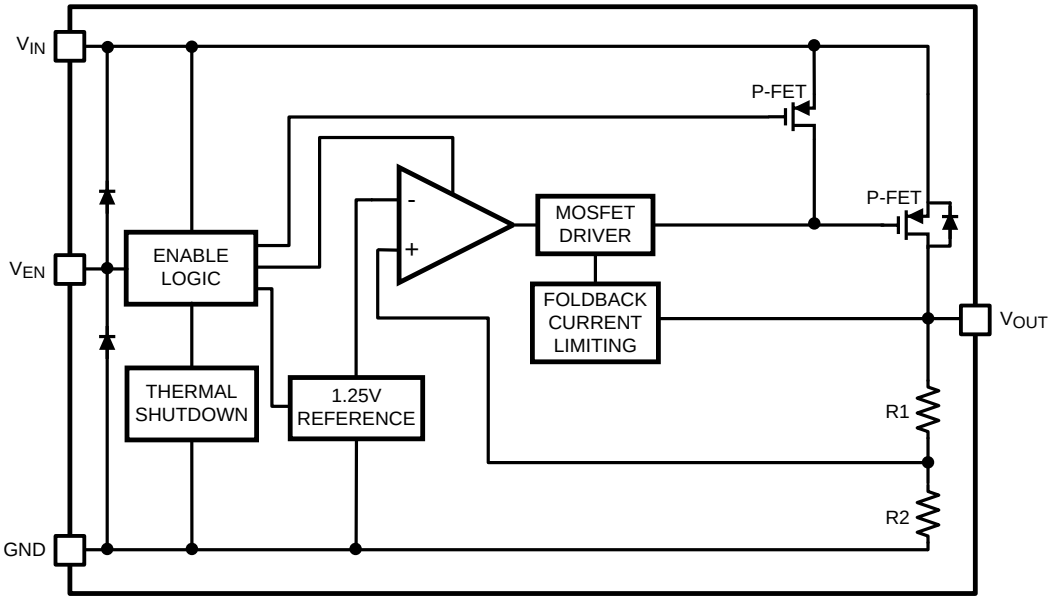


Figure 8. LP38692 Functional Diagram (SOT-223)

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, Enable pin is tied to V_{IN} (LP38692 only), V_{OUT} = 1.8V, V_{IN} = V_{OUT} +1V, I_L = 10mA.

Noise vs Frequency

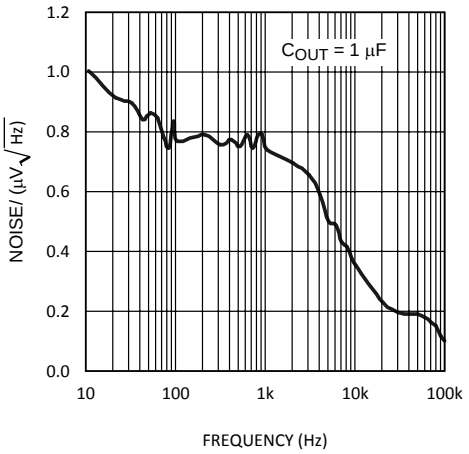


Figure 9.

Noise vs Frequency

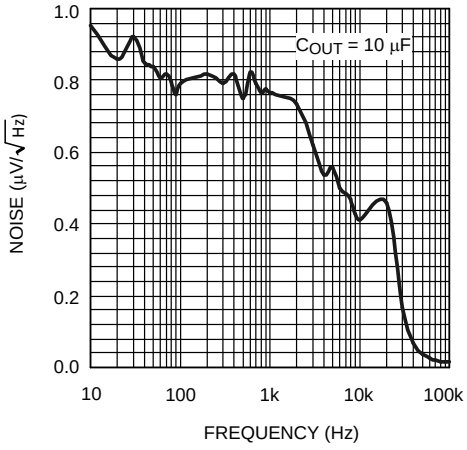


Figure 10.

Noise vs Frequency

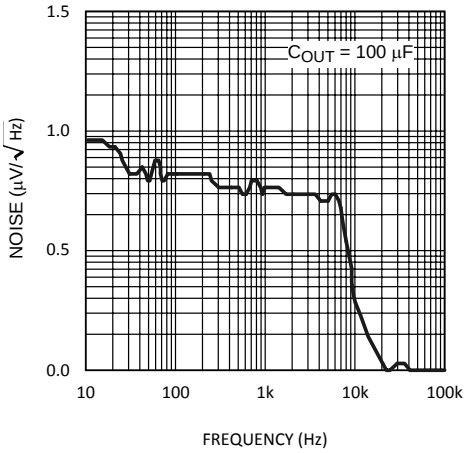


Figure 11.

Ripple Rejection

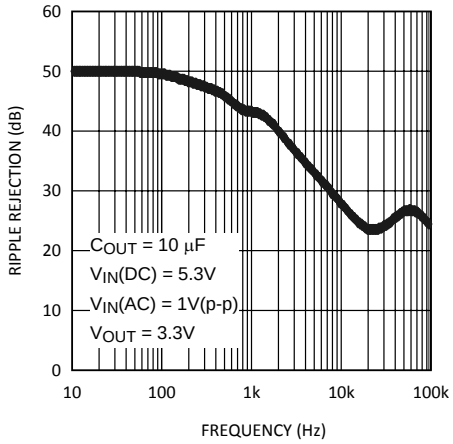


Figure 12.

Ripple Rejection

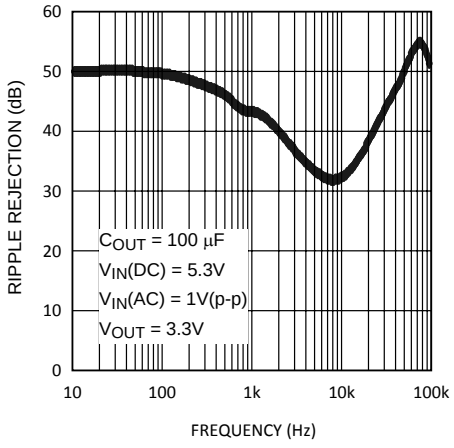


Figure 13.

Ripple Rejection

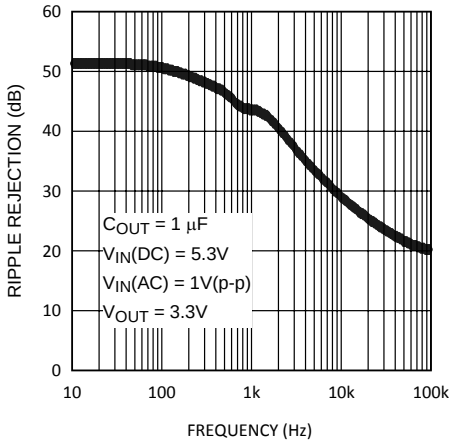


Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, Enable pin is tied to V_{IN} (LP38692 only), V_{OUT} = 1.8V, V_{IN} = V_{OUT} +1V, I_L = 10mA.

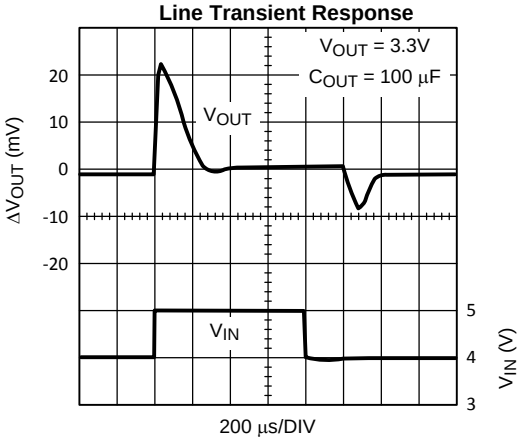


Figure 15.

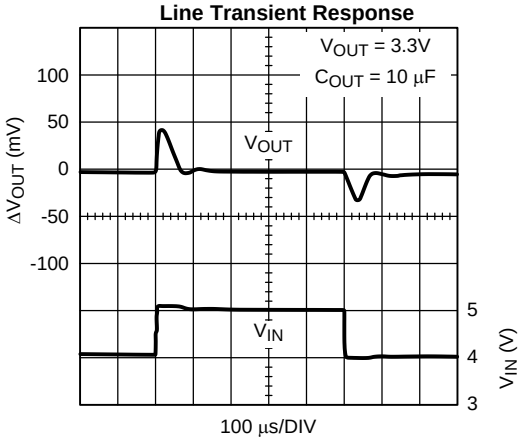


Figure 16.

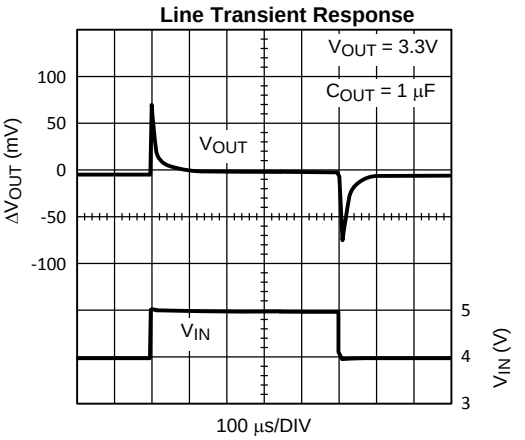


Figure 17.

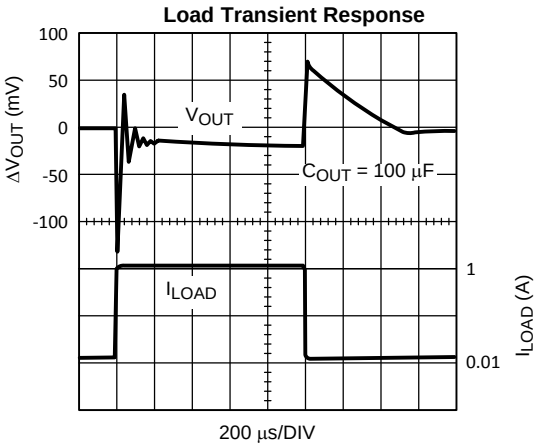


Figure 18.

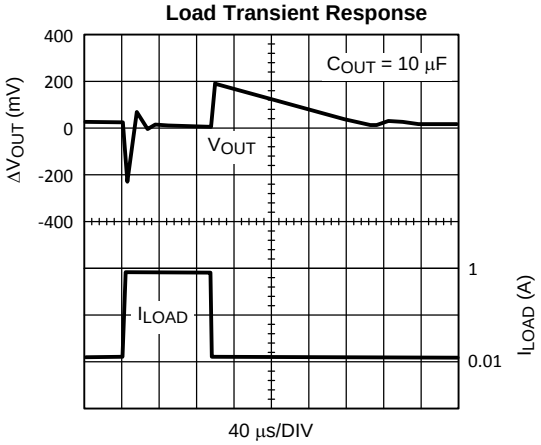


Figure 19.

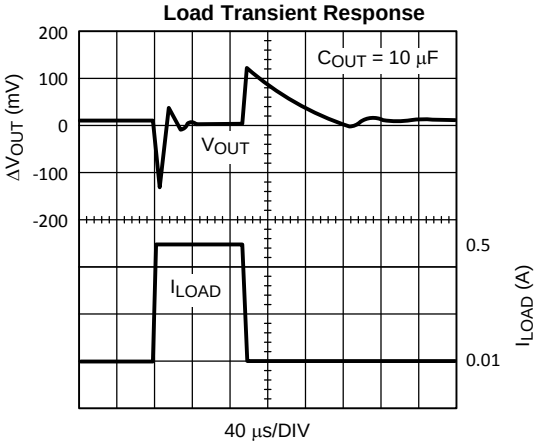


Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, Enable pin is tied to V_{IN} (LP38692 only), V_{OUT} = 1.8V, V_{IN} = V_{OUT} +1V, I_L = 10mA.

Load Transient Response

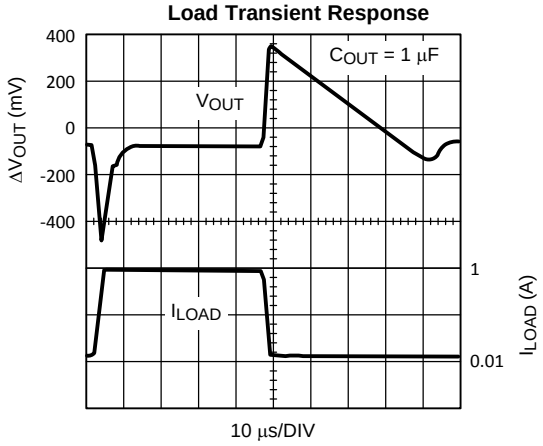


Figure 21.

Load Transient Response

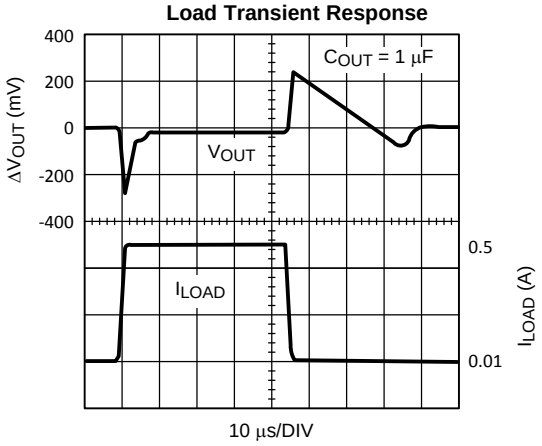


Figure 22.

V_{OUT} vs Temperature (5.0V)

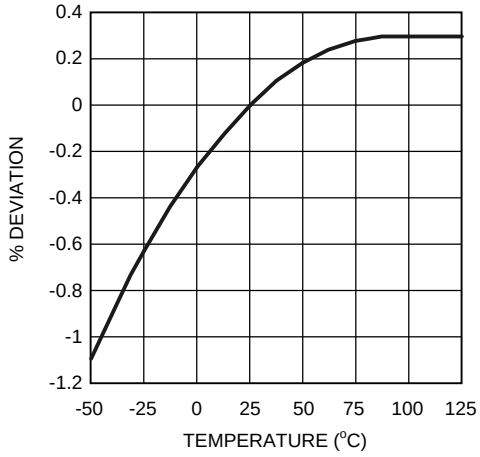


Figure 23.

V_{OUT} vs Temperature (3.3V)

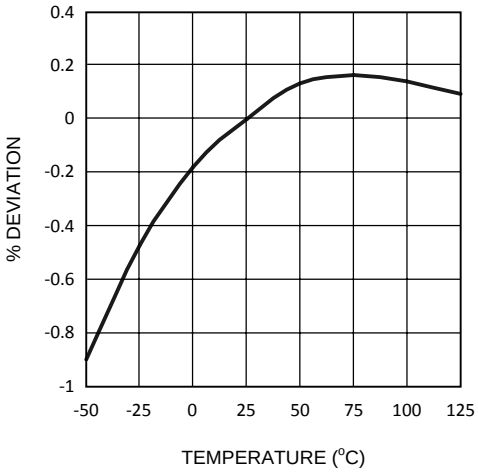


Figure 24.

V_{OUT} vs Temperature (2.5V)

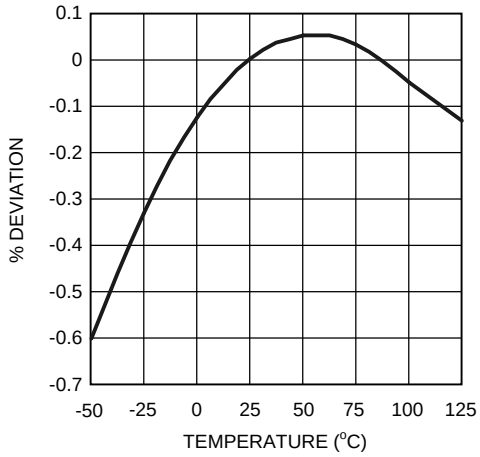


Figure 25.

V_{OUT} vs Temperature (1.8V)

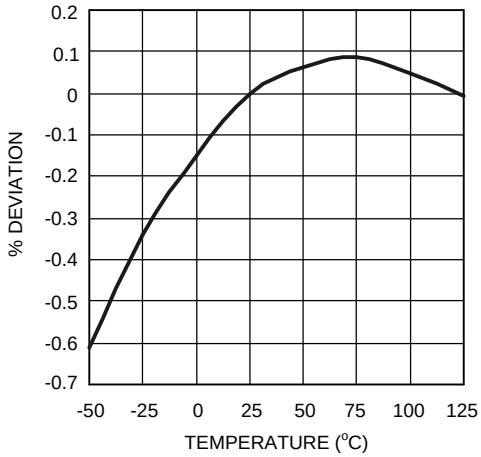


Figure 26.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, Enable pin is tied to V_{IN} (LP38692 only), V_{OUT} = 1.8V, V_{IN} = V_{OUT} +1V, I_L = 10mA.

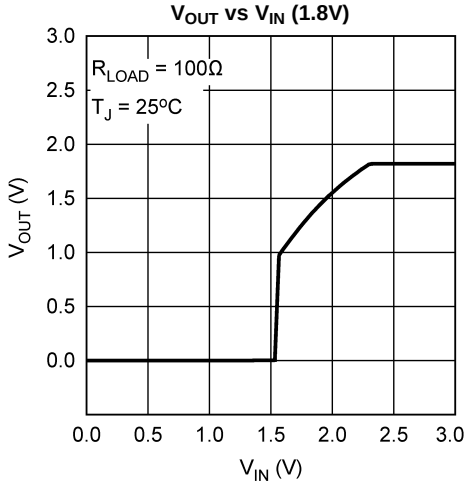


Figure 27.

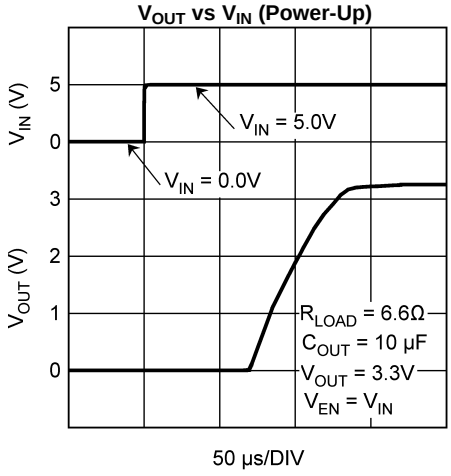


Figure 28.

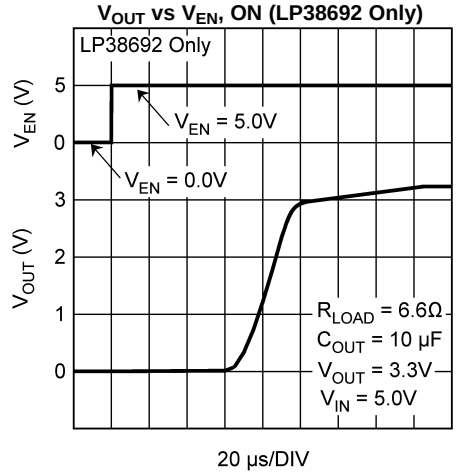


Figure 29.

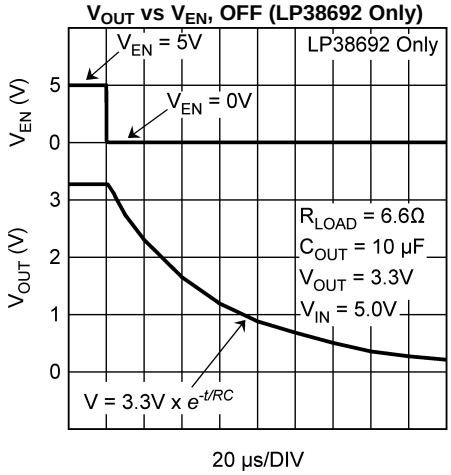


Figure 30.

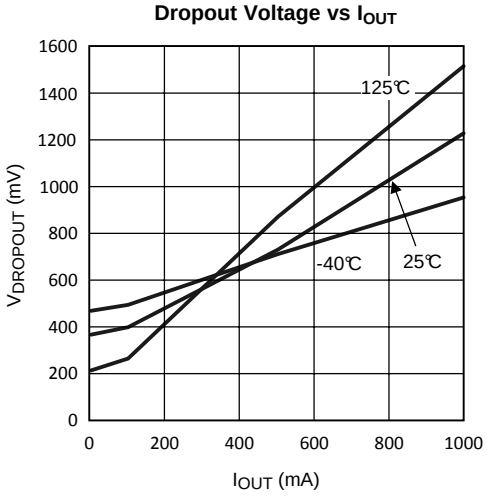


Figure 31.

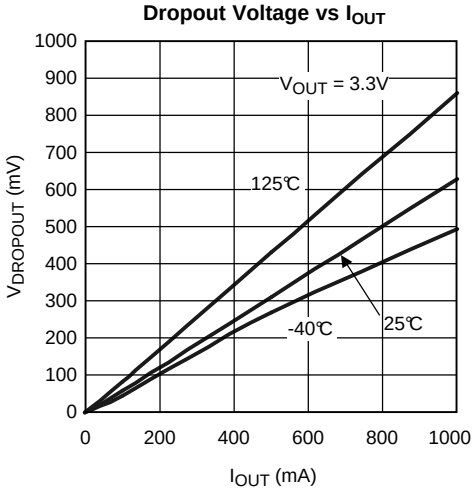


Figure 32.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: T_J = 25°C, C_{IN} = C_{OUT} = 10 µF, Enable pin is tied to V_{IN} (LP38692 only), V_{OUT} = 1.8V, V_{IN} = V_{OUT} +1V, I_L = 10mA.

Enable Voltage vs Temperature

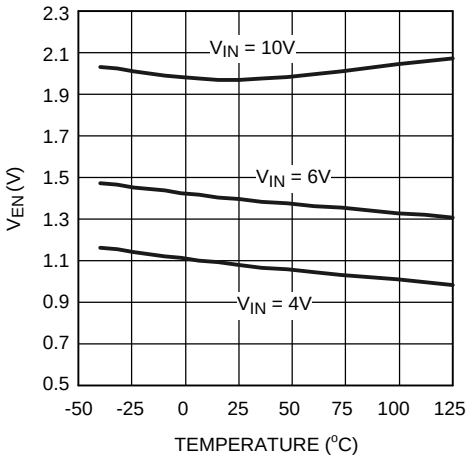


Figure 33.

Load Regulation vs Temperature

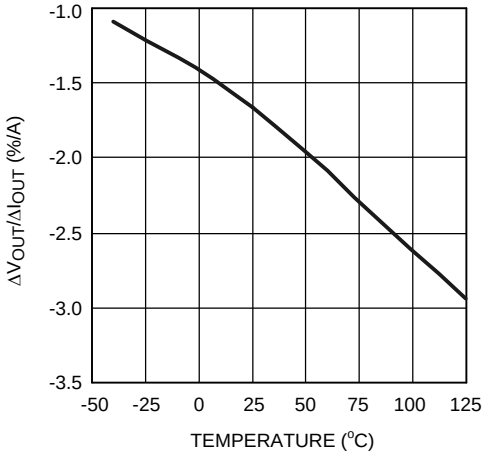


Figure 34.

Line Regulation vs Temperature

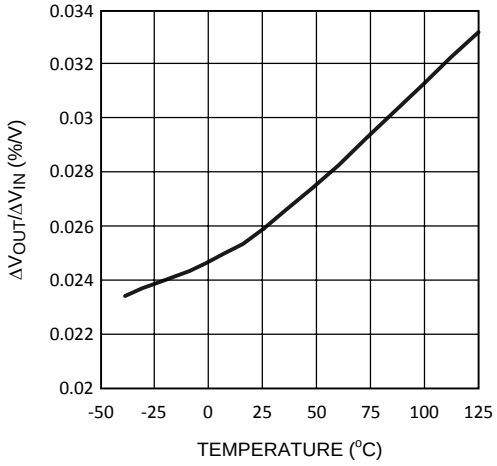


Figure 35.

APPLICATION HINTS

EXTERNAL CAPACITORS

Like any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

INPUT CAPACITOR:

An input capacitor of at least 1µF is required (ceramic recommended). The capacitor must be located not more than one centimeter from the input pin and returned to a clean analog ground.

OUTPUT CAPACITOR:

An output capacitor is required for loop stability. It must be located less than 1 centimeter from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them.

The minimum amount of output capacitance that can be used for stable operation is 1µF. Ceramic capacitors are recommended (the LP38690/2 was designed for use with ultra low ESR capacitors). The LP38690/2 is stable with any output capacitor ESR between zero and 100 Ohms.

ENABLE PIN (LP38692 only):

The LP38692 has an Enable pin (EN) which allows an external control signal to turn the regulator output On and Off. The Enable On/Off threshold has no hysteresis. The voltage signal must rise and fall cleanly, and promptly, through the ON and OFF voltage thresholds. The Enable pin has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated either actively or passively. If the Enable pin is driven from a source that actively pulls high and low, the drive voltage should not be allowed to go below ground potential or higher than V_{IN}. If the application does not require the Enable function, the pin should be connected directly to the V_{IN} pin.

Foldback Current Limiting:

Foldback current limiting is built into the LP38690/2 which reduces the amount of output current the part can deliver as the output voltage is reduced. The amount of load current is dependent on the differential voltage between V_{IN} and V_{OUT}. Typically, when this differential voltage exceeds 5V, the load current will limit at about 450 mA. When the V_{IN} - V_{OUT} differential is reduced below 4V, load current is limited to about 1500 mA.

SELECTING A CAPACITOR

It is important to note that capacitance tolerance and variation with temperature must be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range.

Capacitor Characteristics

CERAMIC

For values of capacitance in the 10 to 100 µF range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

X7R and X5R dielectric ceramic capacitors are strongly recommended if ceramics are used, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

TANTALUM

Solid Tantalum capacitors have good temperature stability: a high quality Tantalum will typically show a capacitance value that varies less than 10-15% across the full temperature range of -40°C to +125°C. ESR will vary only about 2X going from the high to low temperature limits.

REVERSE VOLTAGE

A reverse voltage condition will exist when the voltage at the output pin is higher than the voltage at the input pin. Typically this will happen when V_{IN} is abruptly taken low and C_{OUT} continues to hold a sufficient charge such that the input to output voltage becomes reversed. A less common condition is when an alternate voltage source is connected to the output.

There are two possible paths for current to flow from the output pin back to the input during a reverse voltage condition.

1) While V_{IN} is high enough to keep the control circuity alive, and the Enable pin (LP38692 only) is above the $V_{EN(ON)}$ threshold, the control circuitry will attempt to regulate the output voltage. If the input voltage is less than the programmed output voltage, the control circuit will drive the gate of the pass element to the full ON condition. In this condition, reverse current will flow from the output pin to the input pin, limited only by the $R_{DS(ON)}$ of the pass element and the output to input voltage differential. Discharging an output capacitor up to 1000 µF in this manner will not damage the device as the current will rapidly decay. However, continuous reverse current should be avoided. When the Enable pin is low this condition will be prevented.

2) The internal PFET pass element has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, when V_{IN} is below the value where the control circuity is alive, or the Enable pin is low (LP38692 only), and the output voltage is more than 500 mV (typical) above the input voltage the parasitic diode becomes forward biased and current flows from the output pin to the input pin through the diode. The current in the parasitic diode should be limited to less than 1A continuous and 5A peak.

If used in a dual-supply system where the regulator output load is returned to a negative supply, the output pin must be diode clamped to ground to limit the negative voltage transition. A Schottky diode is recommended for this protective clamp.

PCB LAYOUT

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the input, output, and ground pins of the regulator using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out C_{IN} and C_{OUT} near the device with short traces to the V_{IN}, V_{OUT}, and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a "single point ground".

It should be noted that stability problems have been seen in applications where "vias" to an internal ground plane were used at the ground points of the IC and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and it's capacitors fixed the problem. Since high current flows through the traces going into V_{IN} and coming from V_{OUT}, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

WSON MOUNTING

The NGG0006A (No Pullback) 6-Lead WSON package requires specific mounting techniques which are detailed in the TI AN-1187 Application Report. Referring to the section **PCB Design Recommendations** (Page 5), it should be noted that the pad style which should be used with the WSON package is the NSMD (non-solder mask defined) type. Additionally, it is recommended the PCB terminal pads to be 0.2 mm longer than the package pads to create a solder fillet to improve reliability and inspection.

The input current is split between two V_{IN} pins, 1 and 6. The two V_{IN} pins must be connected together to ensure that the device can meet all specifications at the rated current.

The thermal dissipation of the WSON package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP.

The DAP (exposed pad) on the bottom of the WSON package is connected to the die substrate with a conductive die attach adhesive. The DAP has no direct electrical (wire) connection to any of the pins. There is a parasitic PN junction between the die substrate and the device ground. As such, it is strongly recommend that the DAP be connected directly to the ground at device lead 2 (i.e. GND). Alternately, but not recommended, the DAP may be left floating (i.e. no electrical connection). The DAP must not be connected to any potential other than ground.

For the LP38690SD and LP38692SD in the NGG0006A 6-Lead WSON package, the junction-to-case thermal rating, θ_{JC}, is 10.4°C/W, where the case is the bottom of the package at the center of the DAP. The junction-to-ambient thermal performance for the LP38690SD and LP38692SD in the NGG0006A 6-Lead WSON package, using the JEDEC JESD51 standards is summarized in the following table:

Board Type	Thermal Vias	θ_{JC}	θ_{JA}
JEDEC 2–Layer JESD 51-3	None	10.4°C/W	237°C/W
JEDEC 4–Layer JESD 51-7	1	10.4°C/W	74°C/W
	2	10.4°C/W	60°C/W
	4	10.4°C/W	49°C/W
	6	10.4°C/W	45°C/W

RFI/EMI SUSCEPTIBILITY

RFI (radio frequency interference) and EMI (electromagnetic interference) can degrade any integrated circuit's performance because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the IC regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the IC.

If a load is connected to the IC output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the IC output. Since the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. This means the effective output impedance of the IC at frequencies above 100 kHz is determined only by the output capacitor(s).

In applications where the load is switching at high speed, the output of the IC may need RF isolation from the load. It is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

PCB layout is also critical in high noise environments, since RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from "clean" circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/ EMI can cause ground bounce across the ground plane. In multi-layer PCB applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

OUTPUT NOISE

Noise is specified in two ways: **Spot Noise** or **Output Noise Density** is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency. **Total Output Noise** or **Broad-Band Noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units µV/root-Hz or nV/root-Hz and total output noise is measured in µV(rms)

The primary source of noise in low-dropout regulators is the internal reference. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current).

REVISION HISTORY

Changes from Revision I (April 2013) to Revision J	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38690DT-1.8/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38690 DT-1.8	Samples
LP38690DT-2.5	ACTIVE	TO-252	NDP	3	75	TBD	Call TI	Call TI	-40 to 125		Samples
LP38690DT-2.5/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38690 DT-2.5	Samples
LP38690DT-3.3	NRND	TO-252	NDP	3	75	TBD	Call TI	Call TI	-40 to 125	LP38690 DT-3.3	
LP38690DT-3.3/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38690 DT-3.3	Samples
LP38690DT-5.0	NRND	TO-252	NDP	3	75	TBD	Call TI	Call TI	-40 to 125	LP38690 DT-5.0	
LP38690DT-5.0/NOPB	ACTIVE	TO-252	NDP	3	75	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38690 DT-5.0	Samples
LP38690DTX-1.8	ACTIVE	TO-252	NDP	3	2500	TBD	Call TI	Call TI	-40 to 125		Samples
LP38690DTX-1.8/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38690 DT-1.8	Samples
LP38690DTX-2.5	ACTIVE	TO-252	NDP	3	2500	TBD	Call TI	Call TI	-40 to 125		Samples
LP38690DTX-2.5/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38690 DT-2.5	Samples
LP38690DTX-3.3	ACTIVE	TO-252	NDP	3	2500	TBD	Call TI	Call TI	-40 to 125	LP38690 DT-3.3	Samples
LP38690DTX-3.3/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38690 DT-3.3	Samples
LP38690DTX-5.0/NOPB	ACTIVE	TO-252	NDP	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	LP38690 DT-5.0	Samples
LP38690SD-1.8	NRND	WSON	NGG	6	1000	TBD	Call TI	Call TI	-40 to 125	L113B	
LP38690SD-1.8/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L113B	Samples
LP38690SD-2.5	NRND	WSON	NGG	6	1000	TBD	Call TI	Call TI	-40 to 125	L114B	
LP38690SD-2.5/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L114B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38690SD-3.3/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L115B	Samples
LP38690SD-5.0/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L116B	Samples
LP38690SDX-1.8/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L113B	Samples
LP38690SDX-2.5	NRND	WSON	NGG	6	4500	TBD	Call TI	Call TI	-40 to 125	L114B	
LP38690SDX-2.5/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L114B	Samples
LP38690SDX-3.3/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L115B	Samples
LP38690SDX-5.0/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L116B	Samples
LP38692MP-1.8/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJPB	Samples
LP38692MP-2.5	NRND	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LJRB	
LP38692MP-2.5/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJRB	Samples
LP38692MP-3.3	NRND	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LJSB	
LP38692MP-3.3/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJSB	Samples
LP38692MP-5.0	NRND	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LJTB	
LP38692MP-5.0/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJTB	Samples
LP38692MPX-1.8/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJPB	Samples
LP38692MPX-2.5/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJRB	Samples
LP38692MPX-3.3/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJSB	Samples
LP38692MPX-5.0/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJTB	Samples
LP38692SD-1.8/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L123B	Samples
LP38692SD-2.5/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L124B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38692SD-3.3/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L125B	Samples
LP38692SD-5.0	NRND	WSON	NGG	6	1000	TBD	Call TI	Call TI	-40 to 125	L126B	
LP38692SD-5.0/NOPB	ACTIVE	WSON	NGG	6	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L126B	Samples
LP38692SDX-1.8/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L123B	Samples
LP38692SDX-2.5/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L124B	Samples
LP38692SDX-3.3/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L125B	Samples
LP38692SDX-5.0/NOPB	ACTIVE	WSON	NGG	6	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L126B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

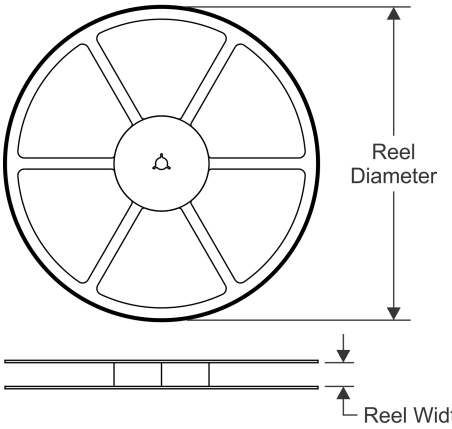
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

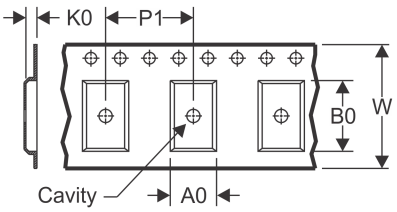
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

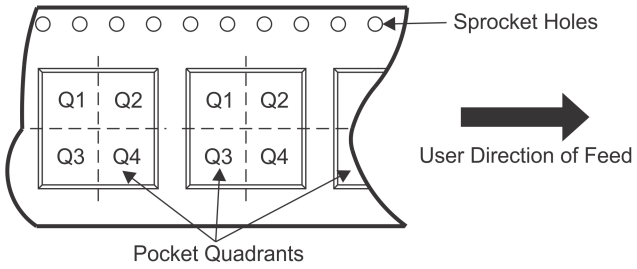


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

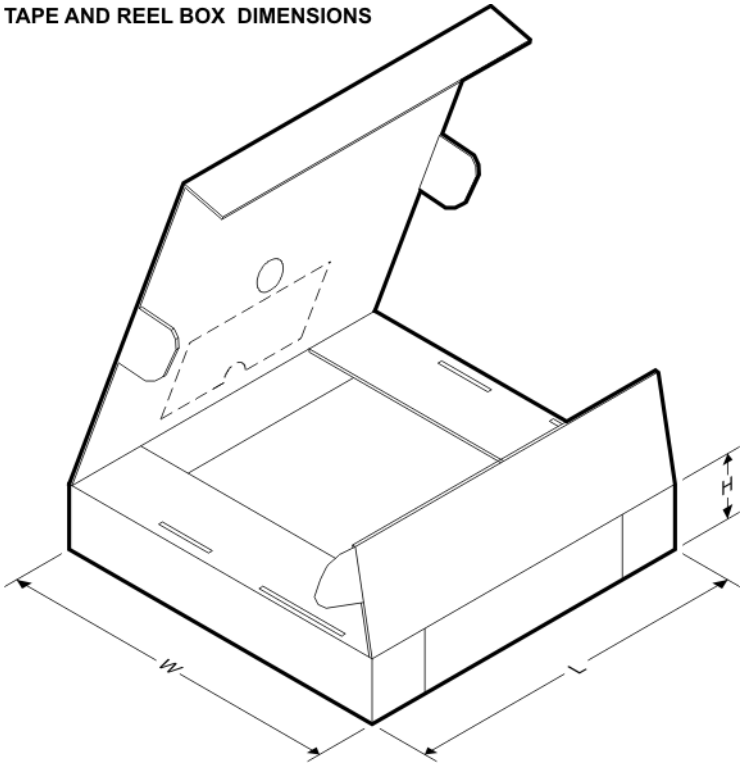


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38690DTX-1.8/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP38690DTX-2.5/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP38690DTX-3.3	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP38690DTX-3.3/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP38690DTX-5.0/NOPB	TO-252	NDP	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
LP38690SD-1.8	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38690SD-1.8/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38690SD-2.5	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38690SD-2.5/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38690SD-3.3/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38690SD-5.0/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38690SDX-1.8/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38690SDX-2.5	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38690SDX-2.5/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38690SDX-3.3/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38690SDX-5.0/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38692MP-1.8/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38692MP-2.5	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38692MP-2.5/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38692MP-3.3	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38692MP-3.3/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38692MP-5.0	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38692MP-5.0/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38692MPX-1.8/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38692MPX-2.5/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38692MPX-3.3/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38692MPX-5.0/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP38692SD-1.8/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38692SD-2.5/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38692SD-3.3/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38692SD-5.0	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38692SD-5.0/NOPB	WSON	NGG	6	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38692SDX-1.8/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38692SDX-2.5/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38692SDX-3.3/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP38692SDX-5.0/NOPB	WSON	NGG	6	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

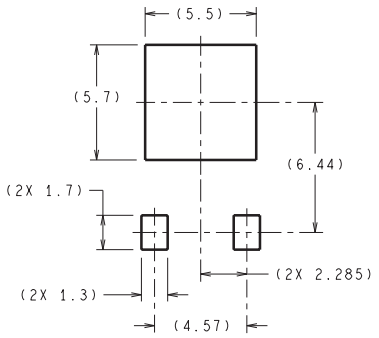
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

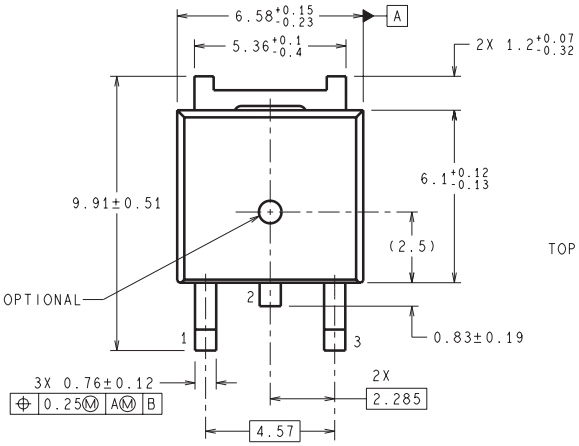
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38690DTX-1.8/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LP38690DTX-2.5/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LP38690DTX-3.3	TO-252	NDP	3	2500	367.0	367.0	35.0
LP38690DTX-3.3/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LP38690DTX-5.0/NOPB	TO-252	NDP	3	2500	367.0	367.0	38.0
LP38690SD-1.8	WSON	NGG	6	1000	210.0	185.0	35.0
LP38690SD-1.8/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38690SD-2.5	WSON	NGG	6	1000	210.0	185.0	35.0
LP38690SD-2.5/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38690SD-3.3/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38690SD-5.0/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38690SDX-1.8/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38690SDX-2.5	WSON	NGG	6	4500	367.0	367.0	35.0
LP38690SDX-2.5/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38690SDX-3.3/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38690SDX-5.0/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38692MP-1.8/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP38692MP-2.5	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP38692MP-2.5/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP38692MP-3.3	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP38692MP-3.3/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP38692MP-5.0	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP38692MP-5.0/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP38692MPX-1.8/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP38692MPX-2.5/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP38692MPX-3.3/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP38692MPX-5.0/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP38692SD-1.8/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38692SD-2.5/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38692SD-3.3/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38692SD-5.0	WSON	NGG	6	1000	210.0	185.0	35.0
LP38692SD-5.0/NOPB	WSON	NGG	6	1000	210.0	185.0	35.0
LP38692SDX-1.8/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38692SDX-2.5/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38692SDX-3.3/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0
LP38692SDX-5.0/NOPB	WSON	NGG	6	4500	367.0	367.0	35.0

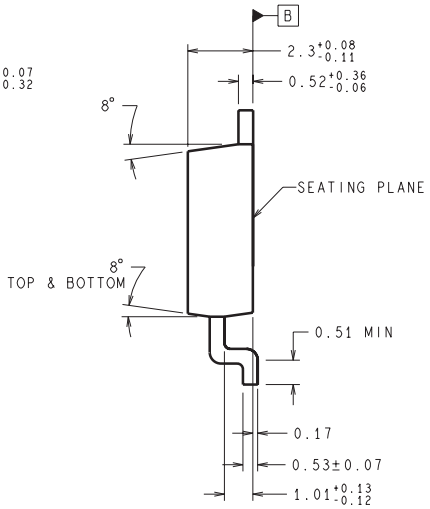
NDP0003B

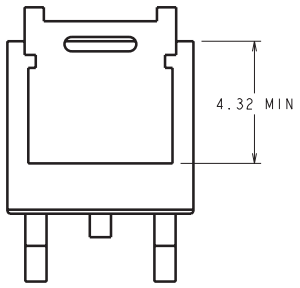


LAND PATTERN RECOMMENDATION

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

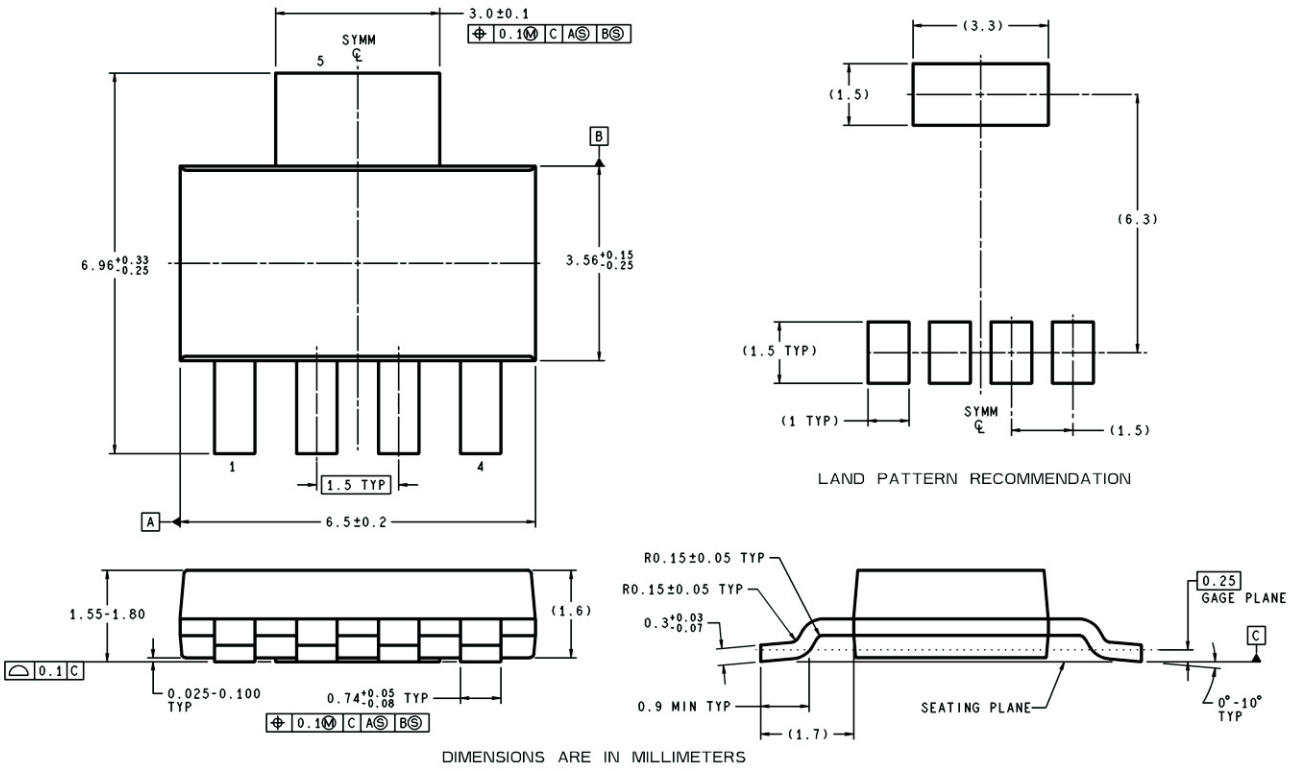




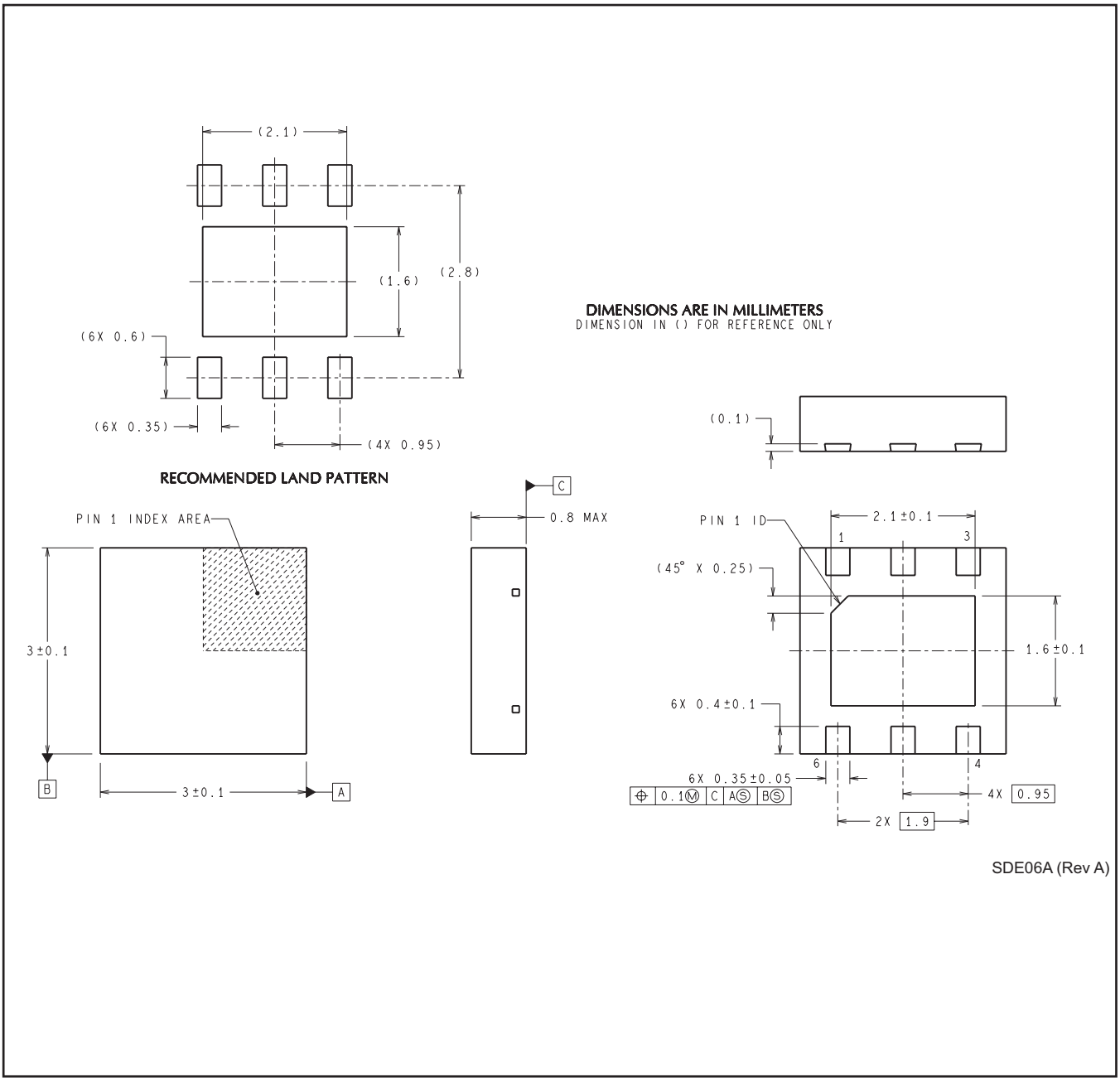


TD03B (Rev F)

NDC0005A


3.0±0.1
0.1 M C A S B S
SYMM
5
B
6.96 +0.33 -0.25
3.56 +0.15 -0.25
1
4
1.5 TYP
A
6.5±0.2
(3.3)
(1.5)
(6.3)
(1.5 TYP)
(1 TYP)
SYMM
(1.5)
LAND PATTERN RECOMMENDATION
1.55-1.80
(1.6)
0.1 C
0.025-0.100 TYP
0.74 +0.05 -0.08 TYP
0.1 M C A S B S
R0.15±0.05 TYP
R0.15±0.05 TYP
0.3 +0.03 -0.07
0.25
GAGE PLANE
C
0.9 MIN TYP
(1.7)
SEATING PLANE
0°-10° TYP
DIMENSIONS ARE IN MILLIMETERS
MP05A (Rev A)

NGG0006A



SDE06A (Rev A)

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122