# Spartan-6 FPGA Data Sheet: DC and Switching Characteristics

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**Advance Product Specification**

## Spartan-6 FPGA Electrical Characteristics

Spartan®-6 FPGAs are available in -3, -2, -1L speed grades, with -3 having the highest performance. Spartan-6 FPGA DC and AC characteristics are specified for both commercial and industrial grades. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -2 speed grade industrial device are the same as for a -2 speed grade commercial device). However, only selected speed grades and/or devices might be available in the industrial range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Spartan-6 FPGA data sheet, part of an overall set of documentation on the Spartan-6 family of FPGAs, is available on the Xilinx website.

All specifications are subject to change without notice.

## Spartan-6 FPGA DC Characteristics

*Table 1:* **Absolute Maximum Ratings**

| Symbol | Description | | Units |
|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage relative to GND | –0.5 to 1.32 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage relative to GND | –0.5 to 3.75 | V |
| $V_{CCO}$ | Output drivers supply voltage relative to GND | –0.5 to 3.75 | V |
| $V_{BATT}$ | Key memory battery backup supply (XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T only) | –0.5 to 4.05 | V |
| $V_{FS}$ | External voltage supply for eFUSE programming (XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T only).(5) | –0.5 to 3.75 | V |
| $V_{REF}$ | Input reference voltage | –0.5 to 3.75 | V |
| $V_{IN}$(2) | I/O input voltage relative to GND(3) (user and dedicated I/Os) | –0.95 to 4.4 | V |
| $V_{TS}$ | Voltage applied to 3-state output (user and dedicated I/Os) | –0.95 to 4.4 | V |
| $T_{STG}$ | Storage temperature (ambient) | –65 to 150 | °C |
| $T_{SOL}$ | Maximum soldering temperature(4) (TQG144, CSG225, CSG324, and FTG256) | +260 | °C |
| | Maximum soldering temperature(4) (Pb-free packages: FGG484 and FGG676) | +250 | °C |
| | Maximum soldering temperature(4) (Pb packages: FT256, FG484, FG676) | +220 | °C |
| $T_J$ | Maximum junction temperature(4) | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. I/O absolute maximum limit applied to DC and AC signals.
3. For I/O operation, refer to the Spartan-6 FPGA SelectIO Resources User Guide.
4. For soldering guidelines and thermal considerations, see Spartan-6 FPGA Packaging and Pinout Specification.
5. When not programming eFUSE, connect $V_{FS}$ to $V_{CCAUX}$.

*Table 2:* **Recommended Operating Conditions**

| Symbol | Description | Temperature Range | Speed Grade | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{CCINT}$ | Internal supply voltage relative to GND, $T_J$ = 0°C to +85°C | Commercial | -3, -2 | 1.14 | 1.2 | 1.26 | V |
| | Internal supply voltage relative to GND, $T_J$ = –40°C to +100°C | Industrial | -2 | 1.14 | 1.2 | 1.26 | V |
| | | | -1L | 0.95 | 1.0 | 1.05 | V |
| $V_{CCAUX}$(1) | Auxiliary supply voltage relative to GND when $V_{CCAUX}$ = 2.5V, $T_J$ = 0°C to +85°C | Commercial | -3, -2 | 2.375 | 2.5 | 2.625 | V |
| | Auxiliary supply voltage relative to GND when $V_{CCAUX}$ = 2.5V, $T_J$ = –40°C to +100°C | Industrial | -2, -1L | | | | |
| | Auxiliary supply voltage relative to GND when $V_{CCAUX}$ = 3.3V, $T_J$ = 0°C to +85°C | Commercial | -3, -2 | 3.15 | 3.3 | 3.45 | V |
| | Auxiliary supply voltage relative to GND when $V_{CCAUX}$ = 3.3V, $T_J$ = –40°C to +100°C | Industrial | -2, -1L | | | | |
| $V_{CCO}$(2,3) | Output supply voltage relative to GND, $T_J$ = 0°C to +85°C | Commercial | -3, -2 | 1.1 | | 3.45 | V |
| | Output supply voltage relative to GND, $T_J$ = –40°C to +100°C | Industrial | -2, -1L | | | | |
| $V_{IN}$ | Input voltage relative to GND, $T_J$ = 0°C to +85°C | Commercial | -3, -2 | – 0.5 | | 4.1 | V |
| | Input voltage relative to GND, $T_J$ = –40°C to +100°C | Industrial | -2, -1L | | | | |
| $V_{BATT}$(4) | Battery voltage relative to GND, $T_J$ = 0°C to +85°C (XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T only) | Commercial | -3, -2 | 1.0 | | 3.6 | V |
| | Battery voltage relative to GND, $T_J$ = –40°C to +100°C (XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T only) | Industrial | -2, -1L | | | | |
| $V_{FS}$ | External voltage supply for eFUSE programming (XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T only).(6) | All | All | 3.2 | 3.3 | 3.4 | V |
| $R_{FUSE}$ | External resistor for eFUSE programming (XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T only). | All | All | 1129 | 1140 | 1151 | Ω |

**Notes:**
1. Recommended maximum voltage droop for $V_{CCAUX}$ is 10 mV/ms.
2. Configuration data is retained even if $V_{CCO}$ drops to 0V.
3. Includes $V_{CCO}$ of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
4. $V_{BATT}$ is required only when using bitstream encryption. If battery is not used, connect $V_{BATT}$ to either GND or $V_{CCAUX}$.
5. All voltages are relative to ground.
6. When not programming eFUSE, connect $V_{FS}$ to $V_{CCAUX}$.

*Table 3:* **DC Characteristics Over Recommended Operating Conditions**

| Symbol | Description | Speed Grade | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{DRINT}$ | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) | -3, -2 | 0.8 | | | V |
| | | -1L | 0.8 | | | V |
| $V_{DRAUX}$ | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) | | 2.0 | | | V |
| $I_{REF}$ | $V_{REF}$ leakage current per pin | | –10 | | 10 | µA |
| $I_L$ | Input or output leakage current per pin (sample-tested) | | –10 | | 10 | µA |
| $C_{IN}$ | Input capacitance (sample-tested) | | | | 10 | pF |

*Table 3:* **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

| Symbol | Description | Speed Grade | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{RPU}$(1) | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V or $V_{CCAUX}$ = 3.3V | -3, -2 | | 332 | | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V or $V_{CCAUX}$ = 2.5V | | | 217 | | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | | | 123 | | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | | | 87 | | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | | | 56 | | µA |
| $I_{RPU}$(1) | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V or $V_{CCAUX}$ = 3.3V | -1L | | | | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V or $V_{CCAUX}$ = 2.5V | | | | | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | | | | | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | | | | | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | | | | | µA |
| $I_{RPD}$(1) | Pad pull-down (when selected) @ $V_{CCO}$ = 2.5V, $V_{CCAUX}$ = 3.3V | -3, -2 | | 341 | | µA |
| | Pad pull-down (when selected) @ $V_{CCO}$ = 2.5V, $V_{CCAUX}$ = 2.5V | | | 229 | | µA |
| $I_{RPD}$(1) | Pad pull-down (when selected) @ $V_{CCO}$ = 2.5V, $V_{CCAUX}$ = 3.3V | -1L | | | | µA |
| | Pad pull-down (when selected) @ $V_{CCO}$ = 2.5V, $V_{CCAUX}$ = 2.5V | | | | | µA |
| $I_{BATT}$(2) | Battery supply current (XC6SLX75, XC6SLX75T, XC6SLX100, XC6SLX100T, XC6SLX150, and XC6SLX150T only) | | | | 150 | nA |

**Notes:**
1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.

## Important Note

Typical values for quiescent supply current are specified at nominal voltage, 25°C junction temperatures ($T_j$). Xilinx recommends analyzing static power consumption at $T_j$ = 25°C. Quiescent supply current is specified by speed grade for Spartan-6 devices. Xilinx recommends analyzing static power consumption using the XPOWER™ Estimator (XPE) tool (download at http://www.xilinx.com/power) for conditions other than those specified in Table 4.

*Table 4:* **Typical Quiescent Supply Current**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current | XC6SLX4 | 4.0 | 4.0 | 2.4 | mA |
| | | XC6SLX9 | 4.0 | 4.0 | 2.4 | mA |
| | | XC6SLX16 | 6.0 | 6.0 | 3.6 | mA |
| | | XC6SLX25 | 11.0 | 11.0 | 6.6 | mA |
| | | XC6SLX25T | 11.0 | 11.0 | N/A | mA |
| | | XC6SLX45 | 18.0 | 18.0 | 10.8 | mA |
| | | XC6SLX45T | 18.0 | 18.0 | N/A | mA |
| | | XC6SLX75 | | | | mA |
| | | XC6SLX75T | | | N/A | mA |
| | | XC6SLX100 | 36.0 | 36.0 | 21.6 | mA |
| | | XC6SLX100T | 36.0 | 36.0 | N/A | mA |
| | | XC6SLX150 | 51.0 | 51.0 | 30.6 | mA |
| | | XC6SLX150T | 51.0 | 51.0 | N/A | mA |

*Table 4:* **Typical Quiescent Supply Current *(Cont'd)***

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current | XC6SLX4 | 1.0 | 1.0 | 1.0 | mA |
| | | XC6SLX9 | 1.0 | 1.0 | 1.0 | mA |
| | | XC6SLX16 | 2.0 | 2.0 | 2.0 | mA |
| | | XC6SLX25 | 2.0 | 2.0 | 2.0 | mA |
| | | XC6SLX25T | 2.0 | 2.0 | N/A | mA |
| | | XC6SLX45 | 3.0 | 3.0 | 3.0 | mA |
| | | XC6SLX45T | 3.0 | 3.0 | N/A | mA |
| | | XC6SLX75 | | | | mA |
| | | XC6SLX75T | | | N/A | mA |
| | | XC6SLX100 | 5.0 | 5.0 | 5.0 | mA |
| | | XC6SLX100T | 5.0 | 5.0 | N/A | mA |
| | | XC6SLX150 | 7.0 | 7.0 | 7.0 | mA |
| | | XC6SLX150T | 7.0 | 7.0 | N/A | mA |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current | XC6SLX4 | 3.0 | 3.0 | 3.0 | mA |
| | | XC6SLX9 | 3.0 | 3.0 | 3.0 | mA |
| | | XC6SLX16 | 3.0 | 3.0 | 3.0 | mA |
| | | XC6SLX25 | 4.0 | 4.0 | 4.0 | mA |
| | | XC6SLX25T | 4.0 | 4.0 | N/A | mA |
| | | XC6SLX45 | 5.0 | 5.0 | 5.0 | mA |
| | | XC6SLX45T | 5.0 | 5.0 | N/A | mA |
| | | XC6SLX75 | | | | mA |
| | | XC6SLX75T | | | N/A | mA |
| | | XC6SLX100 | 8.0 | 8.0 | 8.0 | mA |
| | | XC6SLX100T | 8.0 | 8.0 | N/A | mA |
| | | XC6SLX150 | 12.0 | 12.0 | 12.0 | mA |
| | | XC6SLX150T | 12.0 | 12.0 | N/A | mA |

**Notes:**
1. Typical values are specified at nominal voltage, 25°C junction temperatures ($T_j$). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 25°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

*Table 5:* **Power Supply Ramp Time**

| Symbol | Description | Speed Grade | Ramp Time | Units |
|---|---|---|---|---|
| $V_{CCINTR}$ | Internal supply voltage ramp time | -3, -2 | 0.20 to 50.0 | ms |
| | | -1L | 0.20 to 40.0 | ms |
| $V_{CCOR}$ | Output drivers supply voltage ramp time | All | 0.20 to 50.0 | ms |
| $V_{CCAUXR}$ | Auxiliary supply voltage ramp time | All | 0.20 to 50.0 | ms |

## SelectIO™ Interface DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

*Table 6:* **Single-Ended I/O Standard DC Input and Output Levels**

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVTTL | –0.5 | 0.8 | 2.0 | 4.1 | 0.4 | 2.4 | Note(2) | Note(2) |
| LVCMOS33 | –0.5 | 0.8 | 2.0 | 4.1 | 0.4 | $V_{CCO}$ – 0.4 | Note(2) | Note(2) |
| LVCMOS25 | –0.5 | 0.7 | 1.7 | 4.1 | 0.4 | $V_{CCO}$ – 0.4 | Note(2) | Note(2) |
| LVCMOS18 | –0.5 | 0.38 | 0.8 | 4.1 | 0.45 | $V_{CCO}$ – 0.45 | Note(2) | Note(2) |
| LVCMOS18_JEDEC | –0.5 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | 4.1 | 0.45 | $V_{CCO}$ – 0.45 | Note(2) | Note(2) |
| LVCMOS15 | –0.5 | 0.38 | 0.8 | 4.1 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | Note(3) | Note(3) |
| LVCMOS15_JEDEC | –0.5 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | 4.1 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | Note(3) | Note(3) |
| LVCMOS12 | –0.5 | 0.38 | 0.8 | 4.1 | 0.4 | $V_{CCO}$ – 0.4 | Note(4) | Note(4) |
| LVCMOS12_JEDEC | –0.5 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | 4.1 | 0.4 | $V_{CCO}$ – 0.4 | Note(4) | Note(4) |
| PCI33_3[5] | –0.5 | 30% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ + 0.5 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note(5) | Note(5) |
| PCI66_3[5] | –0.5 | 30% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ + 0.5 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note(5) | Note(5) |
| I2C | –0.5 | 30% $V_{CCO}$ | 70% $V_{CCO}$ | 4.1 | 20% $V_{CCO}$ | – | 3 | – |
| SMBUS | –0.5 | 0.8 | 2.1 | 4.1 | 0.4 | – | 4 | – |
| SDIO | –0.5 | 12.5% $V_{CCO}$ | 75% $V_{CCO}$ | 4.1 | 12.5% $V_{CCO}$ | 75% $V_{CCO}$ | 0.1 | –0.1 |
| MOBILE_DDR | –0.5 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 4.1 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 0.1 | –0.1 |
| HSTL_I | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 4.1 | 0.4 | $V_{CCO}$ – 0.4 | 8 | –8 |
| HSTL_II | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 4.1 | 0.4 | $V_{CCO}$ – 0.4 | 16 | –16 |
| HSTL_III | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 4.1 | 0.4 | $V_{CCO}$ – 0.4 | 24 | –8 |
| HSTL_I_18 | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 4.1 | 0.4 | $V_{CCO}$ – 0.4 | 11 | –11 |
| HSTL_II_18 | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 4.1 | 0.4 | $V_{CCO}$ – 0.4 | 22 | –22 |
| HSTL_III_18 | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 4.1 | 0.4 | $V_{CCO}$ – 0.4 | 30 | –11 |
| SSTL3_I | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 4.1 | $V_{TT}$ – 0.6 | $V_{TT}$ + 0.6 | 8 | –8 |
| SSTL3_II | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 4.1 | $V_{TT}$ – 0.8 | $V_{TT}$ + 0.8 | 16 | –16 |
| SSTL2_I | –0.5 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 4.1 | $V_{TT}$ – 0.61 | $V_{TT}$ + 0.61 | 8.1 | –8.1 |
| SSTL2_II | –0.5 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 4.1 | $V_{TT}$ – 0.81 | $V_{TT}$ + 0.81 | 16.2 | –16.2 |
| SSTL18_I | –0.5 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | 4.1 | $V_{TT}$ – 0.47 | $V_{TT}$ + 0.47 | 6.7 | –6.7 |
| SSTL18_II | –0.5 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | 4.1 | $V_{TT}$ – 0.60 | $V_{TT}$ + 0.60 | 13.4 | –13.4 |
| SSTL15_II | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 4.1 | $V_{TT}$ – 0.4 | $V_{TT}$ + 0.4 | 13.4 | –13.4 |

**Notes:**
1. Tested according to relevant specifications.
2. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
3. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
4. Using drive strengths of 2, 4, 6, 8, or 12 mA.
5. For more information on PCI33_3 and PCI66_3 refer to refer to the Spartan-6 FPGA SelectIO Resources User Guide.

*Table 7:* **Differential I/O Standard DC Input and Output Levels**

| I/O Standard | $V_{ID}$ | | $V_{ICM}$ | | $V_{OD}$ | | $V_{OCM}$ | | $V_{OH}$ | $V_{OL}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| | mV, Min | mV, Max | V, Min | V, Max | mV, Min | mV, Max | V, Min | V, Max | V, Min | V, Max |
| LVDS_33 | 100 | 600 | 0.3 | 2.35 | 247 | 454 | 1.125 | 1.375 | – | – |
| LVDS_25 | 100 | 600 | 0.3 | 2.35 | 247 | 454 | 1.125 | 1.375 | – | – |
| BLVDS_25 | 100 | – | 0.3 | 2.35 | 240 | 460 | Typical 50% $V_{CCO}$ | | – | – |
| MINI_LVDS_33 | 200 | 600 | 0.3 | 1.95 | 300 | 600 | 1.0 | 1.4 | – | – |
| MINI_LVDS_25 | 200 | 600 | 0.3 | 1.95 | 300 | 600 | 1.0 | 1.4 | – | – |
| LVPECL_33 | 100 | 1000 | 0.3 | 2.8 | Inputs only | | | | | |
| LVPECL_25 | 100 | 1000 | 0.3 | 1.95 | Inputs only | | | | | |
| RSDS_33 | 100 | – | 0.3 | 1.5 | 100 | 400 | 1.0 | 1.4 | – | – |
| RSDS_25 | 100 | – | 0.3 | 1.5 | 100 | 400 | 1.0 | 1.4 | – | – |
| TMDS_33 | 150 | 1200 | 2.7 | 3.23 | 400 | 600 | $V_{CCO}$ – 0.3 | $V_{CCO}$ – 0.19 | – | – |
| PPDS_33 | 100 | 400 | 0.2 | 2.3 | 100 | 400 | 0.5 | 1.4 | – | – |
| PPDS_25 | 100 | 400 | 0.2 | 2.3 | 100 | 400 | 0.5 | 1.4 | – | – |
| DISPLAY_PORT | 190 | 1260 | 0.3 | 2.35 | – | – | Typical 50% $V_{CCO}$ | | – | – |
| DIFF_HSTL_I | 100 | – | 0.68 | 0.9 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_HSTL_II | 100 | – | 0.68 | 0.9 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_HSTL_III | 100 | – | 0.68 | 0.9 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_HSTL_I_18 | 100 | – | 0.8 | 1.1 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_HSTL_II_18 | 100 | – | 0.8 | 1.1 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_HSTL_III_18 | 100 | – | 0.8 | 1.1 | – | – | – | – | $V_{CCO}$ – 0.4 | 0.4 |
| DIFF_SSTL3_I | 100 | – | 1.0 | 1.9 | – | – | – | – | $V_{TT}$ + 0.6 | $V_{TT}$ – 0.6 |
| DIFF_SSTL3_II | 100 | – | 1.0 | 1.9 | – | – | – | – | $V_{TT}$ + 0.8 | $V_{TT}$ – 0.8 |
| DIFF_SSTL2_I | 100 | – | 1.0 | 1.5 | – | – | – | – | $V_{TT}$ + 0.61 | $V_{TT}$ – 0.61 |
| DIFF_SSTL2_II | 100 | – | 1.0 | 1.5 | – | – | – | – | $V_{TT}$ + 0.81 | $V_{TT}$ – 0.81 |
| DIFF_SSTL18_I | 100 | – | 0.7 | 1.1 | – | – | – | – | $V_{TT}$ + 0.47 | $V_{TT}$ – 0.47 |
| DIFF_SSTL18_II | 100 | – | 0.7 | 1.1 | – | – | – | – | $V_{TT}$ + 0.6 | $V_{TT}$ – 0.6 |
| DIFF_SSTL15_II | 100 | – | 0.55 | 0.95 | – | – | – | – | $V_{TT}$ + 0.4 | $V_{TT}$ – 0.4 |

*Table 8:* **eFUSE Read Endurance**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| DNA_CYCLES | Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations. | 30,000,000 | | | Read Cycles |
| AES_CYCLES | Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations. | 30,000,000 | | | Read Cycles |

# GTP Transceiver Specifications

## GTP Transceiver DC Characteristics

*Table 9:* **Absolute Maximum Ratings for GTP Transceivers**

| Symbol | Description | Specification | Units |
|---|---|---|---|
| MGTAVCC | Analog supply voltage for the GTP transmitter and receiver circuits relative to GND | –0.5 to 1.32 | V |
| MGTAVTTTX | Analog supply voltage for the GTP transmitter termination circuit relative to GND | –0.5 to 1.32 | V |
| MGTAVTTRX | Analog supply voltage for the GTP receiver termination circuit relative to GND | –0.5 to 1.32 | V |
| MGTAVCCPLL | Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND | –0.5 to 1.32 | V |
| MGTAVTTRCAL | Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom) | –0.5 to 1.32 | V |
| $V_{IN}$ | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage | | V |
| $V_{MGTREFCLK}$ | Reference clock absolute input voltage | | V |

**Notes:**
1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

*Table 10:* **Recommended Operating Conditions for GTP Transceivers(1)(2)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| MGTAVCC | Analog supply voltage for the GTP transmitter and receiver circuits relative to GND | 1.14 | 1.26 | V |
| MGTAVTTTX | Analog supply voltage for the GTP transmitter termination circuit relative to GND | 1.14 | 1.26 | V |
| MGTAVTTRX | Analog supply voltage for the GTP receiver termination circuit relative to GND | 1.14 | 1.26 | V |
| MGTAVCCPLL | Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND | 1.14 | 1.26 | V |
| MGTAVTTRCAL | Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom) | 1.14 | 1.26 | V |

**Notes:**
1. Each voltage listed requires the filter circuit described in *Spartan-6 FPGA GTP Transceiver User Guide*.
2. Voltages are specified for the temperature range of $T_J$ = –40°C to +100°C.

*Table 11:* **DC Characteristics Over Recommended Operating Conditions for GTP Transmitters(1)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $I_{MGTAVCC}$ | GTP transceiver internal analog supply current | | | | mA |
| $I_{MGTAVTTTX}$ | GTP transmitter termination supply current(2) | | | | mA |
| $I_{MGTAVTTRX}$ | GTP receiver termination supply current(2) | | | | mA |
| $I_{MGTAVCCPLL}$ | GTP transmitter and receiver PLL supply current | | | | mA |
| $I_{MGTAVTTRCAL}$ | GTP transceiver resistor termination calibration supply current | | | | mA |
| MGTRREF | Precision reference resistor for internal calibration termination | 50.0 ± 1% tolerance | | | Ω |

**Notes:**
1. Typical values are specified at nominal voltage, 25°C, with a 3.125 Gb/s line rate.
2. $I_{CC}$ numbers are given per GTP transceiver operating with default settings.
3. Values for currents other than the values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

*Table 12:* **GTP Transceiver Quiescent Supply Current**

| Symbol | Description | Typ(1) | Max | Units |
|---|---|---|---|---|
| $I_{AVTTQ}$ | Quiescent MGTAVTT (transmitter termination) supply current | | | mA |
| $I_{AVCCQ}$ | Quiescent MGTAVCC (analog) supply current | | | mA |

**Notes:**
1. Typical values are specified at nominal voltage, 25°C.
2. Device powered and unconfigured.
3. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
4. GTP transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTP transceivers.

## GTP Transceiver DC Input and Output Levels

Table 13 summarizes the DC output specifications of the GTP transceivers in Spartan-6 FPGAs. Figure 1 shows the single-ended output voltage swing. Figure 2 shows the peak-to-peak differential output voltage.

Consult the *Spartan-6 FPGA GTP Transceiver User Guide* for further details.

*Table 13:* **GTP Transceiver DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $DV_{PPIN}$ | Differential peak-to-peak input voltage | External AC coupled | 125 | | 2000 | mV |
| $V_{IN}$ | Input voltage | DC coupled MGTAVTTRX = 1.2V | –400 | | MGTAVTTRX | mV |
| $V_{CMIN}$ | Common mode input voltage | DC coupled MGTAVTTRX = 1.2V | | 2/3 MGTAVTTRX | | mV |
| $DV_{PPOUT}$ | Differential peak-to-peak output voltage(1) | | | | 1000 | mV |
| $V_{SEOUT}$ | Single-ended output voltage swing(1) | | | | 500 | mV |
| $V_{CMOUT}$ | Common mode output voltage | Equation based | MGTAVTTTX – $V_{SEOUT/2}$ | | | mV |
| $R_{IN}$ | Differential input resistance | | | 100 | | Ω |
| $R_{OUT}$ | Differential output resistance | | | 100 | | Ω |
| $T_{OSKEW}$ | Transmitter output skew | | | | | ps |
| $C_{EXT}$ | Recommended external AC coupling capacitor(2) | | 75 | 100 | 200 | nF |

**Notes:**
1. The output swing and preemphasis levels are programmable using the attributes discussed in *Spartan-6 FPGA GTP Transceiver User Guide* and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

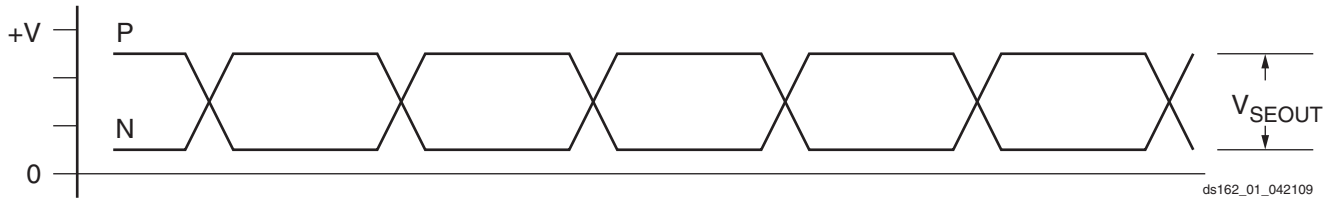


*Figure 1:* **Single-Ended Output Voltage Swing**

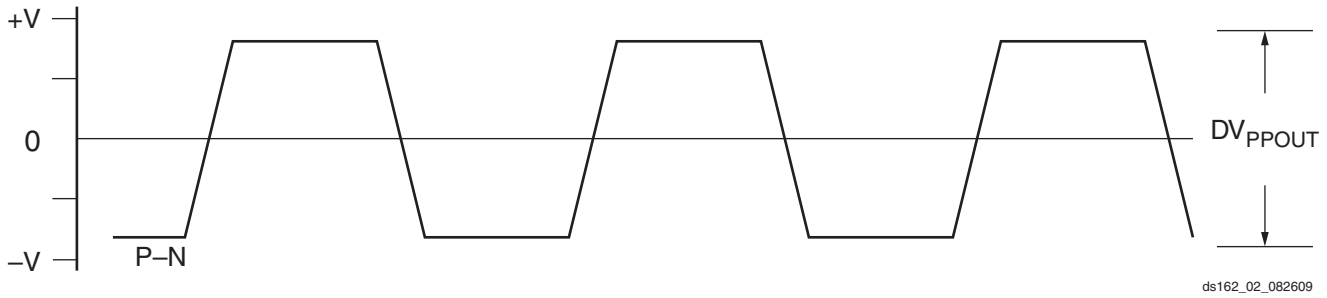


*Figure 2:* **Peak-to-Peak Differential Output Voltage**

Table 14 summarizes the DC specifications of the clock input of the GTP transceiver. Figure 3 shows the single-ended input voltage swing. Figure 4 shows the peak-to-peak differential clock input voltage swing. Consult the Spartan-6 FPGA GTP Transceiver User Guide for further details.

*Table 14:* **GTP Transceiver Clock DC Input Level Specification(1)**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage | | | 800 | | mV |
| $V_{ISE}$ | Single-ended input voltage | | | 400 | | mV |
| $R_{IN}$ | Differential input resistance | | | 100 | | Ω |
| $C_{EXT}$ | Required external AC coupling capacitor | | | 100 | | nF |

**Notes:**
1. $V_{MIN}$ = 0V and $V_{MAX}$ = MGTAVCC

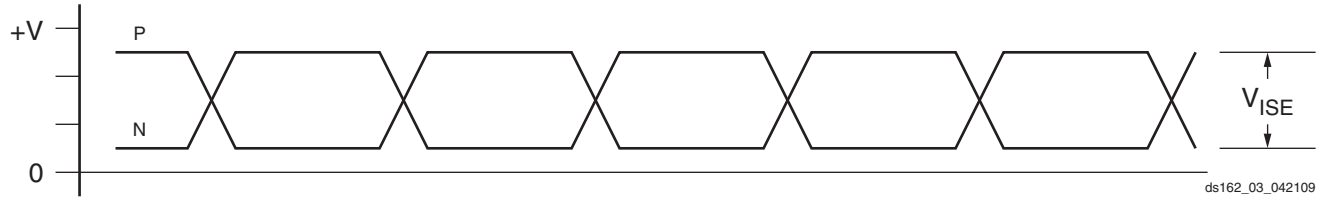


*Figure 3:* **Single-Ended Clock Input Voltage Swing Peak-to-Peak**

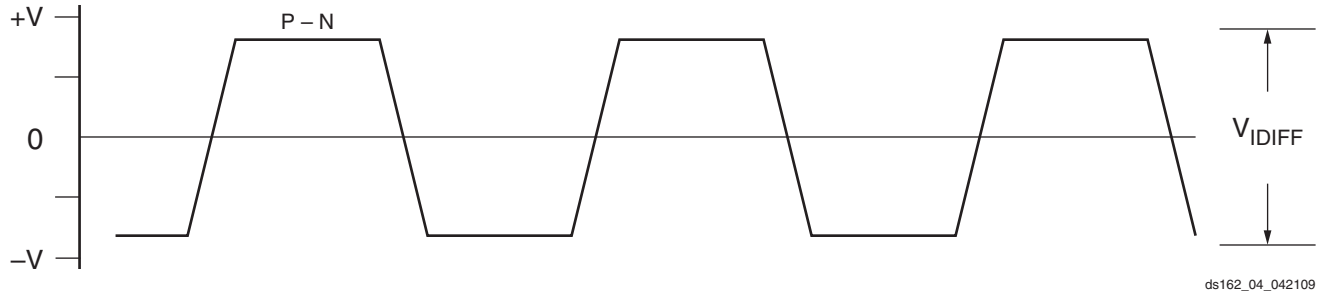


*Figure 4:* **Differential Clock Input Voltage Swing Peak-to-Peak**

## GTP Transceiver Switching Characteristics

Consult the Spartan-6 FPGA GTP Transceiver User Guide for further information.

*Table 15:* **GTP Transceiver Performance**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| $F_{GTPMAX}$ | Maximum GTP transceiver data rate | 3.125 | 2.7 | N/A | Gb/s |
| $F_{GPLLMAX}$ | Maximum PLL frequency | 1.62 | 1.62 | N/A | GHz |
| $F_{GPLLMIN}$ | Minimum PLL frequency | 1.2 | 1.2 | N/A | GHz |

*Table 16:* **Dynamic Reconfiguration Port (DRP) in the GTP Transceiver Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| $F_{GTPDRPCLK}$ | GTPDRPCLK maximum frequency | 100 | 100 | N/A | MHz |

*Table 17:* **GTP Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range | | 60 | | 160 | MHz |
| $T_{RCLK}$ | Reference clock rise time | 20% – 80% | | 200 | | ps |
| $T_{FCLK}$ | Reference clock fall time | 80% – 20% | | 200 | | ps |
| $T_{DCREF}$ | Reference clock duty cycle | Transceiver PLL only | 45 | 50 | 55 | % |
| $T_{LOCK}$ | Clock recovery frequency acquisition time | Initial PLL lock | | | 1 | ms |
| $T_{PHASE}$ | Clock recovery phase acquisition time | Lock to data after PLL has locked to the reference clock | | | | µs |

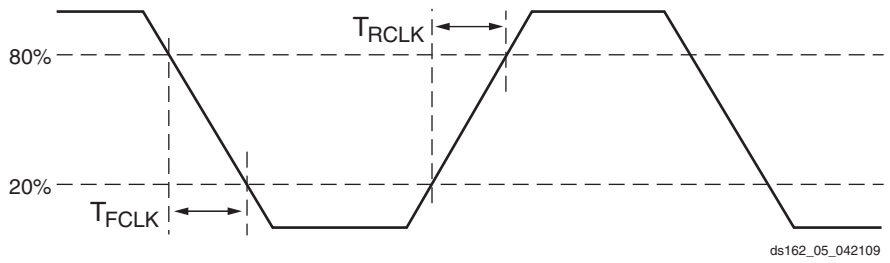


*Figure 5:* **Reference Clock Timing Parameters**

*Table 18:* **GTP Transceiver User Clock Switching Characteristics(1)**

| Symbol | Description | Conditions | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| $F_{TXOUT}$ | TXOUTCLK maximum frequency | Internal 10-bit data path | | | N/A | MHz |
| | | Internal 8-bit data path | | | N/A | MHz |
| $F_{RXREC}$ | RXRECCLK maximum frequency | | | | N/A | MHz |
| $T_{RX}$ | RXUSRCLK maximum frequency | | | | N/A | MHz |
| $T_{RX2}$ | RXUSRCLK2 maximum frequency | 1 byte interface | | | N/A | MHz |
| | | 2 byte interface | | | N/A | MHz |
| | | 4 byte interface | | | N/A | MHz |
| $T_{TX}$ | TXUSRCLK maximum frequency | | | | N/A | MHz |
| $T_{TX2}$ | TXUSRCLK2 maximum frequency | 1 byte interface | | | N/A | MHz |
| | | 2 byte interface | | | N/A | MHz |
| | | 4 byte interface | | | N/A | MHz |
| $T_{DCUSRCLK}$ | TXUSRCLK, TXUSRCLK2, RXUSRCLK, and RXUSRCLK2 duty cycle | 1 byte interface | | | N/A | % |
| | | 2 byte interface | | | N/A | % |
| | | 4 byte interface | | | N/A | % |

**Notes:**
1. Clocking must be implemented as described in Spartan-6 FPGA GTP Transceiver User Guide.

*Table 19:* **GTP Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTPTX}$ | Serial data rate range | | 0.600 | | $F_{GTPMAX}$ | Gb/s |
| $T_{RTX}$ | TX Rise time | 20%–80% | | | | ps |
| $T_{FTX}$ | TX Fall time | 80%–20% | | | | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | | | | ps |
| $V_{TXOOBVDPP}$ | Electrical idle amplitude | | | | 20 | mV |
| $T_{TXOOBTRANSITION}$ | Electrical idle transition time | | | | | ns |
| $T_{J3.125}$ | Total Jitter(2) | 3.125 Gb/s | | | | UI |
| $D_{J3.125}$ | Deterministic Jitter(2) | | | | | UI |
| $T_{J2.5}$ | Total Jitter(2) | 2.5 Gb/s | | | | UI |
| $D_{J2.5}$ | Deterministic Jitter(2) | | | | | UI |
| $T_{J1.62}$ | Total Jitter(2) | 1.62 Gb/s | | | | UI |
| $D_{J1.62}$ | Deterministic Jitter(2) | | | | | UI |
| $T_{J1.25}$ | Total Jitter(2) | 1.25 Gb/s | | | | UI |
| $D_{J1.25}$ | Deterministic Jitter(2) | | | | | UI |
| $T_{J614}$ | Total Jitter(2) | 614 Mb/s | | | | UI |
| $D_{J614}$ | Deterministic Jitter(2) | | | | | UI |

**Notes:**
1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP transceiver sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.

*Table 20:* **GTP Transceiver Receiver Switching Characteristics**

| Symbol | Description | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTPRX}$ | Serial data rate | | 0.600 | | $F_{GTPMAX}$ | Gb/s |
| $T_{RXELECIDLE}$ | Time for RXELECIDLE to respond to loss or restoration of data | | | | | ns |
| $R_{XOOBVDPP}$ | OOB detect threshold peak-to-peak | | 60 | | 150 | mV |
| $R_{XSST}$ | Receiver spread-spectrum tracking(1) | Modulated @ 33 KHz | | | | ppm |
| $R_{XRL}$ | Run length (CID) | Internal AC capacitor bypassed | | | | UI |
| $R_{XPPMTOL}$ | Data/REFCLK PPM offset tolerance | CDR 2nd-order loop disabled | | | | ppm |
| | | CDR 2nd-order loop enabled | | | | ppm |
| **SJ Jitter Tolerance(2)** | | | | | | |
| $JT\_SJ_{3.125}$ | Sinusoidal Jitter(3) | 3.125 Gb/s | | | | UI |
| $JT\_SJ_{2.5}$ | Sinusoidal Jitter(3) | 2.5 Gb/s | | | | UI |
| $JT\_SJ_{1.62}$ | Sinusoidal Jitter(3) | 1.62 Gb/s | | | | UI |
| $JT\_SJ_{1.25}$ | Sinusoidal Jitter(3) | 1.25 Gb/s | | | | UI |
| $JT\_SJ_{614}$ | Sinusoidal Jitter(3) | 614 Mb/s | | | | UI |
| **SJ Jitter Tolerance with Stressed Eye(2)** | | | | | | |
| $JT\_TJSE_{3.125}$ | Total Jitter with Stressed Eye | 3.125 Gb/s | | | | UI |

**Notes:**
1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a Bit Error Ratio of $1e^{-12}$.
3. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.

## Endpoint Block for PCI Express Designs Switching Characteristics

Consult *Spartan-6 FPGA Integrated Endpoint Block for PCI Express* for further information.

*Table 21:* **Maximum Performance for PCI Express Designs**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| $F_{PCIEUSER}$ | User clock maximum frequency | 62.5 | 62.5 | N/A | MHz |

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics, page 14.

*Table 22:* **Interface Performances**

| Description | Speed Grade | | |
|---|---|---|---|
| | -3 | -2 | -1L |
| **Networking Applications** | | | |
| SDR LVDS transmitter (using IOB SDR register) | | | |
| DDR LVDS transmitter (using IOB ODDR2 register) | | | |
| SDR LVDS transmitter (using OSERDES2; DATA WIDTH = 2 to 8) | | | |
| DDR LVDS transmitter (using OSERDES2; DATA WIDTH = 2 to 8) | 1.05 Gb/s | | |
| SDR LVDS receiver (1:7 / 7:1 video link (LDI interface))(1) | | | |
| **Memory Interfaces (Implemented using the Spartan-6 FPGA Memory Controller Block)** | | | |
| DDR | 400 Mb/s | | |
| DDR2 | 800 Mb/s | | |
| DDR3 | 800 Mb/s | | |
| Mobile_DDR | 400 Mb/s | | |

**Notes:**
1. LVDS receivers are typically bounded with certain applications where specific DPA algorithms dominate deterministic performance. Please refer to actual application notes for details.

## Switching Characteristics

All values represented in this data sheet are based on an advanced speed specification (version 1.0). Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

**Advance**

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

**Preliminary**

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

**Production**

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 23 correlates the current status of each Spartan-6 device on a per speed grade basis.

*Table 23:* **Spartan-6 Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC6SLX4 | -2 | | |
| XC6SLX9 | -2 | | |
| XC6SLX16 | -2 | | |
| XC6SLX25 | -2 | | |
| XC6SLX25T | -2 | | |
| XC6SLX45 | -2 | | |
| XC6SLX45T | -2 | | |
| XC6SLX75 | -2 | | |
| XC6SLX75T | -2 | | |
| XC6SLX100 | -2 | | |
| XC6SLX100T | -2 | | |
| XC6SLX150 | -2 | | |
| XC6SLX150T | -2 | | |

## Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-6 devices.

## Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 24 lists the production released Spartan-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE software revisions. The ISE™ software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

*Table 24:* **Spartan-6 Device Production Software and Speed Specification Release**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | -3 | -2 | -1L |
| XC6SLX4 | | | |
| XC6SLX9 | | | |
| XC6SLX16 | | | |
| XC6SLX25 | | | |
| XC6SLX25T | | | N/A |
| XC6SLX45 | | | |
| XC6SLX45T | | | N/A |
| XC6SLX75 | | | |
| XC6SLX75T | | | N/A |
| XC6SLX100 | | | |
| XC6SLX100T | | | N/A |
| XC6SLX150 | | | |
| XC6SLX150T | | | N/A |

**Notes:**
1. Blank entries indicate a device and/or speed grade in advance or preliminary status.

## IOB Pad Input/Output/3-State Switching Characteristics

Table 25 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

$T_{IOPI}$ is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

$T_{IOOP}$ is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

$T_{IOTP}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 26 summarizes the value of $T_{IOTPHZ}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

*Table 25:* **IOB Switching Characteristics**

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -3 | -2 | -1L | -3 | -2 | -1L | -3 | -2 | -1L | |
| LVDS_33 | | 1.50 | | | 1.90 | | | 1.90 | | ns |
| LVDS_25 | | 1.36 | | | 2.03 | | | 2.03 | | ns |
| BLVDS_25 | | 1.36 | | | 2.18 | | | 2.18 | | ns |
| MINI_LVDS_33 | | 1.50 | | | 1.89 | | | 1.89 | | ns |
| MINI_LVDS_25 | | 1.36 | | | 2.03 | | | 2.03 | | ns |
| LVPECL_33 | | 1.50 | | | N/A | | | N/A | | ns |
| LVPECL_25 | | 1.36 | | | N/A | | | N/A | | ns |

*Table 25:* **IOB Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -3 | -2 | -1L | -3 | -2 | -1L | -3 | -2 | -1L | |
| RSDS_33 (point to point) | | 1.50 | | | 1.90 | | | 1.90 | | ns |
| RSDS_25 (point to point) | | 1.36 | | | 2.02 | | | 2.02 | | ns |
| TMDS_33 | | 1.53 | | | 1.85 | | | 1.85 | | ns |
| PPDS_33 | | 1.50 | | | 1.90 | | | 1.90 | | ns |
| PPDS_25 | | 1.36 | | | 2.03 | | | 2.03 | | ns |
| DISPLAY_PORT | | 1.36 | | | 3.32 | | | 3.32 | | ns |
| I2C | | 1.66 | | | 6.39 | | | 6.39 | | ns |
| SMBUS | | 1.66 | | | 6.39 | | | 6.39 | | ns |
| SDIO | | 1.69 | | | 3.03 | | | 3.03 | | ns |
| MOBILE_DDR | | 1.26 | | | 2.83 | | | 2.83 | | ns |
| HSTL_I | | 1.22 | | | 1.99 | | | 1.99 | | ns |
| HSTL_II | | 1.22 | | | 1.98 | | | 1.98 | | ns |
| HSTL_III | | 1.28 | | | 2.01 | | | 2.01 | | ns |
| HSTL_I _18 | | 1.27 | | | 2.02 | | | 2.02 | | ns |
| HSTL_II _18 | | 1.27 | | | 2.05 | | | 2.05 | | ns |
| HSTL_III _18 | | 1.32 | | | 1.94 | | | 1.94 | | ns |
| SSTL3_I | | 1.92 | | | 1.98 | | | 1.98 | | ns |
| SSTL3_II | | 1.92 | | | 2.02 | | | 2.02 | | ns |
| SSTL2_I | | 1.63 | | | 1.94 | | | 1.94 | | ns |
| SSTL2_II | | 1.64 | | | 1.99 | | | 1.99 | | ns |
| SSTL18_I | | 1.23 | | | 1.89 | | | 1.89 | | ns |
| SSTL18_II | | 1.22 | | | 1.92 | | | 1.92 | | ns |
| SSTL15_II | | 1.20 | | | 1.95 | | | 1.95 | | ns |
| DIFF_HSTL_I | | 1.27 | | | 2.03 | | | 2.03 | | ns |
| DIFF_HSTL_II | | 1.27 | | | 1.99 | | | 1.99 | | ns |
| DIFF_HSTL_III | | 1.27 | | | 1.97 | | | 1.97 | | ns |
| DIFF_HSTL_I_18 | | 1.31 | | | 2.05 | | | 2.05 | | ns |
| DIFF_HSTL_II_18 | | 1.30 | | | 1.97 | | | 1.97 | | ns |
| DIFF_HSTL_III_18 | | 1.31 | | | 1.99 | | | 1.99 | | ns |
| DIFF_SSTL3_I | | 1.50 | | | 2.03 | | | 2.03 | | ns |
| DIFF_SSTL3_II | | 1.50 | | | 2.06 | | | 2.06 | | ns |
| DIFF_SSTL2_I | | 1.36 | | | 2.05 | | | 2.05 | | ns |
| DIFF_SSTL2_II | | 1.36 | | | 2.03 | | | 2.03 | | ns |
| DIFF_SSTL18_I | | 1.31 | | | 1.97 | | | 1.97 | | ns |
| DIFF_SSTL18_II | | 1.31 | | | 1.97 | | | 1.97 | | ns |
| DIFF_SSTL15_II | | 1.28 | | | 1.95 | | | 1.95 | | ns |

*Table 25:* **IOB Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -3 | -2 | -1L | -3 | -2 | -1L | -3 | -2 | -1L | |
| LVTTL, QUIETIO, 2 mA | | 1.69 | | | 5.68 | | | 5.68 | | ns |
| LVTTL, QUIETIO, 4 mA | | 1.69 | | | 4.55 | | | 4.55 | | ns |
| LVTTL, QUIETIO, 6 mA | | 1.69 | | | 4.07 | | | 4.07 | | ns |
| LVTTL, QUIETIO, 8 mA | | 1.69 | | | 3.59 | | | 3.59 | | ns |
| LVTTL, QUIETIO, 12 mA | | 1.69 | | | 3.60 | | | 3.60 | | ns |
| LVTTL, QUIETIO, 16 mA | | 1.69 | | | 3.31 | | | 3.31 | | ns |
| LVTTL, QUIETIO, 24 mA | | 1.69 | | | 3.10 | | | 3.10 | | ns |
| LVTTL, Slow, 2 mA | | 1.69 | | | 4.73 | | | 4.73 | | ns |
| LVTTL, Slow, 4 mA | | 1.69 | | | 3.57 | | | 3.57 | | ns |
| LVTTL, Slow, 6 mA | | 1.69 | | | 3.18 | | | 3.18 | | ns |
| LVTTL, Slow, 8 mA | | 1.69 | | | 3.03 | | | 3.03 | | ns |
| LVTTL, Slow, 12 mA | | 1.69 | | | 2.94 | | | 2.94 | | ns |
| LVTTL, Slow, 16 mA | | 1.69 | | | 2.81 | | | 2.81 | | ns |
| LVTTL, Slow, 24 mA | | 1.69 | | | 2.53 | | | 2.53 | | ns |
| LVTTL, Fast, 2 mA | | 1.69 | | | 4.16 | | | 4.16 | | ns |
| LVTTL, Fast, 4 mA | | 1.69 | | | 2.97 | | | 2.97 | | ns |
| LVTTL, Fast, 6 mA | | 1.69 | | | 2.60 | | | 2.60 | | ns |
| LVTTL, Fast, 8 mA | | 1.69 | | | 2.42 | | | 2.42 | | ns |
| LVTTL, Fast, 12 mA | | 1.69 | | | 2.29 | | | 2.29 | | ns |
| LVTTL, Fast, 16 mA | | 1.69 | | | 2.25 | | | 2.25 | | ns |
| LVTTL, Fast, 24 mA | | 1.69 | | | 2.25 | | | 2.25 | | ns |
| LVCMOS33, QUIETIO, 2 mA | | 1.69 | | | 5.68 | | | 5.68 | | ns |
| LVCMOS33, QUIETIO, 4 mA | | 1.69 | | | 4.40 | | | 4.40 | | ns |
| LVCMOS33, QUIETIO, 6 mA | | 1.69 | | | 3.89 | | | 3.89 | | ns |
| LVCMOS33, QUIETIO, 8 mA | | 1.69 | | | 3.69 | | | 3.69 | | ns |
| LVCMOS33, QUIETIO, 12 mA | | 1.69 | | | 3.30 | | | 3.30 | | ns |
| LVCMOS33, QUIETIO, 16 mA | | 1.69 | | | 3.17 | | | 3.17 | | ns |
| LVCMOS33, QUIETIO, 24 mA | | 1.69 | | | 3.03 | | | 3.03 | | ns |
| LVCMOS33, Slow, 2 mA | | 1.69 | | | 4.73 | | | 4.73 | | ns |
| LVCMOS33, Slow, 4 mA | | 1.69 | | | 3.41 | | | 3.41 | | ns |
| LVCMOS33, Slow, 6 mA | | 1.69 | | | 3.02 | | | 3.02 | | ns |
| LVCMOS33, Slow, 8 mA | | 1.69 | | | 3.03 | | | 3.03 | | ns |
| LVCMOS33, Slow, 12 mA | | 1.69 | | | 2.77 | | | 2.77 | | ns |
| LVCMOS33, Slow, 16 mA | | 1.69 | | | 2.77 | | | 2.77 | | ns |
| LVCMOS33, Slow, 24 mA | | 1.69 | | | 2.52 | | | 2.52 | | ns |
| LVCMOS33, Fast, 2 mA | | 1.69 | | | 4.18 | | | 4.18 | | ns |
| LVCMOS33, Fast, 4 mA | | 1.69 | | | 2.98 | | | 2.98 | | ns |
| LVCMOS33, Fast, 6 mA | | 1.69 | | | 2.60 | | | 2.60 | | ns |

*Table 25:* **IOB Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -3 | -2 | -1L | -3 | -2 | -1L | -3 | -2 | -1L | |
| LVCMOS33, Fast, 8 mA | | 1.69 | | | 2.40 | | | 2.40 | | ns |
| LVCMOS33, Fast, 12 mA | | 1.69 | | | 2.17 | | | 2.17 | | ns |
| LVCMOS33, Fast, 16 mA | | 1.69 | | | 2.17 | | | 2.17 | | ns |
| LVCMOS33, Fast, 24 mA | | 1.69 | | | 2.17 | | | 2.17 | | ns |
| LVCMOS25, QUIETIO, 2 mA | | 1.18 | | | 5.15 | | | 5.15 | | ns |
| LVCMOS25, QUIETIO, 4 mA | | 1.18 | | | 4.07 | | | 4.07 | | ns |
| LVCMOS25, QUIETIO, 6 mA | | 1.18 | | | 3.77 | | | 3.77 | | ns |
| LVCMOS25, QUIETIO, 8 mA | | 1.18 | | | 3.53 | | | 3.53 | | ns |
| LVCMOS25, QUIETIO, 12 mA | | 1.18 | | | 3.21 | | | 3.21 | | ns |
| LVCMOS25, QUIETIO, 16 mA | | 1.18 | | | 3.04 | | | 3.04 | | ns |
| LVCMOS25, QUIETIO, 24 mA | | 1.18 | | | 2.89 | | | 2.89 | | ns |
| LVCMOS25, Slow, 2 mA | | 1.18 | | | 4.17 | | | 4.17 | | ns |
| LVCMOS25, Slow, 4 mA | | 1.18 | | | 3.22 | | | 3.22 | | ns |
| LVCMOS25, Slow, 6 mA | | 1.18 | | | 3.14 | | | 3.14 | | ns |
| LVCMOS25, Slow, 8 mA | | 1.18 | | | 2.91 | | | 2.91 | | ns |
| LVCMOS25, Slow, 12 mA | | 1.18 | | | 2.49 | | | 2.49 | | ns |
| LVCMOS25, Slow, 16 mA | | 1.18 | | | 2.49 | | | 2.49 | | ns |
| LVCMOS25, Slow, 24 mA | | 1.18 | | | 2.29 | | | 2.29 | | ns |
| LVCMOS25, Fast, 2 mA | | 1.18 | | | 3.76 | | | 3.76 | | ns |
| LVCMOS25, Fast, 4 mA | | 1.18 | | | 2.75 | | | 2.75 | | ns |
| LVCMOS25, Fast, 6 mA | | 1.18 | | | 2.35 | | | 2.35 | | ns |
| LVCMOS25, Fast, 8 mA | | 1.18 | | | 2.28 | | | 2.28 | | ns |
| LVCMOS25, Fast, 12 mA | | 1.18 | | | 2.10 | | | 2.10 | | ns |
| LVCMOS25, Fast, 16 mA | | 1.18 | | | 2.10 | | | 2.10 | | ns |
| LVCMOS25, Fast, 24 mA | | 1.18 | | | 2.10 | | | 2.10 | | ns |
| LVCMOS18, QUIETIO, 2 mA | | 1.38 | | | 6.06 | | | 6.06 | | ns |
| LVCMOS18, QUIETIO, 4 mA | | 1.38 | | | 4.91 | | | 4.91 | | ns |
| LVCMOS18, QUIETIO, 6 mA | | 1.38 | | | 4.30 | | | 4.30 | | ns |
| LVCMOS18, QUIETIO, 8 mA | | 1.38 | | | 4.03 | | | 4.03 | | ns |
| LVCMOS18, QUIETIO, 12 mA | | 1.38 | | | 3.67 | | | 3.67 | | ns |
| LVCMOS18, QUIETIO, 16 mA | | 1.38 | | | 3.52 | | | 3.52 | | ns |
| LVCMOS18, QUIETIO, 24 mA | | 1.38 | | | 3.38 | | | 3.38 | | ns |
| LVCMOS18, Slow, 2 mA | | 1.38 | | | 4.88 | | | 4.88 | | ns |
| LVCMOS18, Slow, 4 mA | | 1.38 | | | 4.02 | | | 4.02 | | ns |
| LVCMOS18, Slow, 6 mA | | 1.38 | | | 3.41 | | | 3.41 | | ns |
| LVCMOS18, Slow, 8 mA | | 1.38 | | | 2.67 | | | 2.67 | | ns |
| LVCMOS18, Slow, 12 mA | | 1.38 | | | 2.42 | | | 2.42 | | ns |
| LVCMOS18, Slow, 16 mA | | 1.38 | | | 2.42 | | | 2.42 | | ns |

*Table 25:* **IOB Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -3 | -2 | -1L | -3 | -2 | -1L | -3 | -2 | -1L | |
| LVCMOS18, Slow, 24 mA | | 1.38 | | | 2.37 | | | 2.37 | | ns |
| LVCMOS18, Fast, 2 mA | | 1.38 | | | 3.96 | | | 3.96 | | ns |
| LVCMOS18, Fast, 4 mA | | 1.38 | | | 2.87 | | | 2.87 | | ns |
| LVCMOS18, Fast, 6 mA | | 1.38 | | | 2.26 | | | 2.26 | | ns |
| LVCMOS18, Fast, 8 mA | | 1.38 | | | 2.22 | | | 2.22 | | ns |
| LVCMOS18, Fast, 12 mA | | 1.38 | | | 2.14 | | | 2.14 | | ns |
| LVCMOS18, Fast, 16 mA | | 1.38 | | | 2.14 | | | 2.14 | | ns |
| LVCMOS18, Fast, 24 mA | | 1.38 | | | 2.14 | | | 2.14 | | ns |
| LVCMOS18_JEDEC, QUIETIO, 2 mA | | 1.26 | | | 6.02 | | | 6.02 | | ns |
| LVCMOS18_JEDEC, QUIETIO, 4 mA | | 1.26 | | | 4.91 | | | 4.91 | | ns |
| LVCMOS18_JEDEC, QUIETIO, 6 mA | | 1.26 | | | 4.29 | | | 4.29 | | ns |
| LVCMOS18_JEDEC, QUIETIO, 8 mA | | 1.26 | | | 4.02 | | | 4.02 | | ns |
| LVCMOS18_JEDEC, QUIETIO, 12 mA | | 1.26 | | | 3.67 | | | 3.67 | | ns |
| LVCMOS18_JEDEC, QUIETIO, 16 mA | | 1.26 | | | 3.52 | | | 3.52 | | ns |
| LVCMOS18_JEDEC, QUIETIO, 24 mA | | 1.26 | | | 3.38 | | | 3.38 | | ns |
| LVCMOS18_JEDEC, Slow, 2 mA | | 1.26 | | | 4.87 | | | 4.87 | | ns |
| LVCMOS18_JEDEC, Slow, 4 mA | | 1.26 | | | 4.00 | | | 4.00 | | ns |
| LVCMOS18_JEDEC, Slow, 6 mA | | 1.26 | | | 3.41 | | | 3.41 | | ns |
| LVCMOS18_JEDEC, Slow, 8 mA | | 1.26 | | | 2.67 | | | 2.67 | | ns |
| LVCMOS18_JEDEC, Slow, 12 mA | | 1.26 | | | 2.42 | | | 2.42 | | ns |
| LVCMOS18_JEDEC, Slow, 16 mA | | 1.26 | | | 2.42 | | | 2.42 | | ns |
| LVCMOS18_JEDEC, Slow, 24 mA | | 1.26 | | | 2.37 | | | 2.37 | | ns |
| LVCMOS18_JEDEC, Fast, 2 mA | | 1.26 | | | 3.95 | | | 3.95 | | ns |
| LVCMOS18_JEDEC, Fast, 4 mA | | 1.26 | | | 2.86 | | | 2.86 | | ns |
| LVCMOS18_JEDEC, Fast, 6 mA | | 1.26 | | | 2.25 | | | 2.25 | | ns |
| LVCMOS18_JEDEC, Fast, 8 mA | | 1.26 | | | 2.21 | | | 2.21 | | ns |
| LVCMOS18_JEDEC, Fast, 12 mA | | 1.26 | | | 2.14 | | | 2.14 | | ns |
| LVCMOS18_JEDEC, Fast, 16 mA | | 1.26 | | | 2.14 | | | 2.14 | | ns |
| LVCMOS18_JEDEC, Fast, 24 mA | | 1.26 | | | 2.14 | | | 2.14 | | ns |
| LVCMOS15, QUIETIO, 2 mA | | 1.23 | | | 5.62 | | | 5.62 | | ns |
| LVCMOS15, QUIETIO, 4 mA | | 1.23 | | | 4.81 | | | 4.81 | | ns |
| LVCMOS15, QUIETIO, 6 mA | | 1.23 | | | 4.32 | | | 4.32 | | ns |
| LVCMOS15, QUIETIO, 8 mA | | 1.23 | | | 4.16 | | | 4.16 | | ns |
| LVCMOS15, QUIETIO, 12 mA | | 1.23 | | | 3.89 | | | 3.89 | | ns |
| LVCMOS15, QUIETIO, 16 mA | | 1.23 | | | 3.69 | | | 3.69 | | ns |
| LVCMOS15, Slow, 2 mA | | 1.23 | | | 4.48 | | | 4.48 | | ns |
| LVCMOS15, Slow, 4 mA | | 1.23 | | | 3.78 | | | 3.78 | | ns |
| LVCMOS15, Slow, 6 mA | | 1.23 | | | 2.71 | | | 2.71 | | ns |

*Table 25:* **IOB Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -3 | -2 | -1L | -3 | -2 | -1L | -3 | -2 | -1L | |
| LVCMOS15, Slow, 8 mA | | 1.23 | | | 2.73 | | | 2.73 | | ns |
| LVCMOS15, Slow, 12 mA | | 1.23 | | | 2.48 | | | 2.48 | | ns |
| LVCMOS15, Slow, 16 mA | | 1.23 | | | 2.47 | | | 2.47 | | ns |
| LVCMOS15, Fast, 2 mA | | 1.23 | | | 3.67 | | | 3.67 | | ns |
| LVCMOS15, Fast, 4 mA | | 1.23 | | | 2.73 | | | 2.73 | | ns |
| LVCMOS15, Fast, 6 mA | | 1.23 | | | 2.16 | | | 2.16 | | ns |
| LVCMOS15, Fast, 8 mA | | 1.23 | | | 2.14 | | | 2.14 | | ns |
| LVCMOS15, Fast, 12 mA | | 1.23 | | | 2.07 | | | 2.07 | | ns |
| LVCMOS15, Fast, 16 mA | | 1.23 | | | 2.05 | | | 2.05 | | ns |
| LVCMOS15_JEDEC, QUIETIO, 2 mA | | 1.36 | | | 5.61 | | | 5.61 | | ns |
| LVCMOS15_JEDEC, QUIETIO, 4 mA | | 1.36 | | | 4.80 | | | 4.80 | | ns |
| LVCMOS15_JEDEC, QUIETIO, 6 mA | | 1.36 | | | 4.32 | | | 4.32 | | ns |
| LVCMOS15_JEDEC, QUIETIO, 8 mA | | 1.36 | | | 4.18 | | | 4.18 | | ns |
| LVCMOS15_JEDEC, QUIETIO, 12 mA | | 1.36 | | | 3.89 | | | 3.89 | | ns |
| LVCMOS15_JEDEC, QUIETIO, 16 mA | | 1.36 | | | 3.69 | | | 3.69 | | ns |
| LVCMOS15_JEDEC, Slow, 2 mA | | 1.36 | | | 4.49 | | | 4.49 | | ns |
| LVCMOS15_JEDEC, Slow, 4 mA | | 1.36 | | | 3.78 | | | 3.78 | | ns |
| LVCMOS15_JEDEC, Slow, 6 mA | | 1.36 | | | 2.72 | | | 2.72 | | ns |
| LVCMOS15_JEDEC, Slow, 8 mA | | 1.36 | | | 2.73 | | | 2.73 | | ns |
| LVCMOS15_JEDEC, Slow, 12 mA | | 1.36 | | | 2.47 | | | 2.47 | | ns |
| LVCMOS15_JEDEC, Slow, 16 mA | | 1.36 | | | 2.47 | | | 2.47 | | ns |
| LVCMOS15_JEDEC, Fast, 2 mA | | 1.36 | | | 3.67 | | | 3.67 | | ns |
| LVCMOS15_JEDEC, Fast, 4 mA | | 1.36 | | | 2.74 | | | 2.74 | | ns |
| LVCMOS15_JEDEC, Fast, 6 mA | | 1.36 | | | 2.15 | | | 2.15 | | ns |
| LVCMOS15_JEDEC, Fast, 8 mA | | 1.36 | | | 2.14 | | | 2.14 | | ns |
| LVCMOS15_JEDEC, Fast, 12 mA | | 1.36 | | | 2.08 | | | 2.08 | | ns |
| LVCMOS15_JEDEC, Fast, 16 mA | | 1.36 | | | 2.05 | | | 2.05 | | ns |
| LVCMOS12, QUIETIO, 2 mA | | 1.10 | | | 6.39 | | | 6.39 | | ns |
| LVCMOS12, QUIETIO, 4 mA | | 1.10 | | | 5.15 | | | 5.15 | | ns |
| LVCMOS12, QUIETIO, 6 mA | | 1.10 | | | 4.84 | | | 4.84 | | ns |
| LVCMOS12, QUIETIO, 8 mA | | 1.10 | | | 4.54 | | | 4.54 | | ns |
| LVCMOS12, QUIETIO, 12 mA | | 1.10 | | | 4.30 | | | 4.30 | | ns |
| LVCMOS12, Slow, 2 mA | | 1.10 | | | 5.18 | | | 5.18 | | ns |
| LVCMOS12, Slow, 4 mA | | 1.10 | | | 3.27 | | | 3.27 | | ns |
| LVCMOS12, Slow, 6 mA | | 1.10 | | | 3.17 | | | 3.17 | | ns |
| LVCMOS12, Slow, 8 mA | | 1.10 | | | 2.78 | | | 2.78 | | ns |
| LVCMOS12, Slow, 12 mA | | 1.10 | | | 2.57 | | | 2.57 | | ns |

*Table 25:* **IOB Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | Speed Grade | | | Speed Grade | | | |
| | -3 | -2 | -1L | -3 | -2 | -1L | -3 | -2 | -1L | |
| LVCMOS12, Fast, 2 mA | | 1.10 | | | 3.84 | | | 3.84 | | ns |
| LVCMOS12, Fast, 4 mA | | 1.10 | | | 2.81 | | | 2.81 | | ns |
| LVCMOS12, Fast, 6 mA | | 1.10 | | | 2.25 | | | 2.25 | | ns |
| LVCMOS12, Fast, 8 mA | | 1.10 | | | 2.16 | | | 2.16 | | ns |
| LVCMOS12, Fast, 12 mA | | 1.10 | | | 2.08 | | | 2.08 | | ns |
| LVCMOS12_JEDEC, QUIETIO, 2 mA | | 1.67 | | | 6.39 | | | 6.39 | | ns |
| LVCMOS12_JEDEC, QUIETIO, 4 mA | | 1.67 | | | 5.15 | | | 5.15 | | ns |
| LVCMOS12_JEDEC, QUIETIO, 6 mA | | 1.67 | | | 4.83 | | | 4.83 | | ns |
| LVCMOS12_JEDEC, QUIETIO, 8 mA | | 1.67 | | | 4.52 | | | 4.52 | | ns |
| LVCMOS12_JEDEC, QUIETIO, 12 mA | | 1.67 | | | 4.30 | | | 4.30 | | ns |
| LVCMOS12_JEDEC, Slow, 2 mA | | 1.67 | | | 5.19 | | | 5.19 | | ns |
| LVCMOS12_JEDEC, Slow, 4 mA | | 1.67 | | | 3.27 | | | 3.27 | | ns |
| LVCMOS12_JEDEC, Slow, 6 mA | | 1.67 | | | 3.17 | | | 3.17 | | ns |
| LVCMOS12_JEDEC, Slow, 8 mA | | 1.67 | | | 2.78 | | | 2.78 | | ns |
| LVCMOS12_JEDEC, Slow, 12 mA | | 1.67 | | | 2.57 | | | 2.57 | | ns |
| LVCMOS12_JEDEC, Fast, 2 mA | | 1.67 | | | 3.85 | | | 3.85 | | ns |
| LVCMOS12_JEDEC, Fast, 4 mA | | 1.67 | | | 2.81 | | | 2.81 | | ns |
| LVCMOS12_JEDEC, Fast, 6 mA | | 1.67 | | | 2.25 | | | 2.25 | | ns |
| LVCMOS12_JEDEC, Fast, 8 mA | | 1.67 | | | 2.16 | | | 2.16 | | ns |
| LVCMOS12_JEDEC, Fast, 12 mA | | 1.67 | | | 2.08 | | | 2.08 | | ns |

*Table 26:* **IOB 3-state ON Output Switching Characteristics ($T_{IOTPHZ}$)**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| $T_{IOTPHZ}$ | T input to Pad high-impedance | | 1.59 | | ns |

# I/O Standard Adjustment Measurement Methodology

## Input Delay Measurements

Table 27 shows the test setup parameters used for measuring input delay.

*Table 27:* **Input Delay Measurement Methodology**

| Description | I/O Standard Attribute | $V_L$ (1) | $V_H$ (1) | $V_{MEAS}$ (3,4) | $V_{REF}$ (2,4) |
|---|---|---|---|---|---|
| LVTTL (Low-Voltage Transistor-Transistor Logic) | LVTTL | 0 | 3.0 | 1.4 | – |
| LVCMOS (Low-Voltage CMOS), 3.3V | LVCMOS33 | 0 | 3.3 | 1.65 | – |
| LVCMOS, 2.5V | LVCMOS25 | 0 | 2.5 | 1.25 | – |
| LVCMOS, 1.8V | LVCMOS18 | 0 | 1.8 | 0.9 | – |
| LVCMOS, 1.5V | LVCMOS15 | 0 | 1.5 | 0.75 | – |
| LVCMOS, 1.2V | LVCMOS12 | 0 | 1.2 | 0.6 | – |
| PCI (Peripheral Component Interface), 33 MHz, 3.3V | PCI33_3 | Per PCI Specification | | | – |
| HSTL (High-Speed Transceiver Logic), Class I & II | HSTL_I, HSTL_II | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.75 |
| HSTL, Class III | HSTL_III | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| HSTL, Class I & II, 1.8V | HSTL_I_18, HSTL_II_18 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| HSTL, Class III 1.8V | HSTL_III_18 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 1.08 |
| SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V | SSTL3_I, SSTL3_II | $V_{REF}$ – 0.75 | $V_{REF}$ + 0.75 | $V_{REF}$ | 1.5 |
| SSTL, Class I & II, 2.5V | SSTL2_I, SSTL2_II | $V_{REF}$ – 0.75 | $V_{REF}$ + 0.75 | $V_{REF}$ | 1.25 |
| SSTL, Class I & II, 1.8V | SSTL18_I, SSTL18_II | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| SSTL, Class II, 1.5V | SSTL15_II | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 0.75 |
| LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V | LVDS_25, LVDS_33 | 1.25 – 0.125 | 1.25 + 0.125 | 0(5) | |
| LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V & 3.3V | LVPECL_25, LVPECL_33 | 1.2 – 0.3 | 1.2 – 0.3 | 0(5) | |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | 1.3 – 0.125 | 1.3 + 0.125 | 0(5) | |
| Mini-LVDS, 2.5V & 3.3V | MINI_LVDS_25, MINI_LVDS_33 | 1.2 – 0.125 | 1.2 + 0.125 | 0(5) | |
| RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V | RSDS_25, RSDS_33 | 1.2 – 0.1 | 1.2 + 0.1 | 0(5) | |
| TMDS (Transition Minimized Differential Signaling), 3.3V | TMDS_33 | 3.0 – 0.1 | 3.0 + 0.1 | 0(5) | |
| PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V | PPDS_25, PPDS_33 | 1.25 – 0.1 | 1.25 + 0.1 | 0(5) | |

**Notes:**

1. Input waveform switches between $V_L$ and $V_H$.
2. Measurements are made at typical, minimum, and maximum $V_{REF}$ values. Reported delays reflect worst case of these measurements. $V_{REF}$ values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the $V_{REF}$ / $V_{MEAS}$ parameters found in IBIS models and/or noted in Figure 6.
5. The value given is the differential input voltage.

## Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 6 and Figure 7.

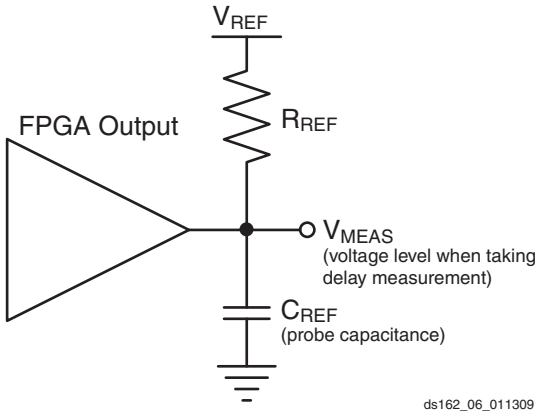


*Figure 6:* **Single-Ended Test Setup**

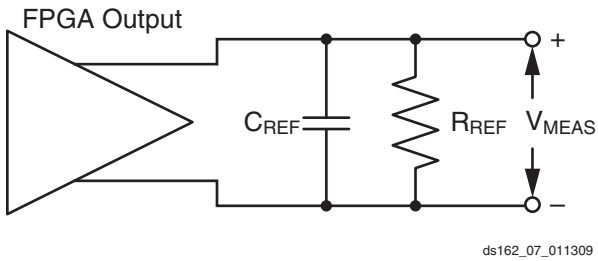


*Figure 7:* **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters $V_{REF}$, $R_{REF}$, $C_{REF}$, and $V_{MEAS}$ fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 28.
2. Record the time to $V_{MEAS}$.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to $V_{MEAS}$.
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

*Table 28:* **Output Delay Measurement Methodology**

| Description | I/O Standard Attribute | $R_{REF}$ (Ω) | $C_{REF}$[1] (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| LVTTL (Low-Voltage Transistor-Transistor Logic) | LVTTL (all) | 1M | 0 | 1.4 | 0 |
| LVCMOS (Low-Voltage CMOS), 3.3V | LVCMOS33 | 1M | 0 | 1.65 | 0 |
| LVCMOS, 2.5V | LVCMOS25 | 1M | 0 | 1.25 | 0 |
| LVCMOS, 1.8V | LVCMOS18 | 1M | 0 | 0.9 | 0 |
| LVCMOS, 1.5V | LVCMOS15 | 1M | 0 | 0.75 | 0 |
| LVCMOS, 1.2V | LVCMOS12 | 1M | 0 | 0.75 | 0 |
| PCI (Peripheral Component Interface), 33 MHz, 3.3V | PCI33_3 (rising edge) | 25 | 10[2] | 0.94 | 0 |
| | PCI33_3 (falling edge) | 25 | 10[2] | 2.03 | 3.3 |
| HSTL (High-Speed Transceiver Logic), Class I | HSTL_I | 50 | 0 | $V_{REF}$ | 0.75 |
| HSTL, Class II | HSTL_II | 25 | 0 | $V_{REF}$ | 0.75 |
| HSTL, Class III | HSTL_III | 50 | 0 | 0.9 | 1.5 |
| HSTL, Class I, 1.8V | HSTL_I_18 | 50 | 0 | $V_{REF}$ | 0.9 |
| HSTL, Class II, 1.8V | HSTL_II_18 | 25 | 0 | $V_{REF}$ | 0.9 |
| HSTL, Class III, 1.8V | HSTL_III_18 | 50 | 0 | 1.1 | 1.8 |
| SSTL (Stub Series Terminated Logic), Class I, 1.8V | SSTL18_I | 50 | 0 | $V_{REF}$ | 0.9 |
| SSTL, Class II, 1.8V | SSTL18_II | 25 | 0 | $V_{REF}$ | 0.9 |
| SSTL, Class I, 2.5V | SSTL2_I | 50 | 0 | $V_{REF}$ | 1.25 |

*Table 28:* **Output Delay Measurement Methodology *(Cont'd)***

| Description | I/O Standard Attribute | $R_{REF}$ (Ω) | $C_{REF}$[1] (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| SSTL, Class II, 2.5V | SSTL2_II | 25 | 0 | $V_{REF}$ | 1.25 |
| SSTL, Class II, 1.5V | SSTL15_II | 25 | 0 | $V_{REF}$ | 0.75 |
| LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V | LVDS_25, LVDS_33 | 100 | 0 | 0[3] | 1.2 |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | 100 | 0 | 0[3] | 0 |
| Mini-LVDS, 2.5V & 3.3V | MINI_LVDS_25, MINI_LVDS_33 | 100 | 0 | 0[3] | |
| RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V | RSDS_25, RSDS_33 | 100 | 0 | 0[3] | |
| TMDS (Transition Minimized Differential Signaling), 3.3V | TMDS_33 | 100 | 0 | 0[3] | |
| PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V | PPDS_25, PPDS_33 | 100 | 0 | 0[3] | |

**Notes:**
1. $C_{REF}$ is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. The value given is the differential input voltage.

## Input/Output Logic Switching Characteristics

*Table 29:* **ILOGIC2 Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| **Setup/Hold** | | | | | |
| $T_{ICE0CK}/T_{ICKCE0}$ | CE0 pin Setup/Hold with respect to CLK | | 1.04<br>–0.58 | | ns |
| $T_{ISRCK}/T_{ICKSR}$ | SR pin Setup/Hold with respect to CLK | | 1.09<br>–0.51 | | ns |
| $T_{IDOCK}/T_{IOCKD}$ | D pin Setup/Hold with respect to CLK without Delay | | 1.73<br>–1.38 | | ns |
| $T_{IDOCKD}/T_{IOCKDD}$ | DDLY pin Setup/Hold with respect to CLK (using IODELAY2) | | 0.51<br>–0.25 | | ns |
| **Combinatorial** | | | | | |
| $T_{IDI}$ | D pin to O pin propagation delay, no Delay | | 1.77 | | ns |
| $T_{IDID}$ | DDLY pin to O pin propagation delay (using IODELAY2) | | 0.53 | | ns |
| **Sequential Delays** | | | | | |
| $T_{IDLO}$ | D pin to Q1 pin using flip-flop as a latch without Delay | | 2.80 | | ns |
| $T_{IDLOD}$ | DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY2) | | 1.58 | | ns |
| $T_{ICKQ}$ | CLK to Q outputs | | 1.38 | | ns |
| $T_{RQ}$ | SR pin to OQ/TQ out | | 2.54 | | ns |
| $T_{GSRQ}$ | Global Set/Reset to Q outputs | | | | ns |
| **Set/Reset** | | | | | |
| $T_{RPW}$ | Minimum Pulse Width, SR inputs | | | | ns, Min |

*Table 30:* **OLOGIC2 Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| **Setup/Hold** | | | | | |
| $T_{ODCK}/T_{OCKD}$ | D1/D2 pins Setup/Hold with respect to CLK | | 0.96<br>–0.26 | | ns |
| $T_{OOCECK}/T_{OCKOCE}$ | OCE pin Setup/Hold with respect to CLK | | 0.47<br>–0.22 | | ns |
| $T_{OSRCK}/T_{OCKSR}$ | SR pin Setup/Hold with respect to CLK | | 0.91<br>–0.47 | | ns |
| $T_{OTCK}/T_{OCKT}$ | T1/T2 pins Setup/Hold with respect to CLK | | 0.72<br>–0.18 | | ns |
| $T_{OTCECK}/T_{OCKTCE}$ | TCE pin Setup/Hold with respect to CLK | | 0.39<br>–0.13 | | ns |
| **Combinatorial** | | | | | |
| $T_{DOQ}$ | D1 to OQ out or T1 to TQ out | | | | ns |
| **Sequential Delays** | | | | | |
| $T_{OCKQ}$ | CLK to OQ/TQ out | | 0.81 | | ns |
| $T_{RQ}$ | SR pin to OQ/TQ out | | 2.54 | | ns |
| $T_{GSRQ}$ | Global Set/Reset to Q outputs | | | | ns |
| **Set/Reset** | | | | | |
| $T_{RPW}$ | Minimum Pulse Width, SR inputs | | | | ns, Min |

## Input Serializer/Deserializer Switching Characteristics

*Table 31:* **ISERDES2 Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| **Setup/Hold for Control Lines** | | | | | |
| $T_{ISCCK\_BITSLIP}/T_{ISCKC\_BITSLIP}$ | BITSLIP pin Setup/Hold with respect to CLKDIV | | 0.31<br>–0.14 | | ns |
| $T_{ISCCK\_CE}/T_{ISCKC\_CE}$ | CE pin Setup/Hold with respect to CLK | | 1.16<br>–0.71 | | ns |
| **Setup/Hold for Data Lines** | | | | | |
| $T_{ISDCK\_D}/T_{ISCKD\_D}$ | D pin Setup/Hold with respect to CLK | | 1.60<br>–1.00 | | ns |
| $T_{ISDCK\_DDLY}/T_{ISCKD\_DDLY}$ | DDLY pin Setup/Hold with respect to CLK (using IODELAY2) | | –0.37<br>0.56 | | ns |
| $T_{ISDCK\_D\_DDR}/T_{ISCKD\_D\_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode | | 1.61<br>–1.00 | | ns |
| $T_{ISDCK\_DDLY\_DDR}$/<br>$T_{ISCKD\_DDLY\_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY2) | | –0.44<br>0.69 | | ns |
| **Sequential Delays** | | | | | |
| $T_{ISCKO\_Q}$ | CLKDIV to out at Q pin | | 2.02 | | ns |
| **Propagation Delays** | | | | | |
| $T_{ISDO\_DO}$ | D input to DO output pin | | 2.06 | | ns |

**Notes:**
1. Recorded at 0 tap value.

## Output Serializer/Deserializer Switching Characteristics

*Table 32:* **OSERDES2 Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| **Setup/Hold** | | | | | |
| $T_{OSDCK\_D}/T_{OSCKD\_D}$ | D input Setup/Hold with respect to CLKDIV | | 0.19<br>0.01 | | ns |
| $T_{OSDCK\_T}/T_{OSCKD\_T}$(1) | T input Setup/Hold with respect to CLK | | 0.23<br>–0.02 | | ns |
| $T_{OSDCK\_T2}/T_{OSCKD\_T2}$(1) | T input Setup/Hold with respect to CLKDIV | | | | ns |
| $T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$ | OCE input Setup/Hold with respect to CLK | | 0.24<br>–0.16 | | ns |
| $T_{OSCCK\_S}$ | SR (Reset) input Setup with respect to CLKDIV | | | | ns |
| $T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$ | TCE input Setup/Hold with respect to CLK | | 0.27<br>–0.15 | | ns |
| **Sequential Delays** | | | | | |
| $T_{OSCKO\_OQ}$ | Clock to out from CLK to OQ | | 1.89 | | ns |
| $T_{OSCKO\_TQ}$ | Clock to out from CLK to TQ | | 1.91 | | ns |
| **Combinatorial** | | | | | |
| $T_{OSDO\_TTQ}$ | T input to TQ Out | | | | ns |
| $T_{OSCO\_OQ}$ | Asynchronous Reset to OQ | | 1.89 | | ns |
| $T_{OSCO\_TQ}$ | Asynchronous Reset to TQ | | 1.91 | | ns |

**Notes:**
1. $T_{OSDCK\_T2}$ and $T_{OSCKD\_T2}$ are reported as $T_{OSDCK\_T}/T_{OSCKD\_T}$ in TRACE report.

## Input/Output Delay Switching Characteristics

*Table 33:* **IODELAY2 Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| $T_{IODCCK\_CAL}$ / $T_{IODCKC\_CAL}$ | CAL pin Setup/Hold with respect to CK | | 0.48<br>–0.22 | | ns |
| $T_{IODCCK\_CE}$ / $T_{IODCKC\_CE}$ | CE pin Setup/Hold with respect to CK | | 0.25<br>–0.02 | | ns |
| $T_{IODCCK\_INC}$/ $T_{IODCKC\_INC}$ | INC pin Setup/Hold with respect to CK | | 0.18<br>0.06 | | ns |
| $T_{IODCCK\_RST}$/ $T_{IODCKC\_RST}$ | RST pin Setup/Hold with respect to CK | | 0.22<br>–0.01 | | ns |
| $T_{IODDO\_T}$ | TSCONTROL delay to MUXE/MUXF switching and through IODELAY2 | Note 1 | Note 1 | Note 1 | |
| $T_{IODDO\_IDATAIN}$ | Propagation delay through IODELAY2 | Note 1 | Note 1 | Note 1 | |
| $T_{IODDO\_ODATAIN}$ | Propagation delay through IODELAY2 | Note 1 | Note 1 | Note 1 | |

**Notes:**
1. Delay depends on IODELAY2 tap setting. See TRACE report for actual values.

## CLB Switching Characteristics (SLICEM Only)

*Table 34:* **CLB Switching Characteristics (SLICEM Only)**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| **Combinatorial Delays** | | | | | |
| $T_{ILO}$ | An – Dn LUT address to A to D outputs | | 0.48 | | ns, Max |
| $T_{ILO}$ | An – Dn LUT address through F7AMUX/F7BMUX to AMUX/CMUX | | 0.77 | | ns, Max |
| $T_{OPAB}$ | An – Dn LUT address through F7AMUX or F7BMUX and F8MUX to BMUX | | 0.79 | | ns, Max |
| $T_{ITO}$ | An – Dn inputs to A – D Q outputs | | 1.36 | | ns, Max |
| $T_{TITO\_LOGIC}$ | An – Dn inputs to A – D Q outputs (Latch as Logic) | | 1.36 | | ns, Max |
| $T_{OPCYA}$ | An input to COUT output | | 0.84 | | ns, Max |
| $T_{OPCYB}$ | Bn input to COUT output | | 0.81 | | ns, Max |
| $T_{OPCYC}$ | Cn input to COUT output | | 0.62 | | ns, Max |
| $T_{OPCYD}$ | Dn input to COUT output | | 0.58 | | ns, Max |
| $T_{AXCY}$ | AX input to COUT output | | 0.41 | | ns, Max |
| $T_{BXCY}$ | BX input to COUT output | | 0.30 | | ns, Max |
| $T_{CXCY}$ | CX input to COUT output | | 0.16 | | ns, Max |
| $T_{DXCY}$ | DX input to COUT output | | 0.14 | | ns, Max |
| $T_{BYP}$ | CIN input to COUT output | | 0.10 | | ns, Max |
| $T_{CINA}$ | CIN input to AMUX output | | 0.41 | | ns, Max |
| $T_{CINB}$ | CIN input to BMUX output | | 0.50 | | ns, Max |
| $T_{CINC}$ | CIN input to CMUX output | | 0.49 | | ns, Max |
| $T_{CIND}$ | CIN input to DMUX output | | 0.56 | | ns, Max |
| **Sequential Delays** | | | | | |
| $T_{CKO}$ | Clock to AQ – DQ outputs | | 0.63 | | ns, Max |
| **Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK** | | | | | |
| $T_{DICK}/T_{CKDI}$ | A – D input to CLK on A – D flip-flops | | 0.79<br>0.46 | | ns, Min |
| $T_{CECK}/T_{CKCE}$ | CE input to CLK on A – D flip-flops | | 0.59<br>–0.15 | | ns, Min |
| $T_{SRCK}/T_{CKSR}$ | SR input to CLK on A – D flip-flops | | 0.55<br>–0.28 | | ns, Min |
| $T_{CINCK}/T_{CKCIN}$ | CIN input to CLK on A – D flip-flops | | 0.62<br>0.33 | | ns, Min |
| **Set/Reset** | | | | | |
| $T_{SRMIN}$ | SR input minimum pulse width | | | | ns, Min |
| $T_{RQ}$ | Delay from SR input to AQ – DQ flip-flops | | 2.54 | | ns, Max |
| $T_{CEO}$ | Delay from CE input to AQ – DQ flip-flops | | 1.15 | | ns, Max |
| $F_{TOG}$ | Toggle frequency (for export control) | | | | MHz |

**Notes:**
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

## CLB Distributed RAM Switching Characteristics (SLICEM Only)

*Table 35:* **CLB Distributed RAM Switching Characteristics (SLICEM Only)**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| **Sequential Delays** | | | | | |
| $T_{SHCKO}$ | Clock to A – D outputs | | 2.06 | | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| $T_{DS}/T_{DH}$ | A – D inputs to CLK | | 1.04<br>0.37 | | ns, Min |
| $T_{AS}/T_{AH}$ | Address An inputs to clock | | 1.21<br>0.67 | | ns, Min |
| $T_{WS}/T_{WH}$ | WE input to clock | | 0.59<br>–0.15 | | ns, Min |
| $T_{CECK}/T_{CKCE}$ | CE input to CLK | | 0.59<br>–0.15 | | ns, Min |
| **Clock CLK** | | | | | |
| $T_{MPW}$ | Minimum pulse width | | | | ns, Min |
| $T_{MCP}$ | Minimum clock period | | | | ns, Min |

**Notes:**
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
2. $T_{SHCKO}$ also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

## CLB Shift Register Switching Characteristics (SLICEM Only)

*Table 36:* **CLB Shift Register Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| **Sequential Delays** | | | | | |
| $T_{REG}$ | Clock to A – D outputs | | 2.34 | | ns, Max |
| $T_{REG\_MUX}$ | Clock to AMUX – DMUX output | | | | ns, Max |
| $T_{REG\_M31}$ | Clock to DMUX output via M31 output | | | | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| $T_{WS}/T_{WH}$ | WE input to CLK | | 0.59<br>–0.15 | | ns, Min |
| $T_{CECK}/T_{CKCE}$ | CE input to CLK | | 0.59<br>–0.15 | | ns, Min |
| $T_{DS}/T_{DH}$ | A – D inputs to CLK | | 1.04<br>0.37 | | ns, Min |
| **Clock CLK** | | | | | |
| $T_{MPW}$ | Minimum pulse width | | | | ns, Min |

**Notes:**
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

## Block RAM Switching Characteristics

*Table 37:* **Block RAM Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| **Block RAM Clock to Out Delays** | | | | | |
| $T_{RCKO\_DO}$ | Clock CLK to DOUT output (without output register)(1) | | 3.00 | | ns, Max |
| $T_{RCKO\_DO\_REG}$ | Clock CLK to DOUT output (with output register)(2) | | 1.60 | | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| $T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$ | ADDR inputs(3) | | 0.40<br>0.10 | | ns, Min |
| $T_{RDCK\_DI}/T_{RCKD\_DI}$ | DIN inputs(4) | | 0.30<br>0.10 | | ns, Min |
| $T_{RCCK\_EN}/T_{RCKC\_EN}$ | Block RAM Enable (EN) input | | 0.20<br>0.05 | | ns, Min |
| $T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$ | CE input of output register | | 0.20<br>0.08 | | ns, Min |
| $T_{RCCK\_WE}/T_{RCKC\_WE}$ | Write Enable (WE) input | | 0.20<br>0.10 | | ns, Min |
| **Maximum Frequency** | | | | | |
| $F_{MAX}$ | Block RAM in all modes | | 260 | | MHz |

**Notes:**
1. $T_{RCKO\_DO}$ includes $T_{RCKO\_DOA}$ and $T_{RCKO\_DOPA}$ as well as the B port equivalent timing parameters.
2. $T_{RCKO\_DO\_REG}$ includes $T_{RCKO\_DOA\_REG}$ and $T_{RCKO\_DOPA\_REG}$ as well as the B port equivalent timing parameters.
3. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
4. $T_{RCKO\_DI}$ includes both A and B inputs as well as the parity inputs of A and B.

## DSP48A1 Switching Characteristics

*Table 38:* **DSP48A1 Switching Characteristics**

| Symbol | Description | Pre-adder | Multiplier | Post-adder | Speed Grade | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | -3 | -2 | -1L | |
| **Setup and Hold Times of Data/Control Pins to the Input Register Clock** | | | | | | | | |
| $T_{DSPDCK\_A\_A1REG}$/<br>$T_{DSPCKD\_A\_A1REG}$ | A input to A1 register CLK | N/A | N/A | N/A | | 0.03<br>0.09 | | ns |
| $T_{DSPDCK\_D\_B1REG}$/<br>$T_{DSPCKD\_D\_B1REG}$ | D input to B1 register CLK | Yes | N/A | N/A | | 1.99<br>–0.07 | | ns |
| $T_{DSPDCK\_C\_CREG}$/<br>$T_{DSPCKD\_C\_CREG}$ | C input to C register CLK | N/A | N/A | N/A | | –0.03<br>0.09 | | ns |
| $T_{DSPDCK\_D\_DREG}$/<br>$T_{DSPCKD\_D\_DREG}$ | D input to D register CLK | N/A | N/A | N/A | | –0.06<br>0.12 | | ns |
| $T_{DSPDCK\_OPMODE\_B1REG}$/<br>$T_{DSPCKD\_OPMODE\_B1REG}$ | OPMODE input to B1 register CLK | Yes | N/A | N/A | | 2.01<br>0.00 | | ns |
| $T_{DSPDCK\_OPMODE\_OPMODEREG}$/<br>$T_{DSPCKD\_OPMODE\_OPMODEREG}$ | OPMODE input to OPMODE register CLK | N/A | N/A | N/A | | 0.28<br>0.12 | | ns |

*Table 38:* **DSP48A1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Pre-adder | Multiplier | Post-adder | Speed Grade | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | -3 | -2 | -1L | |
| **Setup and Hold Times of Data Pins to the Pipeline Register Clock** | | | | | | | | |
| $T_{DSPDCK\_A\_MREG}$/ $T_{DSPCKD\_A\_MREG}$ | A input to M register CLK | N/A | Yes | N/A | | 2.88 –0.40 | | ns |
| $T_{DSPDCK\_B\_MREG}$/ $T_{DSPCKD\_B\_MREG}$ | B input to M register CLK | Yes | Yes | N/A | | 4.93 –0.68 | | ns |
| | | No | Yes | N/A | | 3.22 –0.57 | | ns |
| $T_{DSPDCK\_D\_MREG}$/ $T_{DSPCKD\_D\_MREG}$ | D input to M register CLK | Yes | Yes | N/A | | 4.82 –0.56 | | ns |
| $T_{DSPDCK\_OPMODE\_MREG}$/ $T_{DSPCKD\_OPMODE\_MREG}$ | OPMODE to M register CLK | Yes | Yes | N/A | | 4.84 –0.43 | | ns |
| | | No | Yes | N/A | | 3.02 –0.43 | | ns |
| **Setup and Hold Times of Data/Control Pins to the Output Register Clock** | | | | | | | | |
| $T_{DSPDCK\_A\_PREG}$/ $T_{DSPCKD\_A\_PREG}$ | A input to P register CLK | N/A | Yes | Yes | | 5.38 –0.76 | | ns |
| $T_{DSPDCK\_B\_PREG}$/ $T_{DSPCKD\_B\_PREG}$ | B input to P register CLK | Yes | Yes | Yes | | 7.43 –1.05 | | ns |
| | | No | Yes | Yes | | 5.72 –0.93 | | ns |
| $T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$ | C input to P register CLK | N/A | N/A | Yes | | 2.30 –0.23 | | ns |
| $T_{DSPDCK\_D\_PREG}$/ $T_{DSPCKD\_D\_PREG}$ | D input to P register CLK | Yes | Yes | Yes | | 7.32 –0.92 | | ns |
| $T_{DSPDCK\_OPMODE\_PREG}$/ $T_{DSPCKD\_OPMODE\_PREG}$ | OPMODE input to P register CLK | Yes | Yes | Yes | | 7.43 –0.43 | | ns |
| | | No | Yes | Yes | | 5.42 –0.43 | | ns |
| | | No | No | Yes | | 2.46 –0.39 | | ns |
| **Clock to Out from Output Register Clock to Output Pin** | | | | | | | | |
| $T_{DSPCKO\_P\_PREG}$ | CLK (PREG) to P output | N/A | N/A | N/A | | 1.32 | | ns |
| **Clock to Out from Pipeline Register Clock to Output Pins** | | | | | | | | |
| $T_{DSPCKO\_P\_MREG}$ | CLK (MREG) to P output | N/A | N/A | Yes | | 4.33 | | ns |
| **Clock to Out from Input Register Clock to Output Pins** | | | | | | | | |
| $T_{DSPCKO\_P\_A1REG}$ | CLK (A1REG) to P output | N/A | Yes | Yes | | 6.65 | | ns |
| $T_{DSPCKO\_P\_B1REG}$ | CLK (B1REG) to P output | N/A | Yes | Yes | | 6.64 | | ns |
| $T_{DSPCKO\_P\_CREG}$ | CLK (CREG) to P output | N/A | N/A | Yes | | 3.68 | | ns |
| $T_{DSPCKO\_P\_DREG}$ | CLK (DREG) to P output | Yes | Yes | Yes | | 8.99 | | ns |

*Table 38:* **DSP48A1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Pre-adder | Multiplier | Post-adder | Speed Grade | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | | -3 | -2 | -1L | |
| **Combinatorial Delays from Input Pins to Output Pins** | | | | | | | | |
| $T_{DSPDO\_A\_P}$<br>$T_{DSPDO\_B\_P}$ | A or B input to P output | N/A | No | Yes | | 3.68 | | ns |
| | | N/A | Yes | No | | 5.10 | | ns |
| | | N/A | Yes | Yes | | 6.65 | | ns |
| $T_{DSPDO\_B\_P}$ | B input to P output | Yes | No | No | | 3.84 | | ns |
| | | Yes | Yes | No | | 6.81 | | ns |
| | | Yes | Yes | Yes | | 8.41 | | ns |
| $T_{DSPDO\_C\_P}$ | C input to P output | N/A | N/A | Yes | | 3.28 | | ns |
| $T_{DSPDO\_D\_P}$ | D input to P output | Yes | Yes | Yes | | 8.30 | | ns |
| $T_{DSPDO\_OPMODE\_P}$ | OPMODE input to P output | Yes | Yes | Yes | | 8.27 | | ns |
| | | No | Yes | Yes | | 6.50 | | ns |
| | | No | No | Yes | | 3.68 | | ns |
| **Maximum Frequency** | | | | | | | | |
| $F_{MAX}$ | All registers used | Yes | Yes | Yes | | 250 | | MHz |

**Notes:**
1. A Yes signifies that the component is in the path. A No signifies that the component is being bypassed. N/A signifies not applicable because no path exists.

*Table 39:* **Device DNA Interface Port Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| $T_{DNASSU}$ | Setup time on SHIFT before the rising edge of CLK | 1 | | | ns, min |
| $T_{DNASH}$ | Hold time on SHIFT after the rising edge of CLK | 0.5 | | | ns, min |
| $T_{DNADSU}$ | Setup time on DIN before the rising edge of CLK | 1 | | | ns, min |
| $T_{DNADH}$ | Hold time on DIN after the rising edge of CLK | 0.5 | | | ns, min |
| $T_{DNARSU}$ | Setup time on READ before the rising edge of CLK | 5 | | | ns, min |
| | | 10,000 | | | ns, max |
| $T_{DNARH}$ | Hold time on READ after the rising edge of CLK | 0 | | | ns, min |
| $T_{DNADCKO}$ | Clock-to-output delay on DOUT after rising edge of CLK | 0.5 | | | ns, min |
| | | 1.5 | | | ns, max |
| $T_{DNACLKF}$ | CLK frequency | 33 | | | MHz, max |
| $T_{DNACLKL}$ | CLK High time | 10 | | | ns, min |
| $T_{DNACLKH}$ | CLK Low time | 10 | | | ns, min |

**Notes:**
1. The minimum READ pulse width is 5 ns, the maximum READ pulse width is 10 ms.

*Table 40:* **Suspend Mode Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| **Entering Suspend Mode** | | | | | |
| $T_{SUSPENDHIGH\_AWAKE}$ | Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter (suspend_filter:No) | 7 (typical) | | | ns |
| $T_{SUSPENDFILTER}$ | Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled (suspend_filter:Yes) | 300 (typical) | | | ns |
| $T_{SUSPEND\_GWE}$ | Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior | 10 (typical) | | | ns |
| $T_{SUSPEND\_GTS}$ | Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements | <5 (typical) | | | ns |
| $T_{SUSPEND\_DISABLE}$ | Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled | 800 (typical) | | | ns |
| **Exiting Suspend Mode** | | | | | |
| $T_{SUSPENDLOW\_AWAKE}$ | Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM lock time. | 7 to 39 (typical) | | | µs |
| $T_{SUSPEND\_ENABLE}$ | Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled | 7 to 39 (typical) | | | µs |
| $T_{AWAKE\_GWE1}$ | Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using sw_clk:InternalClock and sw_gwe_cycle:1. | 67 (typical) | | | ns |
| $T_{AWAKE\_GWE512}$ | Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using sw_clk:InternalClock and sw_gwe_cycle:512. | 14 (typical) | | | µs |
| $T_{AWAKE\_GTS1}$ | Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using sw_clk:InternalClock and sw_gts_cycle:1. | 57 (typical) | | | ns |
| $T_{AWAKE\_GTS512}$ | Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using sw_clk:InternalClock and sw_gts_cycle:512. | 14 (typical) | | | µs |
| $T_{SCP\_AWAKE}$ | Rising edge of SCP pins to rising edge of AWAKE pin | 7 to 39 (typical) | | | µs |

**Notes:**
1. All values are specified as typical at nominal conditions.

## Configuration Switching Characteristics

*Table 41:* **Configuration Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| **Power-up Timing Characteristics** | | | | | |
| $T_{PL}$ | PROGRAM_B Latency | | 1.5 | | ms, Max |
| $T_{POR}$ | Power-on-Reset | | 30 | | ms, Max |
| $T_{PROGRAM}$ | PROGRAM_B Pulse Width | | 500 | | ns, Min |
| **Slave Serial Mode Programming Switching** | | | | | |
| $T_{DCCK}/T_{CCKD}$ | DIN Setup/Hold, slave mode | | 6.0/1.0 | | ns, Min |
| $T_{CCO}$ | CCLK to DOUT | | 12 | | ns, Max |
| $F_{MSCCK}$ | Slave mode external CCLK | | | | MHz |
| **Slave SelectMAP Mode Programming Switching** | | | | | |
| $T_{SMDCCK}/T_{SMCCKD}$ | SelectMAP Data Setup/Hold | | 6.0/1.0 | | ns, Min |
| $T_{SMCSCCK}/T_{SMCCKCS}$ | CSI_B Setup/Hold | | 6.0/0.0 | | ns, Min |
| $T_{SMCCKW}/T_{SMWCCK}$ | RDWR_B Setup/Hold | | 15.0/1.0 | | ns, Min |
| $T_{SMCKCSO}$ | CSO_B clock to out | | 14 | | ns, Min |
| $T_{SMCO}$ | CCLK to DATA out in readback | | 13 | N/A | ns, Max |
| $T_{SMCKBY}$ | CCLK to BUSY out in readback | | 12 | N/A | ns, Max |
| $F_{SMCCK}$ | Maximum Frequency with respect to nominal CCLK | | | | MHz, Max |
| $F_{RBCCK}$ | Maximum Readback Frequency with respect to nominal CCLK | | | N/A | MHz, Max |
| **Boundary-Scan Port Timing Specifications** | | | | | |
| $T_{TAPTCK}$ | TMS and TDI Setup time before TCK | | 9 | | ns, Min |
| $T_{TCKTAP}$ | TMS and TDI Hold time after TCK | | 0 | | ns, Min |
| $T_{TCKTDO}$ | TCK falling edge to TDO output valid | | 8 | | ns, Max |
| $F_{TCK}$ | Maximum configuration TCK clock frequency | | 25 | | MHz, Max |
| $F_{TCKB}$ | Maximum boundary-scan TCK clock frequency | | 25 | | MHz, Max |
| **BPI Master Flash Mode Programming Switching** | | | | | |
| $T_{BPICCO}$ (3) | A[25:0], FCS_B, FOE_B, FWE_B, LDC outputs valid after CCLK falling edge | | 15 | | ns |
| $T_{BPIICCK}$ | Master BPI CCLK (output) delay | | | | ns, Min/Max |
| $T_{BPIDCC}/T_{BPICCD}$ | Setup/Hold on D[15:0] data input pins | | | | ns |
| $T_{INITADDR}$ | Minimum period of initial A[25:0] address cycles | | 3 | | CCLK cycles |
| **SPI Master Flash Mode Programming Switching** | | | | | |
| $T_{SPIDCC}/T_{SPIDCCD}$ | DIN, MISO0, MISO1, MISO2, MISO3, Setup/Hold before/after the rising CCLK edge | | 5.0/ 1.0 | | ns |
| $T_{SPIICCK}$ | Master SPI CCLK (output) delay | | | | ns, Min/Max |
| $T_{SPICCM}$ | MOSI clock to out | | | | ns |
| $T_{SPICCFC}$ | CSO_B clock to out | | 14 | | ns |

*Table 41:* **Configuration Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| **CCLK Output (Master Modes)** | | | | | |
| $T_{MCCKL}$ | Master CCLK clock duty cycle Low | 45 | 45 | | %, Min |
| $T_{MCCKH}$ | Master CCLK clock duty cycle High | 45 | 45 | | %, Min |
| $F_{MCCK}$ | Maximum Frequency, master mode with respect to nominal CCLK | | | | MHz, Max |
| $F_{MCCKTOL}$ | Frequency Tolerance, master mode with respect to nominal CCLK | ±50 | ±50 | ±50 | % |
| **CCLK Input (Slave Modes)** | | | | | |
| $T_{SCCKL}$ | Slave CCLK clock minimum Low time | | 5 | | ns, Min |
| $T_{SCCKH}$ | Slave CCLK clock minimum High time | | 5 | | ns, Min |

**Notes:**
1. Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
2. To support longer delays in configuration, use the design solutions described in Spartan-6 FPGA Configuration User Guide.
3. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

## Clock Buffers and Networks

*Table 42:* **Global Clock Switching Characteristics**

| Symbol | Description | Devices | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| $T_{GSI}$ | S pin Setup to I0/I1 inputs | All | | 0.56 | | ns |
| $T_{GIO}$ | BUFGMUX delay from I0/I1 to O | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | 0.42 | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | 0.42 | | ns |
| | | XC6SLX45T | | 0.42 | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |
| **Maximum Frequency** | | | | | | |
| $F_{MAX}$ | Global clock tree (BUFG) | XC6SLX4 | | | | MHz |
| | | XC6SLX9 | | | | MHz |
| | | XC6SLX16 | | 375 | | MHz |
| | | XC6SLX25 | | | | MHz |
| | | XC6SLX25T | | | N/A | MHz |
| | | XC6SLX45 | | 375 | | MHz |
| | | XC6SLX45T | | 375 | N/A | MHz |
| | | XC6SLX75 | | | | MHz |
| | | XC6SLX75T | | | N/A | MHz |
| | | XC6SLX100 | | | | MHz |
| | | XC6SLX100T | | | N/A | MHz |
| | | XC6SLX150 | | | | MHz |
| | | XC6SLX150T | | | N/A | MHz |

*Table 43:* **Input/Output Clock Switching Characteristics (BUFIO2)**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| $T_{BUFCKO\_O}$ | Clock to out delay from I to O | | 1.5 | | ns |
| **Maximum Frequency** | | | | | |
| $F_{MAX}$ | I/O clock tree (BUFIO2) | | | | MHz |

## PLL Switching Characteristics

*Table 44:* **PLL Specification**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| $F_{INMAX}$ | Maximum Input Clock Frequency from I/O Clock | All | | 450 | | MHz |
| | Maximum Input Clock Frequency from Global Clock | All | | 375 | | MHz |
| $F_{INMIN}$ | Minimum Input Clock Frequency | All | | 19 | | MHz |
| $F_{INJITTER}$ | Maximum Input Clock Period Jitter | All | <20% of clock input period or 1 ns Max | | | |
| $F_{INDUTY}$ | Allowable Input Duty Cycle: 19—199 MHz | All | 25/75 | | | % |
| | Allowable Input Duty Cycle: 200—299 MHz | All | 35/65 | | | % |
| | Allowable Input Duty Cycle: > 300 MHz | All | 45/55 | | | % |
| $F_{VCOMIN}$ | Minimum PLL VCO Frequency | All | | | | MHz |
| $F_{VCOMAX}$ | Maximum PLL VCO Frequency | All | | | | MHz |
| $F_{BANDWIDTH}$ | Low PLL Bandwidth at Typical(1) | All | | | | MHz |
| | High PLL Bandwidth at Typical(1) | All | | | | MHz |
| $T_{STAPHAOFFSET}$ | Static Phase Offset of the PLL Outputs | All | | | | ps |
| $T_{OUTJITTER}$ | PLL Output Jitter(2) | All | Note 1 | | | |
| $T_{OUTDUTY}$ | PLL Output Clock Duty Cycle Precision(3) | All | | | | ps |
| $T_{LOCKMAX}$ | PLL Maximum Lock Time(4) | All | | | | µs |
| $F_{OUTMAX}$ | PLL Maximum Output Frequency for BUFGMUX | XC6SLX4 | | | | MHz |
| | | XC6SLX9 | | | | MHz |
| | | XC6SLX16 | | 375 | | MHz |
| | | XC6SLX25 | | | | MHz |
| | | XC6SLX25T | | | N/A | MHz |
| | | XC6SLX45 | | 375 | | MHz |
| | | XC6SLX45T | | 375 | N/A | MHz |
| | | XC6SLX75 | | | | MHz |
| | | XC6SLX75T | | | N/A | MHz |
| | | XC6SLX100 | | | | MHz |
| | | XC6SLX100T | | | N/A | MHz |
| | | XC6SLX150 | | | | MHz |
| | | XC6SLX150T | | | N/A | MHz |

*Table 44:* **PLL Specification *(Cont'd)***

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| $F_{OUTMAX}$ | PLL Maximum Output Frequency for BUFPLL | XC6SLX4 | | | | MHz |
| | | XC6SLX9 | | | | MHz |
| | | XC6SLX16 | | | | MHz |
| | | XC6SLX25 | | | | MHz |
| | | XC6SLX25T | | | N/A | MHz |
| | | XC6SLX45 | | | | MHz |
| | | XC6SLX45T | | | N/A | MHz |
| | | XC6SLX75 | | | | MHz |
| | | XC6SLX75T | | | N/A | MHz |
| | | XC6SLX100 | | | | MHz |
| | | XC6SLX100T | | | N/A | MHz |
| | | XC6SLX150 | | | | MHz |
| | | XC6SLX150T | | | N/A | MHz |
| $F_{OUTMIN}$ | PLL Minimum Output Frequency(5) | All | | | | MHz |
| $T_{EXTFDVAR}$ | External Clock Feedback Variation | All | < 20% of clock input period or 1 ns Max | | | |
| $RST_{MINPULSE}$ | Minimum Reset Pulse Width | All | | | | ns |
| $F_{PFDMAX}$ | Maximum Frequency at the Phase Frequency Detector | All | | | | MHz |
| $F_{PFDMIN}$ | Minimum Frequency at the Phase Frequency Detector | All | | | | MHz |
| $T_{FBDELAY}$ | Maximum Delay in the Feedback Path | All | 3 ns Max or one CLKIN cycle | | | |

**Notes:**
1. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. Values for this parameter are available in the Architecture Wizard.
3. Includes global clock buffer.
4. The LOCK signal must be sampled after $T_{LOCKMAX}$. The LOCK signal is invalid after configuration or reset until the $T_{LOCKMAX}$ time has expired.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

## DCM Switching Characteristics

*Table 45:* **Operating Frequency Ranges and Conditions for the Delay-Locked Loop (DLL)(1)**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | -3 | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | |
| **Input Frequency Ranges** | | | | | | | | |
| CLKIN_FREQ_DLL | Frequency of the CLKIN clock input. Also described as $F_{CLKIN}$. | | | 5(2) | 250(3) | | | MHz |
| **Input Pulse Requirements** | | | | | | | | |
| CLKIN_PULSE | CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL < 150 MHz | | | 40 | 60 | | | % |
| | CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL > 150 MHz | | | 45 | 55 | | | % |
| **Input Clock Jitter Tolerance and Delay Path Variation(4)** | | | | | | | | |
| CLKIN_CYC_JITT_DLL_LF | Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL < 150 MHz | | | | ±300 | | | ps |
| CLKIN_CYC_JITT_DLL_HF | Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL > 150 MHz. | | | | ±150 | | | ps |
| CLKIN_PER_JITT_DLL | Period jitter at the CLKIN input. | | | | ±1 | | | ns |
| CLKFB_DELAY_VAR_EXT | Allowable variation of the off-chip feedback delay from the DCM output to the CLKFB input. | | | | ±1 | | | ns |

**Notes:**
1. DLL specifications apply when using any of the DLL outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV.
2. When operating independently of the DLL, the DFS supports lower CLKIN_FREQ_DLL frequencies. See Table 47.
3. To support double the maximum effective CLKIN_FREQ_DLL limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock period by two as it enters the DCM. The CLK2X output reproduces the clock frequency provided on the CLKIN_FREQ_DLL input.
4. CLKIN_FREQ_DLL input jitter beyond these limits can cause the DCM to lose LOCK, indicated by the LOCKED output deasserting. The user must then reset the DCM.
5. When using both DCMs in a CMT, both DCMs must be LOCKED.

*Table 46:* **Switching Characteristics for the Delay-Locked Loop (DLL) (1)**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | -3 | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | |
| **Output Frequency Ranges** | | | | | | | | |
| CLKOUT_FREQ_CLK0 | Frequency for the CLK0 and CLK180 outputs. | | | 5 | 250 | | | MHz |
| CLKOUT_FREQ_CLK90 | Frequency for the CLK90 and CLK270 outputs. | | | 5 | 200 | | | MHz |
| CLKOUT_FREQ_2X | Frequency for the CLK2X and CLK2X180 outputs. | | | 10 | 334 | | | MHz |
| CLKOUT_FREQ_DV | Frequency for the CLKDV output. | | | 0.3125 | 166 | | | MHz |
| **Output Clock Jitter(2,3,4)** | | | | | | | | |
| CLKOUT_PER_JITT_0 | Period jitter at the CLK0 output. | – | | – | ±100 | – | | ps |
| CLKOUT_PER_JITT_90 | Period jitter at the CLK90 output. | – | | – | ±150 | – | | ps |
| CLKOUT_PER_JITT_180 | Period jitter at the CLK180 output. | – | | – | ±150 | – | | ps |
| CLKOUT_PER_JITT_270 | Period jitter at the CLK270 output. | – | | – | ±150 | – | | ps |

*Table 46:* **Switching Characteristics for the Delay-Locked Loop (DLL) [1] *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | -3 | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | |
| CLKOUT_PER_JITT_2X | Period jitter at the CLK2X and CLK2X180 outputs. | – | | – | ±[0.5% of CLKIN period + 100] | – | | ps |
| CLKOUT_PER_JITT_DV1 | Period jitter at the CLKDV output when performing integer division. | – | | – | ±150 | – | | ps |
| CLKOUT_PER_JITT_DV2 | Period jitter at the CLKDV output when performing non-integer division. | – | | – | ±[0.5% of CLKIN period + 100] | – | | ps |
| **Duty Cycle[4]** | | | | | | | | |
| CLKOUT_DUTY_CYCLE_DLL | Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion. | – | | – | ±[1% of CLKIN period + 350] | – | | ps |
| **Phase Alignment[4]** | | | | | | | | |
| CLKIN_CLKFB_PHASE | Phase offset between the CLKIN and CLKFB inputs. | – | | – | ±150 | – | | ps |
| CLKOUT_PHASE_DLL | Phase offset between DLL outputs for CLK0 to CLK2X (not CLK2X180). | – | | – | ±[1% of CLKIN period + 100] | – | | ps |
| | Phase offset between DLL outputs for all others. | – | | – | | – | | ps |
| LOCK_DLL[3] | When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.<br>5 MHz < CLKIN_FREQ_DLL < 15 MHz. | | | – | 5 | – | | ms |
| | When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase.<br>CLKIN_FREQ_DLL > 15 MHz | | | – | 0.60 | – | | ms |
| **Delay Lines** | | | | | | | | |
| DCM_DELAY_STEP[5] | Finest delay resolution, averaged over all steps. | | | 10 | 40 | | | ps |

**Notes:**
1. The values in this table are based on the operating conditions described in Table 2 and Table 45.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster LOCK time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, this data sheet specifies a maximum jitter of ±(1% of CLKIN period + 150 ps). Assuming that the CLKIN frequency is 100 MHz, the equivalent CLKIN period is 10 ns. Since 1% of 10 ns is 0.1 ns or 100 ps, the maximum jitter is ±(100 ps + 150 ps) = ±250 ps.
5. A typical delay step size is 23 ps.

*Table 47:* **Recommended Operating Conditions for the Digital Frequency Synthesizer (DFS) (1)**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | -3 | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | |
| **Input Frequency Ranges(2)** | | | | | | | | |
| CLKIN_FREQ_FX | Frequency for the CLKIN input. Also described as $F_{CLKIN}$. | | | 0.5 | 333 | | | MHz |
| **Input Clock Jitter Tolerance(3)** | | | | | | | | |
| CLKIN_CYC_JITT_FX_LF | Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: FCLKFX < 150 MHz. | – | | – | ±300 | – | | ps |
| CLKIN_CYC_JITT_FX_HF | Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: FCLKFX > 150 MHz. | – | | – | ±150 | – | | ps |
| CLKIN_PER_JITT_FX | Period jitter at the CLKIN input. | – | | – | ±1 | – | | ns |

**Notes:**
1. DFS specifications apply when using either of the DFS outputs (CLKFX, CLKFXDV, or CLKFX180).
2. When using both DFS and DLL outputs on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 45.
3. CLKIN input jitter beyond these limits can cause the DCM to lose LOCK.

*Table 48:* **Switching Characteristics for the Digital Frequency Synthesizer (DFS) (1)**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | -3 | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | |
| **Output Frequency Ranges** | | | | | | | | |
| CLKOUT_FREQ_FX | Frequency for the CLKFX and CLKFX180 outputs | | | 5 | 320 | | | MHz |
| CLKOUT_FREQ_FXDV | Frequency for the CLKFXDV output | | | 0.15625 | 160 | | | MHz |
| **Output Clock Jitter(2,3)** | | | | | | | | |
| CLKOUT_PER_JITT_FX | Period jitter at the CLKFX, CLKFX180, and CLKFXDV outputs. When CLKIN < 20 MHz | | | Use the Jitter Calculator | | | | ps |
| | Period jitter at the CLKFX, CLKFX180, and CLKFXDV outputs. When CLKIN > 20 MHz | | | ±(1% of CLKFX period + 100) | ±(1% of CLKFX period + 200) | | | ps |
| **Duty Cycle(4,5)** | | | | | | | | |
| CLKOUT_DUTY_CYCLE_FX | Duty cycle precision for the CLKFX, CLKFX180, and CLKFXDV outputs, including the BUFGMUX and clock tree duty-cycle distortion | | – | | ±(1% of CLKFX period + 350) | | – | ps |
| **Phase Alignment(5)** | | | | | | | | |
| CLKOUT_PHASE_FX | Phase offset between the DFS CLKFX or CLKFXDV output and the DLL CLK0 output when both the DFS and DLL are used | | – | | ±200 | | – | ps |
| CLKOUT_PHASE_FX180 | Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used | | – | | ±(1% of CLKFX period + 200) | | – | ps |

*Table 48:* **Switching Characteristics for the Digital Frequency Synthesizer (DFS) (1) *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | -3 | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | |
| **LOCKED Time** | | | | | | | | |
| LOCK_FX(2) | When 5 MHz < FCLKIN < 15 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX, CLKFX180, and CLKFXDV signals are valid. When using both the DLL and the DFS, use the longer locking time. | – | | – | 5 | – | | ms |
| | When FCLKIN > 15 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX, CLKFX180, and CLKFXDV signals are valid. When using both the DLL and the DFS, use the longer locking time. | – | | – | 0.45 | – | | ms |

**Notes:**
1. The values in this table are based on the operating conditions described in Table 2 and Table 47.
2. For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
3. Maximum output jitter is characterized using a reasonable noise environment (40 SSOs and 25% CLB switching). Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
5. Some duty cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.

*Table 49:* **Recommended Operating Conditions for the Phase-Shift Clock in Variable Phase Mode**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | -3 | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | |
| **Operating Frequency Ranges** | | | | | | | | |
| PSCLK_FREQ | Frequency for the PSCLK input. | | | 1 | 167 | | | MHz |
| **Input Pulse Requirements** | | | | | | | | |
| PSCLK_PULSE | PSCLK pulse width as a percentage of the PSCLK period. | | | 40 | 60 | | | % |

*Table 50:* **Switching Characteristics for the Phase-Shift Clock in Variable Phase Mode(1)**

| Symbol | Description | Amount of Phase Shift | Units |
|---|---|---|---|
| **Phase Shifting Range** | | | |
| MAX_STEPS(2) | When CLKIN < 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period. | ±(INTEGER(10 x (TCLKIN – 3 ns))) | steps |
| | When CLKIN ≥ 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period. | ±(INTEGER(15 x (TCLKIN – 3 ns))) | steps |
| FINE_SHIFT_RANGE_MIN | Minimum guaranteed delay for variable phase shifting. | ±(MAX_STEPS x DCM_DELAY_STEP_MIN) | ns |
| FINE_SHIFT_RANGE_MAX | Maximum guaranteed delay for variable phase shifting | ±(MAX_STEPS x DCM_DELAY_STEP_MAX) | ns |

**Notes:**
1. The values in this table are based on the operating conditions described in Table 45 and Table 49.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM has no initial fixed-phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the end of Table 46.

*Table 51:* **Miscellaneous DCM Timing Parameters(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| DCM_RST_PW_MIN | Minimum duration of a RST pulse width | 3 | – | CLKIN cycles |

**Notes:**
1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFXDV, CLKFX180) are unaffected.

*Table 52:* **Frequency Synthesis**

| Attribute | Min | Max |
|---|---|---|
| CLKFX_MULTIPLY | 2 | 32 |
| CLKFX_DIVIDE | 1 | 32 |

*Table 53:* **DCM Switching Characteristics**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| $T_{DMCCK\_PSEN}$/ $T_{DMCKC\_PSEN}$ | PSEN Setup/Hold | | 0.03/ 0.00 | | ns |
| $T_{DMCCK\_PSINCDEC}$/ $T_{DMCKC\_PSINCDEC}$ | PSINCDEC Setup/Hold | | 0.03/ 0.00 | | ns |
| $T_{DMCKO\_PSDONE}$ | Clock to out of PSDONE | | 0.05 | | ns |

## Spartan-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 54. Values are expressed in nanoseconds unless otherwise noted.

*Table 54:* **Global Clock Input to Output Delay Without DCM or PLL**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* DCM or PLL | | | | | | |
| $T_{ICKOF}$ | Global Clock and OUTFF *without* DCM or PLL | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | | | ns |
| | | XC6SLX45T | | | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

*Table 55:* **Global Clock Input to Output Delay With DCM in System-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in System-Synchronous Mode. | | | | | | |
| $T_{ICKOFDCM}$ | Global Clock and OUTFF *with* DCM | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | | | ns |
| | | XC6SLX45T | | | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

*Table 56:* **Global Clock Input to Output Delay With DCM in Source-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in Source-Synchronous Mode. | | | | | | |
| $T_{ICKOFDCM\_0}$ | Global Clock and OUTFF *with* DCM | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | | | ns |
| | | XC6SLX45T | | | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

*Table 57:* **Global Clock Input to Output Delay With PLL in System-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* PLL in System-Synchronous Mode. | | | | | | |
| $T_{ICKOFPLL}$ | Global Clock and OUTFF *with* PLL | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | | | ns |
| | | XC6SLX45T | | | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

*Table 58:* **Global Clock Input to Output Delay With PLL in Source-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* PLL in Source-Synchronous Mode. | | | | | | |
| $T_{ICKOFPLL\_0}$ | Global Clock and OUTFF *with* PLL | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | | | ns |
| | | XC6SLX45T | | | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

*Table 59:* **Global Clock Input to Output Delay With DCM and PLL in System-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM and PLL in System-Synchronous Mode. | | | | | | |
| $T_{ICKOFDCM\_PLL}$ | Global Clock and OUTFF with DCM and PLL | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | | | ns |
| | | XC6SLX45T | | | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

*Table 60:* **Global Clock Input to Output Delay With DCM and PLL in Source-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM and PLL in Source-Synchronous Mode. | | | | | | |
| $T_{ICKOFDCM0\_PLL}$ | Global Clock and OUTFF with DCM and PLL | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | | | ns |
| | | XC6SLX45T | | | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

## Spartan-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 61. Values are expressed in nanoseconds unless otherwise noted.

*Table 61:* **Global Clock Setup and Hold Without DCM or PLL**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)** | | | | | | |
| $T_{PSFD}$/ $T_{PHFD}$ | Full Delay (Legacy Delay or Default Delay) Global Clock and IFF(2) without DCM or PLL | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | | | ns |
| | | XC6SLX45T | | | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |

**Notes:**
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

*Table 62:* **Global Clock Setup and Hold With DCM in System-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)** | | | | | | |
| $T_{PSDCM}$/ $T_{PHDCM}$ | No Delay Global Clock and IFF(2) with DCM in System-Synchronous Mode | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | | | ns |
| | | XC6SLX45T | | | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |

**Notes:**
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 63:* **Global Clock Setup and Hold With DCM in Source-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)** | | | | | | |
| $T_{PSDCM0}$/ $T_{PHDCM0}$ | No Delay Global Clock and IFF(2) with DCM in Source-Synchronous Mode | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | | | ns |
| | | XC6SLX45T | | | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |

**Notes:**
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 64:* **Global Clock Setup and Hold With PLL in System-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)** | | | | | | |
| $T_{PSPLL}$/ $T_{PHPLL}$ | No Delay Global Clock and IFF(2) with PLL in System-Synchronous Mode | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | | | ns |
| | | XC6SLX45T | | | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |

**Notes:**
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 65:* **Global Clock Setup and Hold With PLL in Source-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)** | | | | | | |
| $T_{PSPLL0}$/ $T_{PHPLL0}$ | No Delay Global Clock and IFF(2) with PLL in Source-Synchronous Mode | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | | | ns |
| | | XC6SLX45T | | | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |

**Notes:**
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 66:* **Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard.(1)** | | | | | | |
| $T_{PSDCMPLL}$/ $T_{PHDCMPLL}$ | No Delay Global Clock and IFF(2) with DCM and PLL in System-Synchronous Mode | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | | | ns |
| | | XC6SLX45T | | | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |

**Notes:**
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 67:* **Global Clock Setup and Hold With DCM and PLL in Source-Synchronous Mode**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| Example Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin,(1) Using DCM, PLL, and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in IOB Switching Characteristics, page 15. | | | | | | |
| $T_{PSDCMPLL\_0}$/ $T_{PHDCMPLL\_0}$ | No Delay Global Clock and IFF(2) with DCM and PLL in Source-Synchronous Mode | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | | | ns |
| | | XC6SLX45T | | | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |

**Notes:**
1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG. Package skew is not included in these measurements.
2. IFF = Input Flip-Flop

## Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Spartan-6 FPGA source-synchronous transmitter and receiver data-valid windows.

*Table 68:* **Duty Cycle Distortion and Clock-Tree Skew**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| $T_{DCD\_CLK}$ | Global Clock Tree Duty Cycle Distortion (1) | All | | | | ns |
| $T_{CKSKEW}$ | Global Clock Tree Skew (2) | XC6SLX4 | | | | ns |
| | | XC6SLX9 | | | | ns |
| | | XC6SLX16 | | | | ns |
| | | XC6SLX25 | | | | ns |
| | | XC6SLX25T | | | N/A | ns |
| | | XC6SLX45 | | | | ns |
| | | XC6SLX45T | | | N/A | ns |
| | | XC6SLX75 | | | | ns |
| | | XC6SLX75T | | | N/A | ns |
| | | XC6SLX100 | | | | ns |
| | | XC6SLX100T | | | N/A | ns |
| | | XC6SLX150 | | | | ns |
| | | XC6SLX150T | | | N/A | ns |
| $T_{DCD\_BUFIO}$ | I/O clock tree duty cycle distortion | All | | | | ns |
| $T_{BUFIOSKEW}$ | I/O clock tree skew across one clock region | All | | | | ns |

**Notes:**
1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The $T_{CKSKEW}$ value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

*Table 69:* **Package Skew**

| Symbol | Description | Device | Package(3) | Value | Units |
|---|---|---|---|---|---|
| $T_{PKGSKEW}$ | Package Skew(1) | XC6SLX4 | TQG144 | | ps |
| | | | CPG196 | | ps |
| | | | CSG225 | | ps |
| | | XC6SLX9 | TQG144 | | ps |
| | | | CPG196 | | ps |
| | | | CSG225 | | ps |
| | | | FT(G)256 | | ps |
| | | | CSG324 | | ps |
| | | XC6SLX16 | CPG196 | | ps |
| | | | CSG225 | | ps |
| | | | FT(G)256 | | ps |
| | | | CSG324 | | ps |

*Table 69:* **Package Skew *(Cont'd)***

| Symbol | Description | Device | Package(3) | Value | Units |
|---|---|---|---|---|---|
| $T_{PKGSKEW}$ | Package Skew(1) | XC6SLX25 | FT(G)256 | | ps |
| | | | CSG324 | | ps |
| | | | FG(G)484 | | ps |
| | | XC6SLX25T | CSG324 | | ps |
| | | | FG(G)484 | | ps |
| | | XC6SLX45 | CSG324 | | ps |
| | | | CSG484 | | ps |
| | | | FG(G)484 | | ps |
| | | | FG(G)676 | | ps |
| | | XC6SLX45T | CSG324 | | ps |
| | | | CSG484 | | ps |
| | | | FG(G)484 | | ps |
| | | XC6SLX75 | CSG324 | | ps |
| | | | CSG484 | | ps |
| | | | FG(G)676 | | ps |
| | | XC6SLX75T | CSG324 | | ps |
| | | | CSG484 | | ps |
| | | | FG(G)676 | | ps |
| | | XC6SLX100 | CSG484 | | ps |
| | | | FG(G)484 | | ps |
| | | | FG(G)676 | | ps |
| | | XC6SLX100T | CSG484 | | ps |
| | | | FG(G)484 | | ps |
| | | | FG(G)676 | | ps |
| | | | FG(G)900 | | ps |
| | | XC6SLX150 | CSG484 | | ps |
| | | | FG(G)484 | | ps |
| | | | FG(G)676 | | ps |
| | | | FG(G)900 | | ps |
| | | XC6SLX150T | CSG484 | | ps |
| | | | FG(G)484 | | ps |
| | | | FG(G)676 | | ps |
| | | | FG(G)900 | | ps |

**Notes:**
1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
2. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.
3. Some of these devices are available in both Pb and Pb-free (additional G) packages as standard ordering options.

*Table 70:* **Sample Window**

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | -3 | -2 | -1L | |
| $T_{SAMP}$ | Sampling Error at Receiver Pins(1) | All | | | | ps |
| $T_{SAMP\_BUFIO}$ | Sampling Error at Receiver Pins using BUFIO(2) | All | | | | ps |

**Notes:**
1. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 DCM jitter
   - DCM accuracy (phase offset)
   - DCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

*Table 71:* **Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out**

| Symbol | Description | Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | -3 | -2 | -1L | |
| **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO** | | | | | |
| $T_{PSCS}/T_{PHCS}$ | Setup/Hold of I/O clock | | | | ns |
| **Pin-to-Pin Clock-to-Out Using BUFIO** | | | | | |
| $T_{ICKOFCS}$ | Clock-to-Out of I/O clock | | | | ns |

# Revision History

The following table shows the revision history for this document.

| Date | Version | Description of Revisions |
|---|---|---|
| 06/24/09 | 1.0 | Initial Xilinx release. |
| 08/26/09 | 1.1 | Added $V_{FS}$ to Table 1and Table 2. Added $R_{FUSE}$ to Table 2. Added XC6SLX75 and XC6SLX75T to $V_{BATT}$ and $I_{BATT}$ in Table 1, Table 2, and Table 3. Corrected the quiescent supply current for the XC6SLX4 in Table 4. Updated Table 8. Removed $DV_{PPIN}$ from Figure 2. Removed $F_{PCIECORE}$ from Table 21 and added values to $F_{PCIEUSER}$. Added more networking applications to Table 22. Updated values for $T_{SUSPENDLOW\_AWAKE}$, $T_{SUSPEND\_ENABLE}$, and $T_{SCP\_AWAKE}$ in Table 40. Numerous changes to Table 41, page 33 including the addition of new values to various specifications, revising the $T_{SMCKCSO}$ description, and changing the units of $T_{POR}$. Also, removed *Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK section* from Table 41 and updated all the notes. In Table 44, added to $F_{INMAX}$, revised $F_{OUTMAX}$, and removed PLL Maximum Output Frequency for BUFIO2. Revised values for DCM_DELAY_STEP in Table 46. Updated CLKIN_FREQ_FX values in Table 47. |

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