- **Independent Dual-Outputs Operate 180° Out of Phase**
- **Wide Input Voltage Range: 4.5-V – 28-V**
- **Adjustable Output Voltage Down to 0.9 V**
- **Pin-Selectable PWM/SKIP Mode for High Efficiency Under Light Loads**
- **Synchronous Buck Operation Allows up to 95% Efficiency**
- **Separate Standby Control and Overcurrent Protection for Each Channel**
- **Programmable Short-Circuit Protection**
- **Low Supply (1 mA) and Shutdown (1 nA) Current**
- **Power Good Output**
- **High-Speed Error Amplifiers**
- **Sequencing Easily Achieved by Selecting Softstart Capacitor Values.**
- **5-V Linear Regulator Power Internal IC Circuitry**
- **30-Pin TSSOP Packaging**

DBT PACKAGE
(TOP VIEW)

INV1	1	30	LH1
FB1	2	29	OUT1_u
SOFTSTART1	3	28	LL1
PWM/SKIP	4	27	OUT1_d
CT	5	26	OUTGND1
5V_STBY	6	25	TRIP1
GND	7	24	V_{CC}
REF	8	23	TRIP2
STBY1	9	22	VREF5
STBY2	10	21	REG5V_IN
FLT	11	20	OUTGND2
POWERGOOD	12	19	OUT2_d
SOFTSTART2	13	18	LL2
FB2	14	17	OUT2_u
INV2	15	16	LH2

description

The TPS5120 is a dual channel, high-efficiency synchronous buck controller where the outputs run 180 degrees out of phase, which lowers the input current ripple, thereby reducing the input capacitance cost. The PWM/SKIP pin allows the operating mode to switch from PWM mode to skip mode under light load conditions. The skip mode enables a lower operating frequency and shortens the pulse width to the low-side MOSFET, increasing the efficiency under light load conditions. These two modes, along with synchronous-rectifier drivers, dead time, and very low quiescent current, allow power to be conserved and the battery life to be extended under all load conditions. The 1.5 A (typical) high-side and low-side MOSFET drivers on-chip are designed to drive less expensive N-channel MOSFETs. The resistorless current protection and fixed high-side driver voltage simplify the power supply design and reduce the external parts count. Each channel is independent, offering a separate controller, overcurrent protection, and standby control. Sequencing is flexible and can be tailored by choosing different softstart capacitor values. Other features, such as undervoltage lockout, power good, overvoltage, undervoltage, and programmable short-circuit protection promote system reliability.

typical design

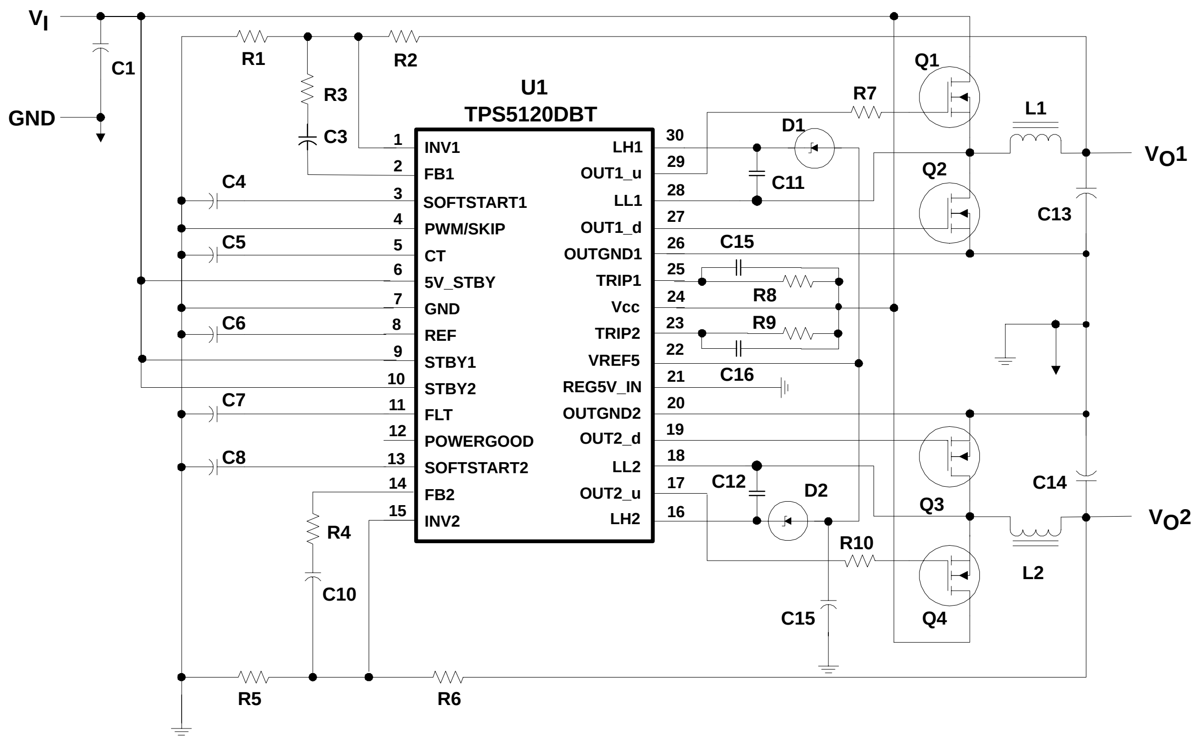
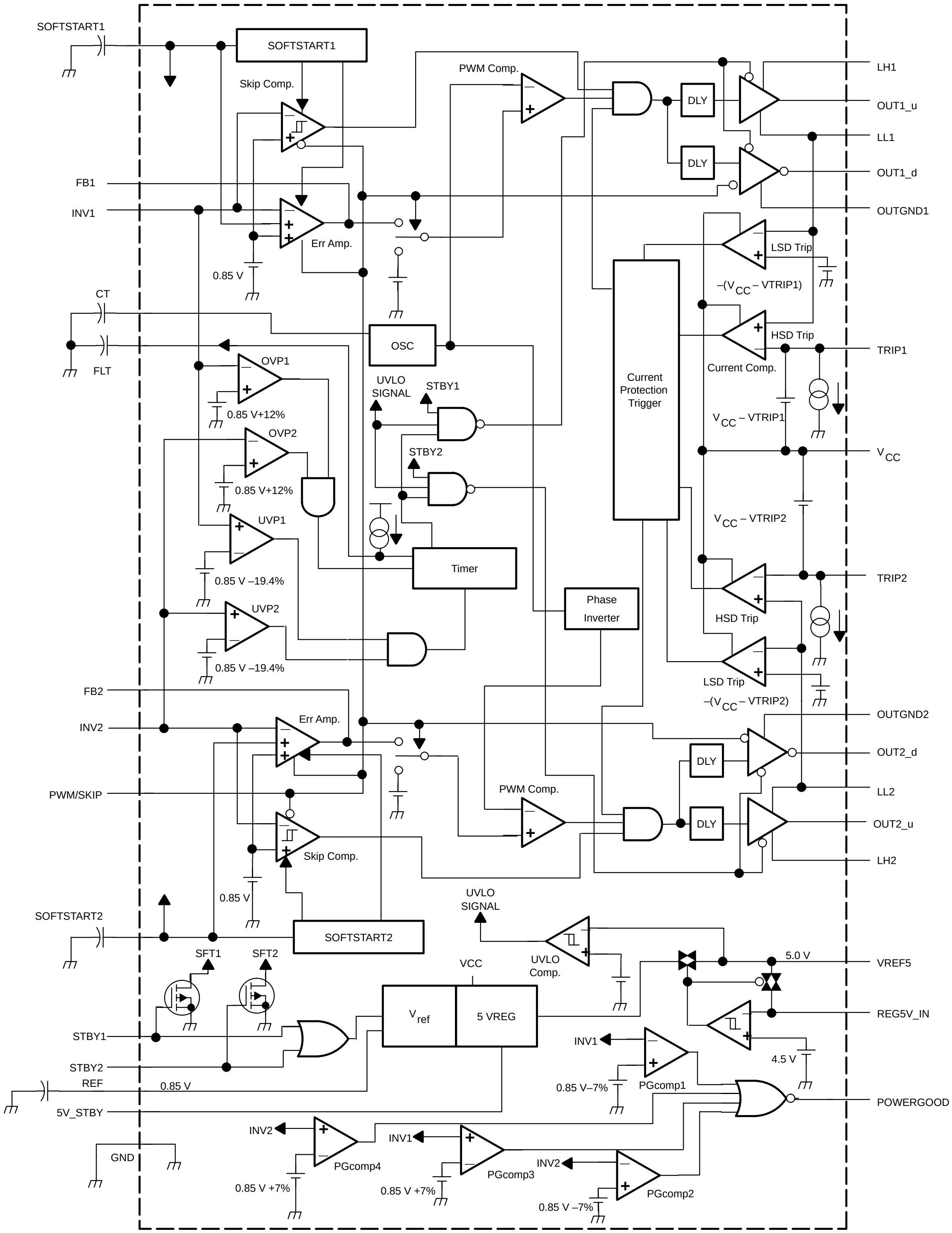


Figure 1. EVM Typical Design

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGE TSSOP (DBT)	EVM
–40°C to 85°C	TPS5120DBT	TPS5120EVM-151
	TPS5120DBTR	

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CT	5	I/O	External capacitor from CT to GND for adjusting the triangle oscillator
FB1	2	O	Feedback output of CH1 error amplifier
FB2	14	O	Feedback output of CH2 error amplifier
GND	7		Control GND
INV1	1	I	Inverting input of the CH1 error amplifier, skip comparator, and OVP1/UVP1 comparator
INV2	15	I	Inverting input of the CH2 error amplifier, skip comparator, and OVP2/UVP2 comparator
LH1	30	I/O	Bootstrap capacitor connection for CH1 high-side gate drive
LH2	16	I/O	Bootstrap capacitor connection for CH2 high-side gate drive
LL1	28	I/O	Bootstrap this pin low for CH1 high-side gate driving return and output current protection. Connect this pin to the junction of the high-side and low-side FETs for a floating drive configuration.
LL2	18	I/O	Bootstrap this pin low for CH2 high-side gate driving return and output current protection. Connect this pin to the junction of the high-side and low-side FETs for a floating drive configuration.
OUT1_d	27	O	Gate drive output for CH1 low-side gate drive
OUT2_d	19	O	Gate drive output for CH2 low-side gate drive
OUT1_u	29	O	Gate drive output for CH1 high-side switching FETs
OUT2_u	17	O	Gate drive output for CH2 high-side switching FETs
OUTGND1	26		Ground for CH1 FET drivers
OUTGND2	20		Ground for CH2 FET drivers
POWERGOOD	12	O	Power good open-drain output. When low, POWERGOOD reports an output fail condition. PG comparators monitor both SMPS's over voltage and UVLO of VREF5. The threshold is ±7%. When the SMPS starts up, the POWERGOOD pin's output goes high. POWERGOOD also monitors VREF5's UVLO output.
PWM/SKIP	4	I	PWM/SKIP mode select pin. The PWM/SKIP pin is used to change the output's operating mode. If this terminal is lower than 0.5 V, it works in PWM mode. When a minimum voltage of 2 V is applied, the device operates in skip mode. In light load condition (< 0.2 A), the skip mode gives a short pulse to the low-side FETs instead of a full pulse. With this control, switching frequency is lowered and switching loss is reduced. Also, the output capacitor energy discharging through the output inductor and low-side FETs is stopped. Therefore, TPS5120 achieves a higher efficiency in light load conditions.
REF	8	O	0.85-V reference voltage output. The 0.85-V reference voltage is used for setting the output voltage and the voltage protection. This reference voltage is dropped down from a 5-V regulator.
REG5V_IN	21	I	External 5-V input
FLT	11	I/O	Fault latch timer pin. An external capacitor is connected between FLT and GND to set the FLT enable time up.
SOFTSTART1	3	I/O	External capacitor from SOFTSTART1 to GND for CH1 softstart control. Separate soft-start terminals make it possible to set the start-up time of each output independently.
SOFTSTART2	13	I/O	External capacitor from SOFTSTART2 to GND for CH2 softstart control. Separate soft-start terminals make it possible to set the start-up time of each output independently.
STBY1	9	I	Standby control for CH1. SMPS1 can be switched into standby mode separately by grounding the STBY1 pin.
STBY2	10	I	Standby control for CH2. SMPS2 can be switched into standby mode separately by grounding the STBY2 pin.
TRIP1	25	I	External resistor connection for CH1 output current control

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TRIP2	23	I	External resistor connection for CH2 output current control
V_{CC}	24		Supply voltage input
VREF5	22	O	5-V internal regulator output
5V_STBY	6	I	5-V linear regulator control

detailed description

switching-mode power supply (SMPS) 1, 2

TPS5120 includes dual SMPS controllers that operate 180° out of phase and at the same frequency. Both channels have standby and softstart.

5-V regulator

An internal linear voltage regulator is used for the high-side driver bootstrap voltage and source of VREF (0.85 V). When the 5-V regulator is disconnected from the MOSFET drivers, it is only used for the source of VREF. Since the input voltage range is from 4.5 V to 28 V, this feature offers a fixed voltage for the bootstrap voltage so that the drive design is much easier. It is also used for powering the low-side driver. The tolerance is 4%. The 5-V regulator is disabled when STBY1, STBY2, and 5V_STBY are all set low.

5-V switch

If the internal 5-V switch senses the 5-V input from the REG5V_IN pin, the internal 5-V linear regulator is disconnected from the MOSFET drivers. The external 5 V is then used for both the low-side driver and the high-side bootstrap, thus, increasing the efficiency.

error amplifier

Each channel has its own error amplifier to regulate the output voltage of the synchronous buck converter. It is used in the PWM mode for the high output current condition (> 0.2 A). The unity gain bandwidth is 2.5 MHz. This decreases the amplifier delay during fast load transients and contributes to a fast transient response.

skip comparator

In skip mode, each channel has its own hysteretic comparator to regulate the output voltage of the synchronous buck converter. The hysteresis is set internally and is typically set at 9 mV. The delay from the comparator input to the driver output is typically 1.2 µs.

low-side driver

The low-side driver is designed to drive low $r_{ds(on)}$ N-channel MOSFETs. The maximum drive voltage is 5 V from VREF5. The current rating of the driver is typically 1.5 A at source and sink.

high-side driver

The high-side driver is designed to drive low $r_{ds(on)}$ N-channel MOSFETs. The current rating of the driver is 1.2 A at source and sink. When configured as a floating driver, the bias voltage to the driver is developed from VREF5, limiting the maximum drive voltage between OUTx_u and LLx to 5 V. The maximum voltage that can be applied between LHx and OUTGND is 33 V.

deadtime

Deadtime prevents shoot through current from flowing through the main power FETs during switching transitions by actively controlling the turnon time of the MOSFETs drivers.

detailed description (continued)

current protection

Overcurrent protection is achieved by comparing the drain-to-source voltage of the high-side and low-side MOSFET devices to a set-point voltage. This voltage is set using an external resistor between V_{CC} and the TRIP1 or TRIP2 terminals. If the drain-to-source voltage up exceeds the set-point voltage during high-side conduction, the current limit circuit terminates the high-side driver pulse. If the set-point voltage is exceeded during low-side conduction, the low-side pulse is extended through the next cycle. Together this action has the effect of decreasing the output voltage until the undervoltage protection circuit is activated and the fault latch is set and both the high and low-side MOSFET drivers are shut off.

overvoltage protection

For overvoltage protection (OVP), the TPS5120 monitors INV pin voltage. When the INV voltage is higher than 0.95 V (+12%), the OVP comparator output goes high and the FLT timer starts to charge an external capacitor connected to FLT. After a set time, the FLT circuit latches the MOSFET drivers off.

undervoltage protection

For undervoltage protection (UVP), the TPS5120 monitors INV pin voltage. When the INV voltage is lower than 0.68 V (–19.4%), the OVP comparator output goes high, and the FLT timer starts to charge an external capacitor connected to FLT. Also, when the current comparator triggers the OCP, the UVP comparator detects the under voltage output and starts the FLT capacitor charge. After a set time, the FLT circuit latches off all of the MOSFET drivers.

FLT

When an OVP or UVP comparator output goes high, the FLT circuit starts to charge the FLT capacitor. If the FLT pin voltage goes beyond a constant level, the TPS5120 latches the MOSFET drivers. At this time, the state of MOSFET is different depending on the OVP alert and the UVP alert. Also, the enable time used to latch the MOSFET driver is decided by the capacity of the FLT capacitor. The charging constant current value is also different depending on whether it is an OVP alert or a UVP alert. The difference is shown in the following equation:

$$\text{FLT source current (OVP)} = \text{FLT source current (UVP)} \times 5$$

shutdown

The TPS5120 can be shut down by grounding STBY1, STBY2, and 5V_STBY. The shutdown current is as low as 1 μA.

UVLO

When the input voltage goes up to about 4 V, the TPS5120 is operational. When the input voltage is lower than the turnon value, the device is turned off. The typical hysteresis voltage is 40 mV.

phase Inverter

Phase inverter controls the phase of SMPS1 and SMPS 2. SMPS1 operates in phase with the OSC. SMPS2 operates 180° out of phase from SMPS1. This allows smaller input capacitors to be used.

oscillator

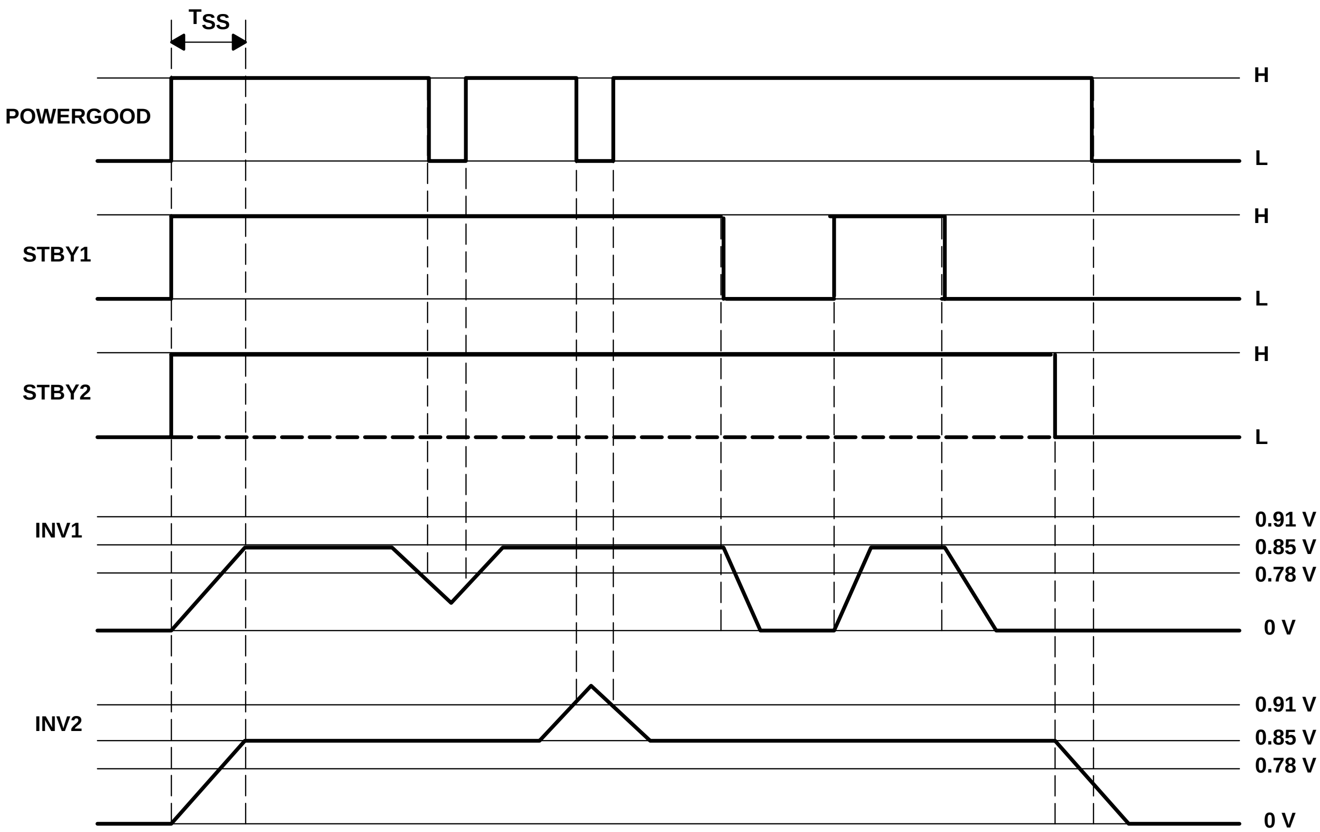
TPS5120 has a triangle oscillator generator internal to the IC. The oscillation frequency is set by the size of the capacitor connected to the CT pin. The voltage amplitude is 0.43 V ~ 1.17 V.

Table 1. Logic Chart

5V_STBY	STBY1	STBY2	SMPS1	SMPS2	5 V REGULATOR	POWERGOOD
L	L	L	Disable	Disable	Disable	Disable
L	L	H	Disable	Enable	Enable	Active†
L	H	L	Enable	Disable	Enable	Active†
L	H	H	Enable	Enable	Enable	Active
H	L	L	Disable	Disable	Enable	L
H	L	H	Disable	Enable	Enable	Active†
H	H	L	Enable	Disable	Enable	Active†
H	H	H	Enable	Enable	Enable	Active

† PG is set high during a softstart.

POWERGOOD timing sequence



During a softstart, this channel’s powergood comparator output is fixed low (POWERGOOD output is high).

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)		–0.3 V to 30 V
Input voltage:	INV1, INV2, CT, PWM/SKIP, REG5V_IN, SOFTSTART1, SOFTSTART2,	–0.3 V to 7 V
	FLT, POWERGOOD	–0.3 V to 7 V
	STBY1, STBY2, 5V_STBY, TRIP1, TRIP2	–0.3 V to 30 V
Output voltage:	LL1, LL2	–1.0 V to 30 V
	OUT1_u, OUT2_u	–1.0 V to 35 V
	LH1, LH2	–0.3 V to 35 V
	OUT1_d, OUT2_d, 5V_OUT, FB1, FB2	–0.3 V to 7 V
	REF	–0.3 V to 3 V
	OUT1_u, LH1 to LL1	–0.3 V to 7 V
	OUT2_u, LH2 to LL2	–0.3 V to 7 V
Power dissipation (T_A ≤ 25°C), P_D		874 mW
Operating free-air temperature range, T_A		–40°C to 85°C
Storage temperature range, T_{stg}		–55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal unless otherwise noted.
2. This rating is specified at duty = 10% on output rise and fall each pulse. Each pulse width (rise and fall) for the peak current should not exceed 2 µs.
3. See Dissipation Rating Table for free-air temperature range above 25°C.

DISSIPATION RATING TABLE

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	POWER DISSIPATION T_A = 85°C
DBT	874 mW	6.993 mW/°C	454 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		28	V
Input voltage, V_I	INV1, INV2, CT, PWM/SKIP, SOFTSTART1, SOFTSTART2, FLT			6	V
	REG5V_IN, POWERGOOD	–0.1		5.5	
	STBY1, STBY2, 5V_STBY			28	
	OUT1_u, OUT2_u, LH1, LH2			33	
	TRIP1, TRIP2	–0.1		28	
Oscillator frequency, f_{osc}			300	500	kHz
Operating free-air temperature range, T_A		–40		85	°C

electrical characteristics over recommended free-air temperature range, V_{CC} = 7 V (unless otherwise noted)

reference voltage

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ref}	Reference voltage				0.85		V
$V_{ref(tol)}$	Reference voltage tolerance	T_A = 25°C,	I = 50 µA	–1%		1%	
		T_A = –20°C to 85°C,	I = 50 µA	–1.5%		1.5%	
		T_A = –40°C to 85°C,	I = 50 µA	–2%		2%	
$R_{(egin)}$	Line regulation	V_{CC} = 4.5 V to 28 V,	I = 50 µA		0.05	3	mV
$R_{(egl)}$	Load regulation	I = 0.1 µA to 1 mA			0.15	5	mV

oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Frequency	PWM mode, CT = 44 pF, T_A = 25 °C		300		kHz
V_{OH}	High level output voltage	DC	1	1.1	1.2	V
		f_{osc} = 300 kHz		1.17		
V_{OL}	Low level output voltage	DC	0.4	0.5	0.6	V
		f_{osc} = 300 kHz		0.43		

error amplifier

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	T_A = 25°C		2	10	mV
	Open-loop voltage gain		50			dB
	Unity-gain bandwidth			2.5		MHz
$I_{(snk)}$	Output sink current	V_O = 1 V	0.3	0.7		mA
$I_{(src)}$	Output source current	V_O = 1 V	0.2	0.9		mA

skip comparator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{hys}	Hysteresis window	SKIP mode		9		mV

duty control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DUTY	Maximum duty cycle	300 kHz, V_I = 0 V		83%		

control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	STBY1, STBY2	2.2			V
		PWM/SKIP, 5V_STBY	2.2			
V_{IL}	Low-level input voltage	STBY1, STBY2			0.3	V
		PWM/SKIP, 5V_STBY			0.3	

5-V internal switch

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TO\_H)}$	Threshold		4.2		4.8	V
$V_{(TO\_L)}$			4.1		4.7	
V_{hys}	Hysteresis		30		200	mV

electrical characteristics over recommended free-air temperature range, V_{CC} = 7 V (unless otherwise noted) (continued)

5-V regulator

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	I_O = 0 mA to 50 mA, T_A = 25°C	V_{CC} = 5.5 V to 28 V,	4.8		5.2	V
$R_{(egin)}$	Line regulation	V_{CC} = 5.5 V to 28 V,	I =10 mA			20	mV
$R_{(egl)}$	Load regulation	I = 1 mA to 10 mA,	V_{CC} = 5.5 V			40	mV
I_{OS}	Short circuit output current	5VREG = 0 V,	T_A = 25°C	65			mA
$V_{(TO\_H)}$	UVLO threshold voltage	5V_OUT voltage		3.6		4.2	V
$V_{(TO\_L)}$				3.5		4.1	
V_{hys}	Hysteresis	5V_OUT voltage		30		150	mV

output drivers

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	OUT_u sink current	V_O = 3 V		1.2		A
	OUT_u source current	V_O = 2 V		–1.5		A
	OUT_d sink current	V_O = 3 V		1.5		A
	OUT_d source current	V_O = 2 V		–1.5		A
$I_{(TRIP)}$	TRIP pin current	T_A = 25°C	11.5	13	14.5	µA

soft start

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SOFT)}$	Soft start current		1.6	2.3	2.9	µA
$V_{(TO\_H)}$	Threshold voltage (SKIP mode)			3.7		V
$V_{(TO\_L)}$				2.5		

output voltage monitor

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVP comparator threshold		0.91	0.95	0.99	V
UVP comparator threshold		0.64	0.68	0.72	V
PG comparator 1, 2 threshold		0.75	0.78	0.81	V
PG comparator 3, 4 threshold		0.88	0.91	0.94	V
PG propagation delay from INV to POWERGOOD	Turnon		13		µs
	Turnoff		1.2		
Timer latch current source	UVP protection	1.5	2.3	3.1	µA
	OVP protection	8	11.5	15	

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	T_A = 25°C, CT = 0 V, INV = 0 V		1.1	1.5	mA
$I_{CC(S)}$	Shutdown current	STBY 1, STBY2, 5V_STBY = 0 V		0.001	10	µA

TYPICAL CHARACTERISTICS

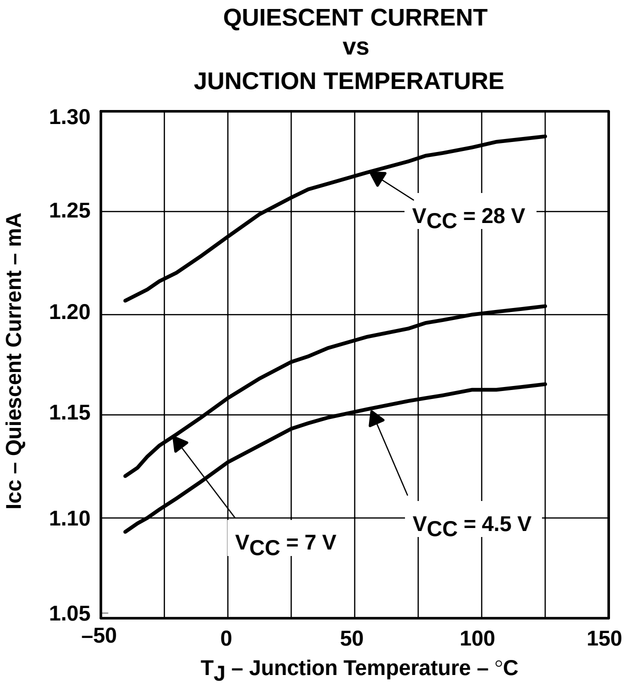


Figure 2

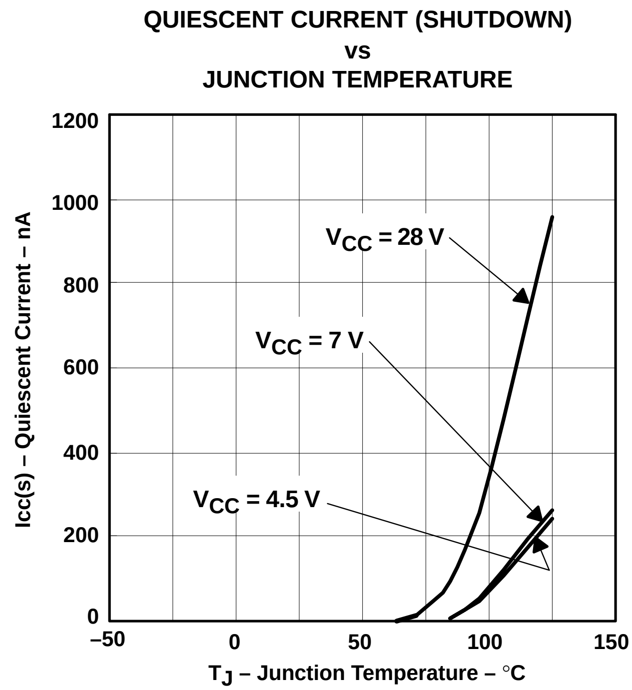


Figure 3

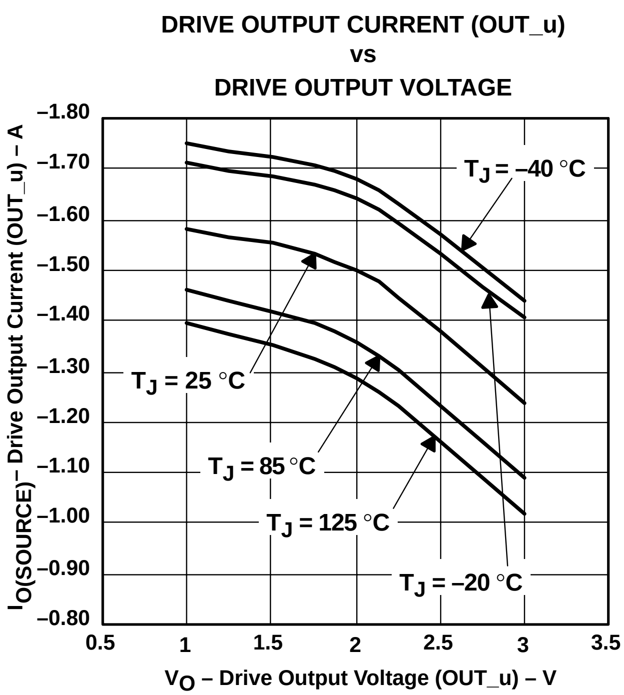


Figure 4

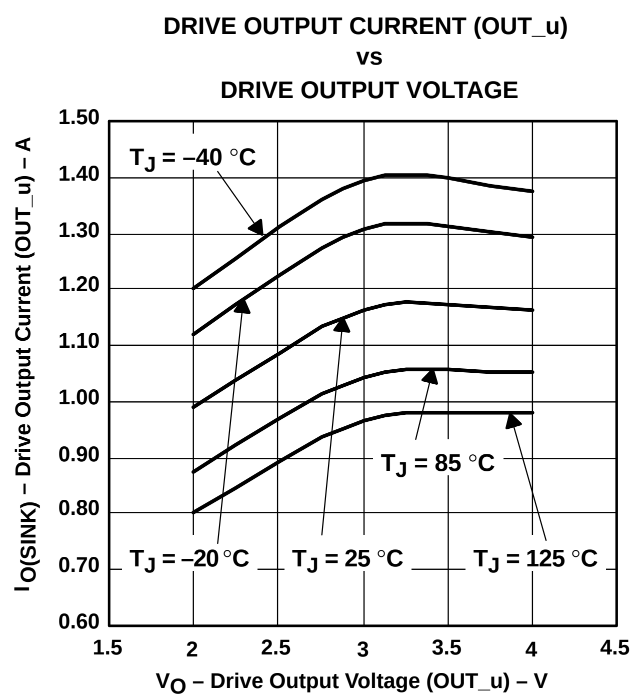


Figure 5

TYPICAL CHARACTERISTICS

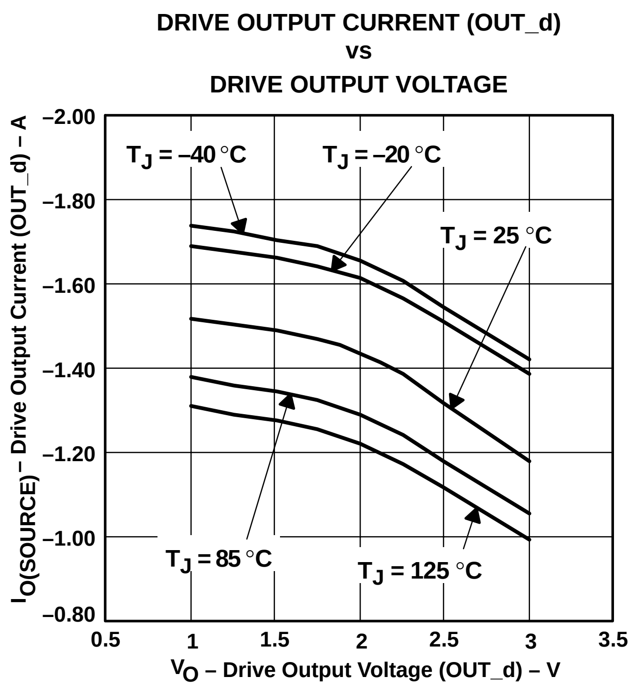


Figure 6

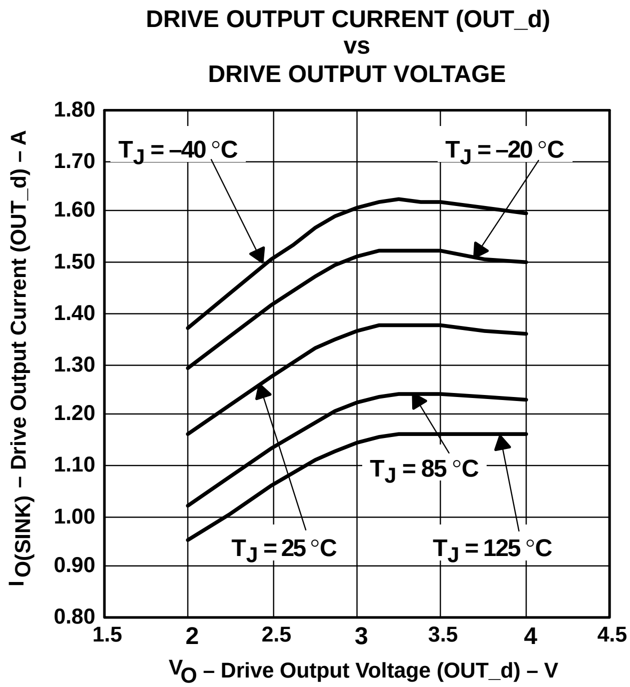


Figure 7

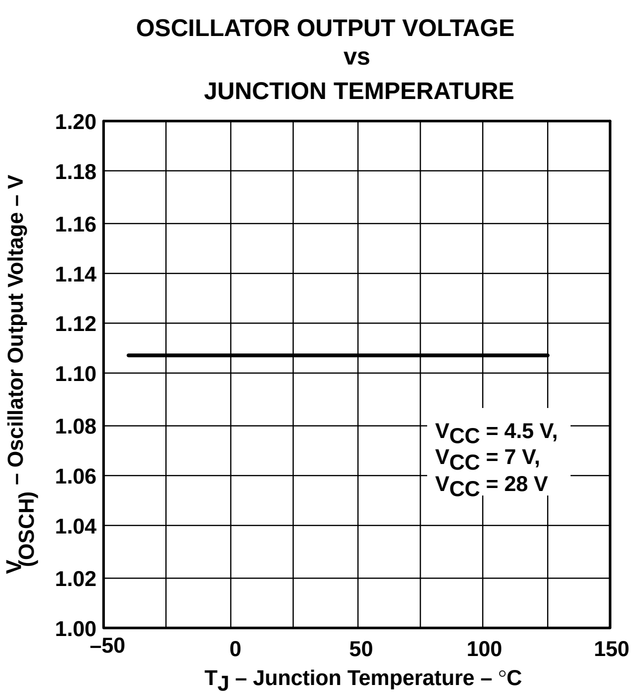


Figure 8

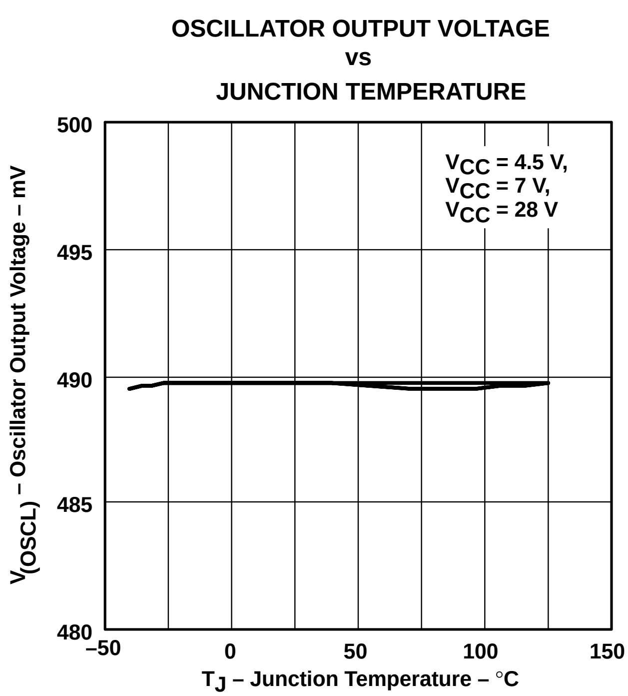


Figure 9

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER INPUT OFFSET VOLTAGE
vs
JUNCTION TEMPERATURE

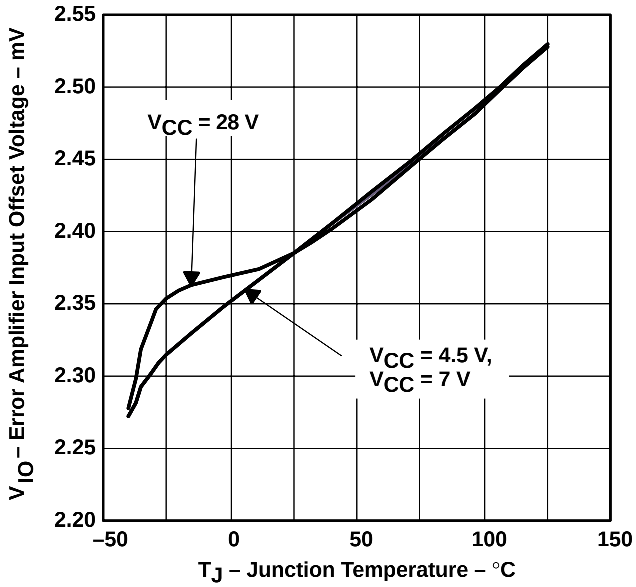


Figure 10

ERROR AMPLIFIER OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

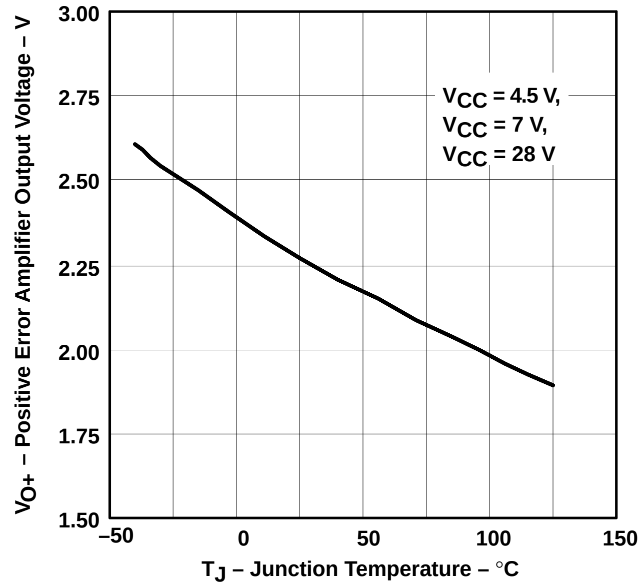


Figure 11

ERROR AMPLIFIER OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

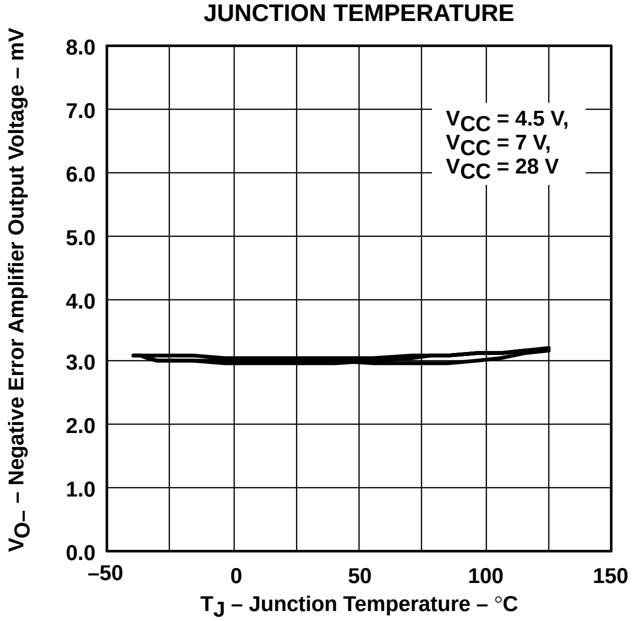


Figure 12

SKIP COMPARATOR HYSTERESIS VOLTAGE
vs
JUNCTION TEMPERATURE

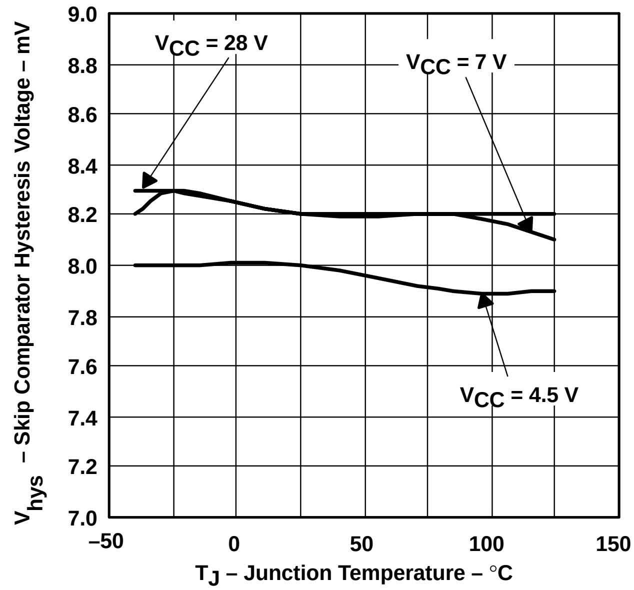


Figure 13

TYPICAL CHARACTERISTICS

VREF5 OUTPUT VOLTAGE vs OUTPUT CURRENT

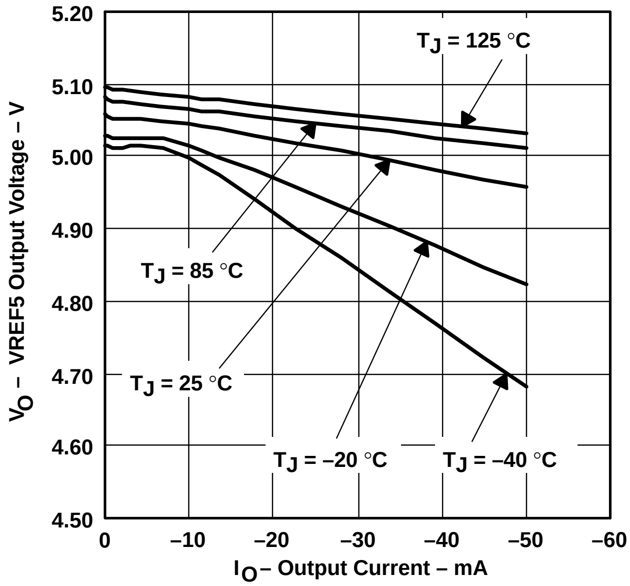


Figure 14

VREF5 SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE

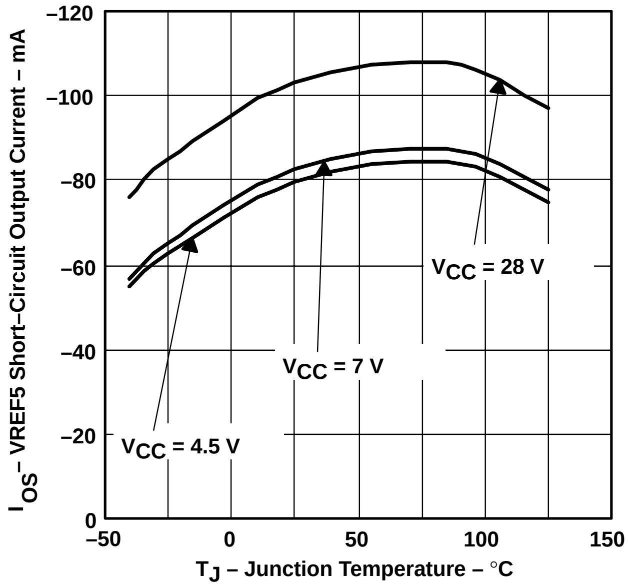


Figure 15

UVLO THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

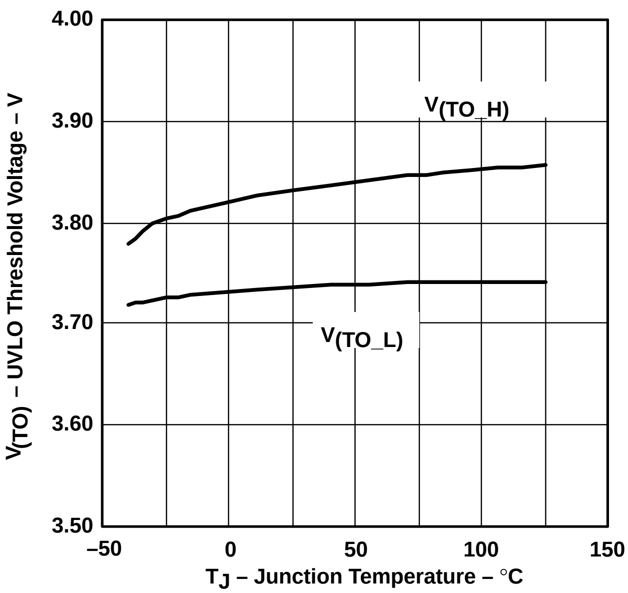


Figure 16

UVLO HYSTERESIS VOLTAGE vs JUNCTION TEMPERATURE

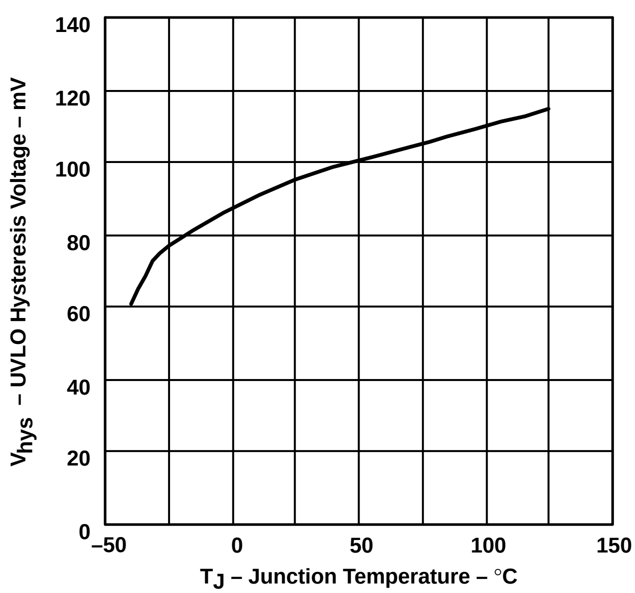


Figure 17

TYPICAL CHARACTERISTICS

REG5V_IN THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

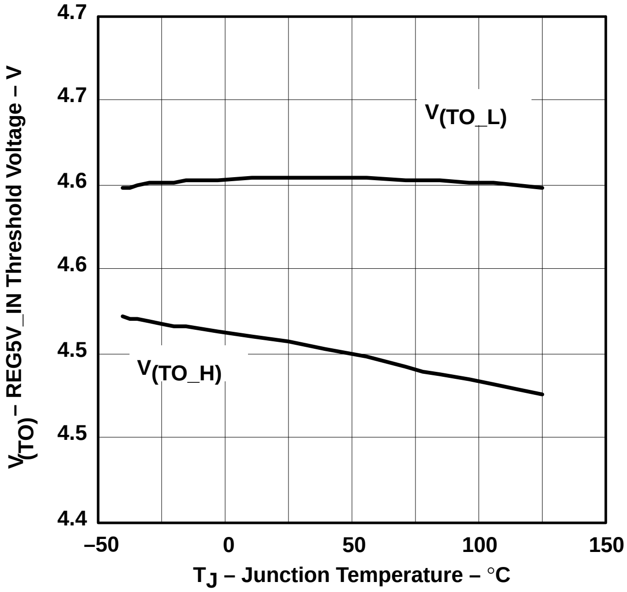


Figure 18

REG5V_IN HYSTERESIS VOLTAGE vs JUNCTION TEMPERATURE

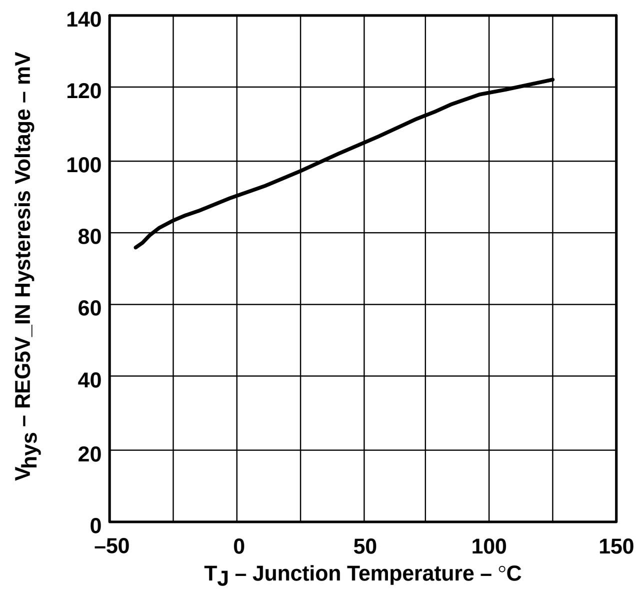


Figure 19

SOFTSTART CURRENT vs JUNCTION TEMPERATURE

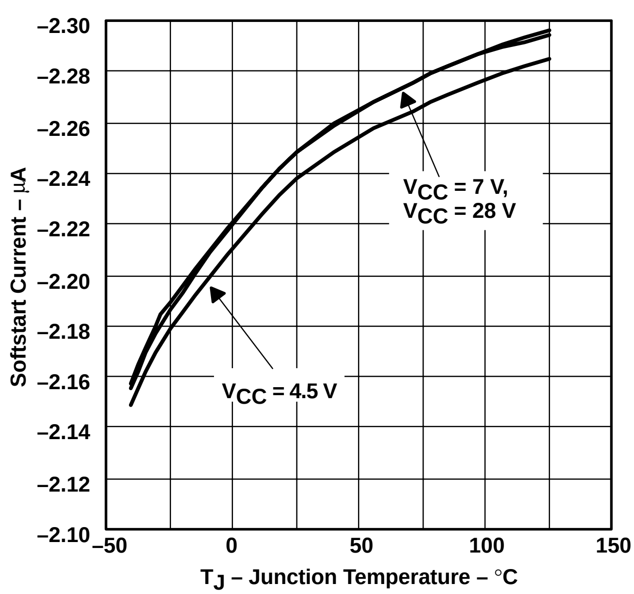


Figure 20

OVP THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

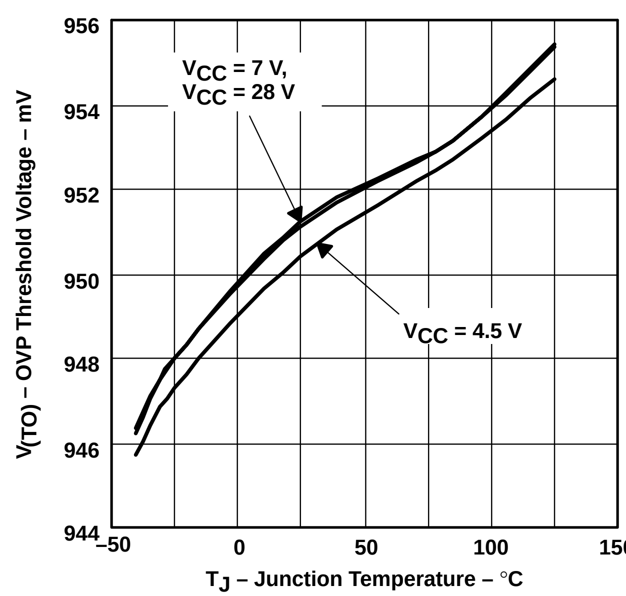


Figure 21

TYPICAL CHARACTERISTICS

POWERGOOD THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

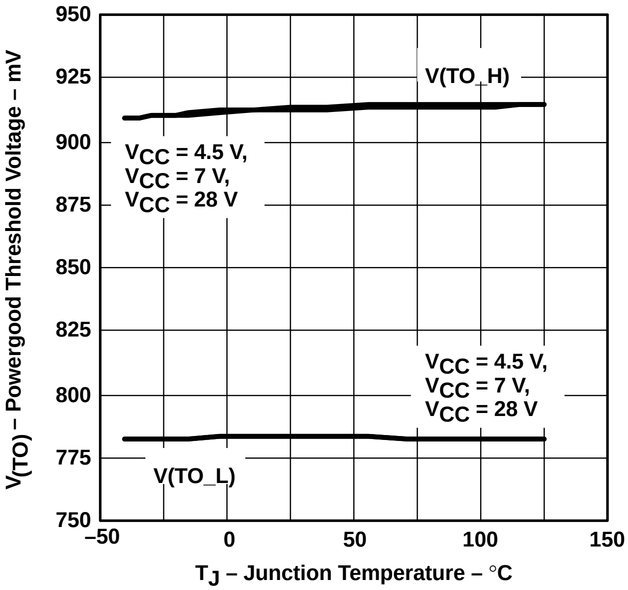


Figure 22

SCP (OVP) SOURCE CURRENT vs JUNCTION TEMPERATURE

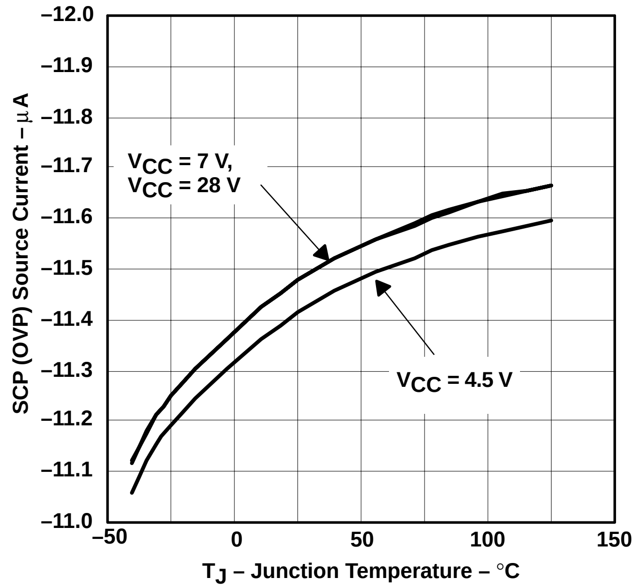


Figure 23

SCP (OVP) SOURCE CURRENT vs JUNCTION TEMPERATURE

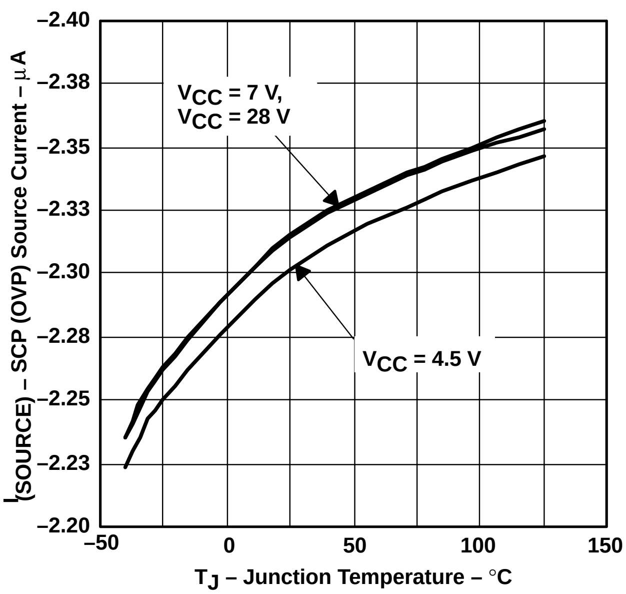


Figure 24

TRIP SINK CURRENT vs TRIP INPUT VOLTAGE

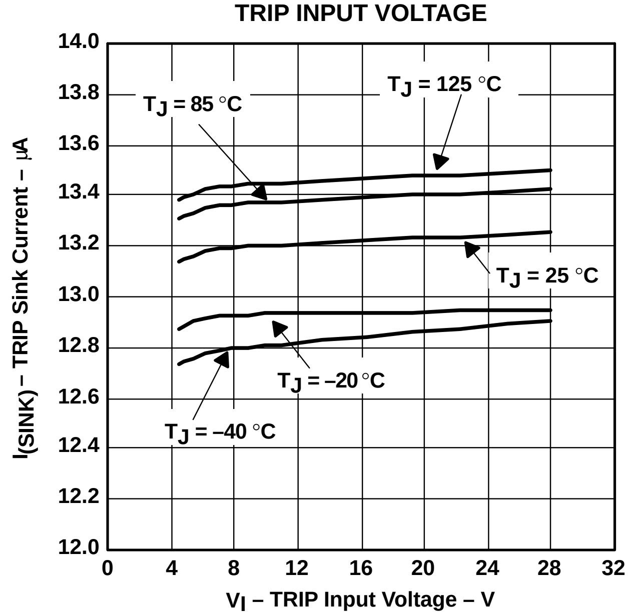


Figure 25

TYPICAL CHARACTERISTICS

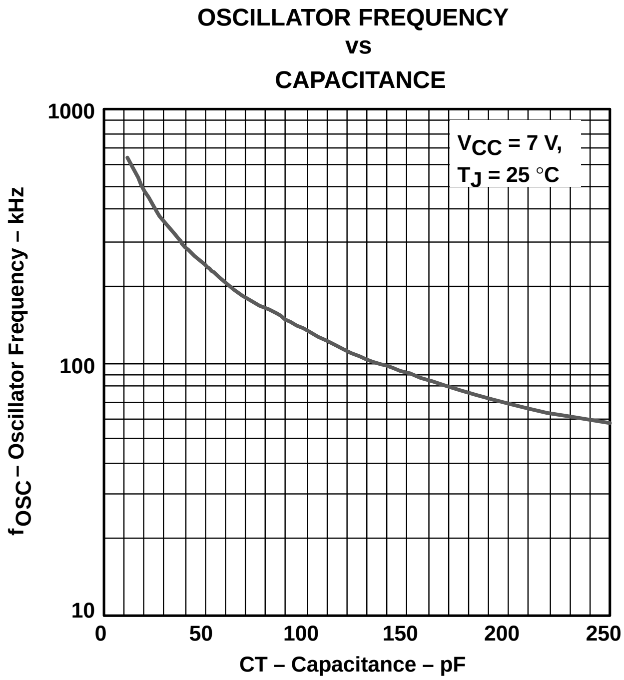


Figure 26

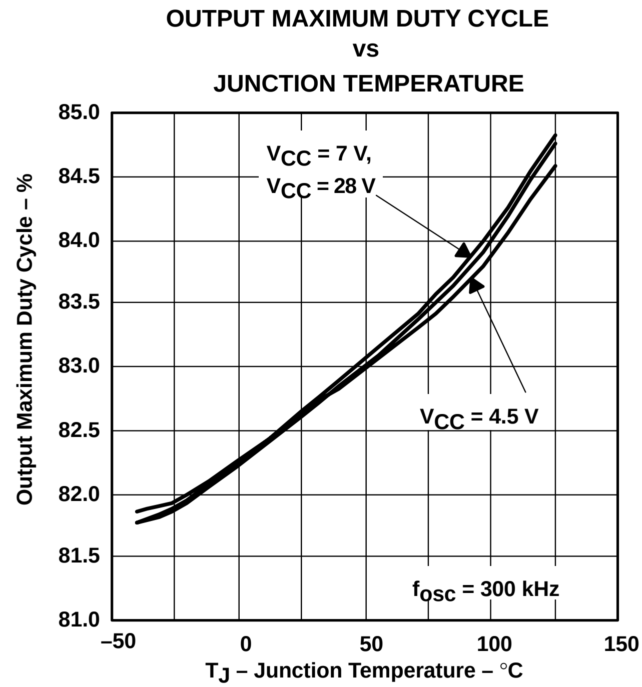


Figure 27

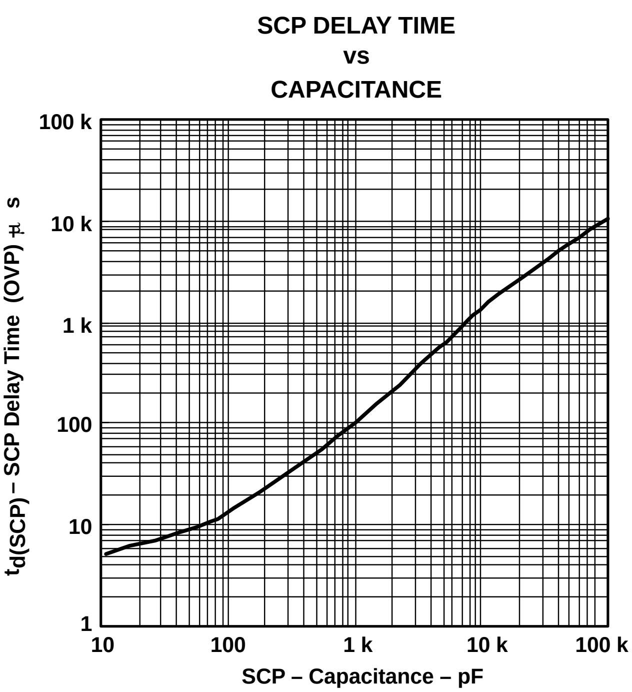


Figure 28

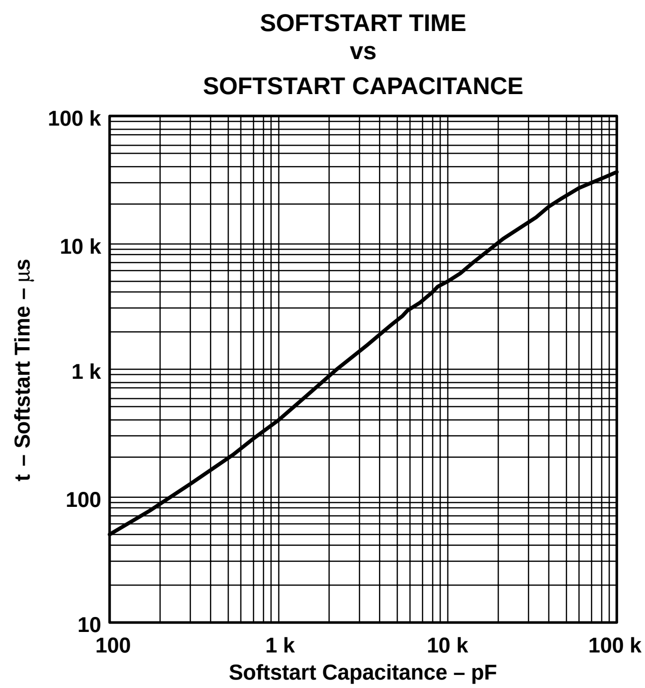


Figure 29

TYPICAL CHARACTERISTICS

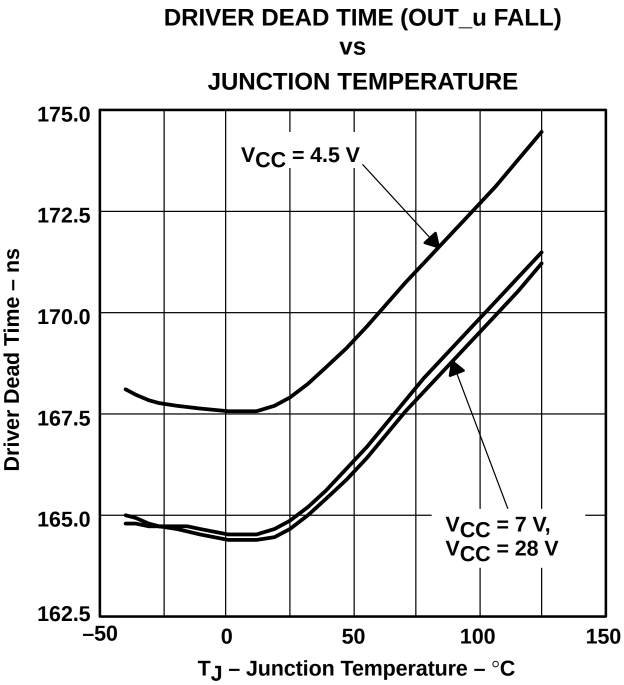


Figure 30

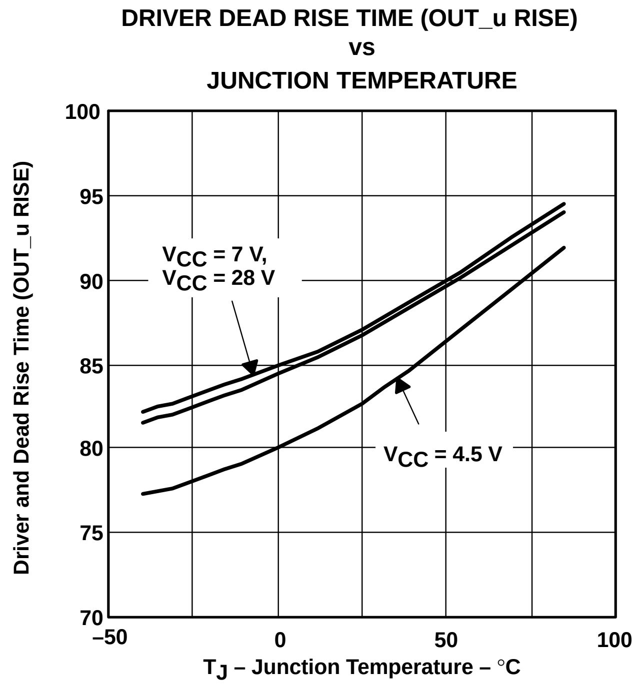


Figure 31

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS5120DBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS5120	Samples
TPS5120DBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS5120	Samples
TPS5120DBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS5120	Samples
TPS5120DBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PS5120	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS5120 :

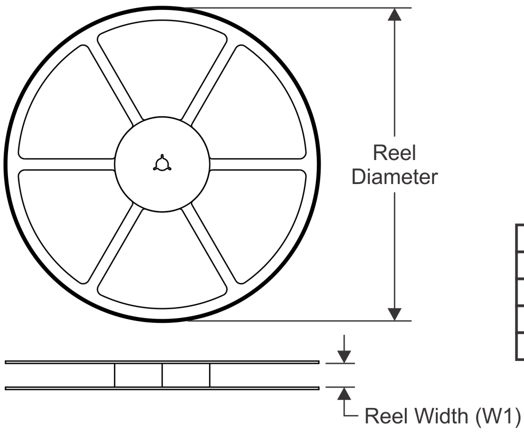
- Automotive: TPS5120-Q1
- Enhanced Product: TPS5120-EP

NOTE: Qualified Version Definitions:

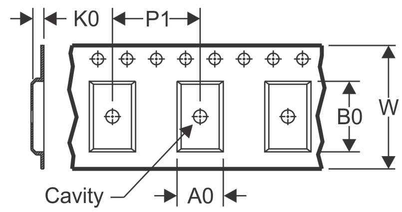
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

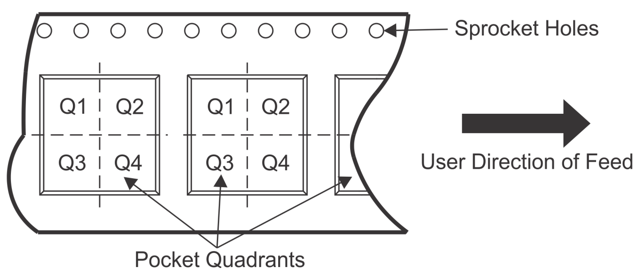


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

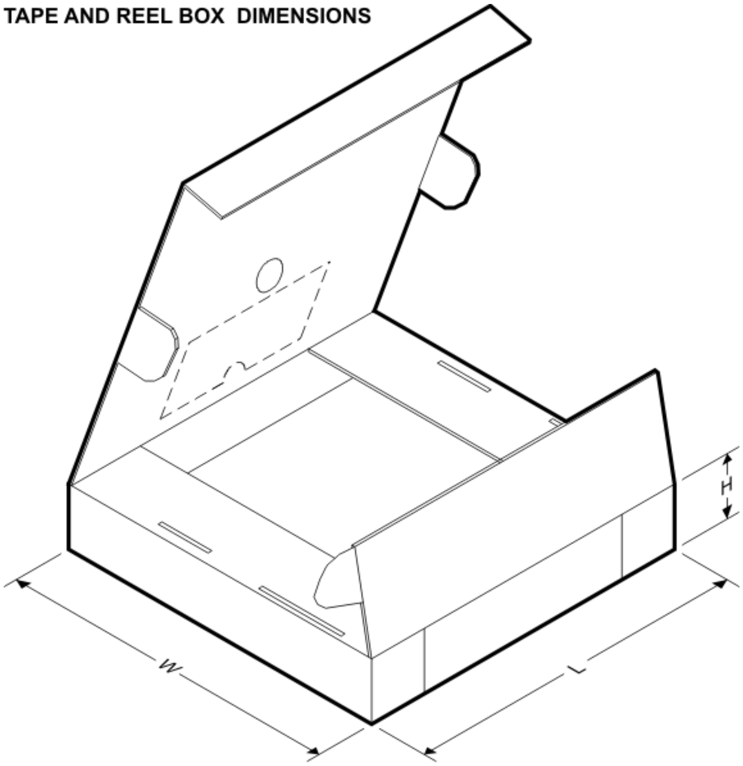
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS5120DBTR	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

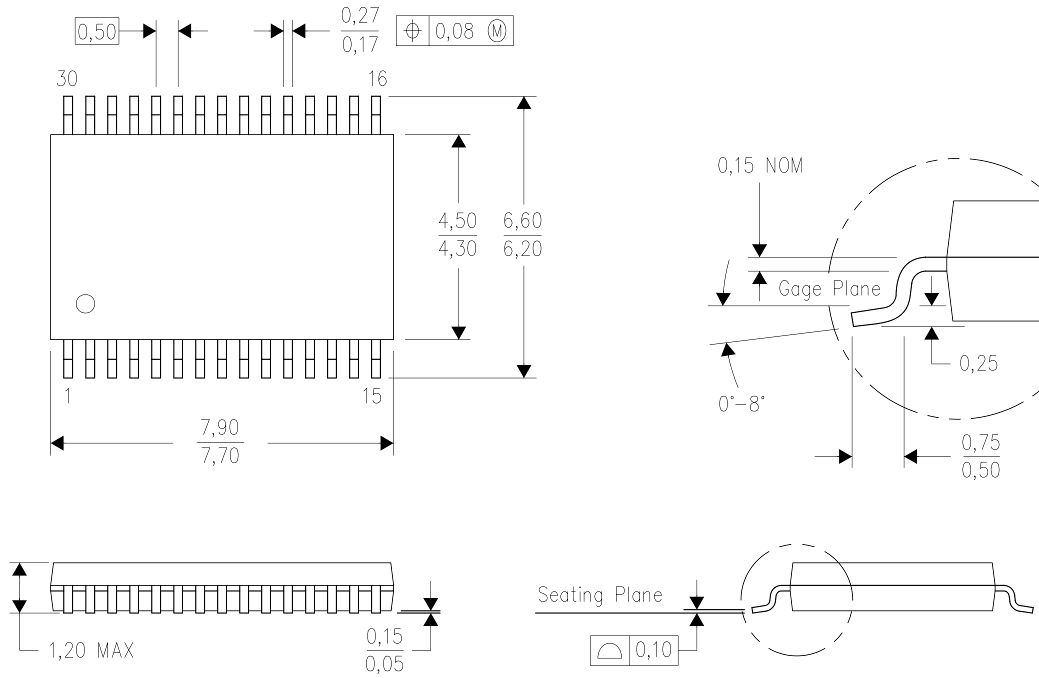
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS5120DBTR	TSSOP	DBT	30	2000	367.0	367.0	38.0

DBT (R-PDSO-G30) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153.