

# SN54LVTH374, SN74LVTH374 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS683H – MARCH 1997 – REVISED OCTOBER 2003

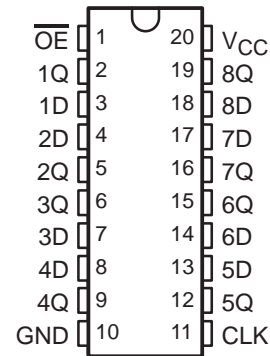
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Unregulated Battery Operation Down to 2.7 V
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

## description/ordering information

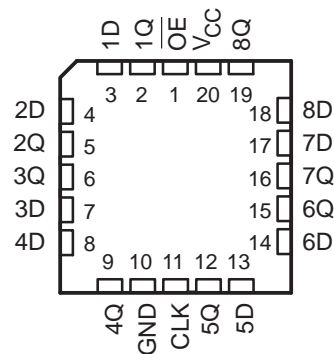
These octal flip-flops are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight flip-flops of the 'LVTH374 devices are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

SN54LVTH374 . . . J OR W PACKAGE  
SN74LVTH374 . . . DB, DW, NS, OR PW PACKAGE  
(TOP VIEW)



SN54LVTH374 . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74LVTH374DW	LVTH374
		Tape and reel	SN74LVTH374DWR	
	SOP – NS	Tape and reel	SN74LVTH374NSR	LVTH374
	SSOP – DB	Tape and reel	SN74LVTH374DBR	LXH374
	TSSOP – PW	Tube	SN74LVTH374PW	LXH374
		Tape and reel	SN74LVTH374PWR	
–55°C to 125°C	CDIP – J	Tube	SNJ54LVTH374J	SNJ54LVTH374J
	CFP – W	Tube	SNJ54LVTH374W	SNJ54LVTH374W
	LCCC – FK	Tube	SNJ54LVTH374FK	SNJ54LVTH374FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54LVTH374, SN74LVTH374

## 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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### description/ordering information (continued)

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

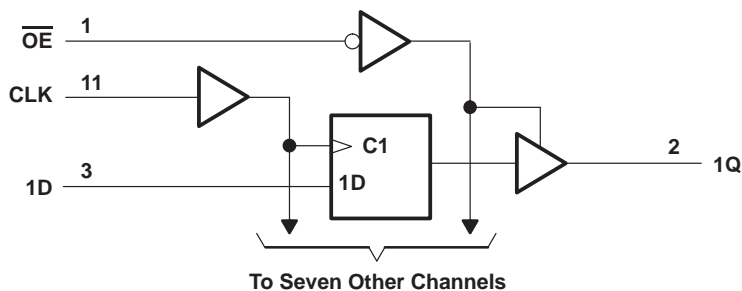
Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z

### logic diagram (positive logic)



# SN54LVTH374, SN74LVTH374 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_{OL}$ : SN54LVTH374 .....	96 mA
SN74LVTH374 .....	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH374 .....	48 mA
SN74LVTH374 .....	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package .....	70°C/W
DW package .....	58°C/W
NS package .....	60°C/W
PW package .....	83°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

	SN54LVTH374		SN74LVTH374		UNIT
	MIN	MAX	MIN	MAX	
$V_{CC}$ Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$ High-level input voltage	2		2		V
$V_{IL}$ Low-level input voltage		0.8		0.8	V
$V_I$ Input voltage		5.5		5.5	V
$I_{OH}$ High-level output current		–24		–32	mA
$I_{OL}$ Low-level output current		48		64	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$ Power-up ramp rate	200		200		μs/V
$T_A$ Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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## 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVTH374			SN74LVTH374			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ ,	$I_I = -18\text{ mA}$			-1.2			-1.2	V
$V_{OH}$	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$ ,	$I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$ ,	$I_{OH} = -8\text{ mA}$	2.4			2.4			
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2			2			
$V_{OL}$	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$			0.2			0.2	V
		$I_{OL} = 24\text{ mA}$			0.5			0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$			0.4			0.4	
		$I_{OL} = 32\text{ mA}$			0.5			0.5	
		$I_{OL} = 48\text{ mA}$			0.55			0.55	
		$I_{OL} = 64\text{ mA}$						0.55	
$I_I$	Control inputs	$V_{CC} = 0\text{ or }3.6\text{ V}$ ,	$V_I = 5.5\text{ V}$			10		10	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}$ ,	$V_I = V_{CC}\text{ or GND}$			$\pm 1$		$\pm 1$	
	Data inputs	$V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}$			1		1	
			$V_I = 0$			-5		-5	
$I_{off}$	$V_{CC} = 0$ ,	$V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$						$\pm 100$	$\mu\text{A}$
$I_I(\text{hold})$	Data inputs	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	75		75			$\mu\text{A}$
			$V_I = 2\text{ V}$	-75		-75			
		$V_{CC} = 3.6\text{ V}\ddagger$ ,	$V_I = 0\text{ to }3.6\text{ V}$					500	
$I_{OZH}$	$V_{CC} = 3.6\text{ V}$ ,	$V_O = 3\text{ V}$			5		5	$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 3.6\text{ V}$ ,	$V_O = 0.5\text{ V}$			-5		-5	$\mu\text{A}$	
$I_{OZPU}$	$V_{CC} = 0\text{ to }1.5\text{ V}$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $OE = \text{don't care}$				$\pm 100^*$		$\pm 100$	$\mu\text{A}$	
$I_{OZPD}$	$V_{CC} = 1.5\text{ V to }0$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $OE = \text{don't care}$				$\pm 100^*$		$\pm 100$	$\mu\text{A}$	
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$	Outputs high			0.19		0.19	mA	
		Outputs low			5		5		
		Outputs disabled			0.19		0.19		
$\Delta I_{CC}\S$	$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$				0.2		0.2	mA	
$C_i$	$V_I = 3\text{ V or }0$				3		3	pF	
$C_o$	$V_O = 3\text{ V or }0$				7		7	pF	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	SN54LVTH374				SN74LVTH374				UNIT
	V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub> Clock frequency	150		150		150		150		MHz
t <sub>w</sub> Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns
t <sub>su</sub> Setup time, data before CLK↑	1.6		2		1.5		2		ns
t <sub>h</sub> Hold time, data after CLK↑	0.8		0.5		0.8		0		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH374				SN74LVTH374				UNIT
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V	
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	
f <sub>max</sub>			150		150		150			150	MHz
t <sub>PLH</sub>	CLK	Q	1 5.1		5.6		1.8 2.9 4.5			5	ns
t <sub>PHL</sub>			1.5 5.1		5.2		1.8 2.9 4.2			4.3	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Q	0.8 5.6		6.6		1.3 2.8 4.7			5.6	ns
t <sub>PZL</sub>			1.2 5.4		6.2		1.6 3 4.7			5.2	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Q	1.5 5.6		5.7		1.9 3 4.6			4.9	ns
t <sub>PLZ</sub>			0.8 5.2		5.3		2 3.1 4.5			4.6	

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

# SN54LVTH374, SN74LVTH374

## 3.3-V ABT OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

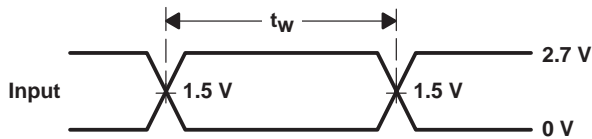
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### PARAMETER MEASUREMENT INFORMATION

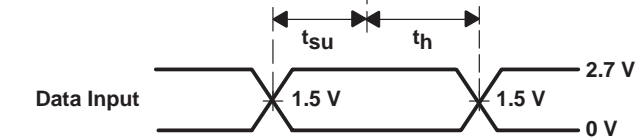
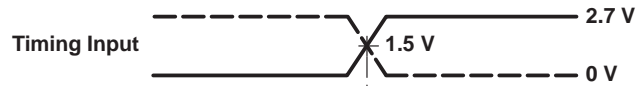


LOAD CIRCUIT

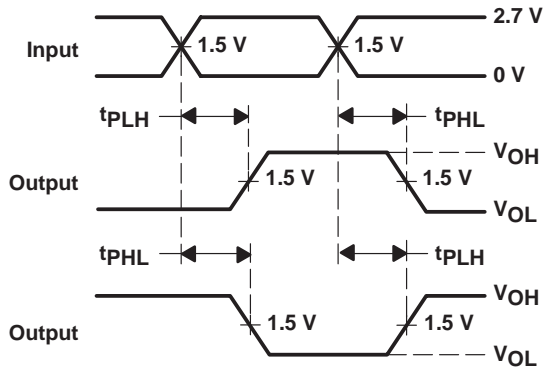
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



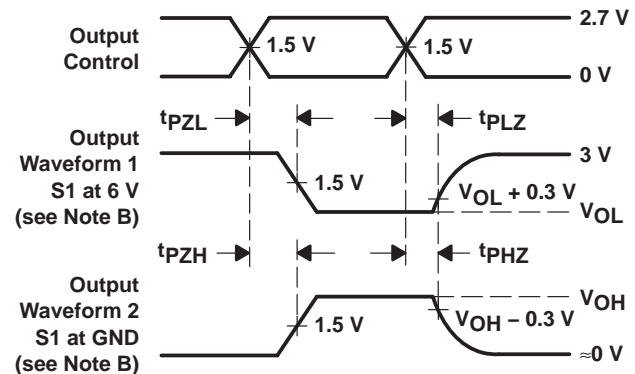
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9951001Q2A	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9951001Q2A SNJ54LVTH 374FK	
5962-9951001QRA	ACTIVE	CDIP	J	20		TBD	Call TI	Call TI	-55 to 125		<a href="#">Samples</a>
5962-9951001QSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9951001QS A SNJ54LVTH374W	<a href="#">Samples</a>
SN74LVTH374DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85		
SN74LVTH374DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH374	<a href="#">Samples</a>
SN74LVTH374DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH374	<a href="#">Samples</a>
SN74LVTH374DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH374	<a href="#">Samples</a>
SN74LVTH374DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH374	<a href="#">Samples</a>
SN74LVTH374DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH374	<a href="#">Samples</a>
SN74LVTH374NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH374	<a href="#">Samples</a>
SN74LVTH374PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH374	<a href="#">Samples</a>
SN74LVTH374PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
SN74LVTH374PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LXH374	<a href="#">Samples</a>
SNJ54LVTH374FK	NRND	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9951001Q2A SNJ54LVTH 374FK	
SNJ54LVTH374W	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9951001QS A SNJ54LVTH374W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54LVTH374, SN74LVTH374 :**

● Catalog: [SN74LVTH374](#)

● Enhanced Product: [SN74LVTH374-EP](#), [SN74LVTH374-EP](#)



- Military: [SN54LVTH374](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH374DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVTH374DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LVTH374NSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LVTH374PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH374DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LVTH374DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVTH374NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LVTH374PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.





PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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