

DUAL 4-CHANNEL ANALOG MULTIPLEXERS/DEMULIPLEXERS

 Check for Samples: [SN54LV4052A](#) , [SN74LV4052A](#)

FEATURES

- 2-V to 5.5-V V_{CC} Operation
- Fast Switching
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Extremely Low Input Current
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

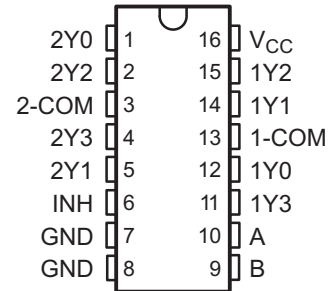
DESCRIPTION

These dual 4-channel CMOS analog multiplexers/demultiplexers are designed for 2-V to 5.5-V V_{CC} operation.

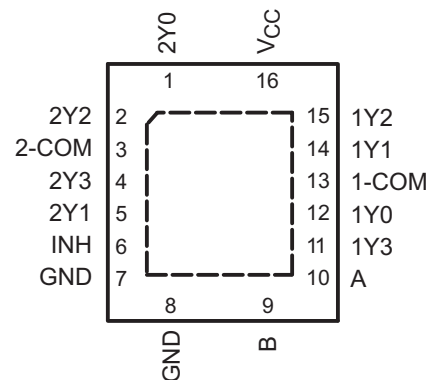
The 'LV4052A devices handle both analog and digital signals. Each channel permits signals with amplitudes up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

SN54LV4052A . . . JO R W PACKAGE
SN74LV4052A . . . D, DB, DGV, N, NS, OR, PW PACKAGE
(TOP VIEW)



SN74LV4052A . . . RGY PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP - N	Tube of 25	SN74LV4052AN	SN74LV4052AN
	QFN - RGY	Reel of 1000	SN74LV4052ARGYR	LW052A
	SOIC - D	Tube of 40	SN74LV4052AD	LV4052A
		Reel of 2500	SN74LV4052ADRG3	
	SOP - NS	Reel of 2000	SN74LV4052ANSR	74LV4052A
	SSOP - DB	Reel of 2000	SN74LV4052ADBR	LW052A
	TSSOP - PW	Tube of 90	SN74LV4052APW	LW052A
		Reel of 2000	SN74LV4052APWR	
Reel of 250		SN74LV4052APWT		
TVSOP - DGV	Reel of 2000	SN74LV4052ADGVR	LW052A	
-55°C to 125°C	CDIP - J	Tube of 25	SNJ54LV4052AJ	SNJ54LV4052AJ
	CFP - W	Tube of 150	SNJ54LV4052AW	SNJ54LV4052AW

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

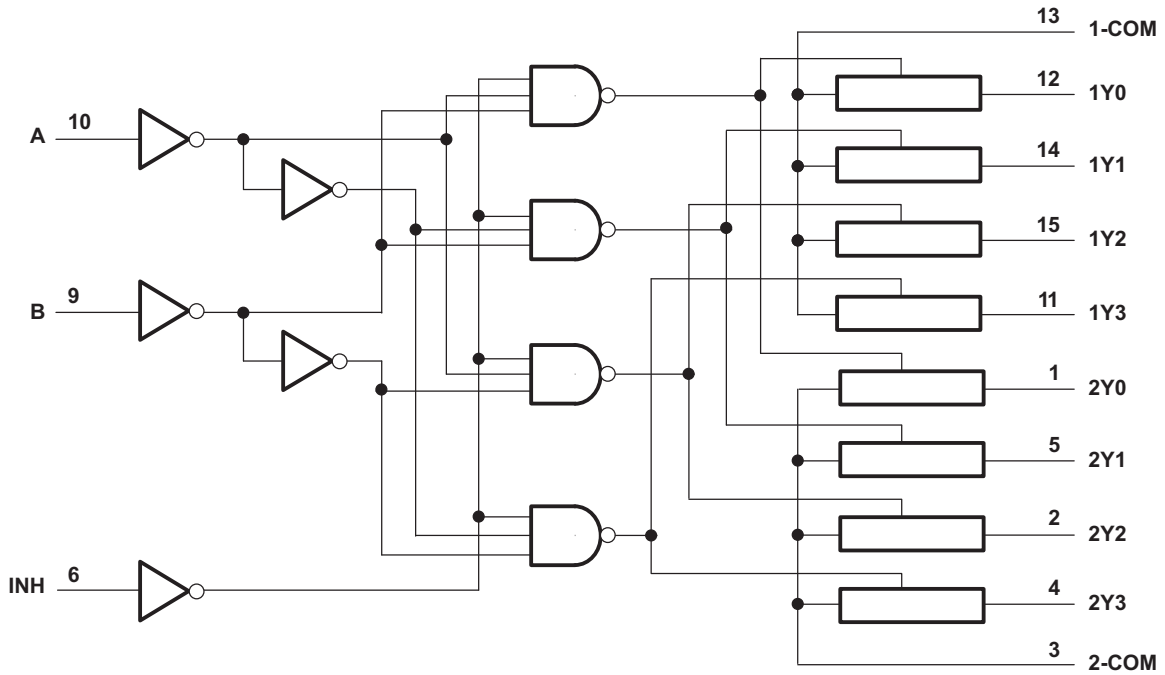


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLE

INPUTS			ON CHANNEL
INH	B	A	
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		VALUE	UNIT
Supply voltage range, V_{CC}		–0.5 to 7.0	V
Input voltage range, V_I ⁽²⁾		–0.5 to 7.0	V
Switch I/O voltage range, V_{IO} ⁽²⁾⁽³⁾		–0.5 to $V_{CC} + 0.5$	V
Input clamp current, I_{IK} ($V_I < 0$)		–20	mA
I/O diode current, I_{IOK} ($V_{IO} < 0$)		–50	mA
Switch through current, I_T ($V_{IO} = 0$ to V_{CC})		±25	mA
Continuous current through VCC or GND		±50	mA
Package thermal impedance, θ_{JA}	D package ⁽⁴⁾	73	°C/W
	DB package ⁽⁴⁾	82	
	DGV package ⁽⁴⁾	120	
	N package ⁽⁴⁾	67	
	NS package ⁽⁴⁾	64	
	PW package ⁽⁴⁾	108	
	RGY package ⁽⁵⁾	39	
Storage temperature range, T_{stg}		–65 to 150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS (see ⁽¹⁾)

		SN54LV4052A ⁽²⁾		SN74LV4052A		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2 ⁽³⁾	5.5	2 ⁽³⁾	5.5	V
V_{IH}	High-level input voltage, control inputs	$V_{CC} = 2$ V	1.5	1.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage, control inputs	$V_{CC} = 2$ V		0.5	0.5	V
		$V_{CC} = 2.3$ V to 2.7 V		$V_{CC} \times 0.3$	$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V		$V_{CC} \times 0.3$	$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V		$V_{CC} \times 0.3$	$V_{CC} \times 0.3$	
V_I	Control input voltage	0	5.5	0	5.5	V
V_{IO}	Input/output voltage	0	V_{CC}	0	V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V		200	200	ns/V
		$V_{CC} = 3$ V to 3.6 V		100	100	
		$V_{CC} = 4.5$ V to 5.5 V		20	20	
T_A	Operating free-air temperature	–55	125	–40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Product Preview
- (3) With supply voltages at or near 2 V, the analog switch on-state resistance becomes very nonlinear. It is recommended that only digital signals be transmitted at these low supply voltages.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54LV4052A ⁽¹⁾		SN74LV4052A		UNIT	
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
r _{on}	On-state switch resistance I _T = 2 mA, , V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 1)	2.3 V		43	180		225		225	Ω	
		3 V		34	150		190		190		
		4.5 V		25	75		100		100		
r _{on(p)}	Peak on-state resistance I _T = 2 mA, V _I = V _{CC} to GND, V _{INH} = V _{IL}	2.3 V		133	500		600		600	Ω	
		3 V		63	180		225		225		
		4.5 V		35	100		125		125		
Δr _{on}	Difference in on-state resistance between switches I _T = 2 mA, V _I = V _{CC} to GND, V _{INH} = V _{IL}	2.3 V		1.5	30		40		40	Ω	
		3 V		1.1	20		30		30		
		4.5 V		0.7	15		20		20		
I _I	Control input current	V _I = 5.5 V or GND	0 to 5.5 V			±0.1		±1		±1	μA
I _{S(off)}	Off-state switch leakage current	V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH} (see Figure 2)	5.5 V			±0.1		±1		±1	μA
I _{S(on)}	On-state switch leakage current	V _I = V _{CC} or GND, V _{INH} = V _{IL} (see Figure 3)	5.5 V			±0.1		±1		±1	μA
I _{CC}	Supply current	V _I = V _{CC} or GND	5.5 V					20		20	μA
C _{IC}	Control input capacitance	f = 10 MHz	3.3 V			2.1					pF
C _{IS}	Common terminal capacitance		3.3 V			13.1					pF
C _{OS}	Switch terminal capacitance		3.3 V			5.6					pF
C _F	Feedthrough capacitance		3.3 V			0.5					pF

(1) Product Preview

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54LV4052A ⁽¹⁾		SN74LV4052A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	$C_L = 15\text{ pF}$, (see Figure 4)				16		16	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	$C_L = 15\text{ pF}$, (see Figure 5)				23		23	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	$C_L = 15\text{ pF}$, (see Figure 5)				23		23	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	$C_L = 50\text{ pF}$, (see Figure 4)				18		18	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	$C_L = 50\text{ pF}$, (see Figure 5)				35		35	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	$C_L = 50\text{ pF}$, (see Figure 5)				35		35	ns

(1) Product Preview

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54LV4052A ⁽¹⁾		SN74LV4052A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	$C_L = 15\text{ pF}$, (see Figure 4)				10		10	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	$C_L = 15\text{ pF}$, (see Figure 5)				15		15	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	$C_L = 15\text{ pF}$, (see Figure 5)				15		15	ns
t_{PLH} t_{PHL}	Propagation delay time	COM or Y	Y or COM	$C_L = 50\text{ pF}$, (see Figure 4)				12		12	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Y	$C_L = 50\text{ pF}$, (see Figure 5)				25		25	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Y	$C_L = 50\text{ pF}$, (see Figure 5)				25		25	ns

(1) Product Preview

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54LV4052A ⁽¹⁾		SN74LV4052A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL} Propagation delay time	COM or Y	Y or COM	$C_L = 15\text{ pF}$, (see Figure 4)		0.7	4		7		7	ns
t_{PZH} t_{PZL} Enable delay time	INH	COM or Y	$C_L = 15\text{ pF}$, (see Figure 5)		4	8		10		10	ns
t_{PHZ} t_{PLZ} Disable delay time	INH	COM or Y	$C_L = 15\text{ pF}$, (see Figure 5)		5	8		10		10	ns
t_{PLH} t_{PHL} Propagation delay time	COM or Y	Y or COM	$C_L = 50\text{ pF}$, (see Figure 4)		1.5	6		8		8	ns
t_{PZH} t_{PZL} Enable delay time	INH	COM or Y	$C_L = 50\text{ pF}$, (see Figure 5)		4.7	14		18		18	ns
t_{PHZ} t_{PLZ} Disable delay time	INH	COM or Y	$C_L = 50\text{ pF}$, (see Figure 5)		6.9	14		18		18	ns

(1) Product Preview

ANALOG SWITCH CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Y	Y or COM	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see ⁽¹⁾ and Figure 6)	2.3 V		30		MHz
				3 V		35		
				4.5 V		50		
Crosstalk (between any switches)	COM or Y	Y or COM	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see ⁽²⁾ and Figure 7)	2.3 V		-45		dB
				3 V		-45		
				4.5 V		-45		
Crosstalk (control input to signal output)	INH	COM or Y	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see Figure 8)	2.3 V		20		mV
				3 V		35		
				4.5 V		65		
Feedthrough attenuation (switch off)	COM or Y	Y or COM	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $f_{in} = 1\text{ MHz}$ (sine wave) (see ⁽²⁾ and Figure 9)	2.3 V		-45		dB
				3 V		-45		
				4.5 V		-45		
Sine-wave distortion	COM or Y	Y or COM	$C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, $f_{in} = 1\text{ kHz}$ (sine wave) (see Figure 10)	$V_I = 2\text{ V}_{p-p}$	2.3 V		0.1	%
				$V_I = 2.5\text{ V}_{p-p}$	3 V		0.1	
				$V_I = 4\text{ V}_{p-p}$	4.5 V		0.1	

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads -3 dB.

(2) Adjust f_{in} voltage to obtain 0 dBm at input.

OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	11.8	pF

PARAMETER MEASUREMENT INFORMATION

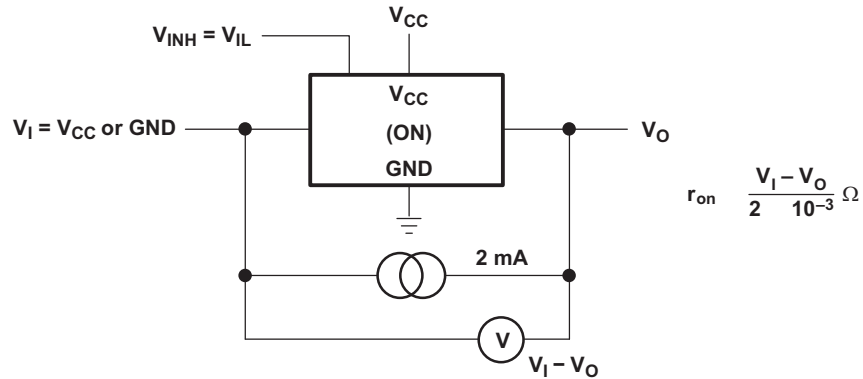


Figure 1. On-State Resistance Test Circuit

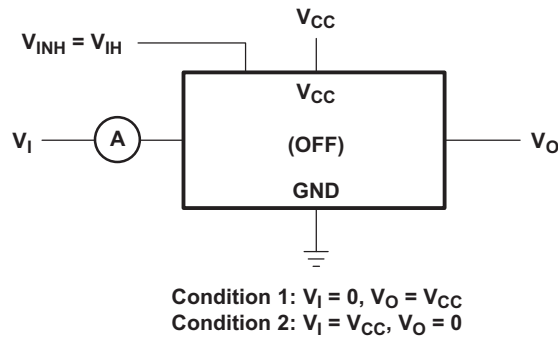


Figure 2. Off-State Switch Leakage-Current Test Circuit

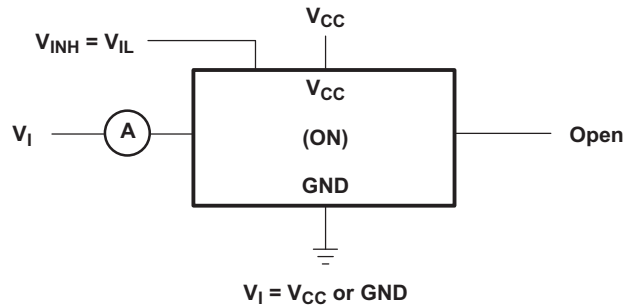


Figure 3. On-State Switch Leakage-Current Test Circuit

PARAMETER MEASUREMENT INFORMATION

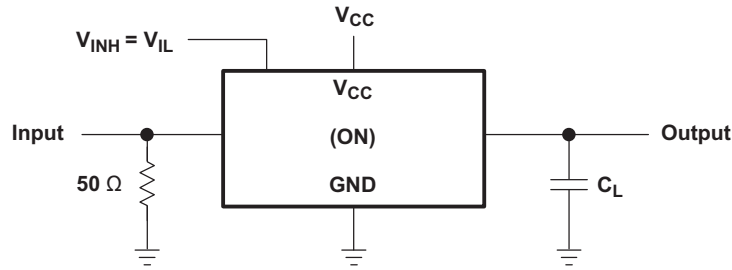
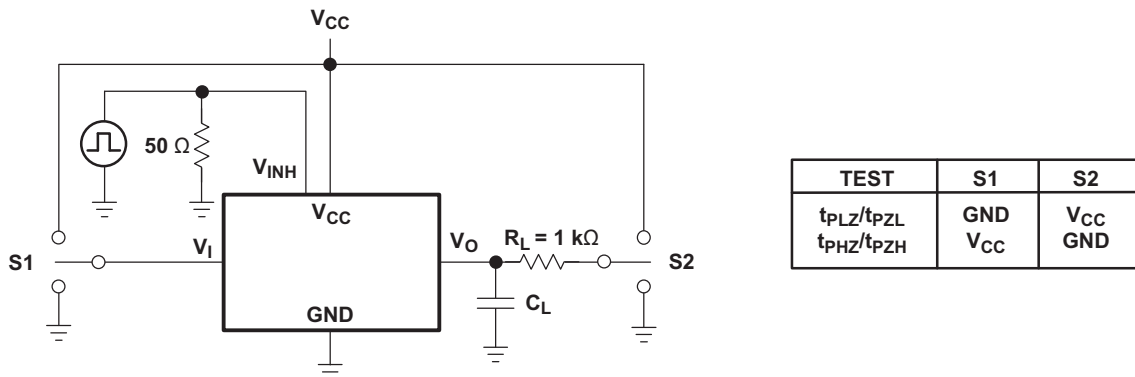
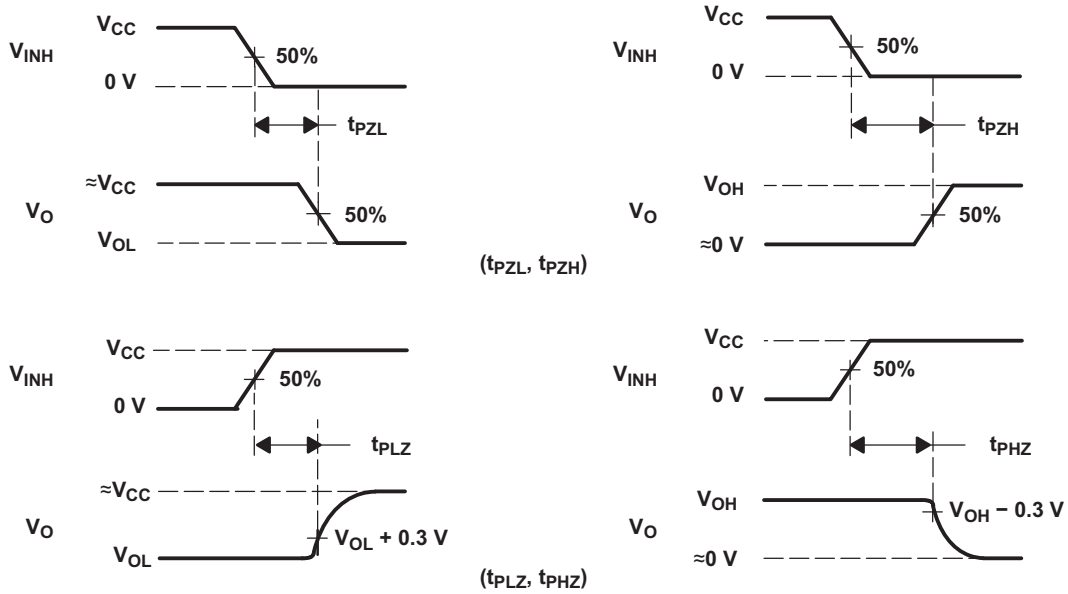


Figure 4. Propagation Delay Time, Signal Input to Signal Output



TEST	S1	S2
t_{PLZ}/t_{PZL}	GND	V_{CC}
t_{PHZ}/t_{PZH}	V_{CC}	GND

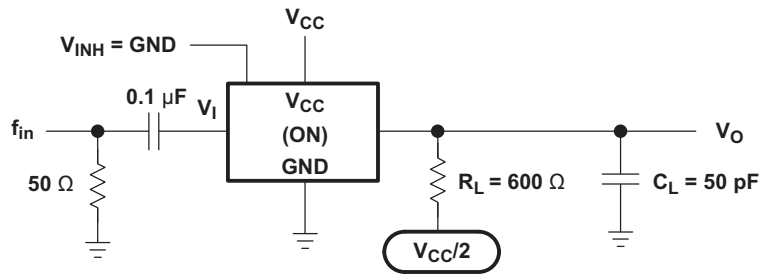
TEST CIRCUIT



VOLTAGE WAVEFORMS

Figure 5. Switching Time (t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}), Control to Signal Output

PARAMETER MEASUREMENT INFORMATION



NOTE A: f_{in} is a sine wave.

Figure 6. Frequency Response (Switch On)

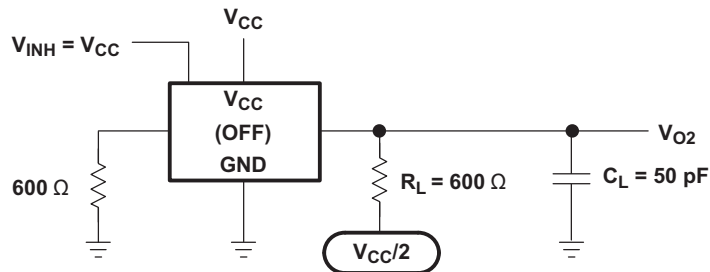
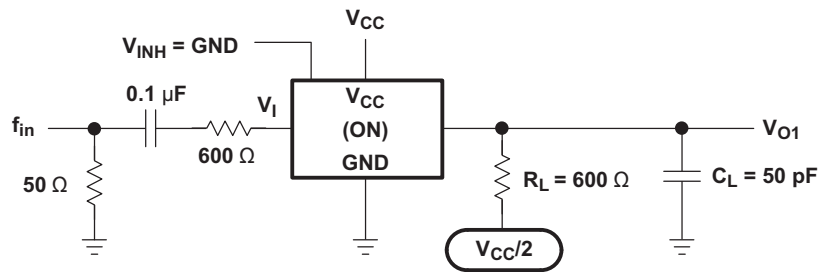


Figure 7. Crosstalk Between Any Two Switches

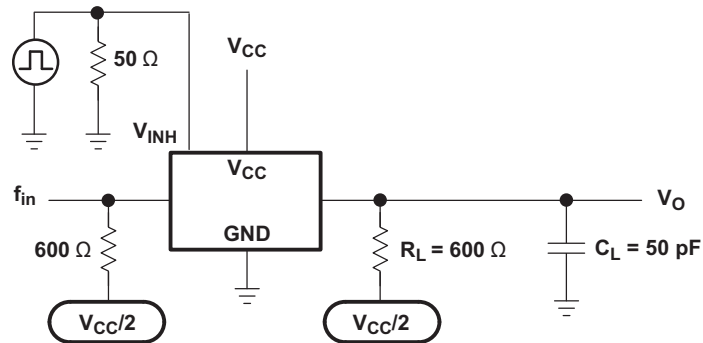


Figure 8. Crosstalk Between Control Input and Switch Output

PARAMETER MEASUREMENT INFORMATION (continued)
PARAMETER MEASUREMENT INFORMATION

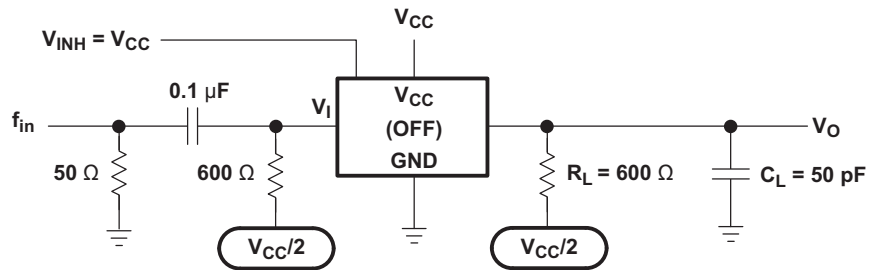


Figure 9. Feedthrough Attenuation (Switch Off)

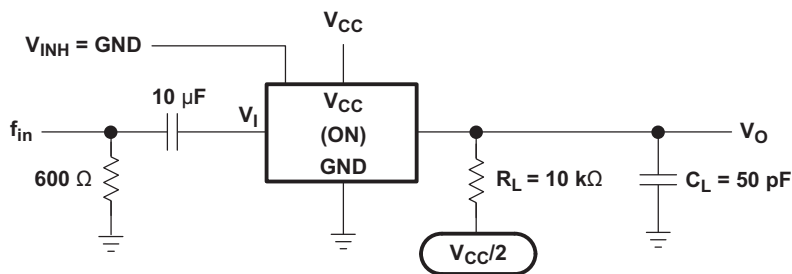


Figure 10. Sine-Wave Distortion

REVISION HISTORY

Changes from Original (January 2011) to Revision J	Page
• Updated ORDERING INFORMATION table.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV4052AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4052A	Samples
SN74LV4052ADBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052ADBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052ADG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV4052A	Samples
SN74LV4052ADGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	LV4052A	Samples
SN74LV4052ADRE4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85		
SN74LV4052ADRG4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	LV4052A	
SN74LV4052AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74LV4052AN	Samples
SN74LV4052ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV4052A	Samples
SN74LV4052APW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052APWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052APWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052APWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052APWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052APWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052APWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LW052A	Samples
SN74LV4052ARGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LW052A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LV4052A :

● Automotive: [SN74LV4052A-Q1](#)

● Enhanced Product: [SN74LV4052A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4052ADBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV4052ADGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV4052ADR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4052ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV4052ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV4052APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4052APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4052APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4052APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4052ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4052ADBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74LV4052ADGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74LV4052ADR	SOIC	D	16	2500	364.0	364.0	27.0
SN74LV4052ADR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LV4052ANSR	SO	NS	16	2000	367.0	367.0	38.0
SN74LV4052APWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74LV4052APWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV4052APWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74LV4052APWT	TSSOP	PW	16	250	367.0	367.0	35.0
SN74LV4052ARGYR	VQFN	RGY	16	3000	367.0	367.0	35.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

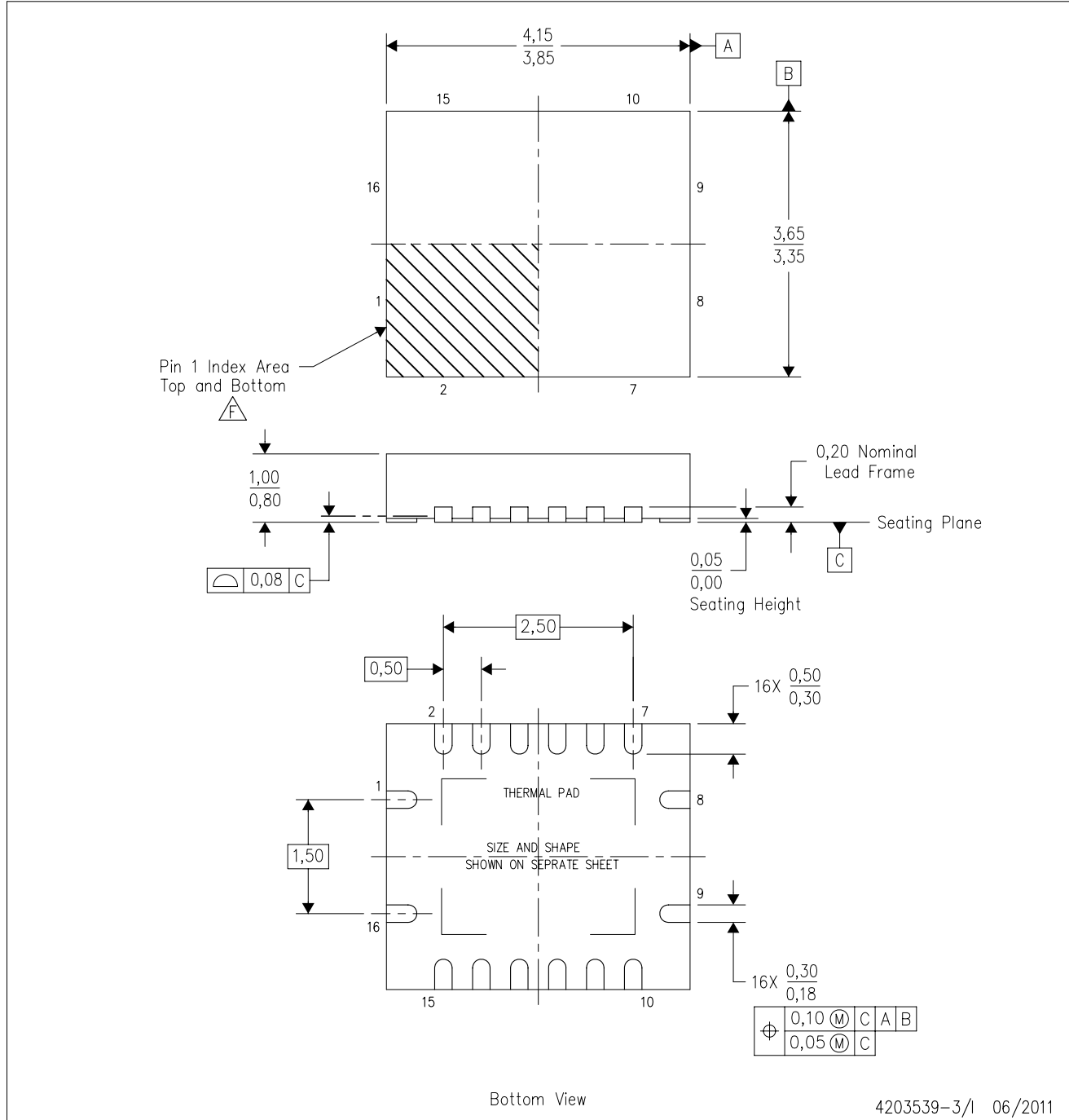
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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