1.8-V, *micro*Power, CMOS Operational Amplifiers, Zero-Drift Series

Check for Samples: OPA333, OPA2333

FEATURES

- **Low Offset Voltage: 10 µV (max)**
- **Zero Drift: 0.05 µV/°C (max)**
- **0.01-Hz to 10-Hz Noise: 1.1 μV_{PP}**
- **Quiescent Current: 17 µA**
- **Single-Supply Operation**
- **Supply Voltage: 1.8 V to 5.5 V**
- **Rail-to-Rail Input/Output**
- ***micro*Size Packages: SC70 and SOT23**

APPLICATIONS

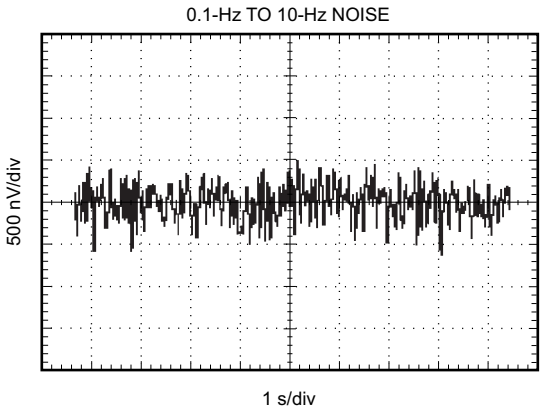
- **Transducers**
- **Temperature Measurements**
- **Electronic Scales**
- **Medical Instrumentation**
- **Battery-Powered Instruments**
- **Handheld Test Equipment**

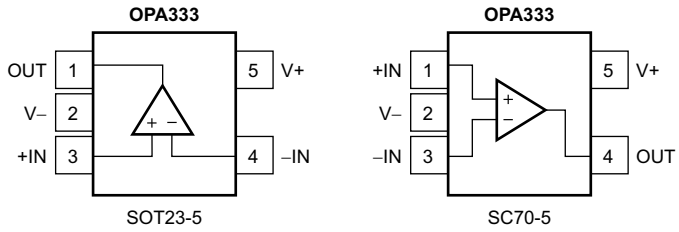
DESCRIPTION

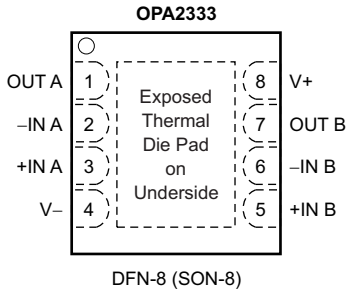
The OPA333 series of CMOS operational amplifiers use a proprietary auto-calibration technique to simultaneously provide very low offset voltage (10 µV, max) and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the rails, and rail-to-rail output that swings within 50 mV of the rails. Single or dual supplies as low as +1.8 V (±0.9 V) and up to +5.5 V (±2.75 V) can be used. These devices are optimized for low-voltage, single-supply operation.

The OPA333 family offers excellent CMRR without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity.

The OPA333 (single version) is available in the SC70-5, SOT23-5, and SO-8 packages. The OPA2333 (dual version) is offered in DFN-8 (3 mm × 3 mm), MSOP-8, and SO-8 packages. All versions are specified for operation from –40°C to +125°C.







This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
Voltage	Supply	+7	V
	Signal input terminals(2)	–0.3 to (V+) + 0.3	V
Curent	Signal input terminals(2)	±10	mA
	Output short-circuit(3)	Continuous	mA
Temperature	Operating, T_A	–40 to +150	°C
	Storage, T_{stg}	–65 to +150	°C
	Junction, T_J	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)	4000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	400	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V

At T_A = +25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = +5 V		2	10	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C		0.02	0.05	µV/°C
PSRR	Power-supply rejection ratio	V_S = +1.8 V to +5.5 V, T_A = –40°C to +125°C		1	5	µV/V
	Long-term stability(1)			See note (1)		µV
	Channel separation, dc			0.1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±70	±200	pA
		T_A = –40°C to +125°C		±150		pA
I_{OS}	Input offset current			±140	±400	pA
NOISE						
	Input voltage noise	f = 0.01 Hz to 1 Hz		0.3		μV_{PP}
		f = 0.1 Hz to 10 Hz		1.1		μV_{PP}
i_n	Input current noise	f = 10 Hz		100		$fA/\sqrt{Hz}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, T_A = –40°C to +125°C	106	130		dB
INPUT CAPACITANCE						
	Differential			2		pF
	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 10 kΩ, T_A = –40°C to +125°C	106	130		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	C_L = 100 pF		350		kHz
SR	Slew rate	G = +1		0.16		V/µs
OUTPUT						
	Voltage output swing from rail	R_L = 10 kΩ		30	50	mV
		R_L = 10 kΩ, T_A = –40°C to +125°C			70	mV
I_{SC}	Short-circuit current			±5		mA
C_L	Capacitive load drive			See Typical Characteristics		
	Open-loop output impedance	f = 350 kHz, I_O = 0 A		2		kΩ
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	I_O = 0 A		17	25	µA
		T_A = –40°C to +125°C			28	µA
	Turn-on time	V_S = +5 V		100		µs
TEMPERATURE						
T_A	Specified range		–40		+125	°C
	Operating range		–40		+150	°C
T_{stg}	Storage range		–65		+150	°C

(1) 300-hour life test at +150°C demonstrated randomly distributed variation of approximately 1 µV.

THERMAL INFORMATION: OPA333

THERMAL METRIC(1)		OPA333			UNITS
		D (SOIC)	DBV (SOT23)	DCK (SC70)	
		8 PINS	5 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	140.1	220.8	298.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	89.8	97.5	65.4	
θ_{JB}	Junction-to-board thermal resistance	80.6	61.7	97.1	
ψ_{JT}	Junction-to-top characterization parameter	28.7	7.6	0.8	
ψ_{JB}	Junction-to-board characterization parameter	80.1	61.1	95.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

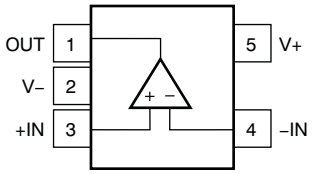
THERMAL INFORMATION: OPA2333

THERMAL METRIC(1)		OPA2333			UNITS
		D (SOIC)	DGK (MSOP)	DRB (DFN)	
		8 PINS	8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	124.0	180.3	46.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	73.7	48.1	26.3	
θ_{JB}	Junction-to-board thermal resistance	64.4	100.9	22.2	
ψ_{JT}	Junction-to-top characterization parameter	18.0	2.4	1.6	
ψ_{JB}	Junction-to-board characterization parameter	63.9	99.3	22.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	10.1	

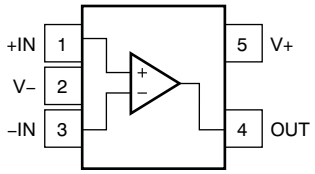
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATIONS: OPA333

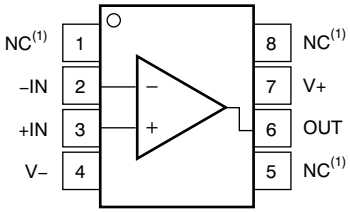
DBV PACKAGE
SOT23-5
(TOP VIEW)



DCK PACKAGE
SC70-5
(TOP VIEW)



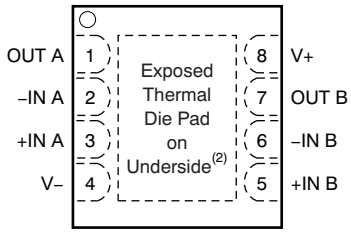
D PACKAGE
SO-8
(TOP VIEW)



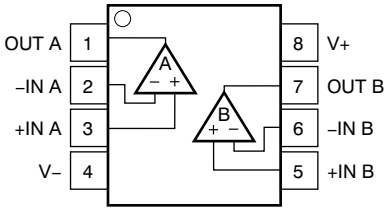
(1) NC denotes no internal connection.

PIN CONFIGURATIONS: OPA2333

DRB PACKAGE
DFN-8 (SON-8)
(TOP VIEW)



D AND DGK PACKAGES
SO-8 AND MSOP-8 (VSSOP-8)
(TOP VIEW)



(2) Connect thermal die pad to V–.

TYPICAL CHARACTERISTICS

Table 1. List of Typical Characteristics

TITLE	FIGURE
OFFSET VOLTAGE PRODUCTION DISTRIBUTION	Figure 1
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION	Figure 2
OPEN-LOOP GAIN vs FREQUENCY	Figure 3
COMMON-MODE REJECTION RATIO vs FREQUENCY	Figure 4
POWER-SUPPLY REJECTION RATIO vs FREQUENCY	Figure 5
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT	Figure 6
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE	Figure 7
INPUT BIAS CURRENT vs TEMPERATURE	Figure 8
QUIESCENT CURRENT vs TEMPERATURE	Figure 9
LARGE-SIGNAL STEP RESPONSE	Figure 10
SMALL-SIGNAL STEP RESPONSE	Figure 11
POSITIVE OVERVOLTAGE RECOVERY	Figure 12
NEGATIVE OVERVOLTAGE RECOVERY	Figure 13
SETTLING TIME vs CLOSED-LOOP GAIN	Figure 14
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE	Figure 15
0.1-Hz TO 10-Hz NOISE	Figure 16
CURRENT AND VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY	Figure 17

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = +5 V, and C_L = 0 pF, unless otherwise noted.

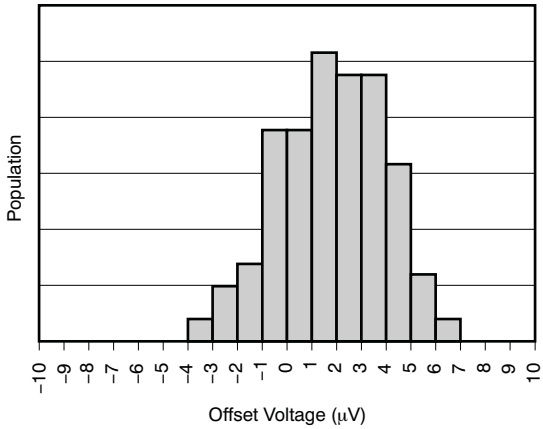


Figure 1. OFFSET VOLTAGE PRODUCTION DISTRIBUTION

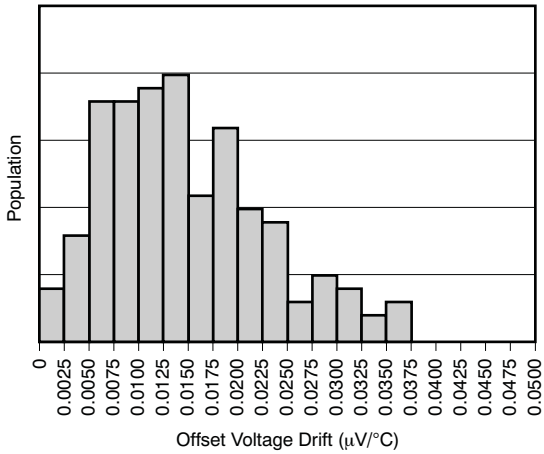


Figure 2. OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

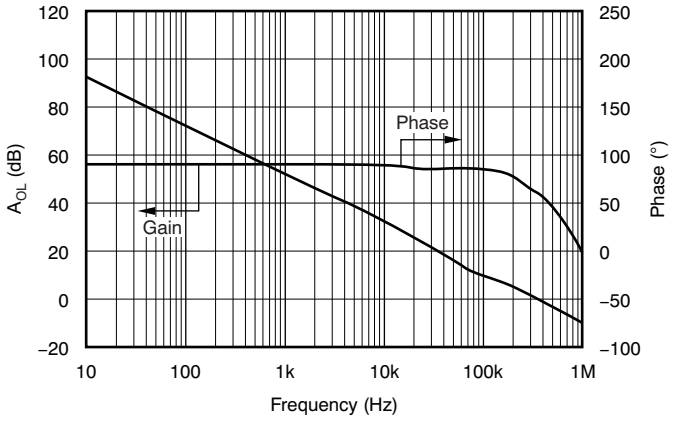


Figure 3. OPEN-LOOP GAIN vs FREQUENCY

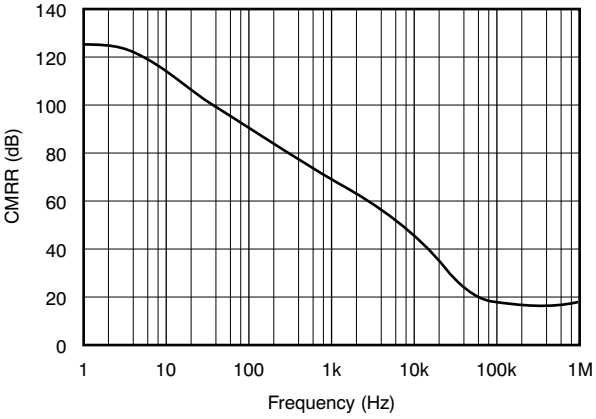


Figure 4. COMMON-MODE REJECTION RATIO vs FREQUENCY

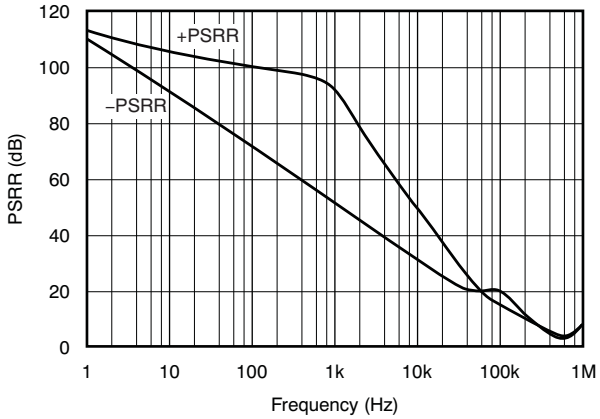


Figure 5. POWER-SUPPLY REJECTION RATIO vs FREQUENCY

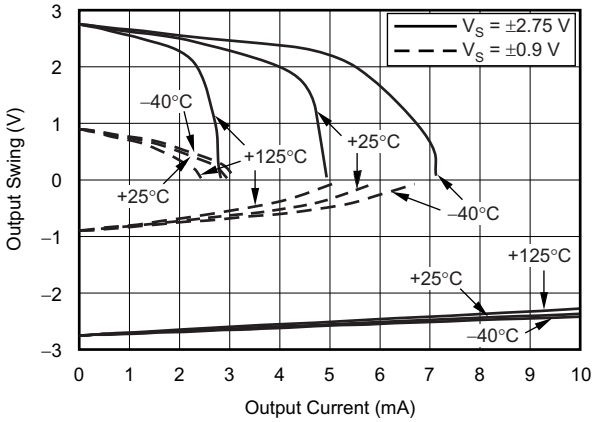


Figure 6. OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5 V, and C_L = 0 pF, unless otherwise noted.

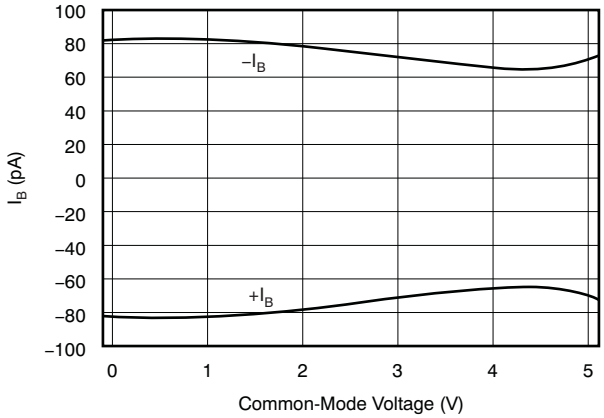


Figure 7. INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

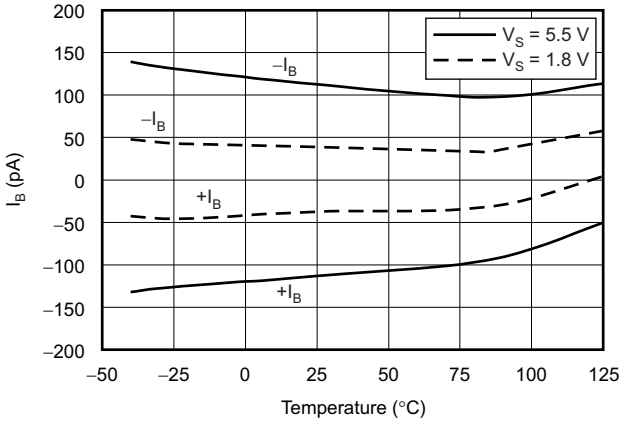


Figure 8. INPUT BIAS CURRENT vs TEMPERATURE

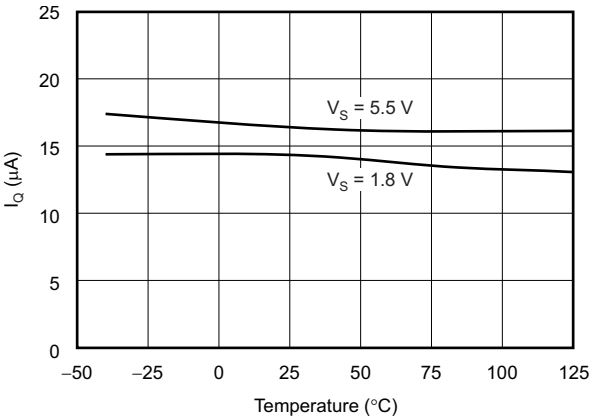


Figure 9. QUIESCENT CURRENT vs TEMPERATURE

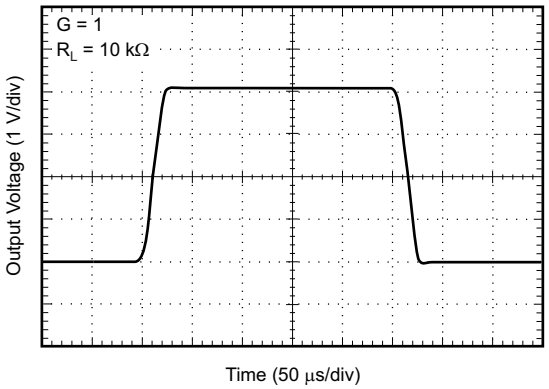


Figure 10. LARGE-SIGNAL STEP RESPONSE

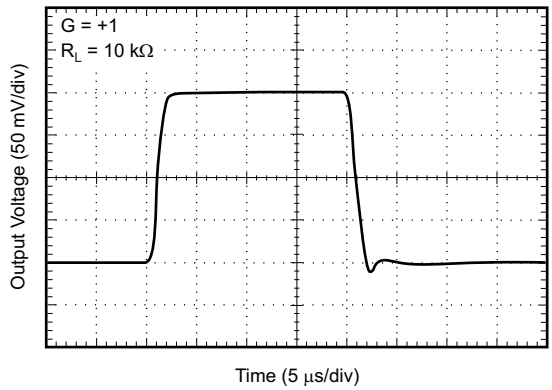


Figure 11. SMALL-SIGNAL STEP RESPONSE

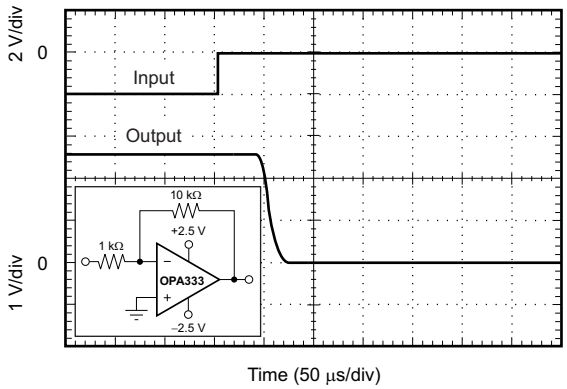


Figure 12. POSITIVE OVERVOLTAGE RECOVERY

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +5 V, and C_L = 0 pF, unless otherwise noted.

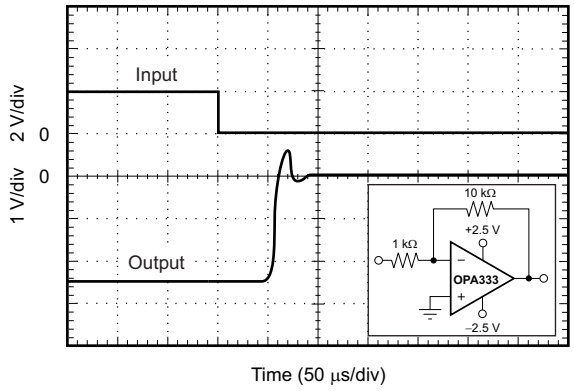


Figure 13. NEGATIVE OVERVOLTAGE RECOVERY

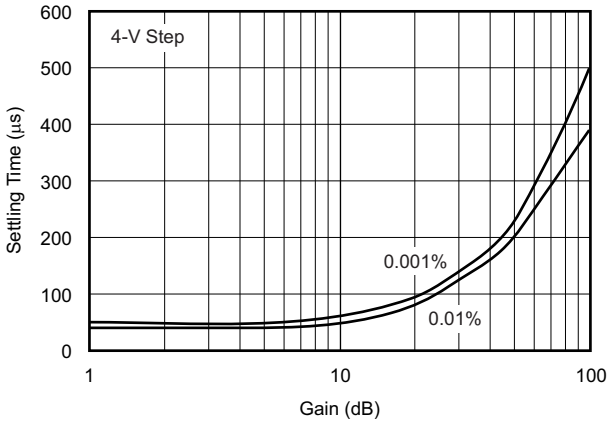


Figure 14. SETTLING TIME vs CLOSED-LOOP GAIN

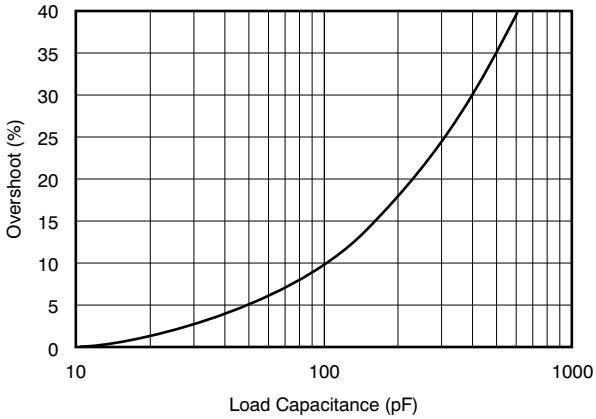


Figure 15. SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

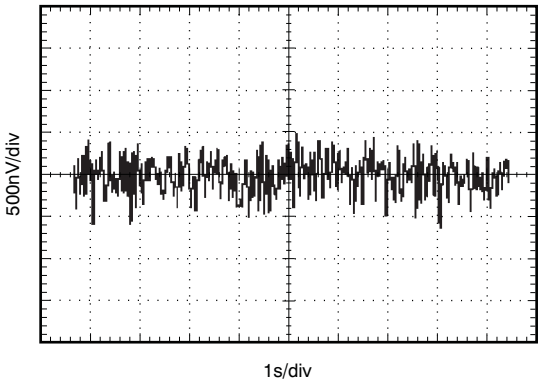


Figure 16. 0.1-Hz TO 10-Hz NOISE

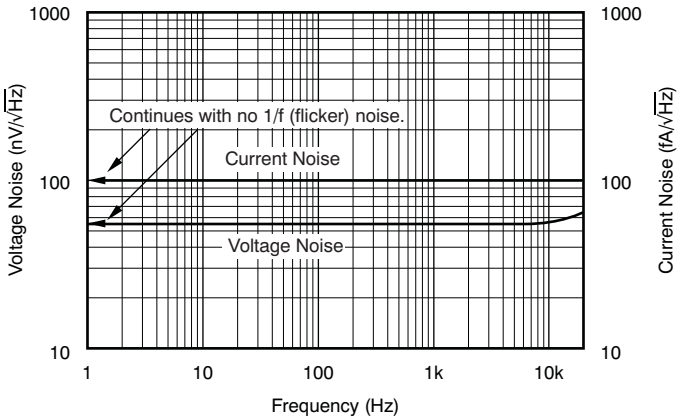


Figure 17. CURRENT AND VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

DETAILED DESCRIPTION

The OPA333 and OPA2333 are unity-gain stable and free from unexpected output phase reversal. These devices use a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μV/°C or higher, depending on materials used.

OPERATING VOLTAGE

The OPA333 and OPA2333 op amps operate over a power-supply range of +1.8 V to +5.5 V (±0.9 V to ±2.75 V). Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section.

CAUTION

Supply voltages higher than +7 V (absolute maximum) can permanently damage the device.

INPUT VOLTAGE

The OPA333 and OPA2333 input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA333 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Typically, input bias current is approximately 70 pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 18.

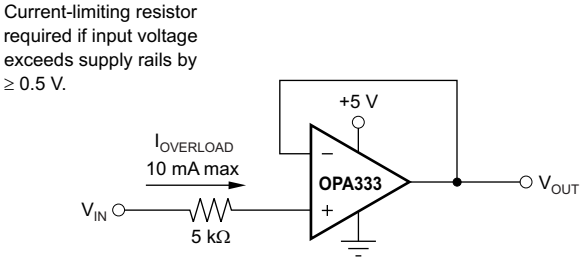


Figure 18. Input Current Protection

INTERNAL OFFSET CORRECTION

The OPA333 and OPA2333 op amps use an auto-calibration technique with a time-continuous, 350-kHz op amp in the signal path. This amplifier is zero-corrected every 8 µs using a proprietary technique. Upon power-up, the amplifier requires approximately 100 µs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

ACHIEVING OUTPUT SWING TO THE OP AMP NEGATIVE RAIL

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as +2.5 V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply op amp. A good, single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA333 and OPA2333 can be made to swing to, or slightly below, ground on a single-supply power source. This swing is acheived with the use of the use of another resistor and an additional, more negative power supply than the op amp negative supply. A pull-down resistor can be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 19.

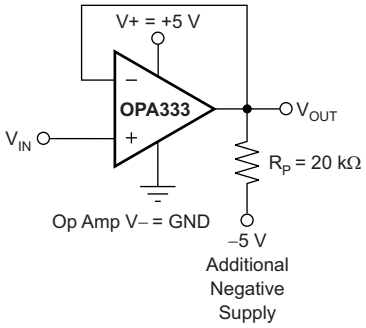


Figure 19. V_{OUT} Range to Ground

The OPA333 and OPA2333 have an output stage that allows the output voltage to be pulled to the negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA333 and OPA2333 are characterized to perform with this technique; the recommended resistor value is approximately 20 kΩ. Note that this configuration increases the current consumption by several hundreds of microamps. Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occurs below –2 mV, but excellent accuracy returns after the output is again driven above –2 mV. Lowering the resistance of the pull-down resistor allows the op amp to swing even further below the negative rail. Resistances as low as 10 kΩ can be used to achieve excellent accuracy down to –10 mV.

APPLICATION INFORMATION

Figure 20 shows a temperature measurement application

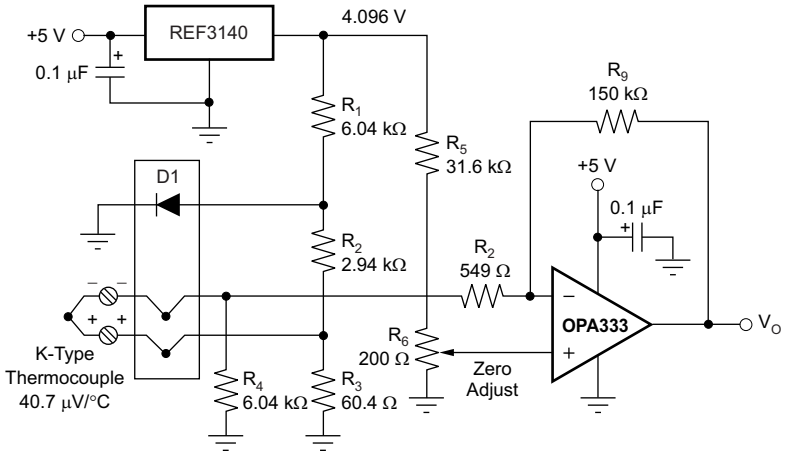


Figure 20. Temperature Measurement

Figure 21 shows the basic configuration for a bridge amplifier.

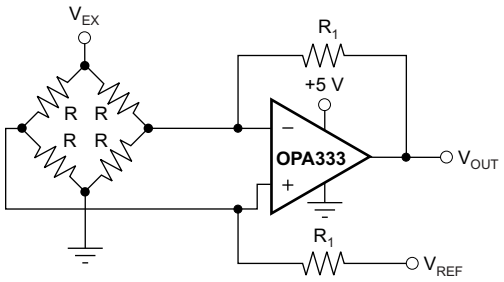
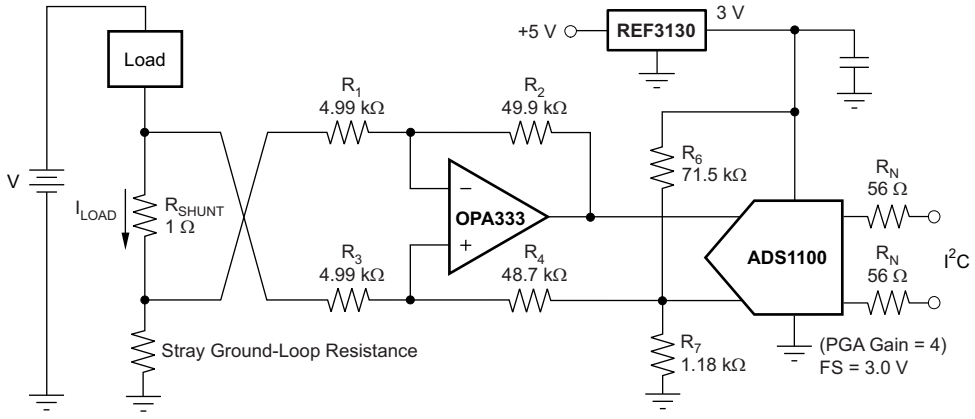


Figure 21. Single Op Amp Bridge Amplifier

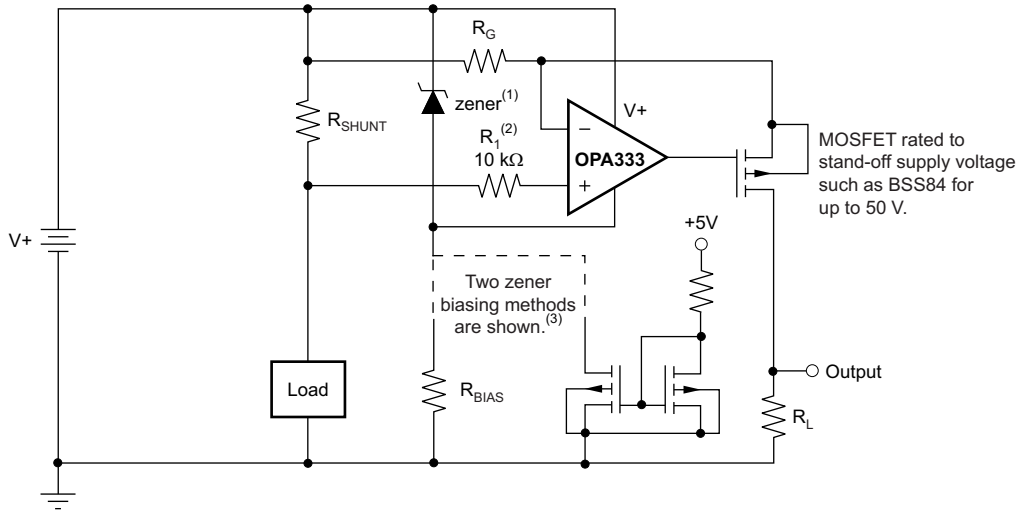
A low-side current shunt monitor is shown in Figure 22. R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I^2C bus. The ADS1100 is a 16-bit converter; therefore, a precise reference is essential for maximum accuracy. If absolute accuracy is not required and the 5-V power supply is sufficiently stable, the REF3130 can be omitted.



NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 22. Low-Side Current Monitor

Additional application ideas are shown in Figure 23 through Figure 26.



(1) Zener rated for op amp supply capability (that is, 5.1 V for OPA333).

(2) Current-limiting resistor.

(3) Choose zener biasing resistor or dual NMOSFETs (FDG6301N, NTJD4001N, or Si1034)

Figure 23. High-Side Current Monitor

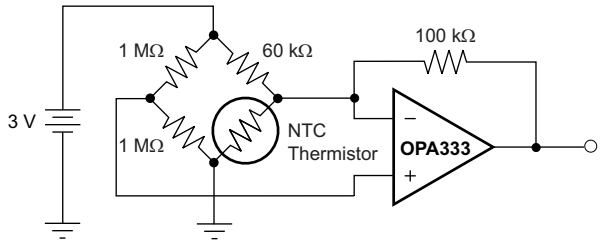


Figure 24. Thermistor Measurement

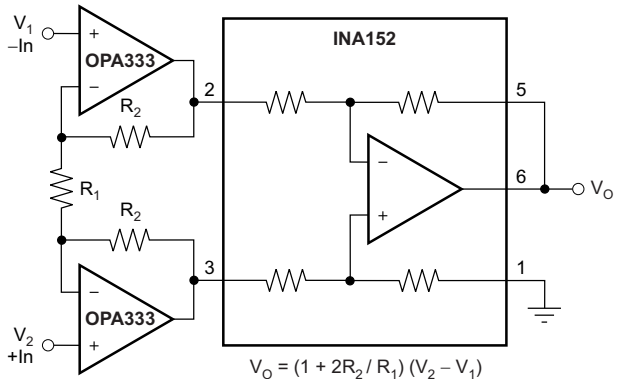
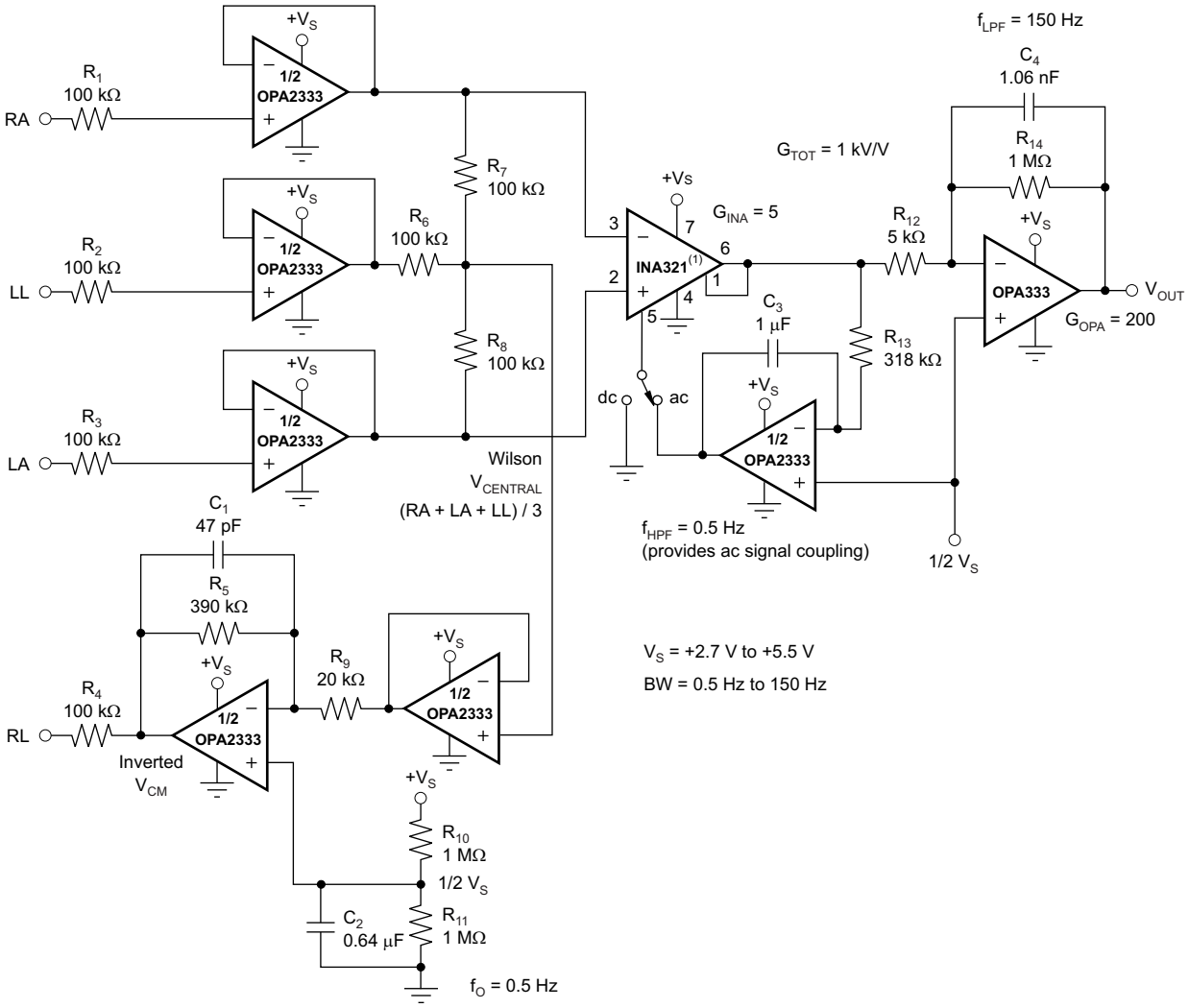


Figure 25. Precision Instrumentation Amplifier



(1) Other instrumentation amplifiers can be used, such as the INA326, which has lower noise, but higher quiescent current.

Figure 26. Single-Supply, Very Low Power, ECG Circuit

LAYOUT GUIDELINES

GENERAL LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short and when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The OPA333 is specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may still cause varying offset levels.

DFN PACKAGE

The OPA2333 is offered in an DFN-8 package (also known as SON). The DFN is a QFN package with lead contacts on only two sides of the bottom of the package. This leadless package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard PCB assembly techniques. See Application Reports SLUA271, *QFN/SON PCB Attachment* and SCBA017, *Quad Flatpack No-Lead Logic Packages*, both available for download at www.ti.com.

NOTE

The exposed leadframe die pad on the bottom of the package should be connected to V– or left unconnected.

DFN LAYOUT GUIDELINES

Solder the exposed leadframe die pad on the DFN package to a thermal pad on the PCB. A mechanical drawing showing an example layout is attached at the end of this data sheet. Refinements to this layout may be necessary based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heatsink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2007) to Revision D	Page
• Changed data sheet format to most current standard look and feel	1
• Added OPA2333 DFN-8 pinout to front page	1
• Changed 2nd *signal input terminals* parameter in the Absolute Maximum Ratings from "voltage" to "current" (typo)	2
• Added OPA333 thermal information table	4
• Added OPA2333 thermal information table	4
• Added Table 1	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2333AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A	Samples
OPA2333AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A	Samples
OPA2333AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OBAQ	Samples
OPA2333AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OBAQ	Samples
OPA2333AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-UNLIM	-40 to 125	OBAQ	Samples
OPA2333AIDGKTG4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-UNLIM	-40 to 125	OBAQ	Samples
OPA2333AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A	Samples
OPA2333AIDRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ	Samples
OPA2333AIDRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ	Samples
OPA2333AIDRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ	Samples
OPA2333AIDRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQZ	Samples
OPA2333AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2333A	Samples
OPA333AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A	Samples
OPA333AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ	Samples
OPA333AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ	Samples
OPA333AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ	Samples
OPA333AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OAXQ	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA333AIDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BQY	Samples
OPA333AIDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BQY	Samples
OPA333AIDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BQY	Samples
OPA333AIDCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BQY	Samples
OPA333AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A	Samples
OPA333AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A	Samples
OPA333AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O333A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA2333, OPA333 :

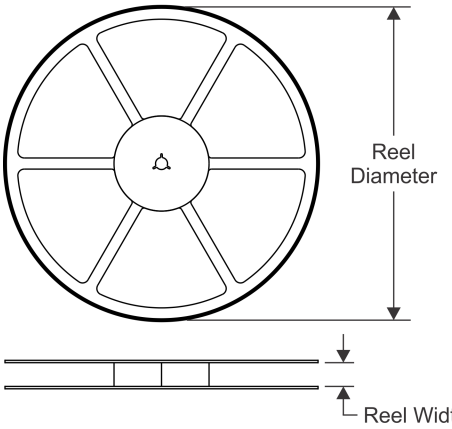
- Automotive: OPA2333-Q1, OPA333-Q1

NOTE: Qualified Version Definitions:

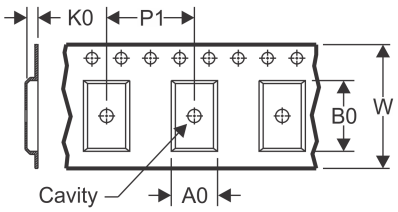
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

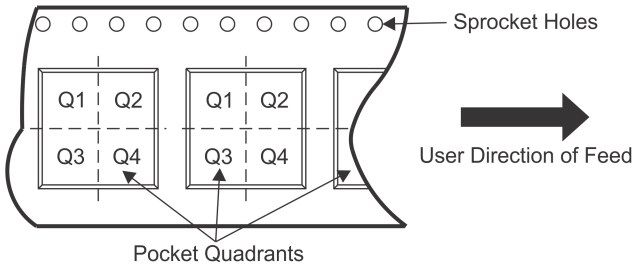


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

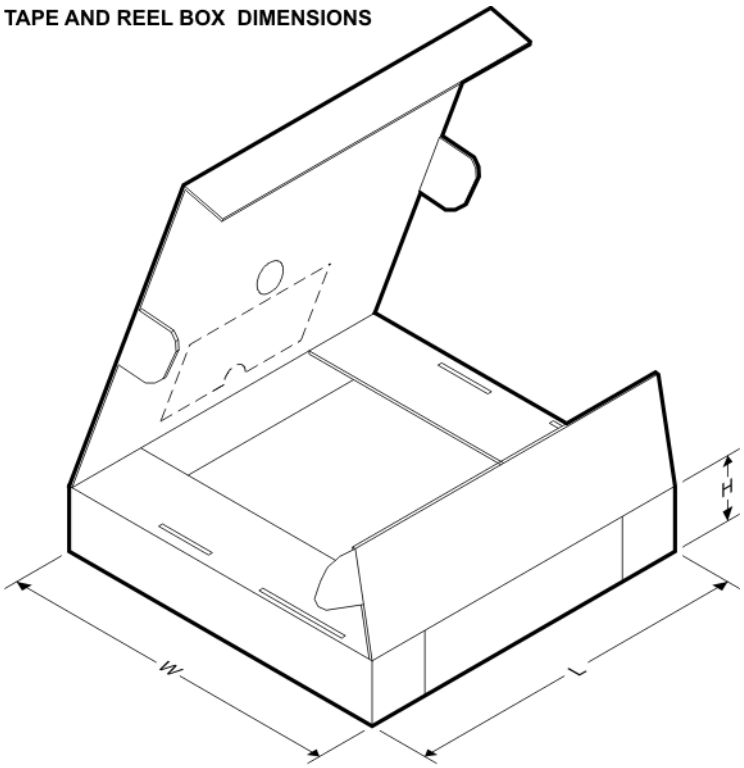
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2333AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2333AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2333AIDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2333AIDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA333AIDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA333AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA333AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA333AIDCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA333AIDCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA333AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

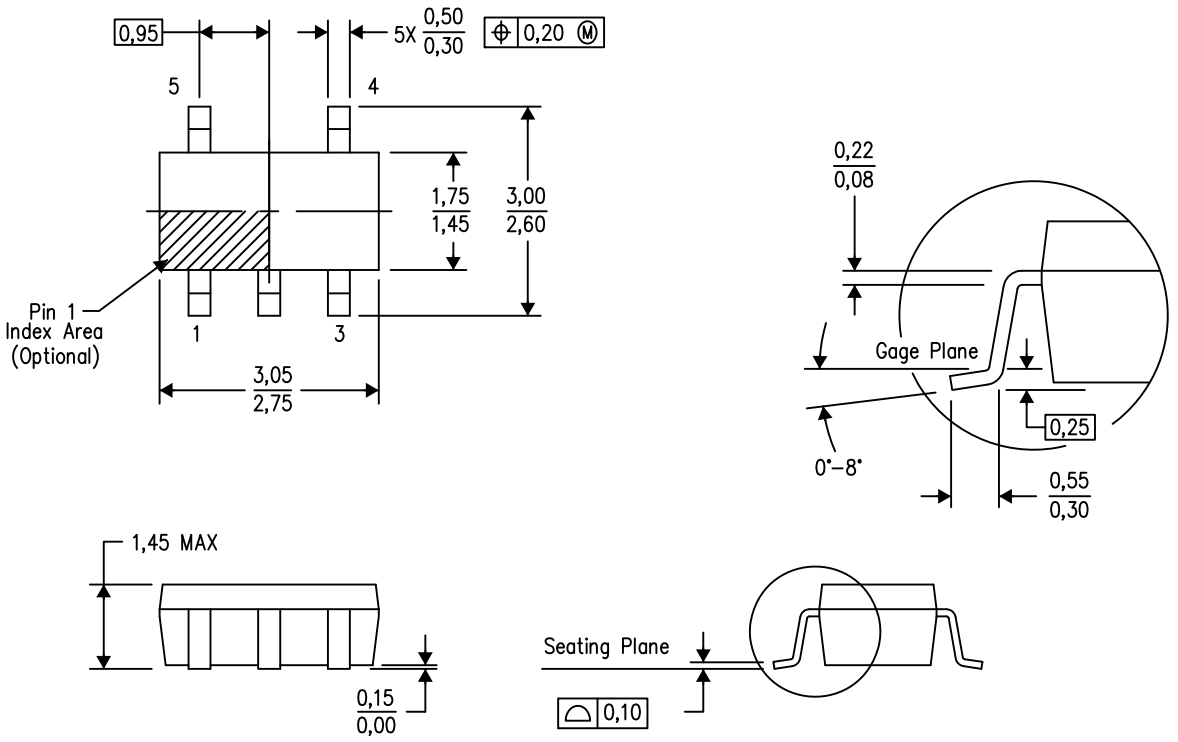
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2333AIDGKT	VSSOP	DGK	8	250	364.0	364.0	27.0
OPA2333AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA2333AIDRBR	SON	DRB	8	3000	367.0	367.0	35.0
OPA2333AIDRBT	SON	DRB	8	250	210.0	185.0	35.0
OPA333AIDBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
OPA333AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA333AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA333AIDCKR	SC70	DCK	5	3000	203.0	203.0	35.0
OPA333AIDCKT	SC70	DCK	5	250	203.0	203.0	35.0
OPA333AIDR	SOIC	D	8	2500	367.0	367.0	35.0

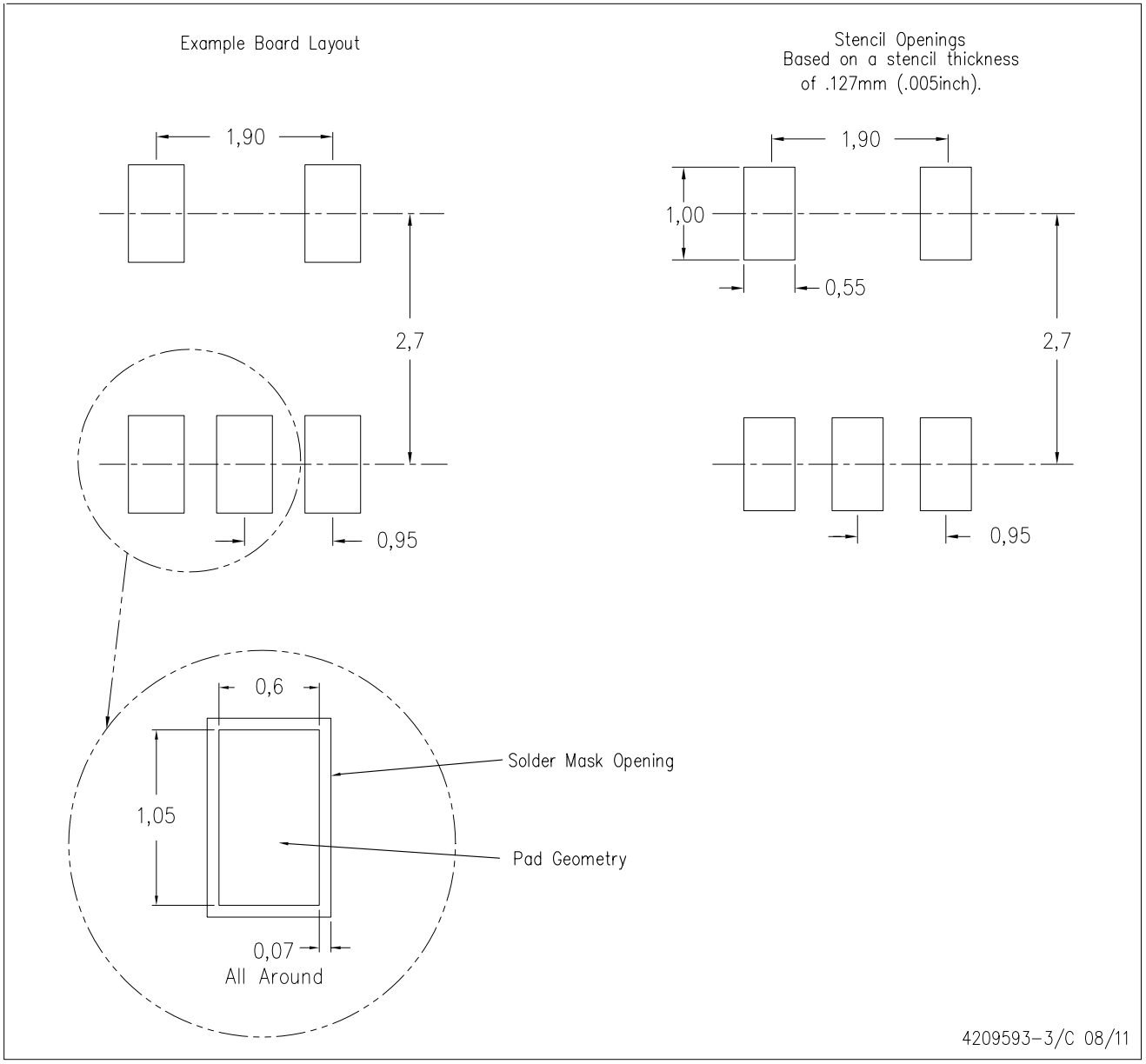
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

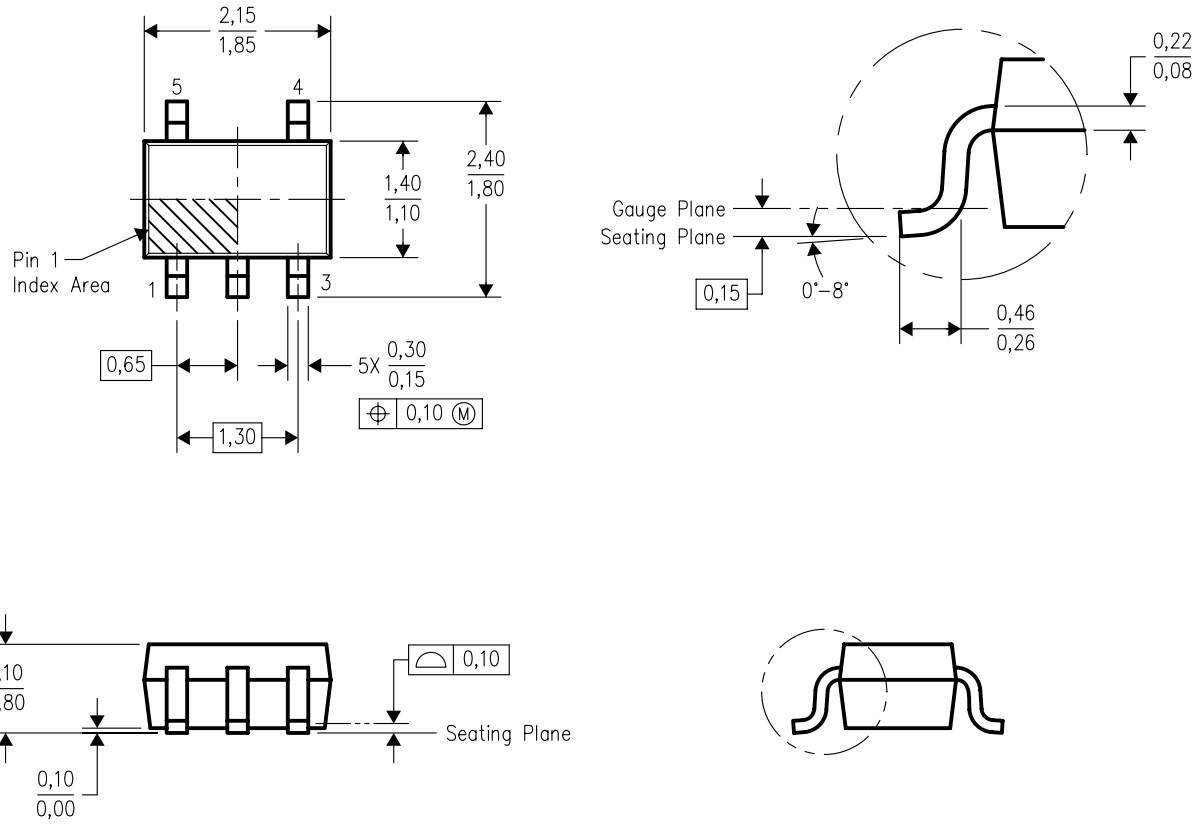
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

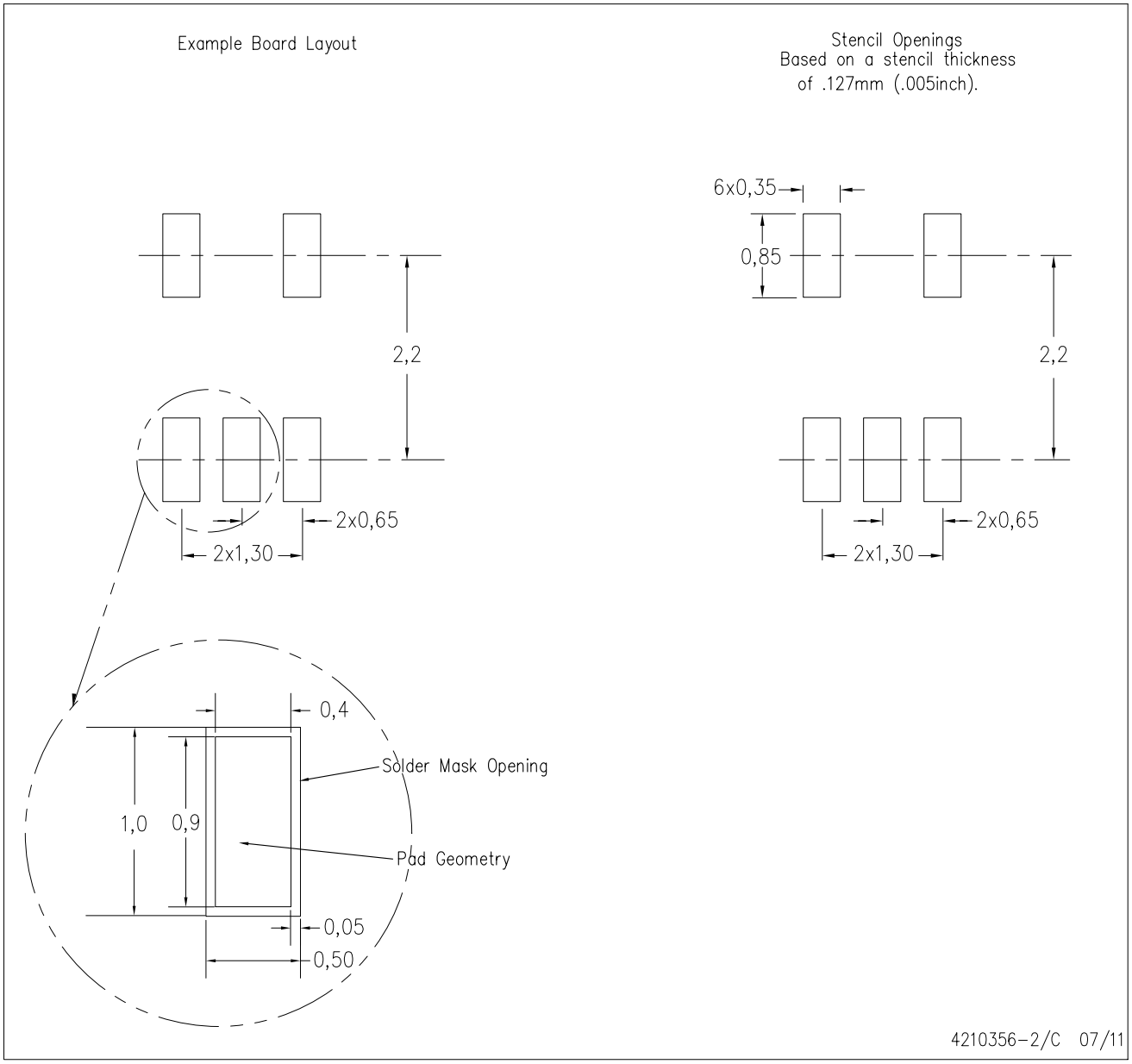
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

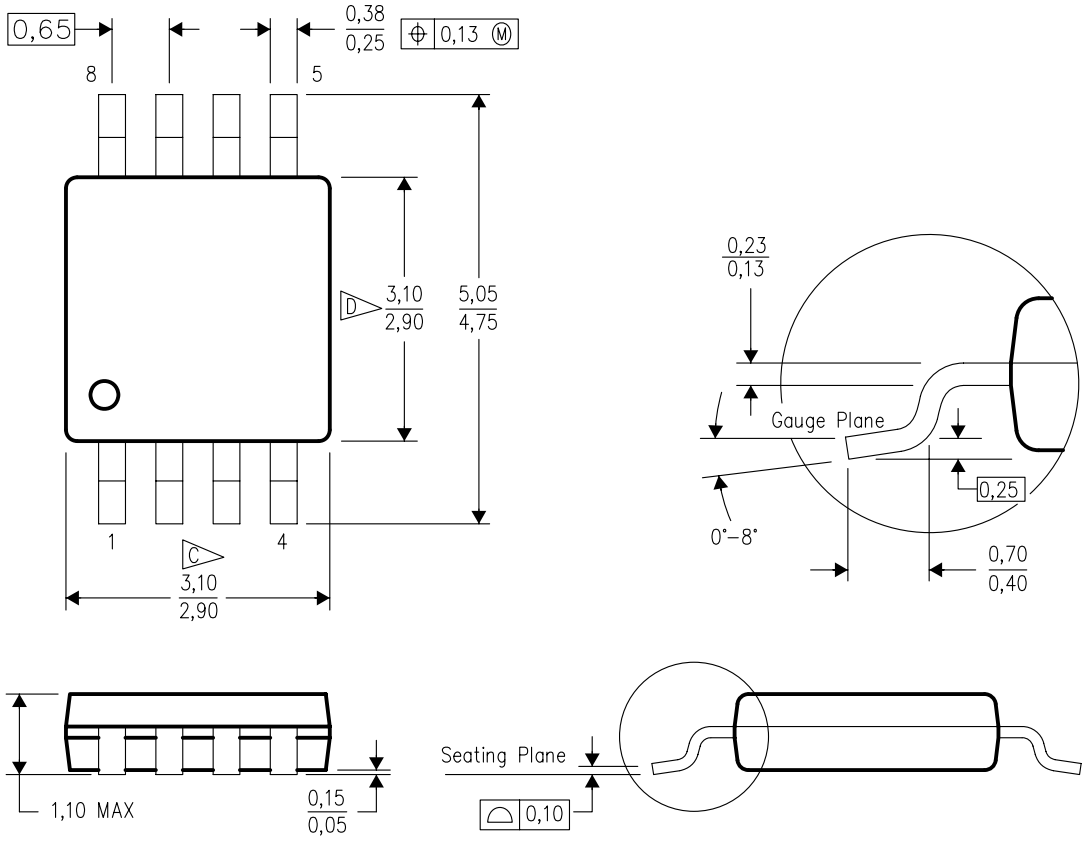
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

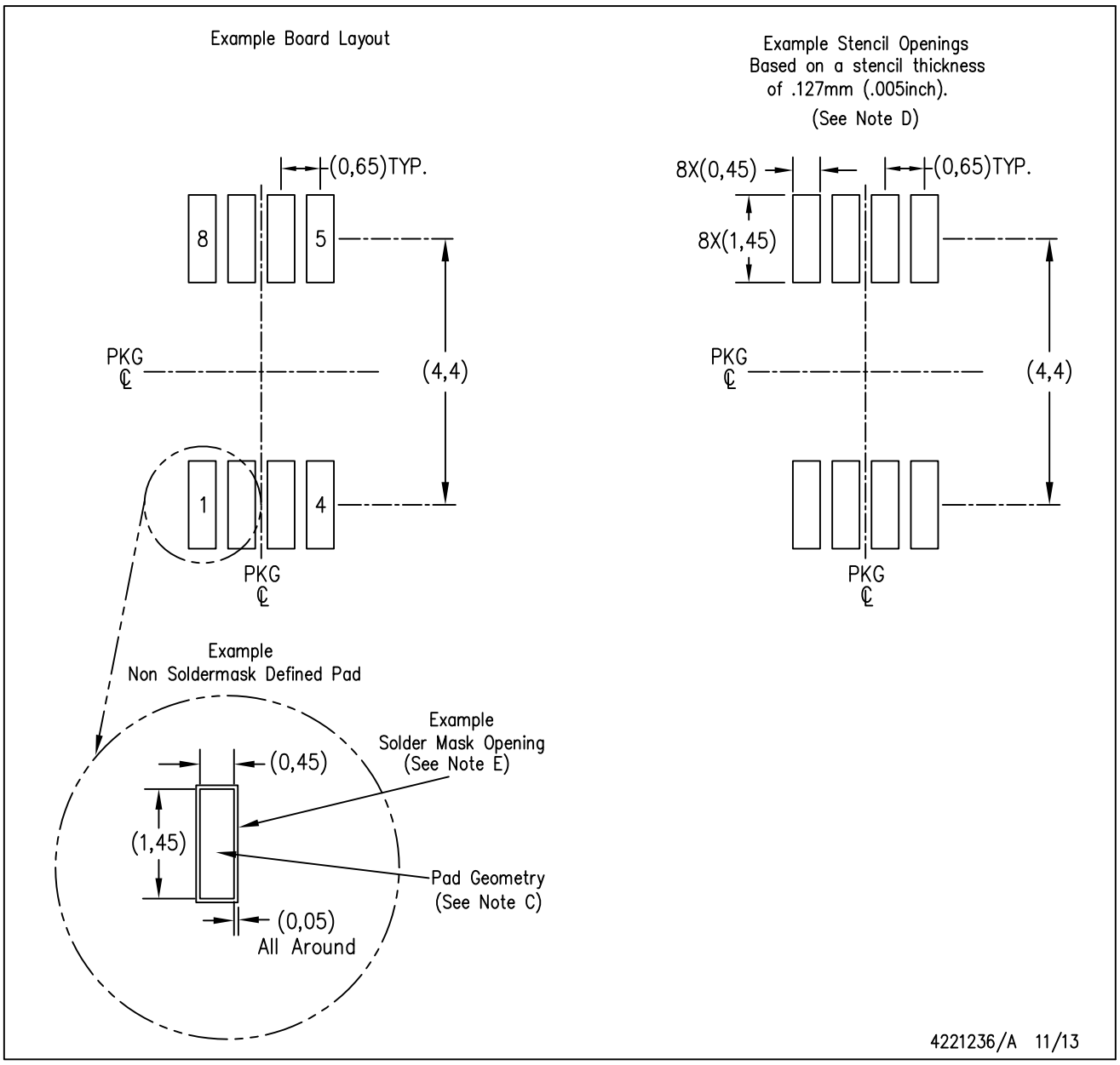
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

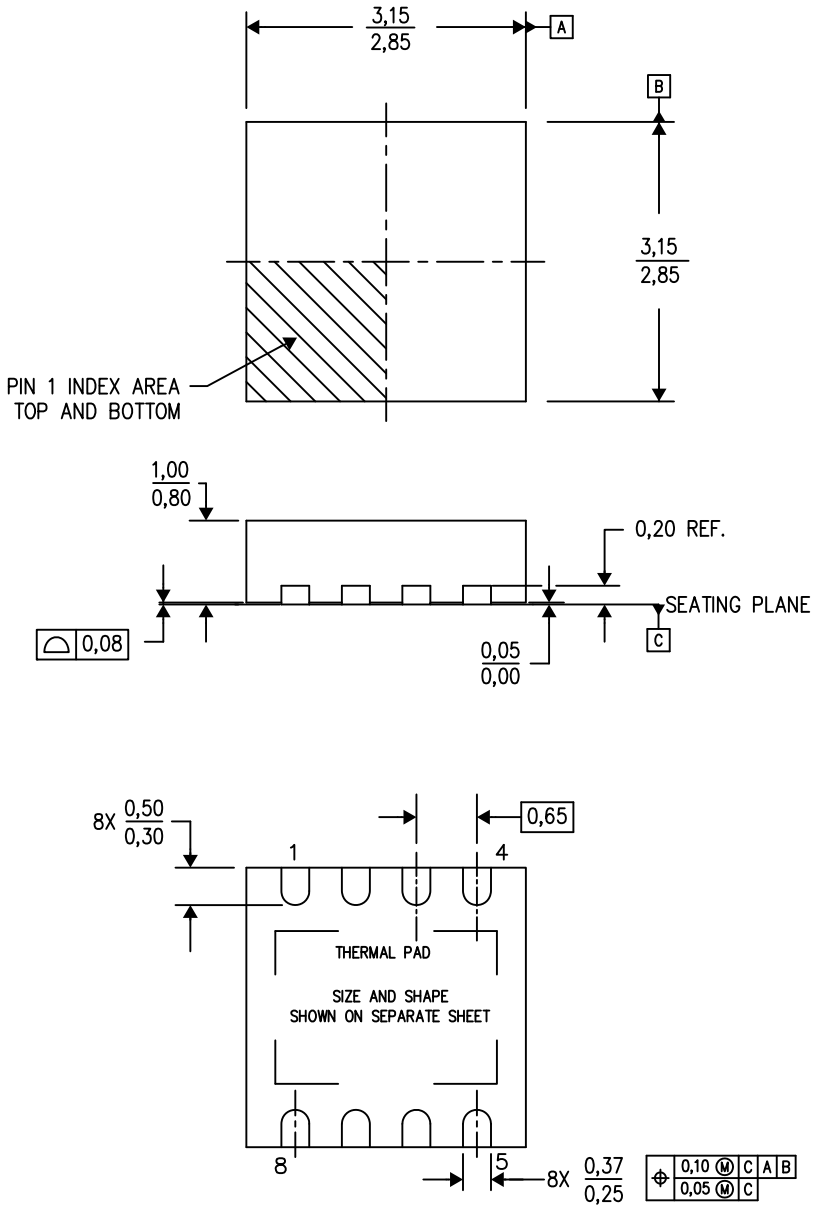
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4203482–2/K 06/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

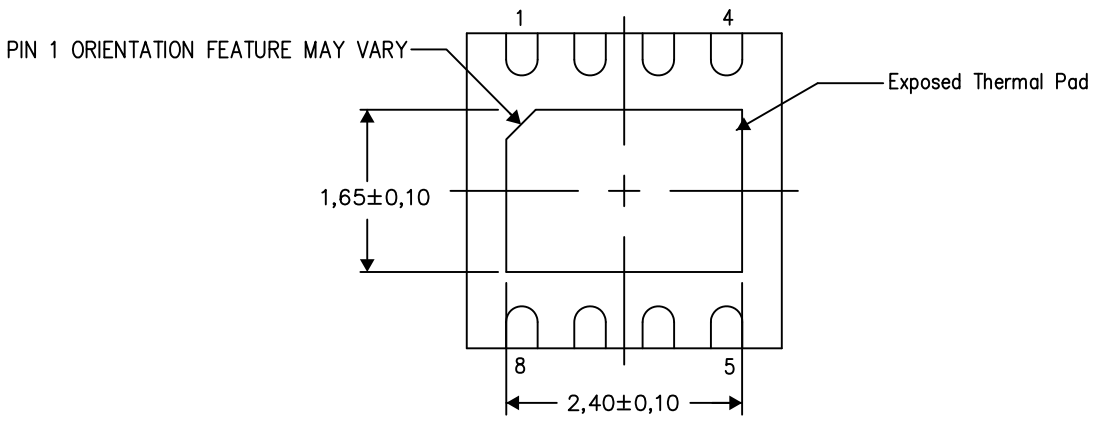
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



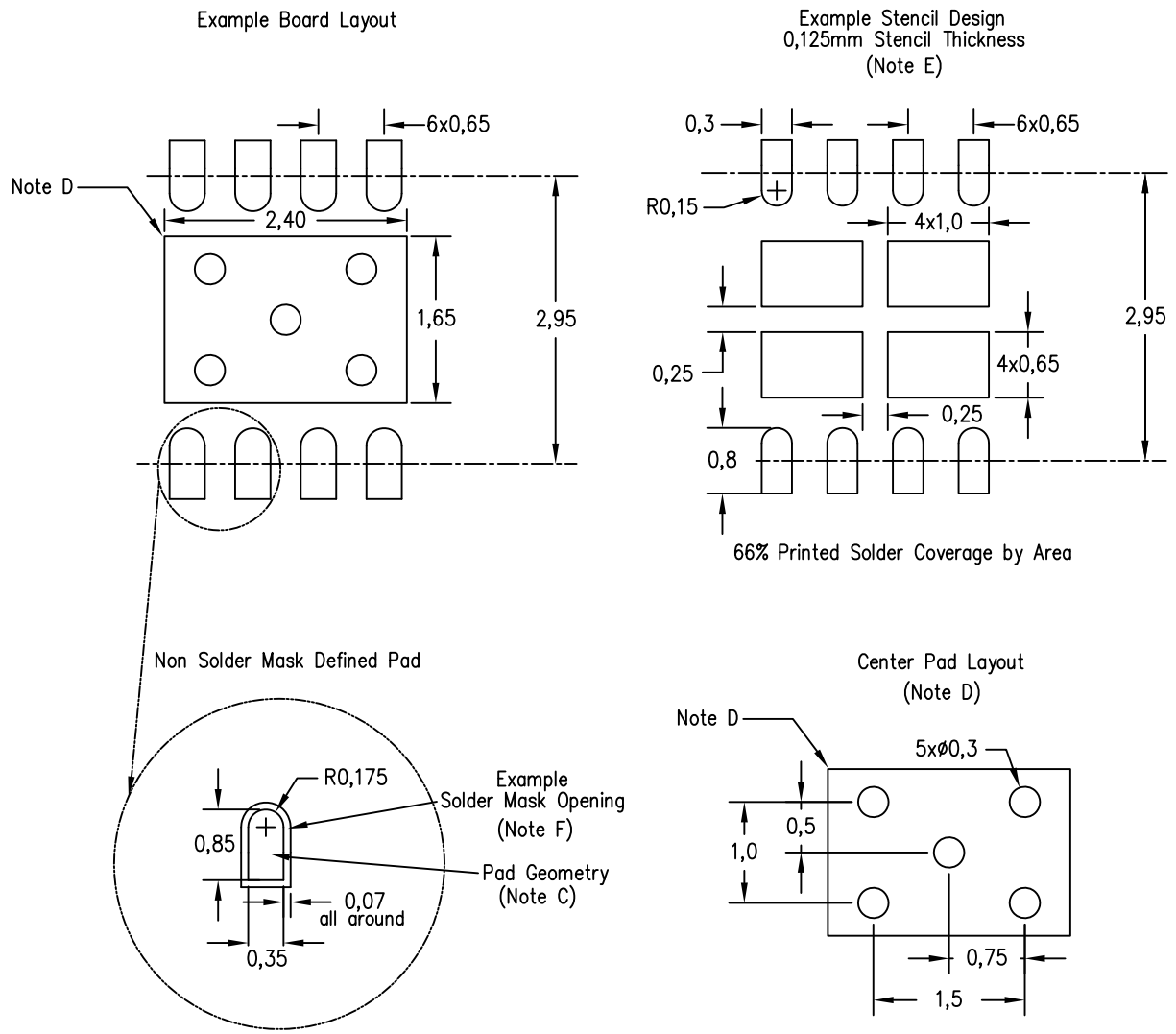
Bottom View

Exposed Thermal Pad Dimensions

4206340–3/N 09/12

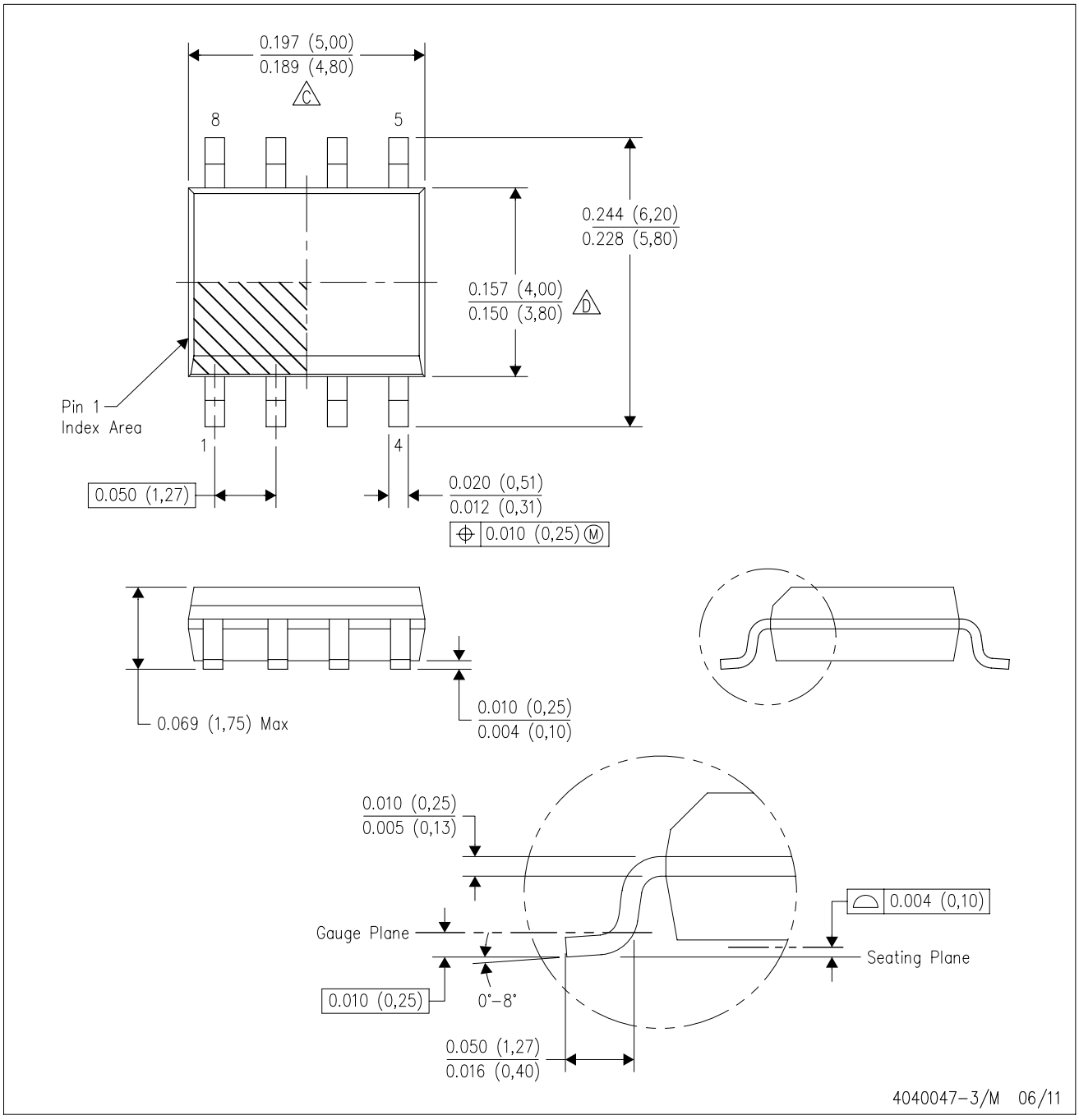
NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



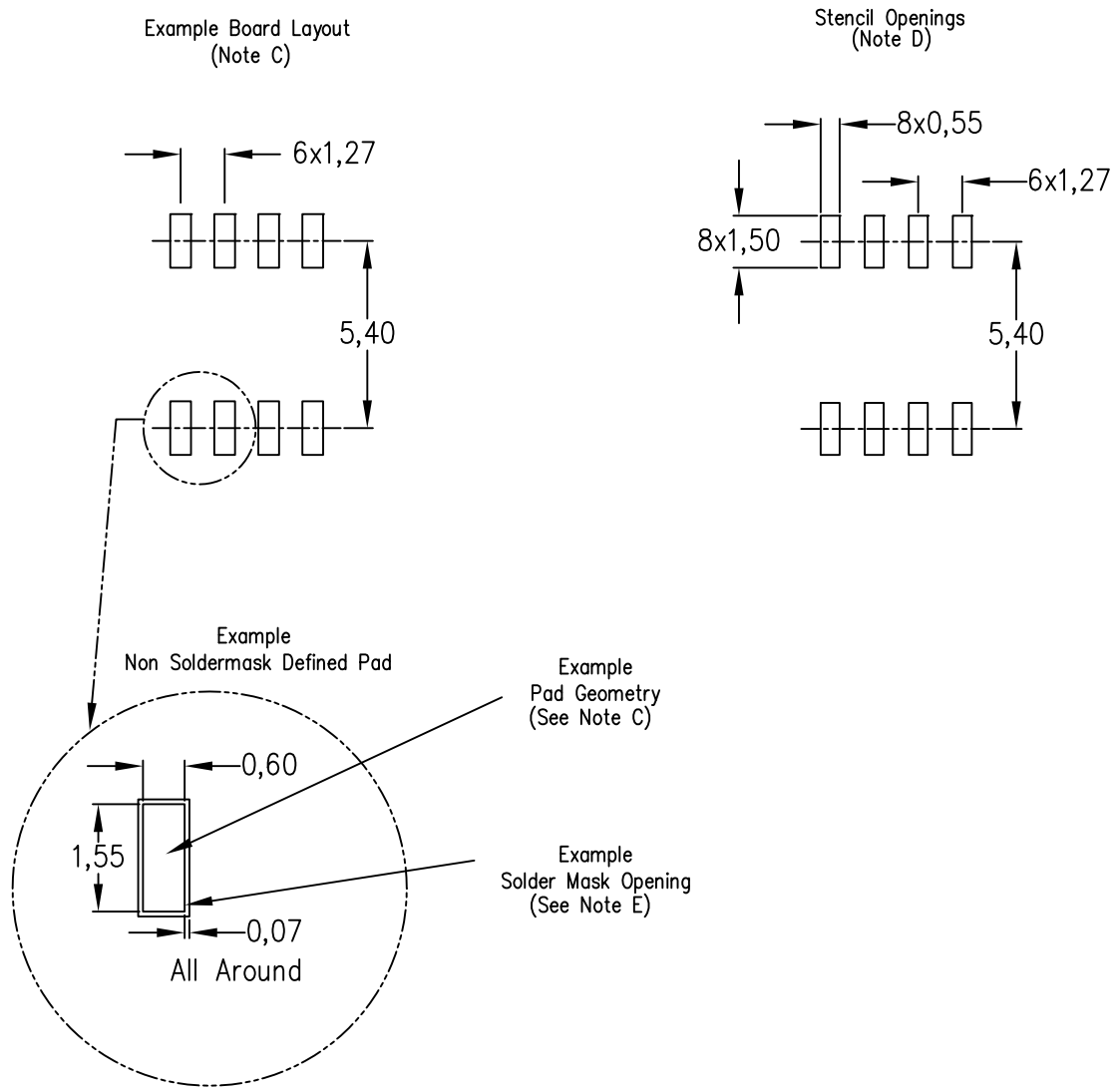
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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