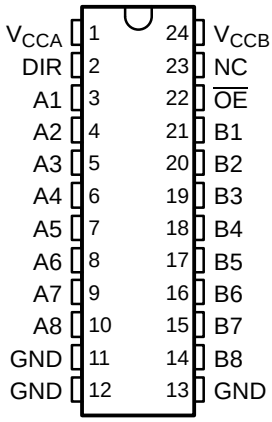
SN74LVCC3245A
OCTAL BUS TRANSCEIVER
WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

SCAS585O – NOVEMBER 1996 – REVISED MARCH 2005

FEATURES

- **Bidirectional Voltage Translator**
- **2.3 V to 3.6 V on A Port and 3 V to 5.5 V on B Port**
- **Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DB, DBQ, DW, NS, OR PW PACKAGE
(TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails. The B port is designed to track V_{CCB}, which accepts voltages from 3 V to 5.5 V, and the A port is designed to track V_{CCA}, which operates at 2.3 V to 3.6 V. This allows for translation from a 3.3-V to a 5-V system environment and vice versa, from a 2.5-V to a 3.3-V system environment and vice versa.

The SN74LVCC3245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, $\overline{OE}$) is powered by V_{CCA}.

ORDERING INFORMATION

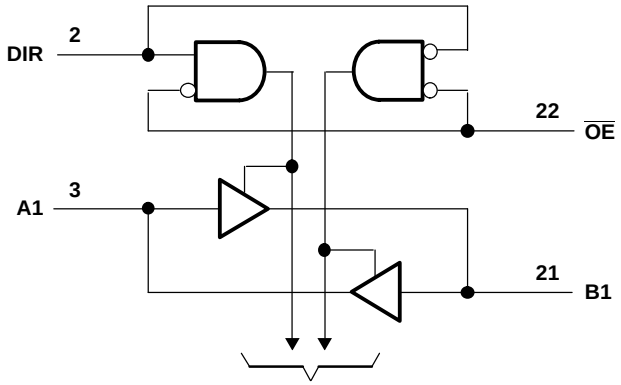
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube of 25	SN74LVCC3245ADW	LVCC3245A
		Reel of 2000	SN74LVCC3245ADWR	
	SOP – NS	Reel of 2000	SN74LVCC3245ANSR	LVCC3245A
	SSOP – DB	Reel of 2000	SN74LVCC3245ADBR	LH245A
	SSOP (QSOP) – DBQ	Reel of 2500	SN74LVCC3245ADBQR	LVCC3245A
	TSSOP – PW	Tube of 60	SN74LVCC3245APW	LH245A
		Reel of 2000	SN74LVCC3245APWR	
		Reel of 250	SN74LVCC3245APWT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(EACH TRANSCEIVER)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		–0.5	6	V
V_I	Input voltage range	All A ports(2)	–0.5	V_{CCA} + 0.5	V
		All B ports(3)	–0.5	V_{CCB} + 0.5	
		Except I/O ports(2)	–0.5	V_{CCA} + 0.5	
V_O	Output voltage range(3)	All A ports	–0.5	V_{CCA} + 0.5	V
		All B ports	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
θ_{JA}	Package thermal impedance(4)	DB package		63	°C/W
		DBQ package		61	
		DW package		46	
		NS package		65	
		PW package		88	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 4.6 V maximum.
(3) This value is limited to 6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

		V_{CCA}	V_{CCB}	MIN	NOM	MAX	UNIT
V_{CCA}	Supply voltage			2.3	3.3	3.6	V
V_{CCB}	Supply voltage			3	5	5.5	V
V_{IHA}	High-level input voltage	2.3 V	3 V	1.7			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	2			
V_{IHB}	High-level input voltage	2.3 V	3 V	2			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	3.85			
V_{ILA}	Low-level input voltage	2.3 V	3 V			0.7	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	
V_{ILB}	Low-level input voltage	2.3 V	3 V			0.8	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			1.65	
V_{IH}	High-level input voltage (control pins) (referenced to V_{CCA})	2.3 V	3 V	1.7			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	2			
V_{IL}	Low-level input voltage (control pins) (referenced to V_{CCA})	2.3 V	3 V			0.7	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	
V_{IA}	Input voltage			0		V_{CCA}	V
V_{IB}	Input voltage			0		V_{CCB}	V
V_{OA}	Output voltage			0		V_{CCA}	V
V_{OB}	Output voltage			0		V_{CCB}	V
I_{OHA}	High-level output current	2.3 V	3 V			–8	mA
		2.7 V	3 V			–12	
		3 V	3 V			–24	
		2.7 V	4.5 V			–24	
I_{OHB}	High-level output current	2.3 V	3 V			–12	mA
		2.7 V	3 V			–12	
		3 V	3 V			–24	
		2.7 V	4.5 V			–24	
I_{OLA}	Low-level output current	2.3 V	3 V			8	mA
		2.7 V	3 V			12	
		3 V	3 V			24	
		2.7 V	4.5 V			24	

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions (continued)

		V_{CCA}	V_{CCB}	MIN	NOM	MAX	UNIT
I_{OLB}	Low-level output current	2.3 V	3 V			12	mA
		2.7 V	3 V			12	
		3 V	3 V			24	
		2.7 V	4.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate					10	ns/V
T_A	Operating free-air temperature			–40		85	°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OHA}		I_{OH} = –100 µA	3 V	3 V	2.9	3		V
		I_{OH} = –8 mA	2.3 V	3 V	2			
		I_{OH} = –12 mA	2.7 V	3 V	2.2	2.5		
			3 V	3 V	2.4	2.8		
		I_{OH} = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	2	2.3		
V_{OHB}		I_{OH} = –100 µA	3 V	3 V	2.9	3		V
		I_{OH} = –12 mA	2.3 V	3 V	2.4			
			2.7 V	3 V	2.4	2.8		
		I_{OH} = –24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	3.2	4.2		
V_{OLA}		I_{OL} = 100 µA	3 V	3 V			0.1	V
		I_{OL} = 8 mA	2.3 V	3 V			0.6	
		I_{OL} = 12 mA	2.7 V	3 V		0.1	0.5	
		I_{OL} = 24 mA	3 V	3 V		0.2	0.5	
			2.7 V	4.5 V		0.2	0.5	
V_{OLB}		I_{OL} = 100 µA	3 V	3 V			0.1	V
		I_{OL} = 12 mA	2.3 V	3 V			0.4	
		I_{OL} = 24 mA	3 V	3 V		0.2	0.5	
			2.7 V	4.5 V		0.2	0.5	
I_I	Control inputs	V_I = V_{CCA} or GND	3.6 V	3.6 V		±0.1	±1	µA
				5.5 V		±0.1	±1	
I_{OZ} (1)	A or B ports	V_O = $V_{CCA/B}$ or GND, V_I = V_{IL} or V_{IH}	3.6 V	3.6 V		±0.5	±5	µA
I_{CCA}	B to A	A port = V_{CCA} or GND, I_O = 0	3.6 V	Open		5	50	µA
		B port = V_{CCB} or GND, I_O = 0	3.6 V	3.6 V		5	50	
				5.5 V		5	50	
I_{CCB}	A to B	A port = V_{CCA} or GND, I_O = 0	3.6 V	3.6 V		5	50	µA
				5.5 V		8	80	
ΔI_{CCA} (2)	A port	V_I = V_{CCA} – 0.6 V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at GND and DIR at V_{CCA}	3.6 V	3.6 V		0.35	0.5	mA
	$\overline{OE}$	V_I = V_{CCA} – 0.6 V, Other inputs at V_{CCA} or GND, DIR at V_{CCA}	3.6 V	3.6 V		0.35	0.5	
	DIR	V_I = V_{CCA} – 0.6 V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at GND	3.6 V	3.6 V		0.35	0.5	
ΔI_{CCB} (2)	B port	V_I = V_{CCB} – 2.1 V, Other inputs at V_{CCB} or GND, $\overline{OE}$ at GND and DIR at GND	3.6 V	5.5 V		1	1.5	mA
C_i	Control inputs	V_I = V_{CCA} or GND	Open	Open		4		pF
C_{io}	A or B ports	V_O = $V_{CCA/B}$ or GND	3.3 V	5 V		18.5		pF

(1) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(2) This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0 V or the associated V_{CC}.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V		V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V		V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	A	B	1	9.4	1	6	1	7.1	ns
t_{PLH}			1	9.1	1	5.3	1	7.2	
t_{PHL}	B	A	1	11.2	1	5.8	1	6.4	ns
t_{PLH}			1	9.9	1	7	1	7.6	
t_{PZL}	$\overline{OE}$	A	1	14.5	1	9.2	1	9.7	ns
t_{PZH}			1	12.9	1	9.5	1	9.5	
t_{PZL}	$\overline{OE}$	B	1	13	1	8.1	1	9.2	ns
t_{PZH}			1	12.8	1	8.4	1	9.9	
t_{PLZ}	$\overline{OE}$	A	1	7.1	1	7	1	6.6	ns
t_{PHZ}			1	6.9	1	7.8	1	6.9	
t_{PLZ}	$\overline{OE}$	B	1	8.8	1	7.3	1	7.5	ns
t_{PHZ}			1	8.9	1	7	1	7.9	

Operating Characteristics

V_{CCA} = 3.3 V, V_{CCB} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50, f = 10 MHz	38	pF
		Outputs disabled		4.5	

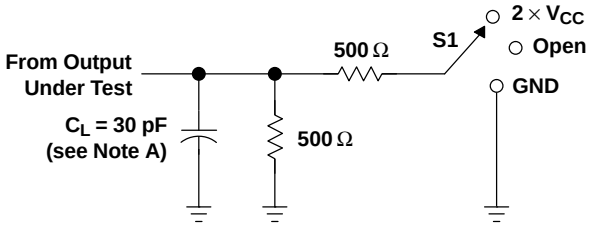
Power-Up Considerations(1)

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. To guard against such power-up problems, take these precautions:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie $\overline{OE}$ to V_{CCA} with a pullup resistor so that it ramps with V_{CCA}.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA}. Otherwise, keep DIR low.

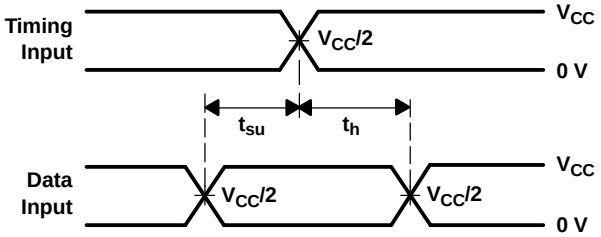
(1) Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

PARAMETER MEASUREMENT INFORMATION FOR A PORT
V_{CCA} = 2.5 V ± 0.2 V AND V_{CCB} = 3.3 V ± 0.3 V

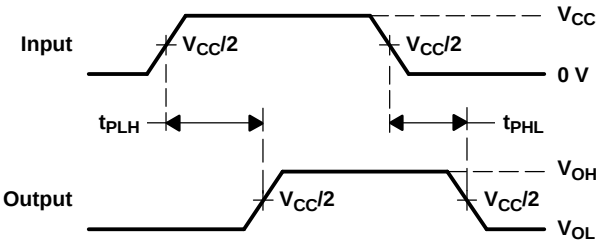


LOAD CIRCUIT

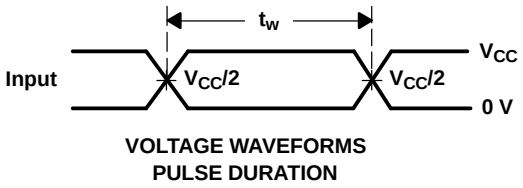
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



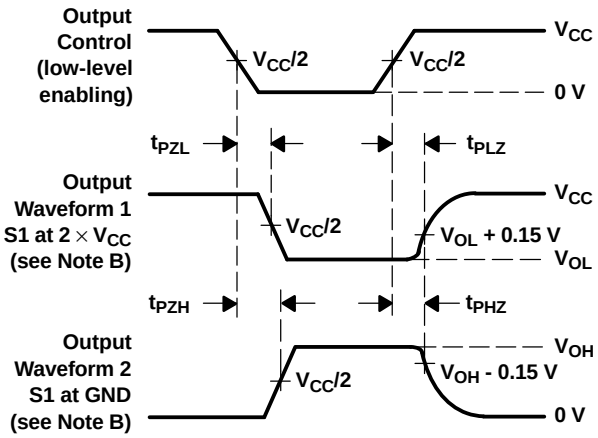
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

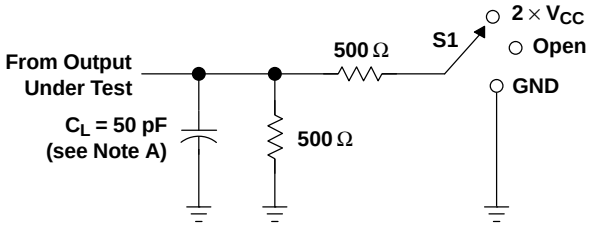


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

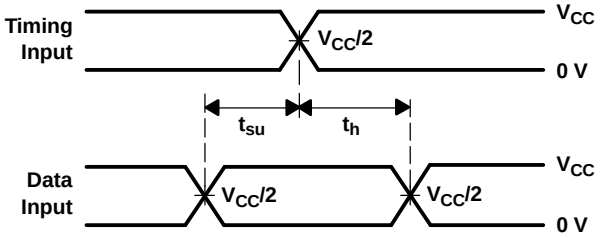
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION FOR B PORT
V_{CCA} = 2.5 V ± 0.2 V AND V_{CCB} = 3.3 V ± 0.3 V

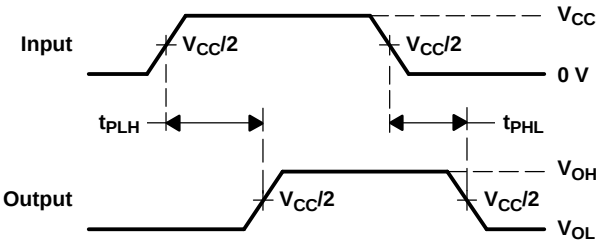


LOAD CIRCUIT

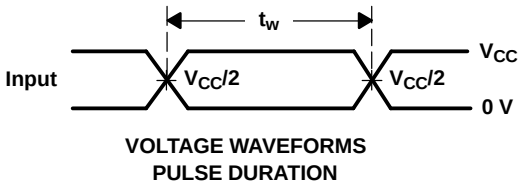
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



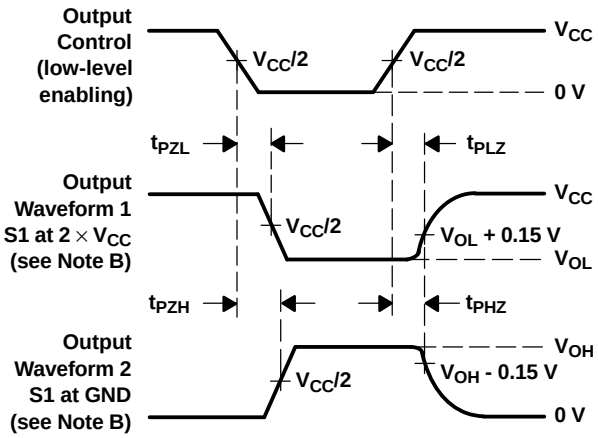
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

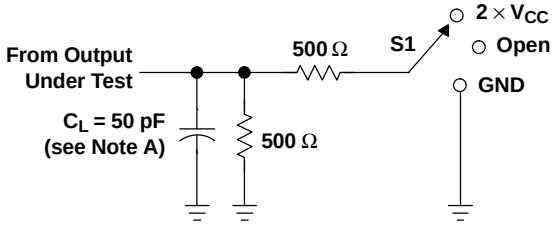


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

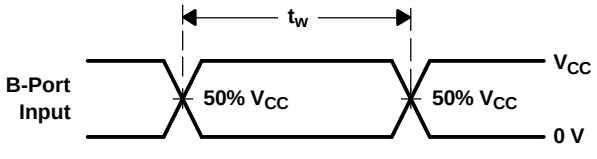
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION FOR B PORT
V_{CCA} = 3.6 V and v_{CCB} = 5.5 V

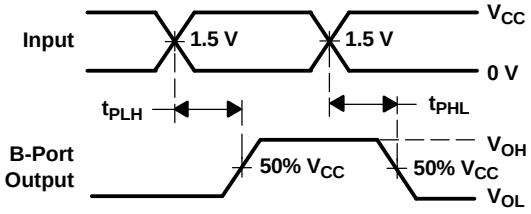


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open

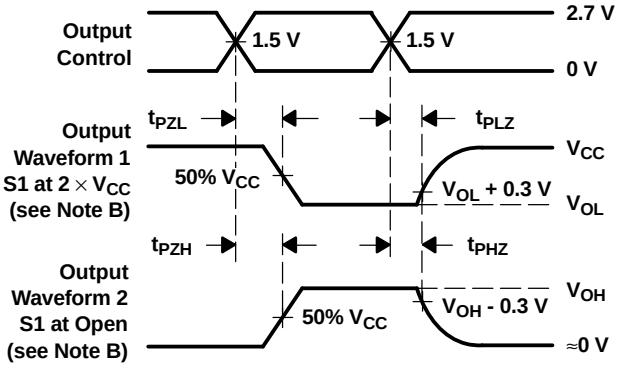
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

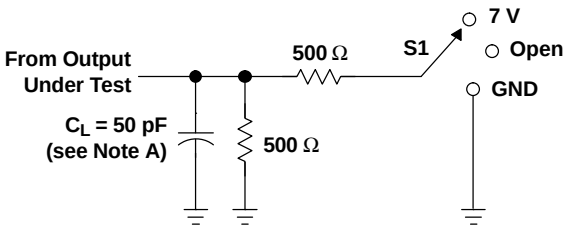


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

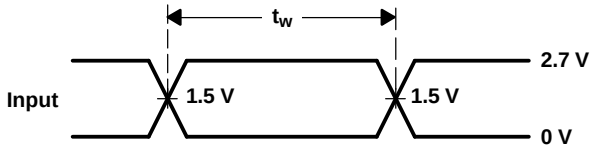
Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION FOR A AND B PORT
V_{CCA} AND V_{CCB} = 3.6 V

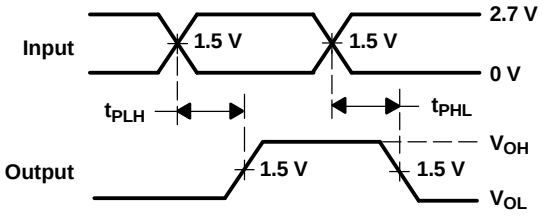


LOAD CIRCUIT

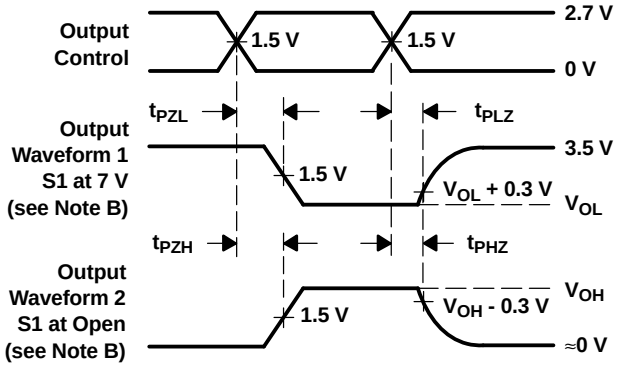
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCC3245ADBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI	-40 to 85		
SN74LVCC3245ADBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245ADBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245ADBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ADWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ANSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ANSRE4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245ANSRG4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
SN74LVCC3245APW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWLE	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		
SN74LVCC3245APWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCC3245APWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWT	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples
SN74LVCC3245APWTG4	ACTIVE	TSSOP	PW	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVCC3245A :

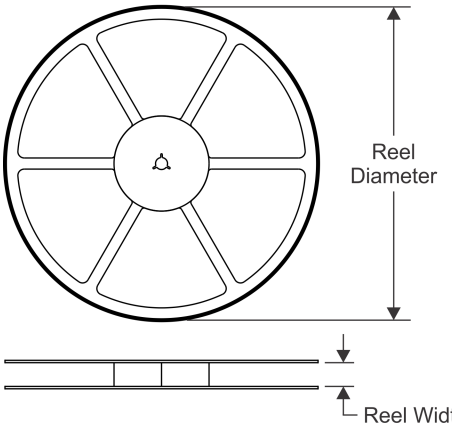
- Enhanced Product: SN74LVCC3245A-EP

NOTE: Qualified Version Definitions:

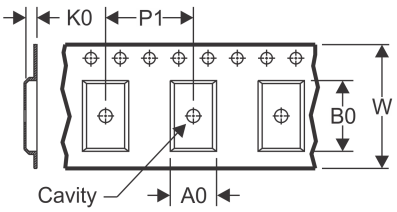
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

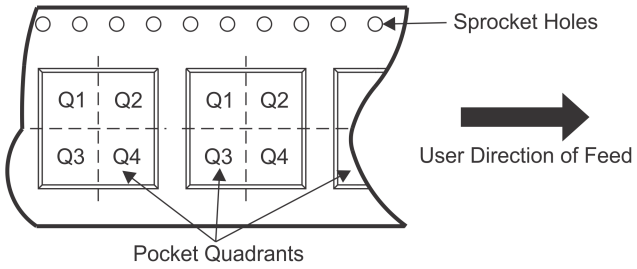


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

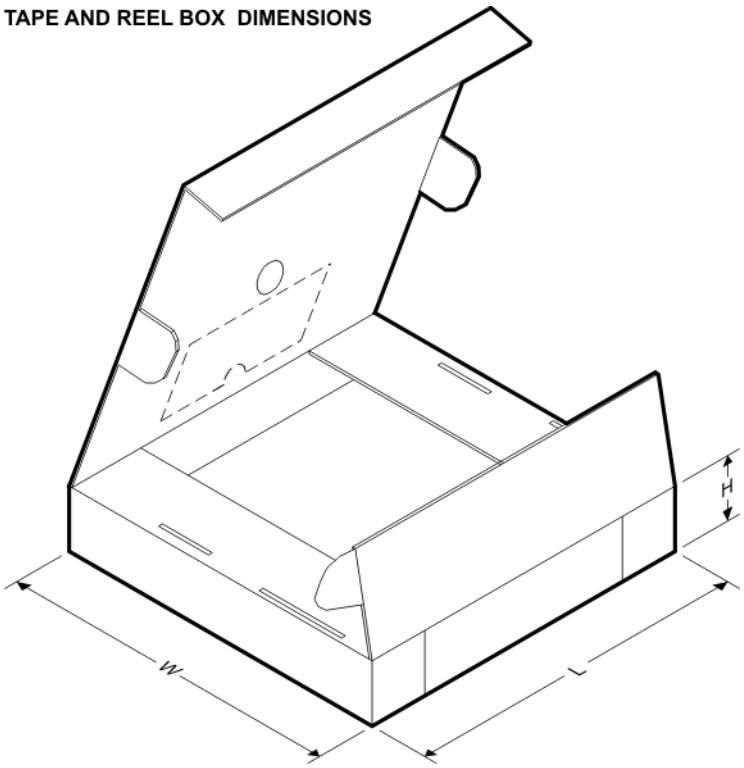
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCC3245ADBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVCC3245ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVCC3245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ADWRG4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVCC3245ANSR	SO	NS	24	2000	330.0	24.4	8.2	15.4	2.5	12.0	24.0	Q1
SN74LVCC3245APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVCC3245APWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

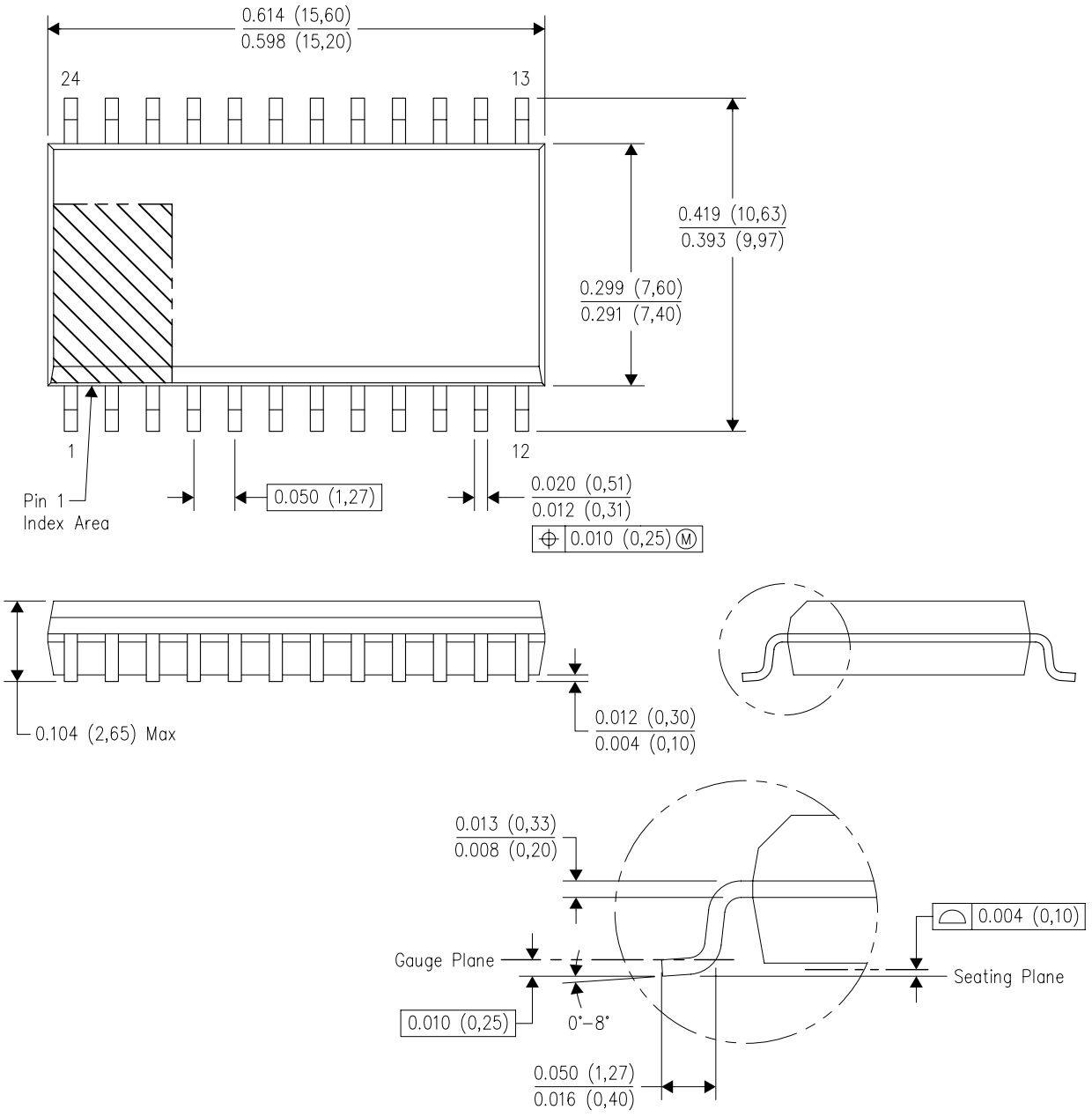
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

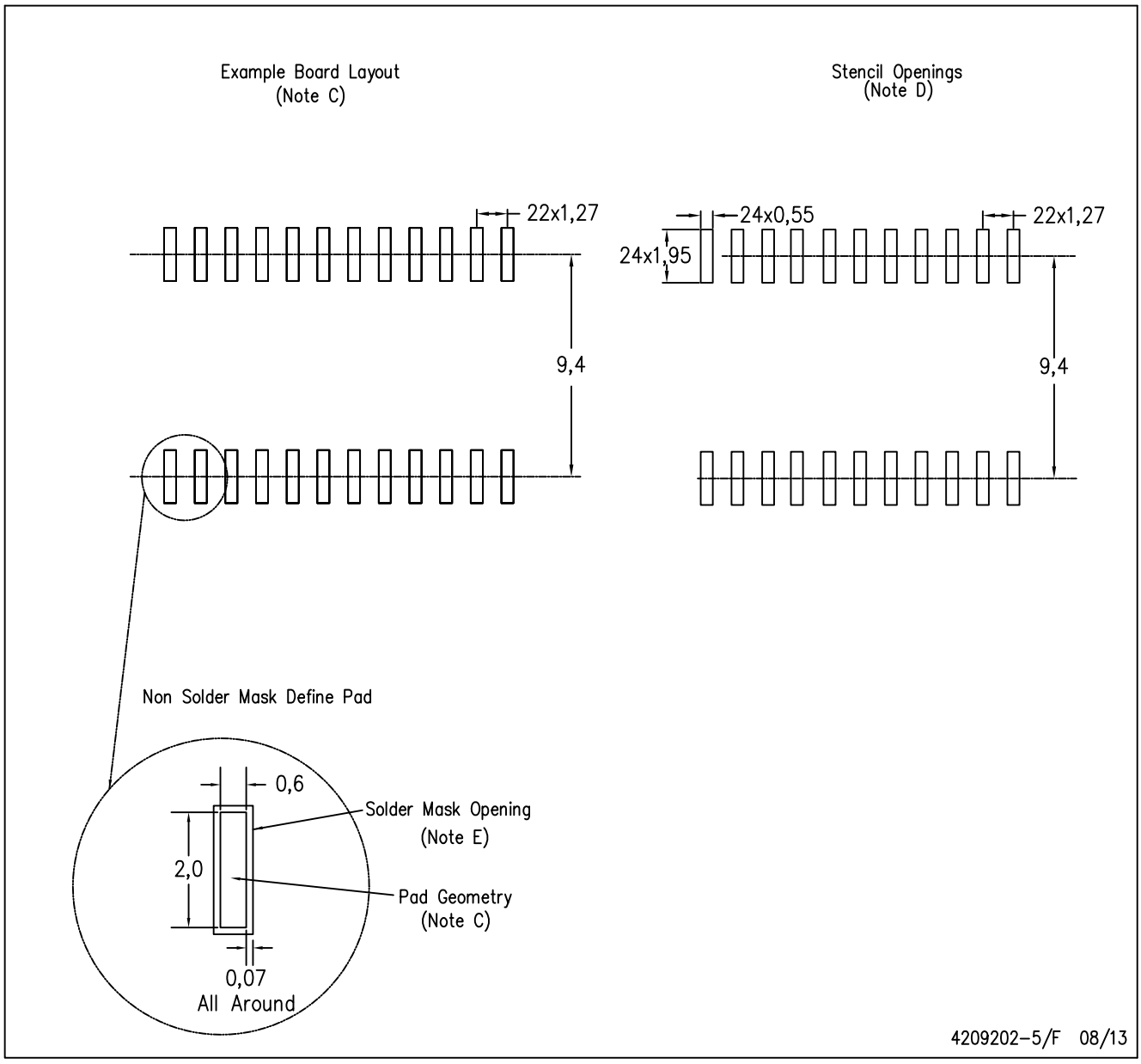
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCC3245ADBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
SN74LVCC3245ADBR	SSOP	DB	24	2000	367.0	367.0	38.0
SN74LVCC3245ADWR	SOIC	DW	24	2000	367.0	367.0	45.0
SN74LVCC3245ADWR	SOIC	DW	24	2000	366.0	364.0	50.0
SN74LVCC3245ADWRG4	SOIC	DW	24	2000	367.0	367.0	45.0
SN74LVCC3245ANSR	SO	NS	24	2000	367.0	367.0	45.0
SN74LVCC3245APWR	TSSOP	PW	24	2000	367.0	367.0	38.0
SN74LVCC3245APWT	TSSOP	PW	24	250	367.0	367.0	38.0

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



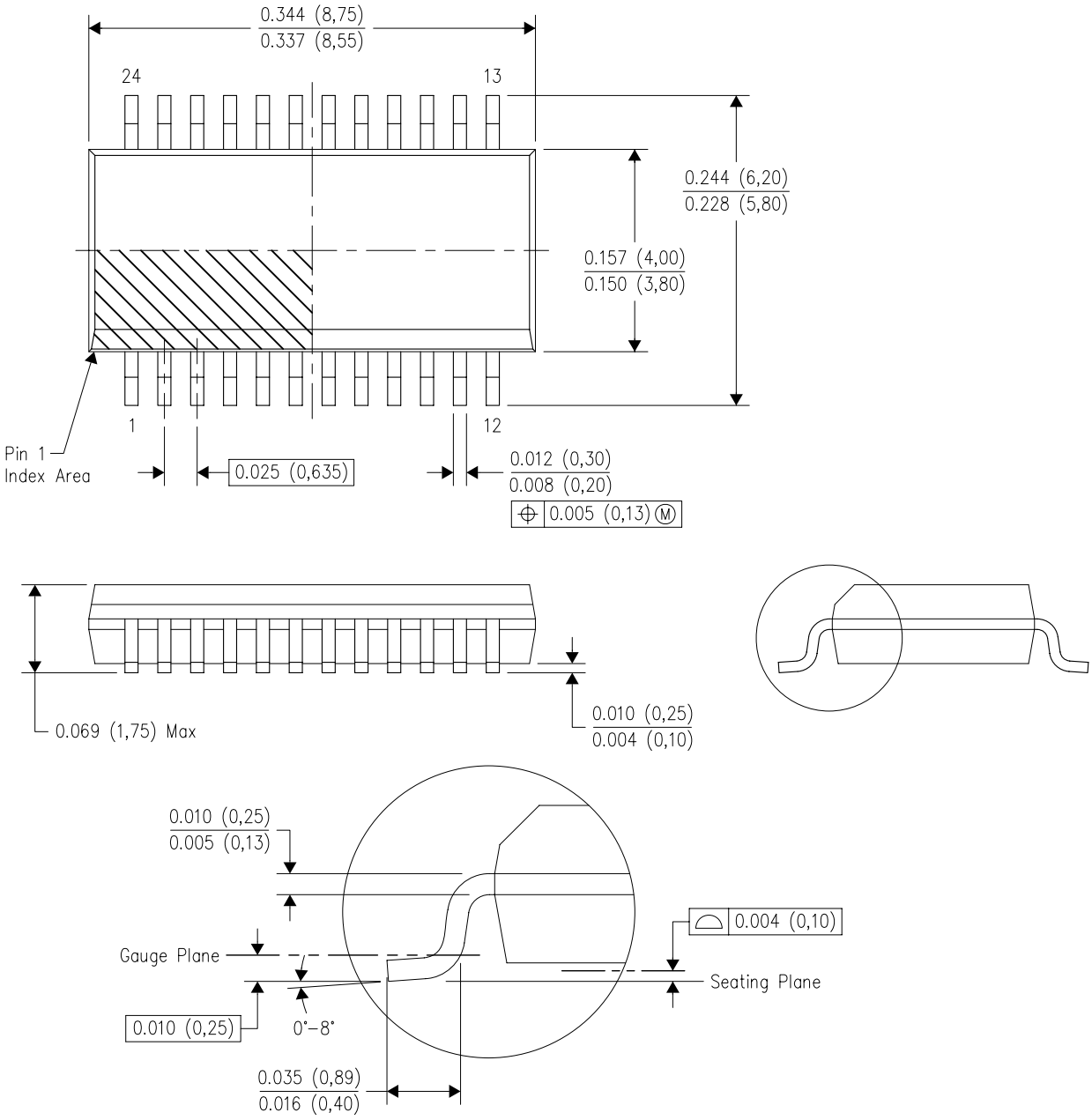
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



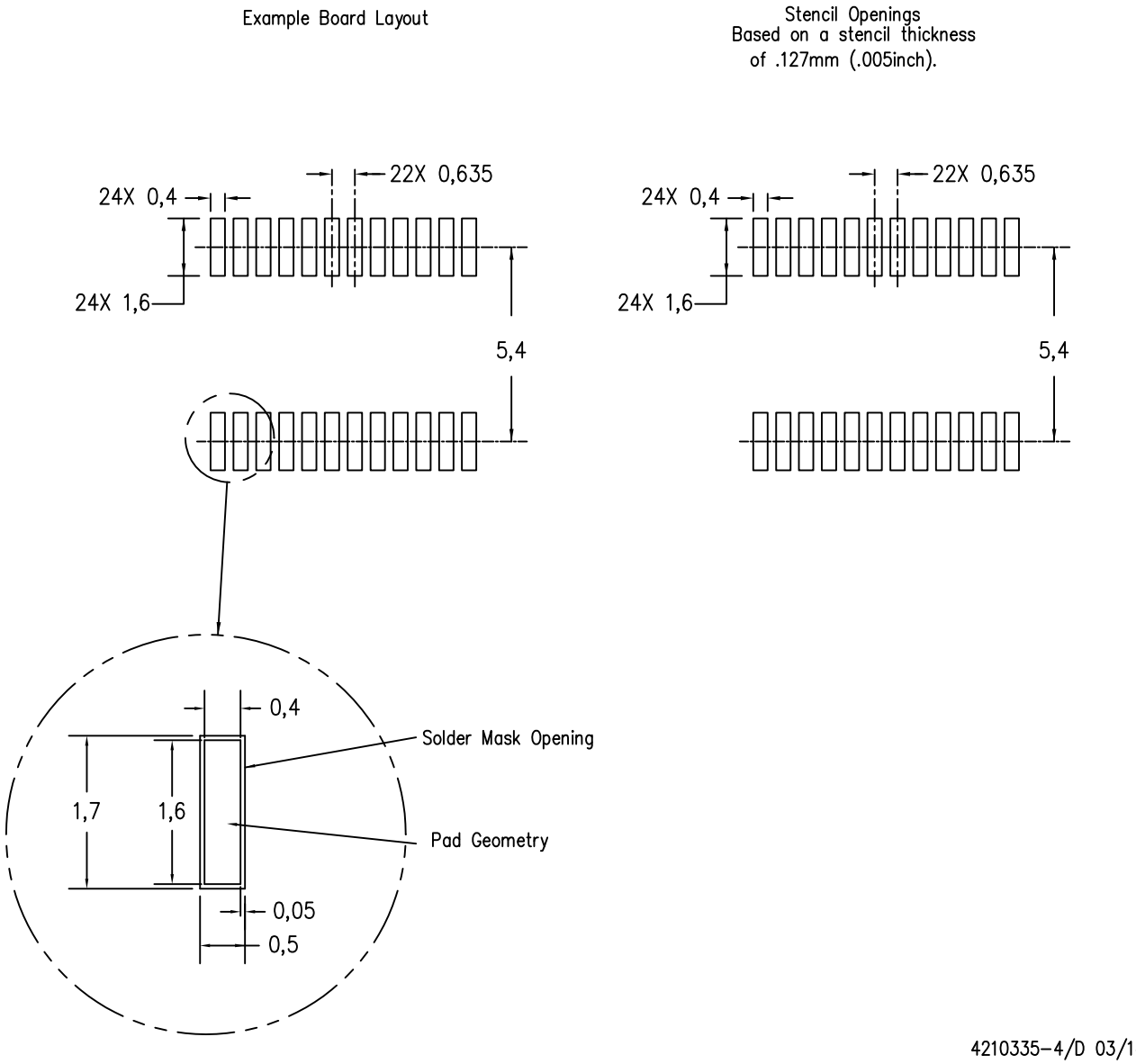
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



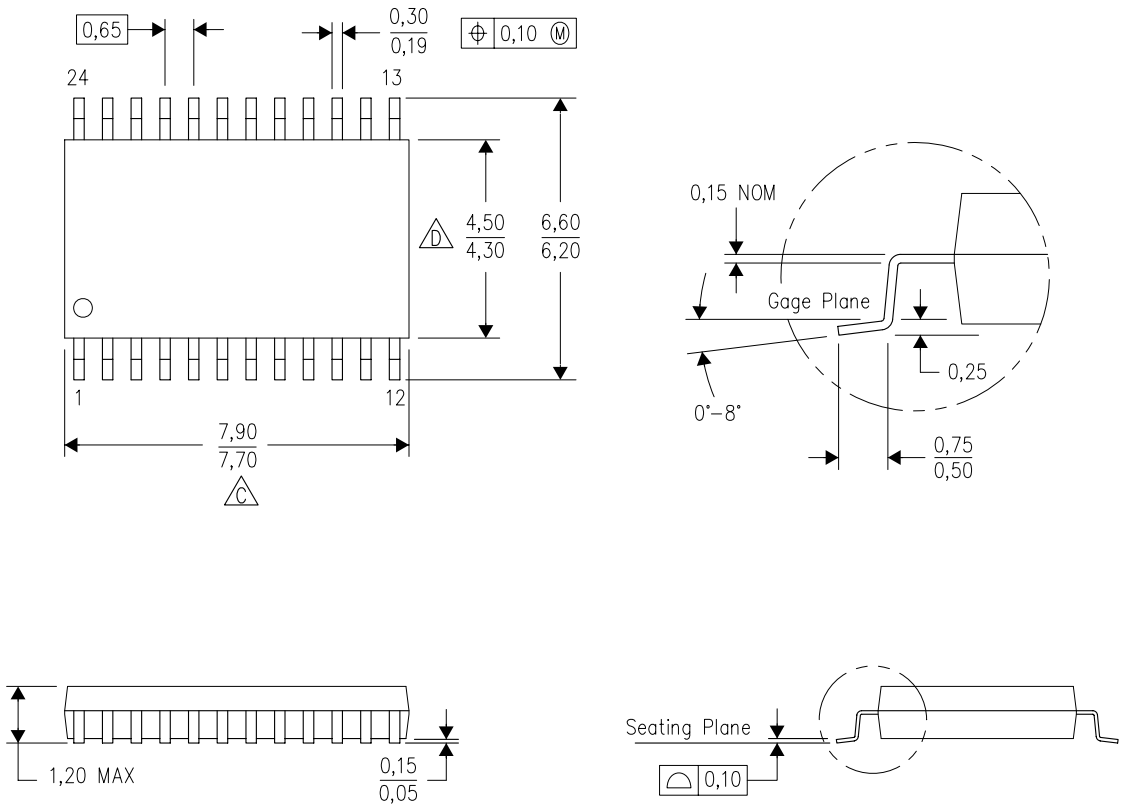
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

DBQ (R–PDSO–G24) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

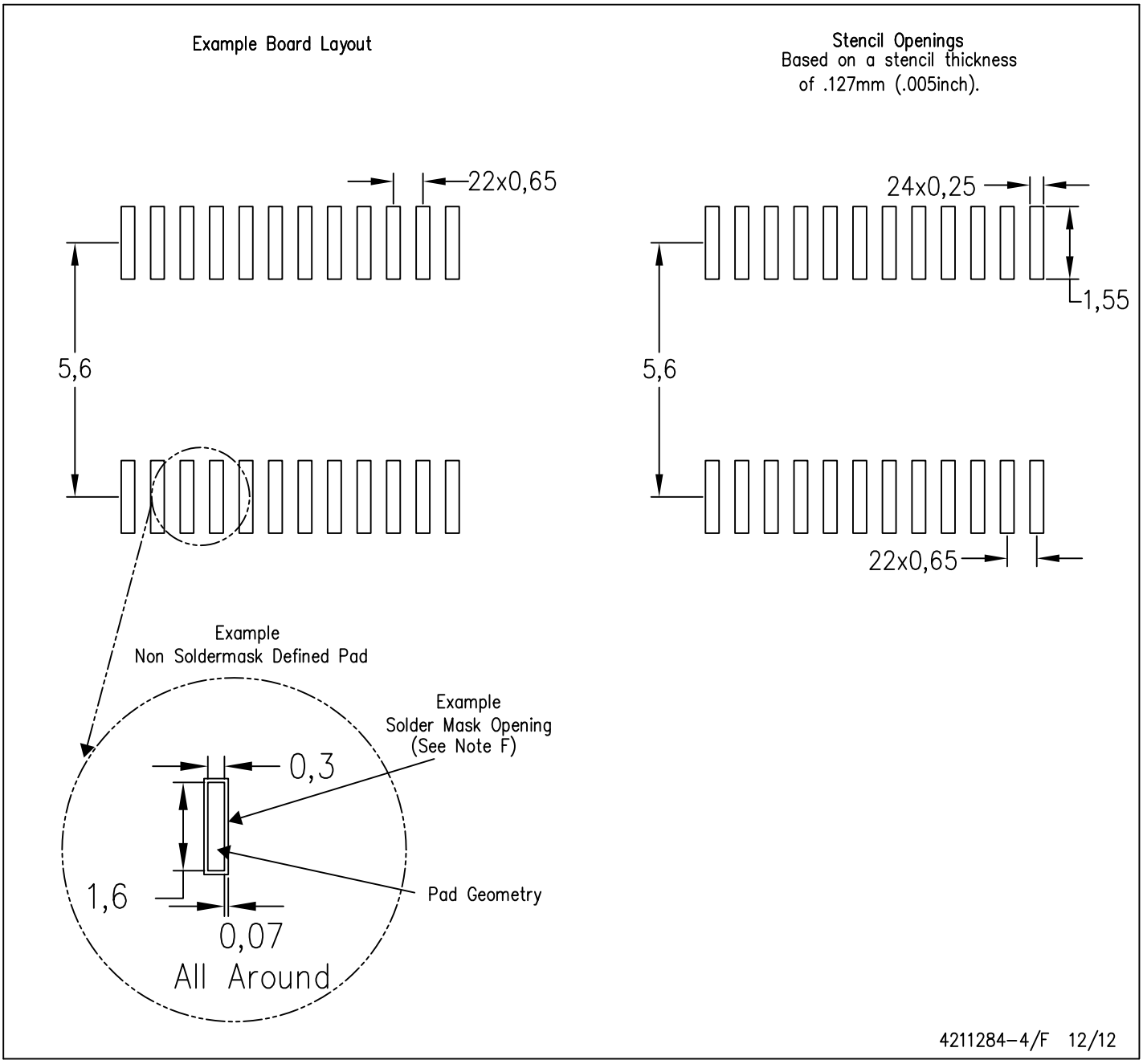
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE

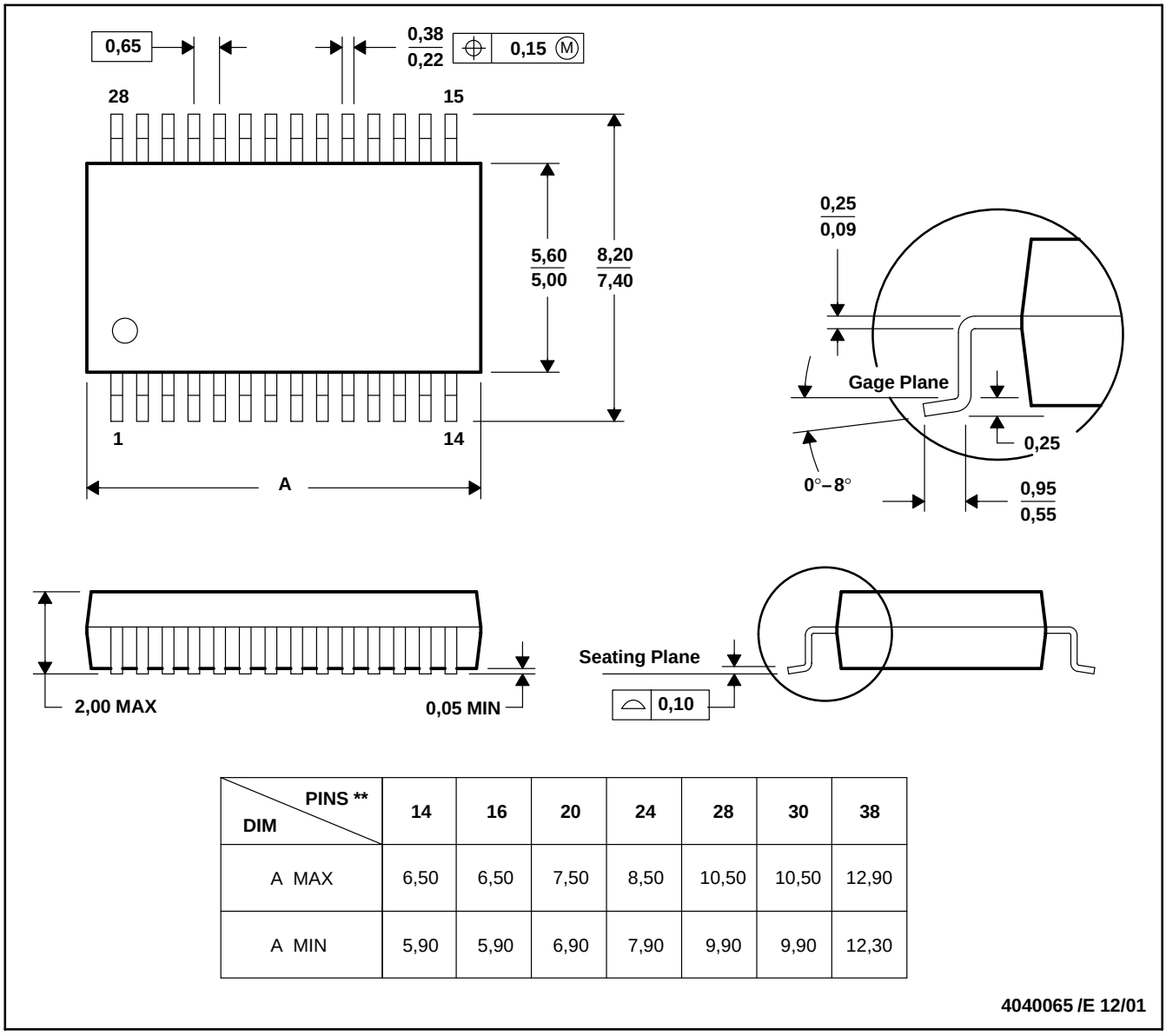


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

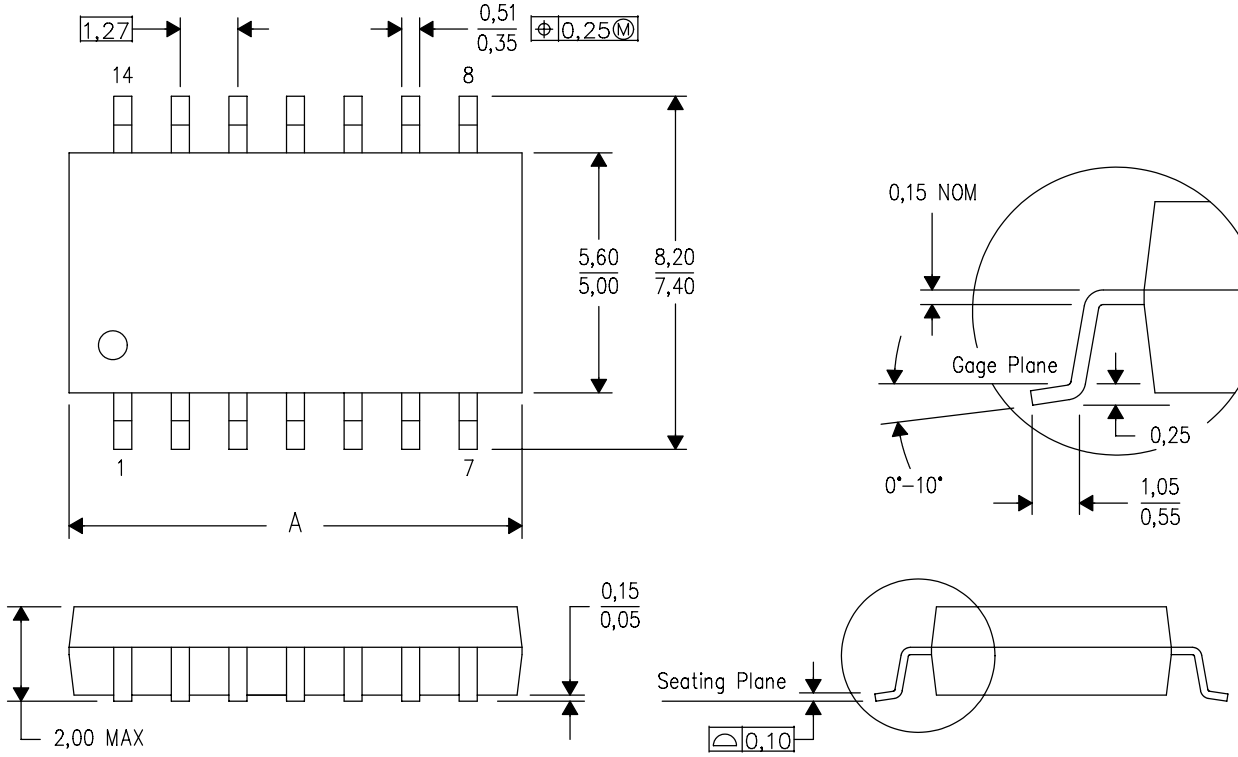
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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