

February 2008

MM74HC74A Dual D-Type Flip-Flop with Preset and Clear

Features

- Typical propagation delay: 20ns
- Wide power supply range: 2V–6V
- Low quiescent current: 40µA maximum (74HC Series)
- Low input current: 1µA maximum
- Fanout of 10 LS-TTL loads

General Description

The MM74HC74A utilizes advanced silicon-gate CMOS technology to achieve operating speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and \overline{Q} outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

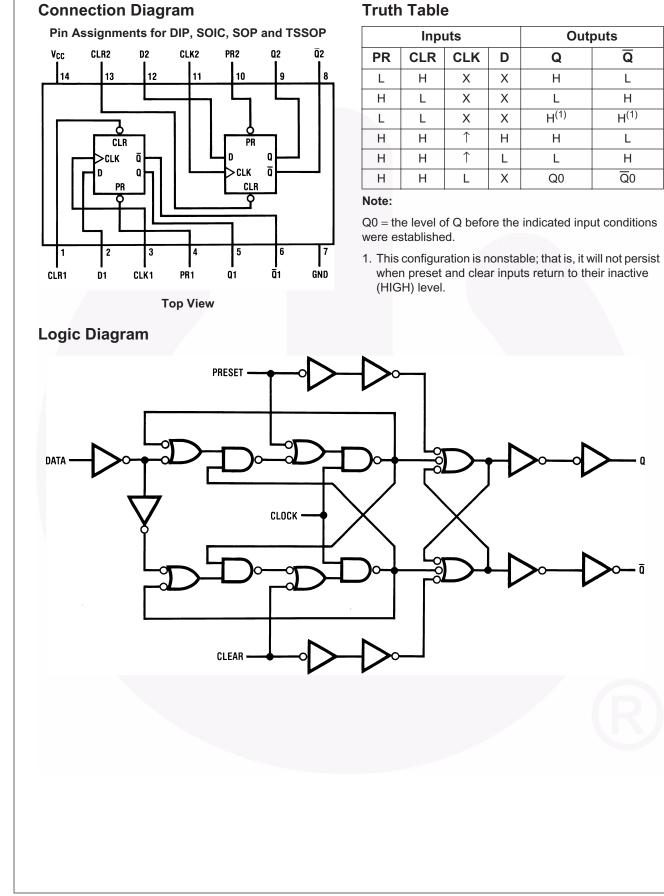
The 74HC logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to $V_{\rm CC}$ and ground.

Ordering Information

Order Number	Package Number	Package Description
MM74HC74AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC74ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC74AMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC74AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.



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Absolute Maximum Ratings⁽²⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V _{CC}	Supply Voltage	-0.5 to +7.0V
V _{IN}	DC Input Voltage	–1.5 to V _{CC} +1.5V
V _{OUT}	DC Output Voltage	–0.5 to V _{CC} +0.5V
I _{IK} , I _{OK}	Clamp Diode Current	±20mA
I _{OUT}	DC Output Current, per pin	±25mA
I _{CC}	DC V _{CC} or GND Current, per pin	±50mA
T _{STG}	Storage Temperature Range	–65°C to +150°C
P _D	Power Dissipation Note 3	600mW
	S.O. Package only	500mW
TL	Lead Temperature (Soldering 10 seconds)	260°C

Notes:

2. Unless otherwise specified all voltages are referenced to ground.

3. Power Dissipation temperature derating - plastic "N" package: -12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V _{CC}	Supply Voltage	2	6	V
V _{IN} , V _{OUT}	DC Input or Output Voltage	0	V _{CC}	V
T _A	Operating Temperature Range	-40	+85	°C
t _r , t _f	Input Rise or Fall Times $V_{CC} = 2.0V$		1000	ns
	$V_{CC} = 4.5V$		500	ns
	$V_{CC} = 6.0 V$		400	ns

				T _A =	25°C	T _A = -40°C to 85°C	T _A = –55°C to 125°C	
Symbol	Parameter	V _{CC} (V)	Conditions	Тур.		Guaranteed Limits		Units
V _{IH}	Minimum HIGH	2.0			1.5	1.5	1.5	V
	Level Input Voltage	4.5			3.15	3.15	3.15	
	voltage	6.0			4.2	4.2	4.2	
V _{IL}	Maximum LOW	2.0			0.5	0.5	0.5	V
	Level Input Voltage	4.5			1.35	1.35	1.35	
	voltage	6.0			1.8	1.8	1.8	
V _{OH}	Minimum HIGH	2.0	$V_{IN} = V_{IH}$ or V_{IL} ,	2.0	1.9	1.9	1.9	V
	Level Output Voltage	4.5	l _{OUT} ≤ 20μΑ	4.5	4.4	4.4	4.4	
	voltage	6.0		6.0	5.9	5.9	5.9	
		4.5	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $ I_{OUT} \le 4.0 \text{mA}$	4.3	3.98	3.84	3.7	
		6.0	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $ I_{OUT} \le 5.2 \text{mA}$	5.2	5.48	5.34	5.2	
V _{OL}	Maximum LOW	2.0	$V_{IN} = V_{IH}$ or V_{IL} ,	0	0.1	0.1	0.1	V
	Level Output Voltage	4.5	l _{OUT} ≤ 20μΑ	0	0.1	0.1	0.1	
	voltage	6.0		0	0.1	0.1	0.1	
		4.5	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $ I_{OUT} \le 4.0 \text{mA}$	0.2	0.26	0.33	0.4	
		6.0	$ V_{IN} = V_{IH} \text{ or } V_{IL},$ $ O_{UT} \le 5.2 \text{mA}$	0.2	0.26	0.33	0.4	
I _{IN}	Maximum Input Current	6.0	$V_{IN} = V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$		4.0	40	80	μA

Note:

4. For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

 $V_{CC} = 5V, T_A = 25^{\circ}C, C_L = 15pF, t_r = t_f = 6ns$

Symbol	Parameter	Conditions	Тур.	Guaranteed Limit	Units
f _{MAX}	Maximum Operating Frequency		72	30	MHz
t _{PHL} , t _{PLH}	Maximum Propagation, Delay Clock to Q or \overline{Q}		10	30	ns
t _{PHL} , t _{PLH}	Maximum Propagation, Delay Preset or Clear to Q or \overline{Q}		17	40	ns
t _{REM}	Minimum Removal Time, Preset or Clear to Clock		6	5	ns
t _s	Minimum Setup Time, Data to Clock		10	20	ns
t _H	Minimum Hold Time, Clock to Data		0	0	ns
t _W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC Electrical Characteristics

 $C_L = 50 \text{ pF}, t_r = t_f = 6ns \text{ (unless otherwise specified)}$

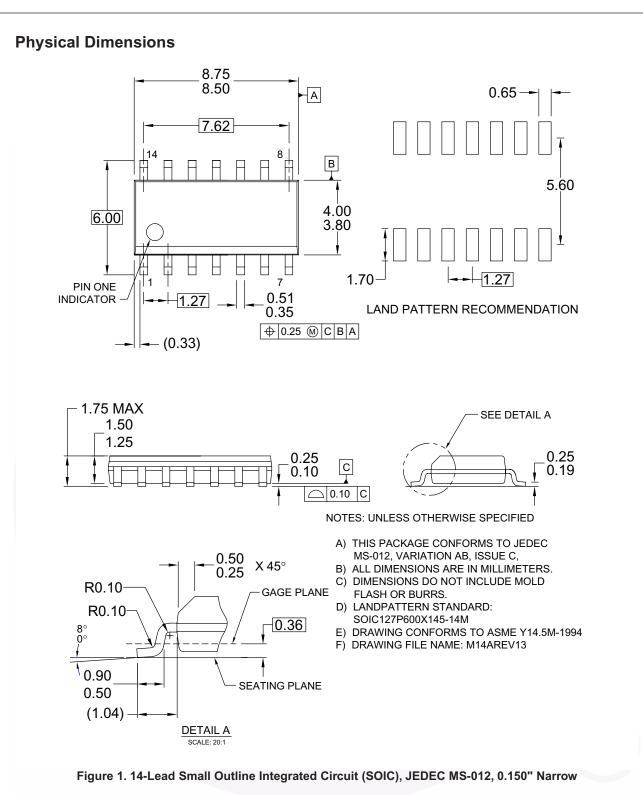
				T _A =	25°C	T _A =-40°C to 85°C	T _A = -55°C to 125°C	
Symbol	Parameter	Conditions	V _{CC} (V)	Тур.		Guaranteed	Limits	Units
f _{MAX}	Maximum Operating		2.0	22	6	5	4	MHz
	Frequency		4.5	72	30	24	20	
			6.0	94	35	28	24	
t _{PHL} , t _{PLH}	Maximum Propagation		2.0	34	110	140	165	ns
	Delay Clock to Q or \overline{Q}		4.5	12	22	28	33	
			6.0	10	19	24	28	
t _{PHL} , t _{PLH}	Maximum Propagation		2.0	66	150	190	225	ns
	Delay Preset or Clear		4.5	20	30	38	45	1
	to Q or \overline{Q}		6.0	16	26	33	38	1
t _{REM}	Minimum Removal		2.0	20	50	65	75	ns
	Time, Preset or Clear		4.5	6	10	13	15	1
	to Clock		6.0	5	9	11	13	
t _s	Minimum Setup Time		2.0	35	80	100) 120 r	ns
	Data to Clock		4.5	10	16	20	24	
			6.0	8	14	17	20	
t _H	Minimum Hold Time		2.0		0	0	0	ns
	Clock to Data		4.5		0	0	0	
			6.0		0	0	0	
t _W	Minimum, Pulse Width		2.0	30	80	101	119	ns
	Clock, Preset or Clear		4.5	9	16	20	24	
			6.0	8	14	17	20	
t _{TLH} , t _{THL}	Maximum Output		2.0	25	75	95	110	ns
	Rise and Fall Time		4.5V	7	15	19	22	
			6.0V	6	13	16	19	
	Maximum Input Rise		2.0		1000	1000	1000	ns
	and Fall Time		4.5		500	500	500	
			6.0		400	400	400	
C _{PD}	Power Dissipation Capacitance ⁽⁵⁾	(per flip-flop)		80				pF
C _{IN}	Maximum Input Capacitance			5	10	10	10	pF

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Note:

5. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

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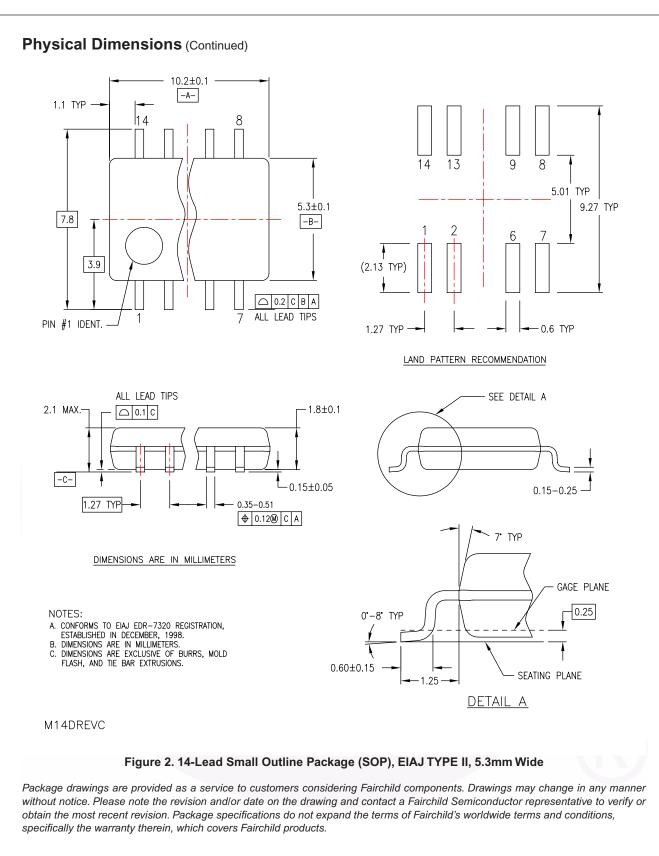


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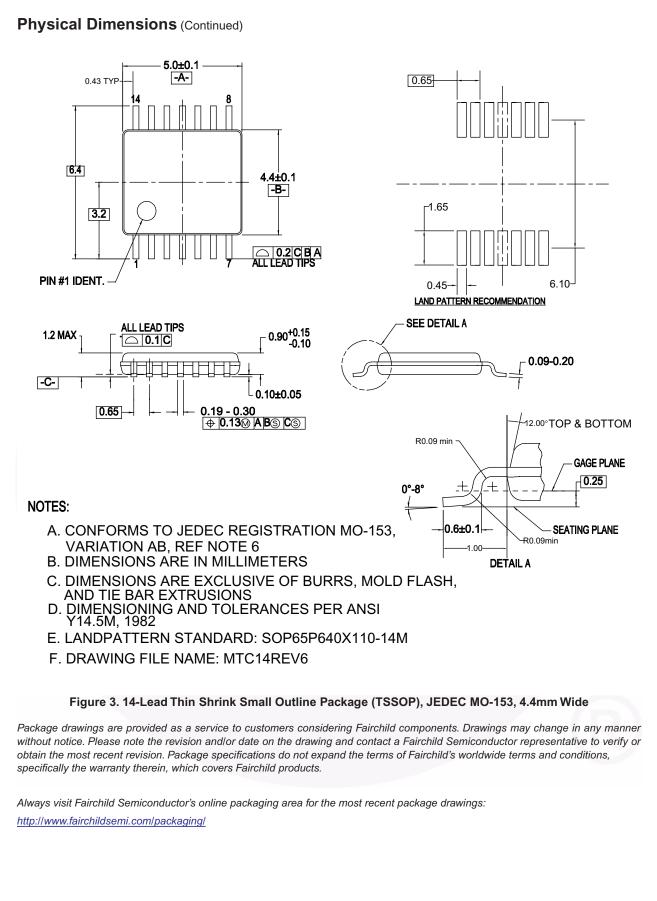
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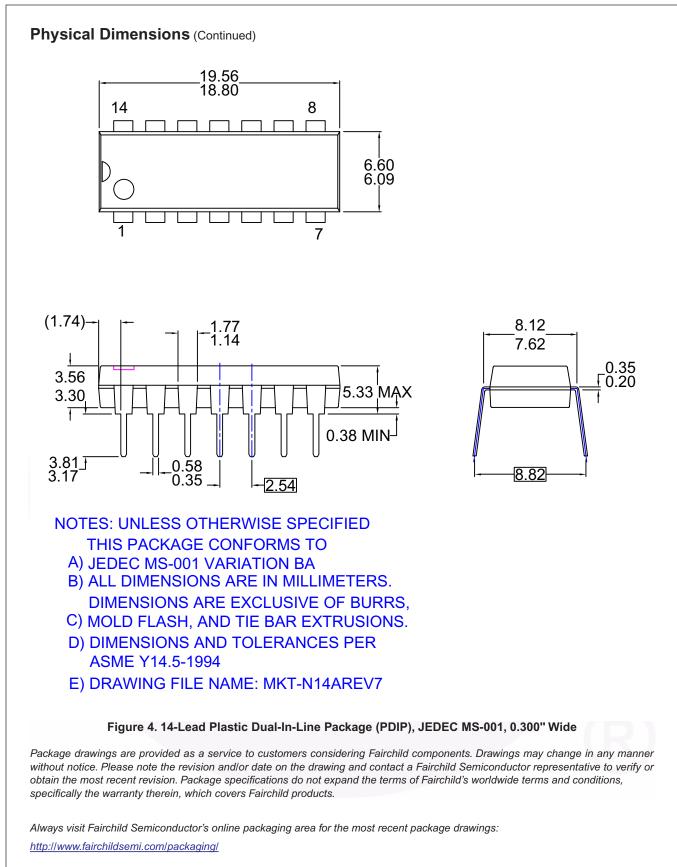
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MM74HC74A Rev. 1.3.0





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