

Spansion® Analog and Microcontroller Products



The following document contains information on Spansion analog and microcontroller products. Although the document is marked with the name "Fujitsu", the company that originally developed the specification, Spansion will continue to offer these products to new and existing customers.

Continuity of Specifications

There is no change to this document as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal document improvements and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

Spansion continues to support existing part numbers beginning with "MB". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local sales office for additional information about Spansion memory, analog, and microcontroller products and solutions.

ASSP

Single Serial Input PLL Frequency Synthesizer On-chip 1.2 GHz Prescaler

MB15E03SL

■ DESCRIPTION

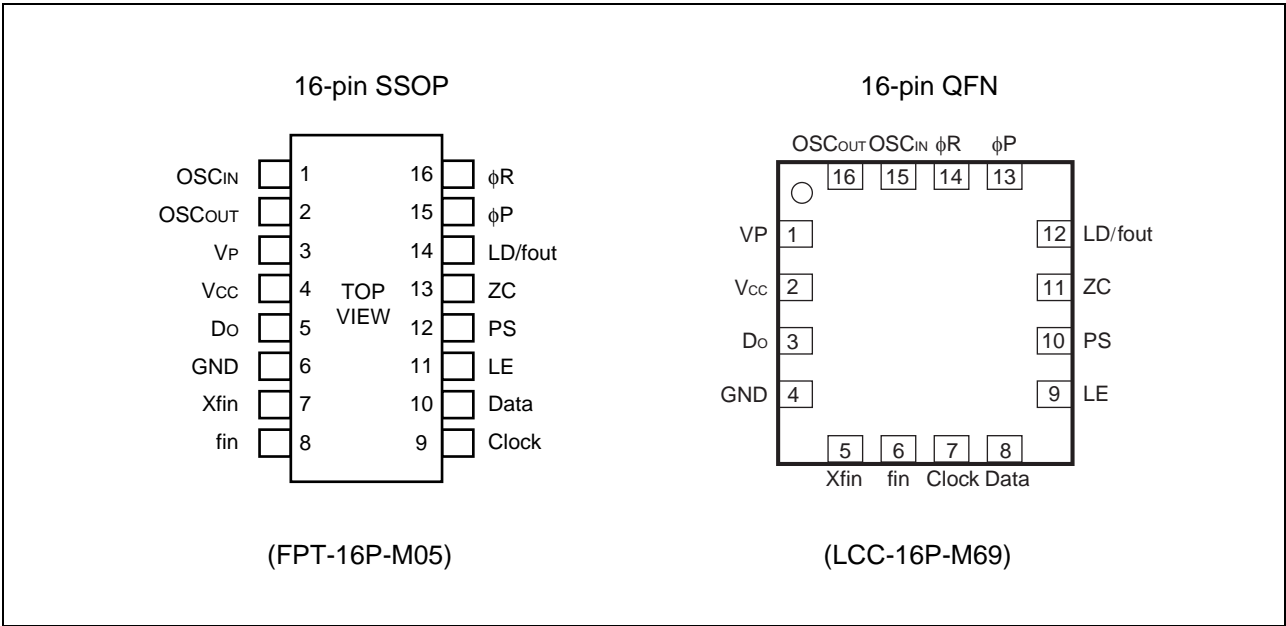
The Fujitsu Semiconductor MB15E03SL is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 1.2 GHz prescaler. The 1.2 GHz prescaler has a dual modulus division ratio of 64/65 or 128/129 enabling pulse swallowing operation.

The supply voltage range is between 2.4 V and 3.6 V. The MB15E03SL uses the latest BiCMOS process, as a result, the supply current is typically 2.0 mA at 2.7 V. A refined charge pump supplies a well balanced output currents of 1.5 mA or 6 mA. The charge pump current is selectable by serial data.

■ FEATURES

- High frequency operation: 1.2 GHz max
- Low power supply voltage: $V_{CC} = 2.4 \text{ V to } 3.6 \text{ V}$
- Ultra Low power supply current: $I_{CC} = 2.0 \text{ mA typ.}$ ($V_{CC} = V_P = 2.7 \text{ V}$, $T_a = +25^\circ\text{C}$, in locking state)
 $I_{CC} = 2.5 \text{ mA typ.}$ ($V_{CC} = V_P = 3 \text{ V}$, $T_a = +25^\circ\text{C}$, in locking state)
- Direct power saving function: Power supply current in power saving mode
Typ. $0.1 \mu\text{A}$ ($V_{CC} = V_P = 3 \text{ V}$, $T_a = +25^\circ\text{C}$), Max. $10 \mu\text{A}$ ($V_{CC} = V_P = 3 \text{ V}$)
- Dual modulus prescaler: 64/65 or 128/129
- Serial input 14-bit programmable reference divider: $R = 3 \text{ to } 16,383$
- Serial input programmable divider consisting of:
 - Binary 7-bit swallow counter: 0 to 127
 - Binary 11-bit programmable counter: 3 to 2,047
- Selectable charge pump current
- On-chip phase control for phase comparator
- Operating temperature: $T_a = -40 \text{ to } +85^\circ\text{C}$

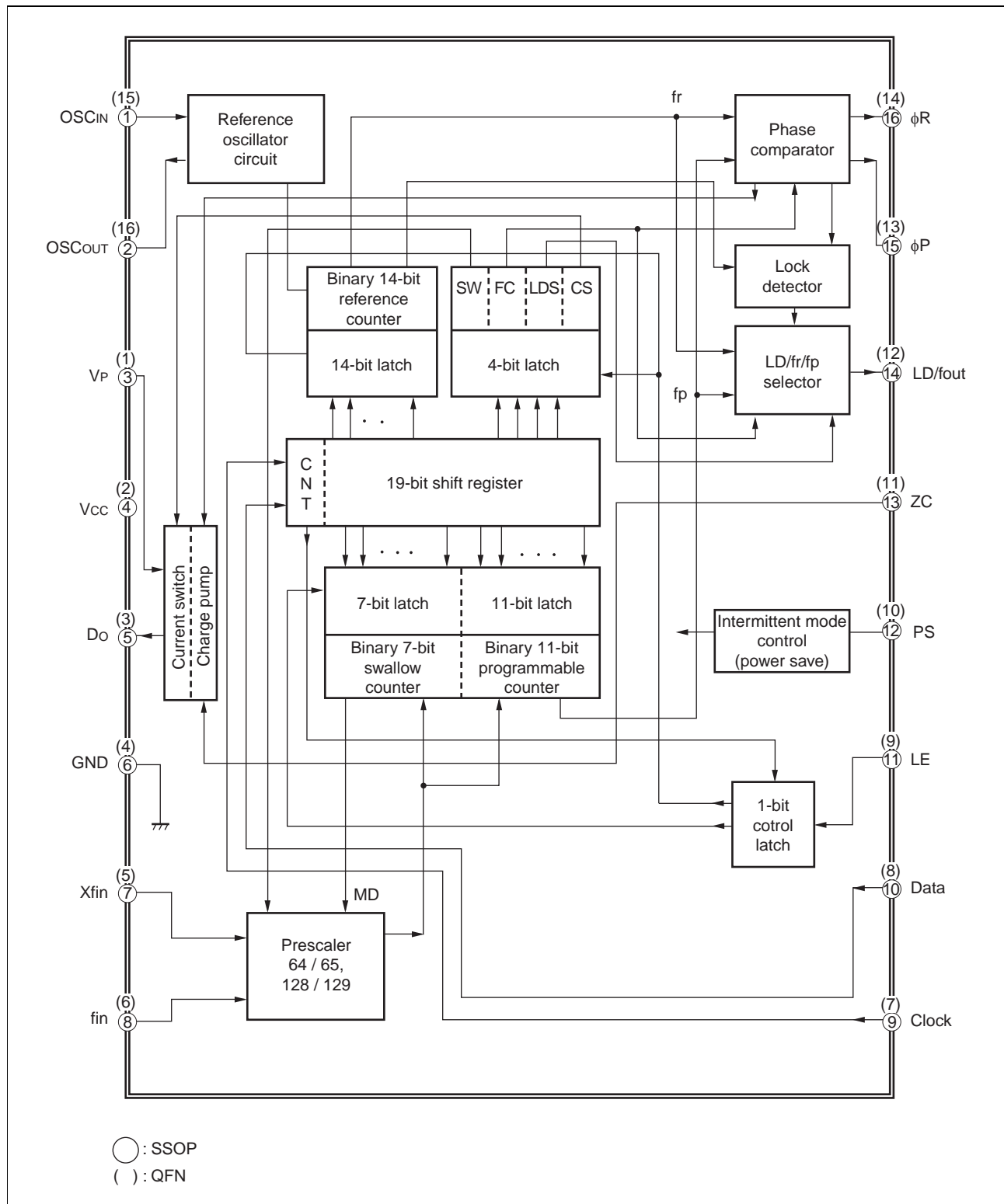
■ PIN ASSIGNMENTS



■ PIN DESCRIPTION

Pin No.		Pin Name	I/O	Descriptions
SSOP	QFN			
1	15	OSC _{IN}	I	Programmable reference divider input. Oscillator input connection to a TCXO.
2	16	OSC _{OUT}	O	Oscillator output.
3	1	V _P	—	Power supply voltage input for the charge pump.
4	2	V _{CC}	—	Power supply voltage input.
5	3	Do	O	Charge pump output. Phase of the charge pump can be selected via programming of the FC bit.
6	4	GND	—	Ground.
7	5	Xfin	I	Prescaler complementary input which should be grounded via a capacitor.
8	6	fin	I	Prescaler input. Connection to an external VCO should be done via AC coupling.
9	7	Clock	I	Clock input for the 19-bit shift register. Data is shifted into the shift register on the rising edge of the clock. (Open is prohibited.)
10	8	Data	I	Serial data input using binary code. The last bit of the data is a control bit. (Open is prohibited.)
11	9	LE	I	Load enable signal input. (Open is prohibited.) When LE is set high, the data in the shift register is transferred to a latch according to the control bit in the serial data.
12	10	PS	I	Power saving mode control. This pin must be set at “L” at Power-ON. (Open is prohibited.) PS = “H”; Normal mode PS = “L”; Power saving mode
13	11	ZC	I	Forced high-impedance control for the charge pump (with internal pull up resistor.) ZC = “H”; Normal Do output. ZC = “L”; Do becomes high impedance.
14	12	LD/fout	O	Lock detect signal output (LD)/phase comparator monitoring output (fout). The output signal is selected via programming of the LDS bit. LDS = “H”; outputs fout (fr/fp monitoring output) LDS = “L”; outputs LD (“H” at locking, “L” at unlocking.)
15	13	φP	O	Phase comparator N-channel open drain output for an external charge pump. Phase can be selected via programming of the FC bit.
16	14	φR	O	Phase comparator CMOS output for an external charge pump. Phase can be selected via programming of the FC bit.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit	Remark
			Min.	Max.		
Power supply voltage	V_{CC}	—	−0.5	4.0	V	
	V_P	—	V_{CC}	6.0	V	
Input voltage	V_I	—	−0.5	$V_{CC} + 0.5$	V	
Output voltage	V_O	Except Do	GND	V_{CC}	V	
	V_O	Do	GND	V_P	V	
Storage temperature	T_{stg}	—	−55	+125	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.4	3.0	3.6	V	
	V_P	V_{CC}	—	5.5	V	
Input voltage	V_I	GND	—	V_{CC}	V	
Operating temperature	T_a	−40	—	+85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

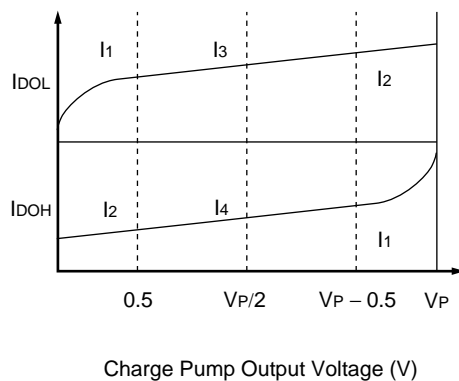
($V_{CC} = 2.4$ to 3.6 V, $T_a = -40$ to $+85^\circ\text{C}$)

Parameter		Symbol	Condition		Value			Unit
					Min.	Typ.	Max.	
Power supply current*1		I _{CC}	V _{CC} = V _P = 2.7 V (V _{CC} = V _P = 3.0 V)		—	2.0 (2.5)	—	mA
Power saving current		I _{PS}	ZC = “H” or open		—	0.1*2	10	μA
Operating frequency	f _{in}	f _{in}	—		100	—	1200	MHz
	OSC _{IN}	f _{OSC}	—		3	—	40	MHz
Input sensitivity	f _{in} *3	P _f in	50 Ω system (Refer to the Measurment circuit.)		−15	—	+2	dBm
	OSC _{IN} *3	V _{OSC}	—		0.5	—	V _{CC}	Vp-p
“H” level input voltage	Data, Clock, LE, PS, ZC	V _{IH}	—		V _{CC} × 0.7	—	—	V
“L” level input voltage		V _{IL}	—		—	—	V _{CC} × 0.3	
“H” level input current	Data, Clock, LE, PS	I _{IH} *4	—		−1.0	—	+1.0	μA
“L” level input current		I _{IL} *4	—		−1.0	—	+1.0	
“H” level input current	OSC _{IN}	I _{IH}	—		0	—	+100	μA
“L” level input current		I _{IL} *4	—		−100	—	0	
“H” level input current	ZC	I _{IH} *4	—		−1.0	—	+1.0	μA
“L” level input current		I _{IL} *4	Pull up input		−100	—	0	
“L” level output voltage	φP	V _{OL}	Open drain output		—	—	0.4	V
“H” level output voltage	φR, LD/fout	V _{OH}	V _{CC} = V _P = 3 V, I _{OH} = −1 mA		V _{CC} − 0.4	—	—	V
“L” level output voltage		V _{OL}	V _{CC} = V _P = 3 V, I _{OL} = 1 mA		—	—	0.4	
“H” level output voltage	Do	V _{DOH}	V _{CC} = V _P = 3 V, I _{DOH} = −0.5 mA		V _P − 0.4	—	—	V
“L” level output voltage		V _{DOL}	V _{CC} = V _P = 3 V, I _{DOL} = 0.5 mA		—	—	0.4	
High impedance cutoff current	Do	I _{OFF}	V _{CC} = V _P = 3 V, V _{OFF} = 0.5 V to V _P − 0.5 V		—	—	2.5	nA
“L” level output current	φP	I _{OL}	Open drain output		1.0	—	—	mA
“H” level output current	φR, LD/fout	I _{OH}	—		—	—	−1.0	mA
“L” level output current		I _{OL}	—		1.0	—	—	
“H” level output current	Do	I _{DOH} *4	V _{CC} = 3 V, V _P = 3 V, V _{DO} = V _P /2 Ta = +25°C	CS bit = “H”	—	−6.0	—	mA
				CS bit = “L”	—	−1.5	—	
		I _{DOL}		CS bit = “H”	—	6.0	—	
				CS bit = “L”	—	1.5	—	
Charge pump current rate	I _{DOL} /I _{DOH}	I _{DOMT} *5	V _{DD} = V _F /2		—	3	—	%
	vs V _{DO}	I _{DOVD} *6	0.5 V ≤ V _{DO} ≤ V _P − 0.5 V		—	10	—	%
	vs Ta	I _{DOTA} *7	− 40°C ≤ Ta ≤ +85°C		—	10	—	%

(Continued)

(Continued)

- *1: Conditions; $f_{in} = 1200 \text{ MHz}$, $f_{osc} = 12 \text{ MHz}$, $T_a = +25^\circ\text{C}$, in locking state.
- *2: $V_{CC} = V_P = 3.0 \text{ V}$, $f_{osc} = 12.8 \text{ MHz}$, $T_a = +25^\circ\text{C}$, in power saving mode
- *3: AC coupling. 1000 pF capacitor is connected under the condition of min. operating frequency.
- *4: The symbol “-” (minus) means direction of current flow.
- *5: $V_{CC} = V_P = 3.0 \text{ V}$, $T_a = +25^\circ\text{C}$ $(|I_3| - |I_4|) / [(|I_3| + |I_4|) / 2] \times 100(\%)$
- *6: $V_{CC} = V_P = 3.0 \text{ V}$, $T_a = +25^\circ\text{C}$ $[(|I_2| - |I_1|) / 2] / [(|I_1| + |I_2|) / 2] \times 100(\%)$ (Applied to each I_{DOL} , I_{DOH})
- *7: $V_{CC} = V_P = 3.0 \text{ V}$, $V_{DO} = V_P/2$ $(|I_{DO(+85^\circ\text{C})} - I_{DO(-40^\circ\text{C})}| / 2) / (|I_{DO(+85^\circ\text{C})} + I_{DO(-40^\circ\text{C})}| / 2) \times 100(\%)$ (Applied to each I_{DOL} , I_{DOH})



■ FUNCTIONAL DESCRIPTION

1. Pulse Swallow Function

The divide ratio can be calculated using the following equation:

$$f_{vco} = [(M \times N) + A] \times f_{osc} \div R \quad (A < N)$$

- f_{vco} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{osc} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)
- M : Preset divide ratio of the dual modulus prescaler (64 or 128)

2. Serial Data Input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the programmable reference divider and the programmable divider separately.

Binary serial data is entered through the Data pin.

One bit of data is shifted into the shift register on the rising edge of the Clock. When the LE pin is taken high, stored data is latched according to the control bit data as follows:

Table 1. Control Bit

Control Bit (CNT)	Destination of Serial Data
H	For the programmable reference divider
L	For the programmable divider

(1) Shift Register Configuration

Programmable Reference Counter																		
<div style="display: flex; justify-content: space-between; align-items: center;"> <div> LSB ↓ </div> <div> Data Flow → </div> <div> MSB ↓ </div> </div>																		
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
CNT	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	SW	FC	LDS	CS
<div style="display: flex; justify-content: space-between;"> <div> CNT : Control bit [Table 1] R1 to R14 : Divide ratio setting bit for the programmable reference counter (3 to 16,383) [Table 2] SW : Divide ratio setting bit for the prescaler (64/65 or 128/129) [Table 5] FC : Phase control bit for the phase comparator [Table 8] LDS : LD/fout signal select bit [Table 7] CS : Charge pump current select bit [Table 6] </div> </div> <p>Note: Start data input with MSB first.</p>																		

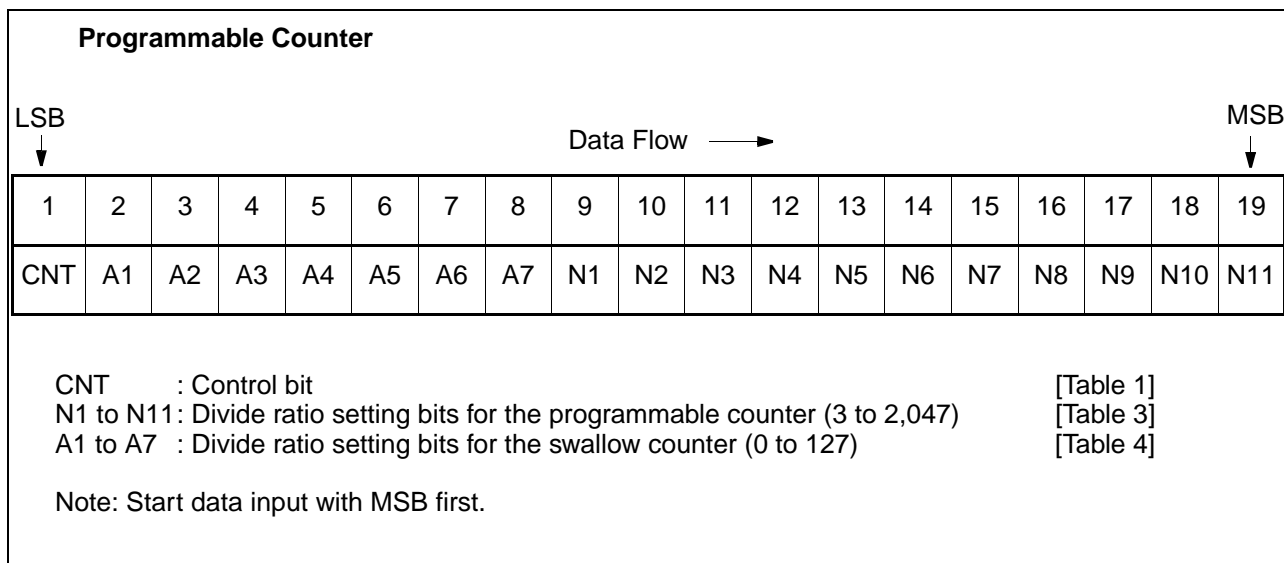


Table 2. Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio (R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Table 3. Binary 11-bit Programmable Counter Data Setting

Divide ratio (N)	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Table 4. Binary 7-bit Swallow Counter Data Setting

Divide ratio (A)	A7	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.
127	1	1	1	1	1	1	1

Table 5. Prescaler Data Setting

SW	Prescaler Divide Ratio
H	64/65
L	128/129

Table 6. Charge Pump Current Setting

CS	Current Value
H	± 6.0 mA
L	± 1.5 mA

Table 7. LD/fout Output Select Data Setting

LDS	LD/f _{OUT} Output Signal
H	f _{OUT} signal
L	LD signal

(2) Relation between the FC Input and Phase Characteristics

The FC bit changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_O) and the phase comparator output (ϕ_R , ϕ_P) are reversed according to the FC bit. Also, the monitor pin (f_{OUT}) output is controlled by the FC bit. The relationship between the FC bit and each of D_O , ϕ_R , and ϕ_P is shown below.

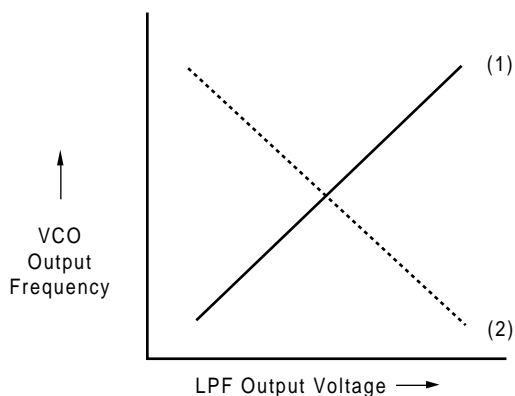
Table 8. FC Bit Data Setting (LDS = "H")

	FC = High				FC = Low			
	D_O	ϕ_R	ϕ_P	LD/f _{OUT}	D_O	ϕ_R	ϕ_P	LD/f _{OUT}
$f_r > f_p$	H	L	L	f _{OUT} = f _r	L	H	Z*	f _{OUT} = f _p
$f_r < f_p$	L	H	Z*		H	L	L	
$f_r = f_p$	Z*	L	Z*		Z*	L	Z*	

* : High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.

- When the LPF and VCO characteristics are similar to (1), set FC bit high.
- When the VCO characteristics are similar to (2), set FC bit low.



3. Do Output Control**Table 9. ZC Pin Setting**

ZC pin	Do output
H	Normal output
L	High impedance

4. Power Saving Mode (Intermittent Mode Control Circuit)

Table 10. PS Pin Setting

PS pin	Status
H	Normal mode
L	Power saving mode

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

For the signal PLL, the lock detector, LD, remains high, indicating a locked condition.

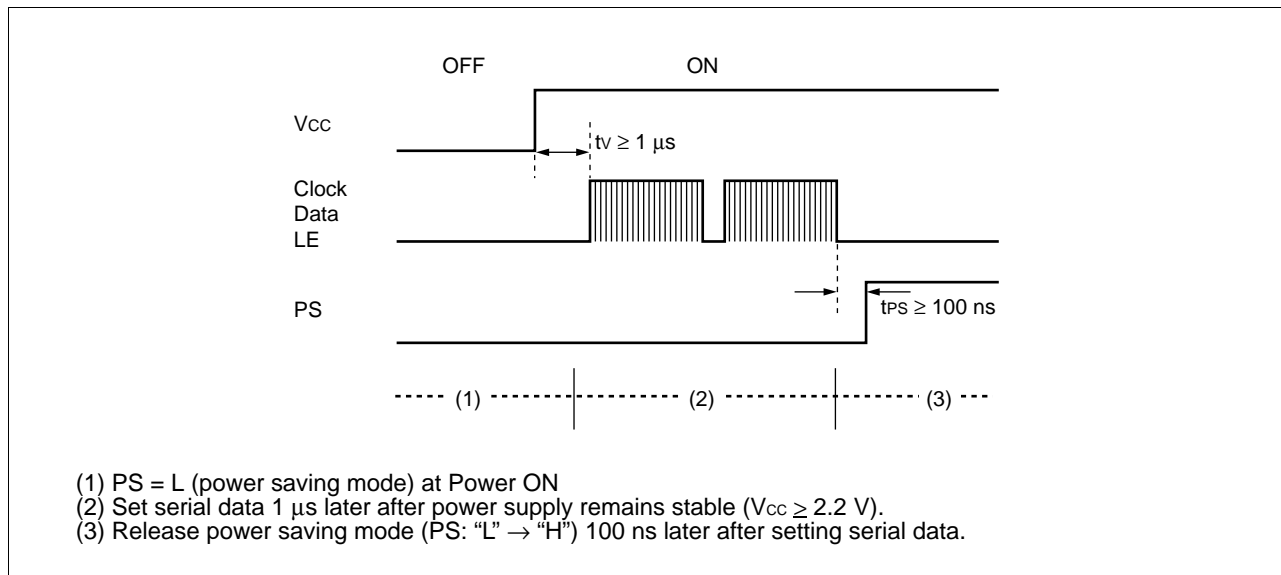
Setting the PS pin high, releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because

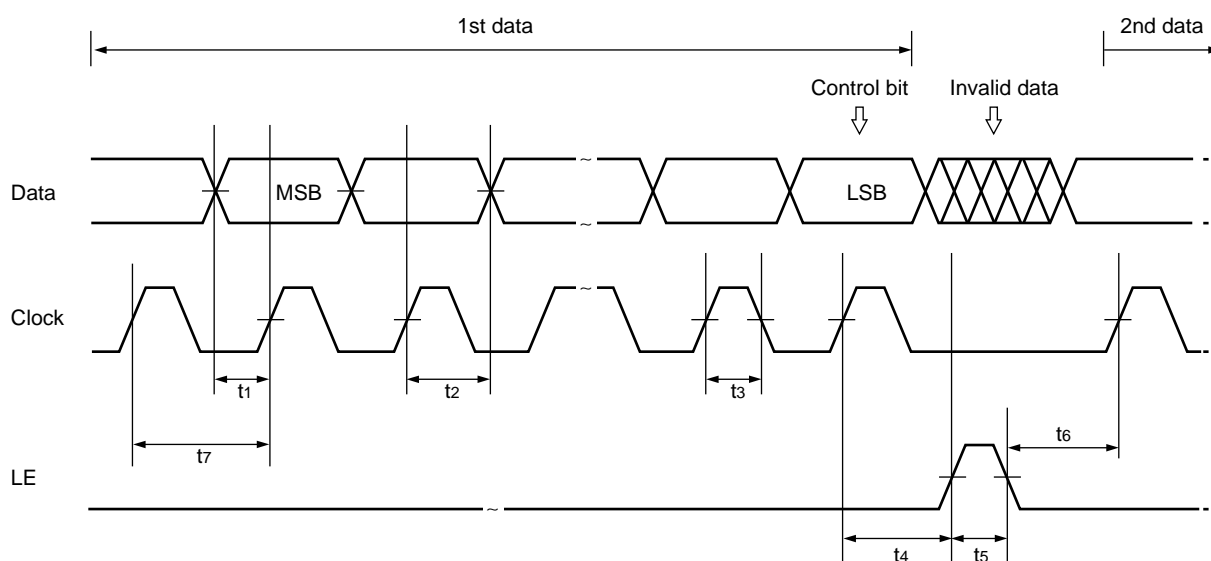
of the unknown relationship between the comparison frequency (f_p) and the reference frequency (f_r) which can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lockup time.

To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

- Notes:
- When power (V_{CC}) is first applied, the device must be in standby mode, PS = Low, for at least 1 μ s.
 - PS pin must be set "L" for Power-ON.



■ SERIAL DATA INPUT TIMING



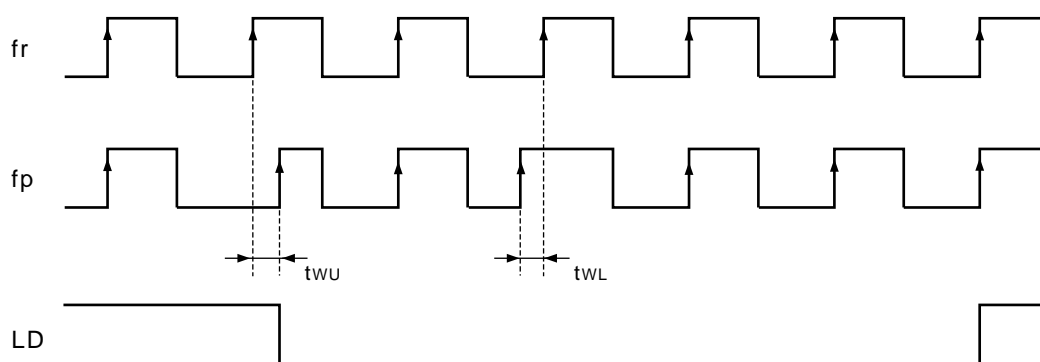
On the rising edge of the clock, one bit of data is transferred into the shift register.

Parameter	Min.	Typ.	Max.	Unit
t_1	20	—	—	ns
t_2	20	—	—	ns
t_3	30	—	—	ns
t_4	30	—	—	ns

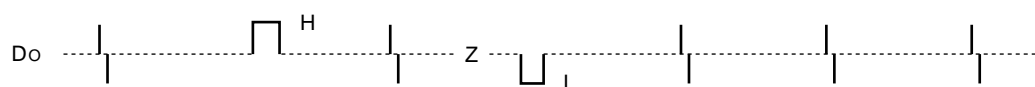
Parameter	Min.	Typ.	Max.	Unit
t_5	100	—	—	ns
t_6	20	—	—	ns
t_7	100	—	—	ns

Note: LE should be "L" when the data is transferred into the shift register.

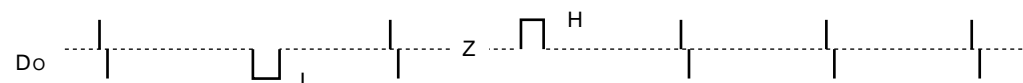
■ PHASE COMPARATOR OUTPUT WAVEFORM



[FC = "H"]

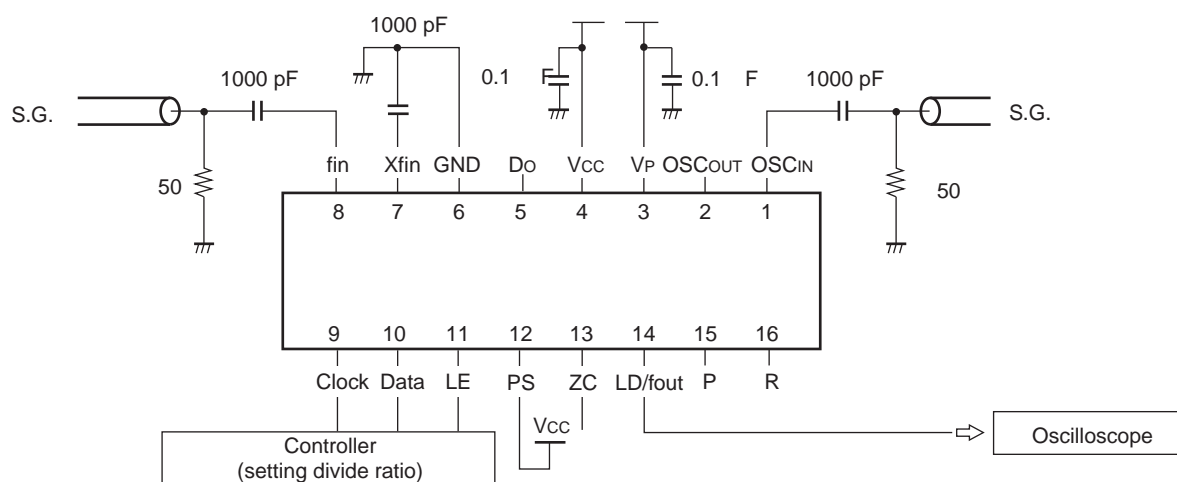


[FC = "L"]



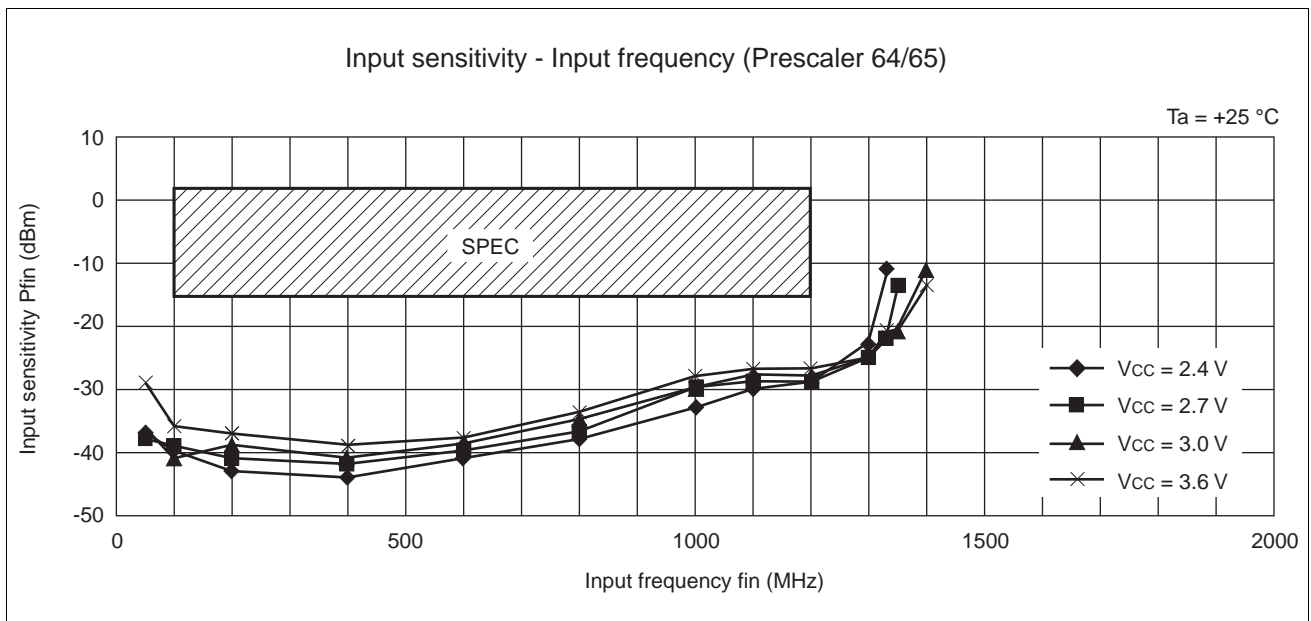
- Notes:
- Phase error detection range: -2π to $+2\pi$
 - Pulses on Do output signal during locked state are output to prevent dead zone.
 - LD output becomes low when phase is t_{wu} or more. LD output becomes high when phase error is t_{wl} or less and continues to be so for three cycles or more.
 - t_{wu} and t_{wl} depend on OSC_{IN} input frequency.
 $t_{wu} \geq 2/f_{osc}$ (s) (e. g. $t_{wu} \geq 156.3$ ns, $f_{osc} = 12.8$ MHz)
 $t_{wl} \leq 4/f_{osc}$ (s) (e. g. $t_{wl} \leq 312.5$ ns, $f_{osc} = 12.8$ MHz)
 - LD becomes high during the power saving mode ($PS = "L"$).

■ MEASUREMENT CIRCUIT (for Measuring Input Sensitivity fin/OSC_{IN})

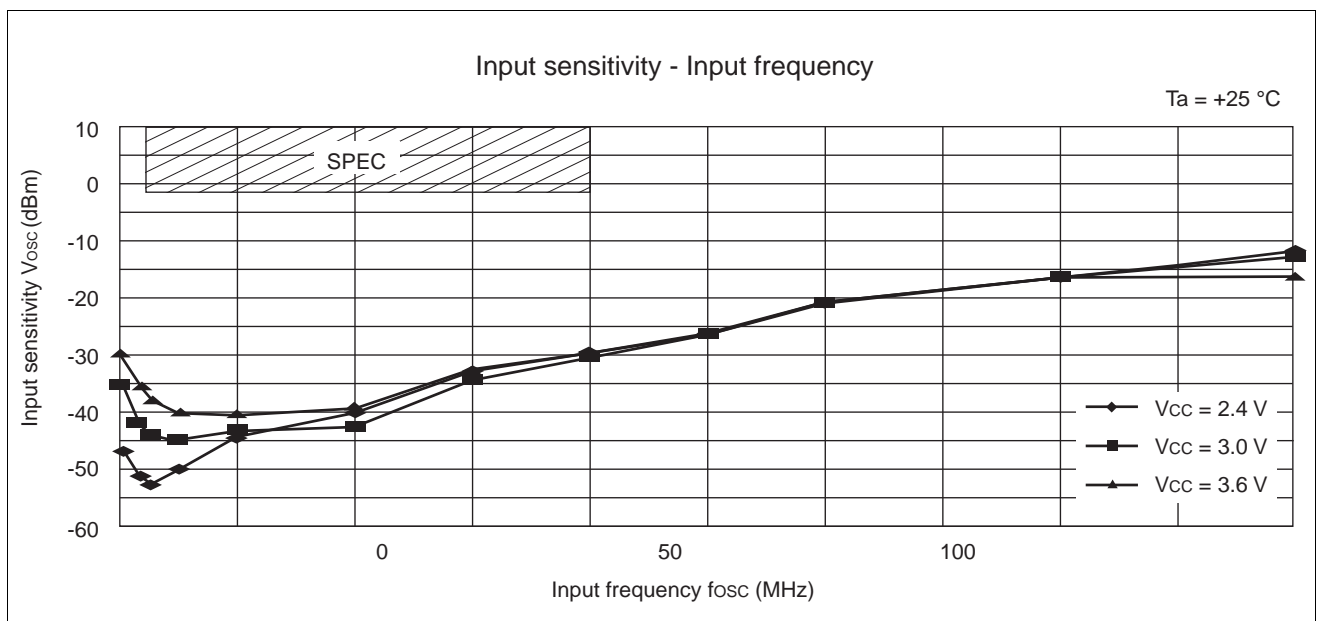


■ TYPICAL CHARACTERISTICS

1. fin input sensitivity

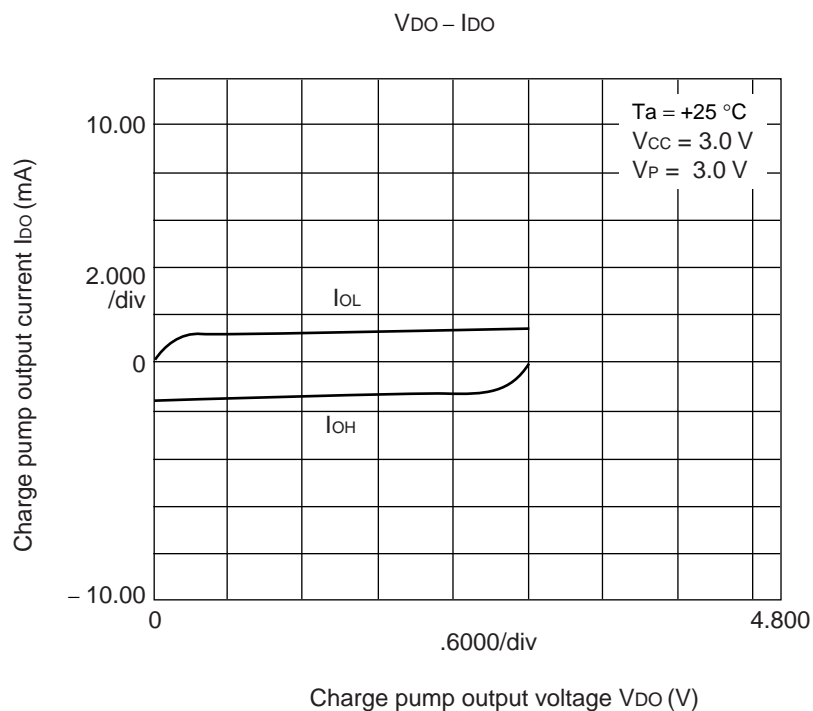


2. OSCIN input sensitivity

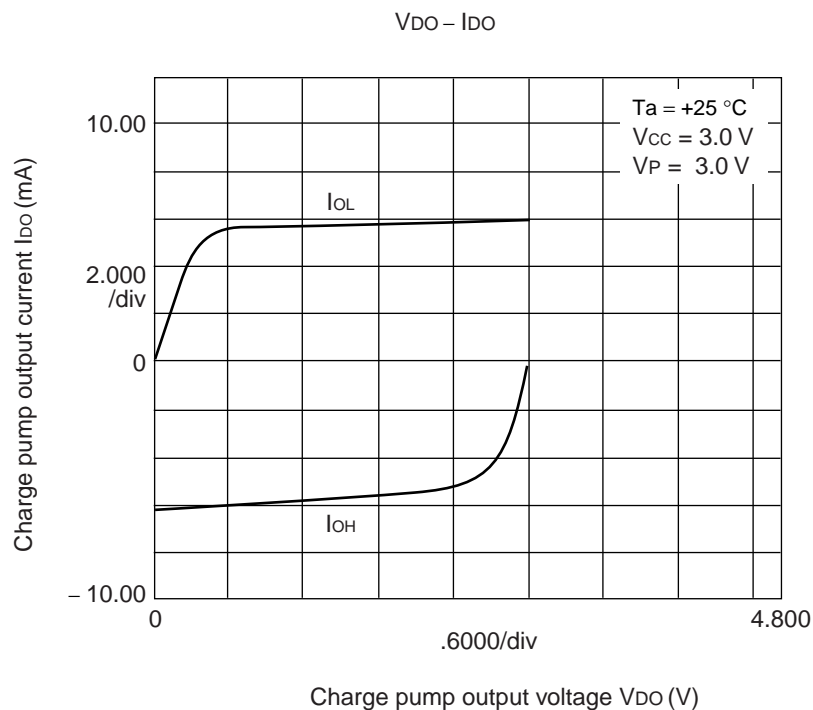


3. Do output current

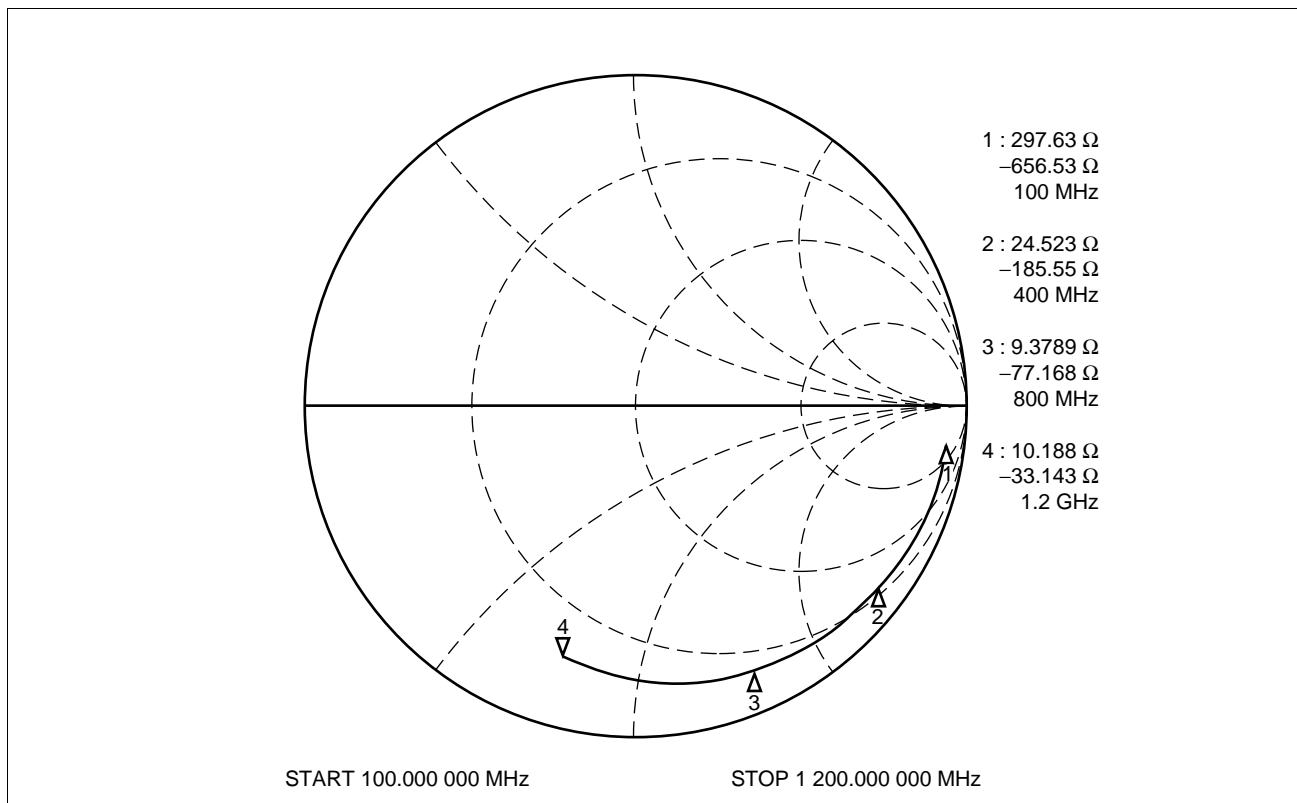
1.5 mA mode



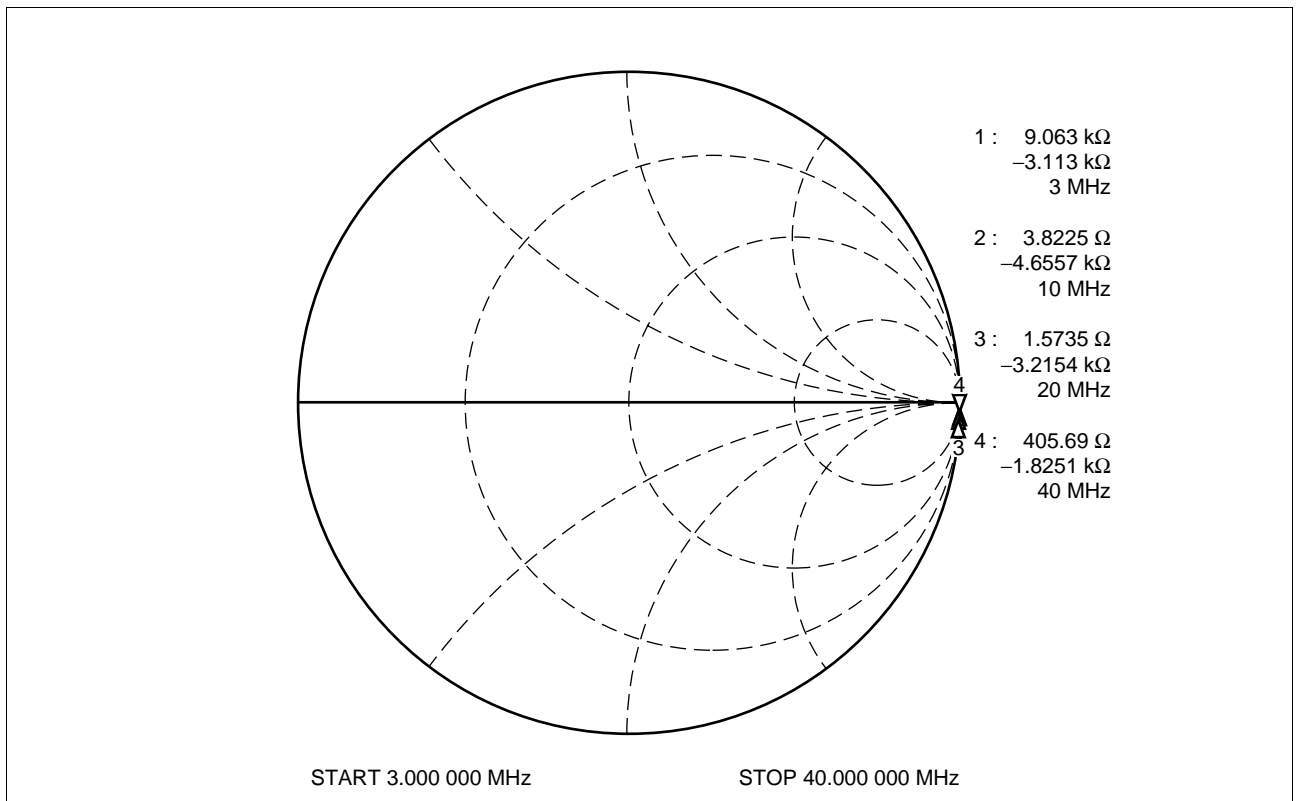
6.0 mA mode



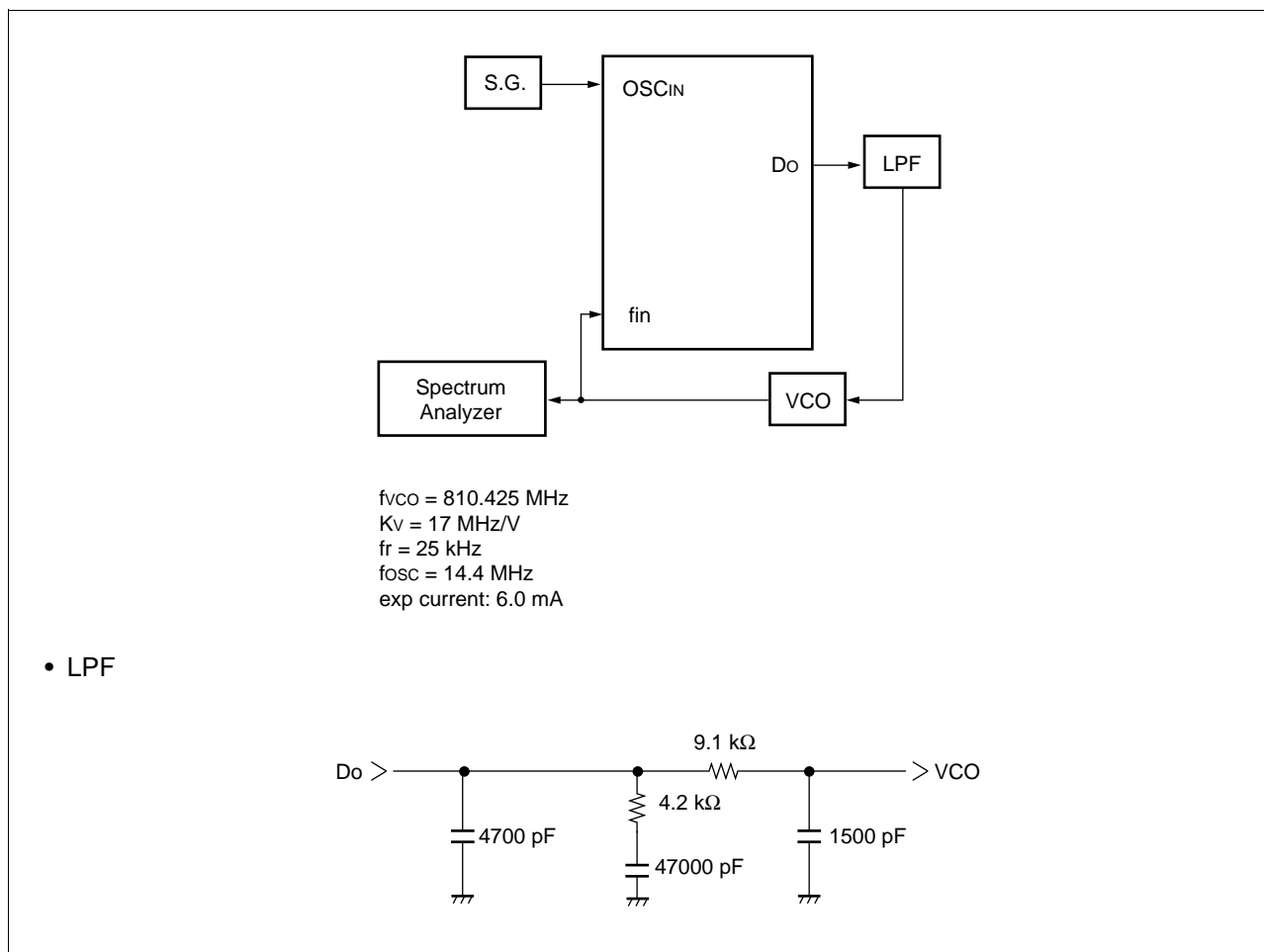
4. fin input impedance



5. OSC_{IN} input impedance

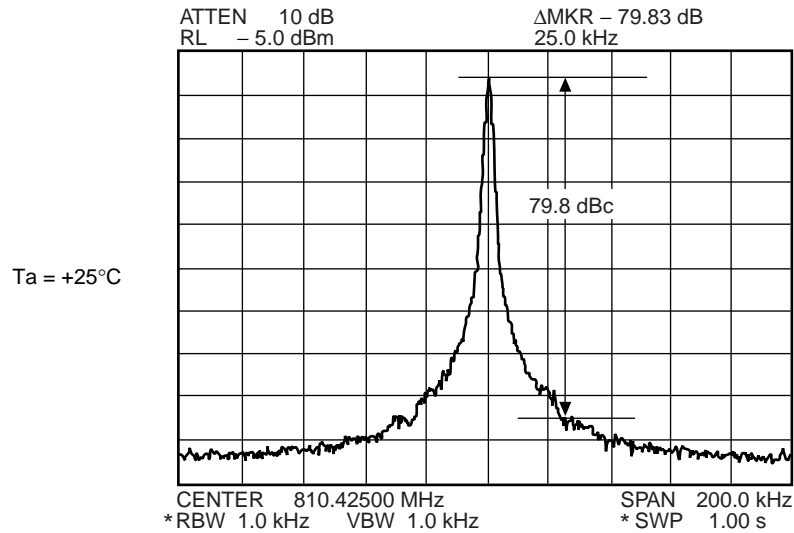


■ REFERENCE INFORMATION

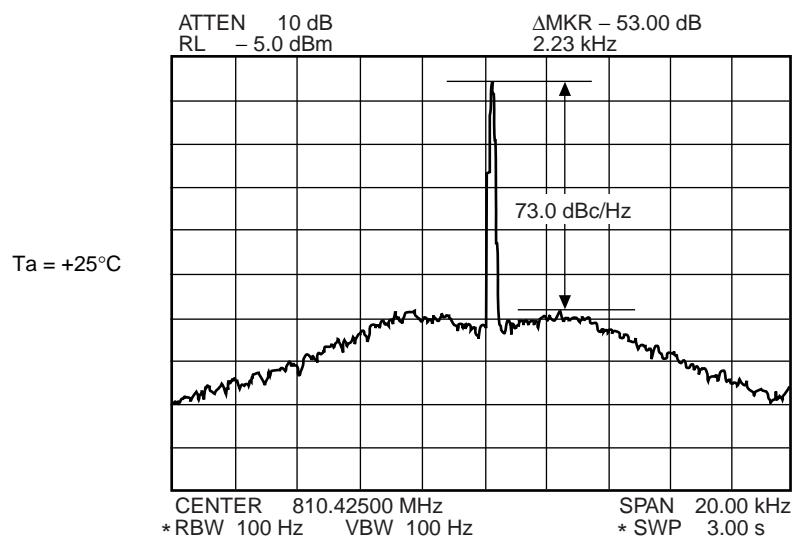


(Continued)

- PLL Reference Leakage



- PLL Phase Noise

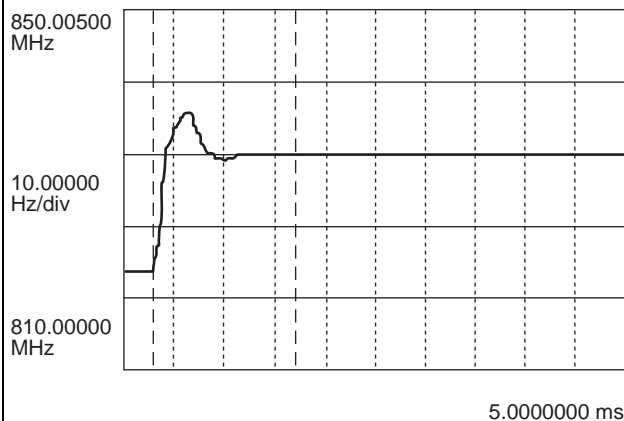


(Continued)

(Continued)

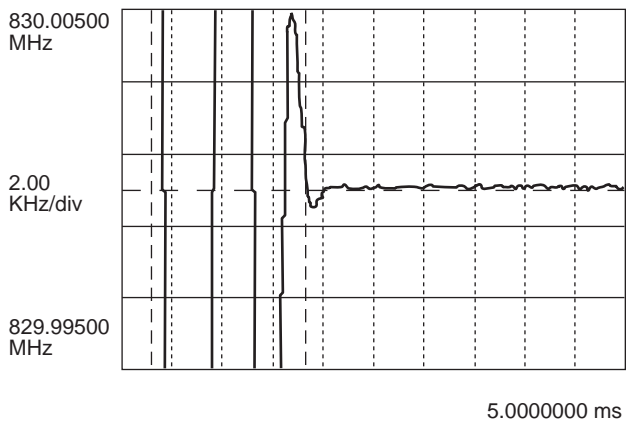
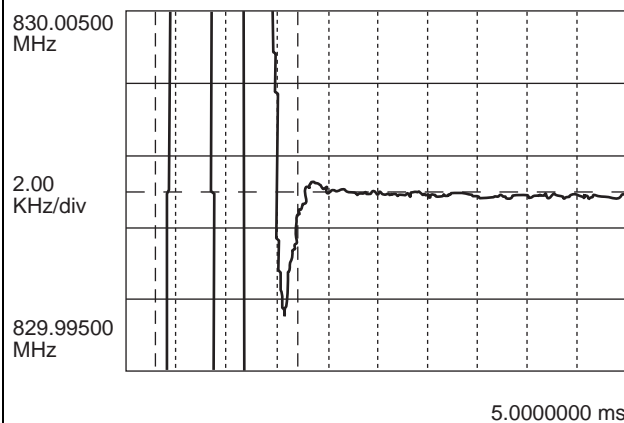
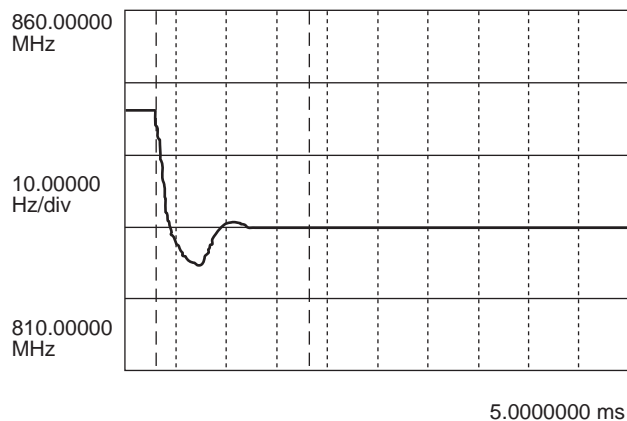
PLL Lock Up Time

810.425 MHz \rightarrow 826.425 \pm 1 kHz
Lch \rightarrow Hch 1.40 ms



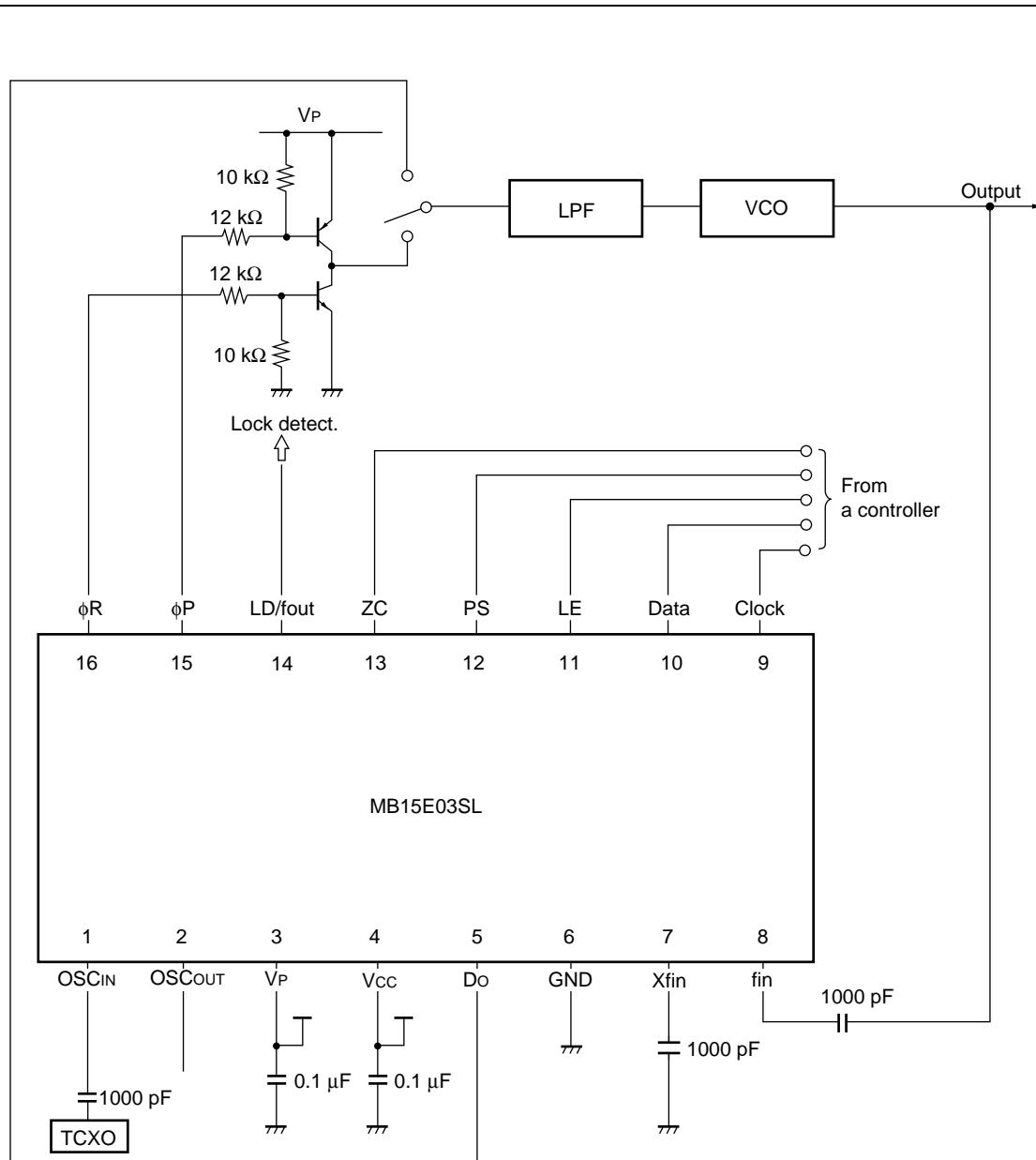
PLL Lock Up Time

826.425 MHz \rightarrow 810.425 \pm 1 kHz
Hch \rightarrow Lch 1.52 ms



MB15E03SL

■ APPLICATION EXAMPLE



V_P: 5.5 V Max

Notes: • In case of using a crystal resonator, it is necessary to optimize matching between the crystal and this LSI, and perform detailed system evaluation. It is recommended to consult with a supplier of the crystal resonator. (Reference oscillator circuit provides its own bias, feedback resistor is 100 k Ω (typ).)

- SSOP-16

■ USAGE PRECAUTIONS

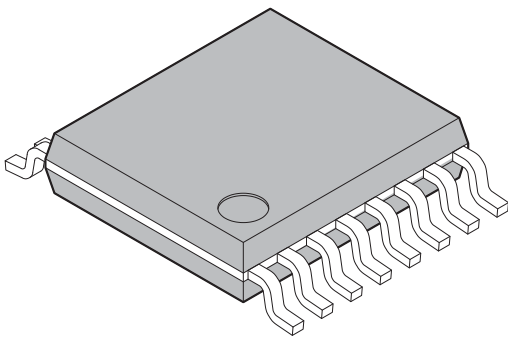
To protect against damage by electrostatic discharge, note the following handling precautions:

- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting device into or removing device from a socket.
- Protect leads with a conductive sheet when transporting a board-mounted device.

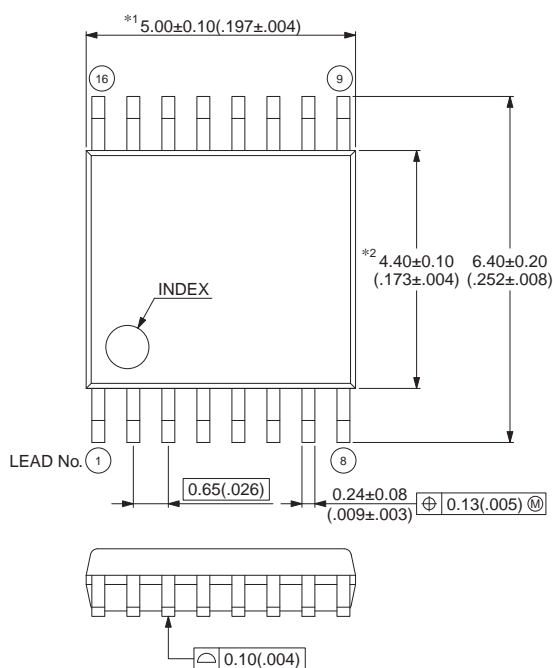
■ ORDERING INFORMATION

Part number	Package	Remarks
MB15E03SLPFV1	16-pin, Plastic SSOP (FPT-16P-M05)	
MB15E03SLWQN	16-pin, Plastic QFN (LCC-16P-M69)	

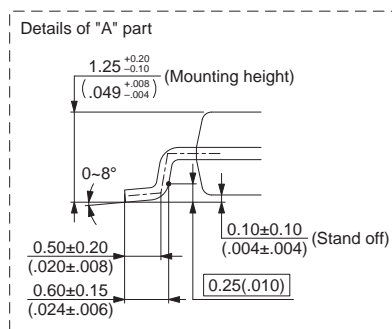
■ PACKAGE DIMENSIONS

 <p>16-pin plastic SSOP</p> <p>(FPT-16P-M05)</p>	Lead pitch	0.65 mm
	Package width × package length	4.40 × 5.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.45mm MAX
	Weight	0.07g
	Code (Reference)	P-SSOP16-4.4×5.0-0.65

16-pin plastic SSOP
(FPT-16P-M05)

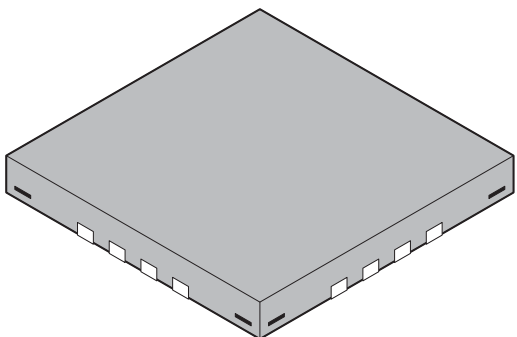


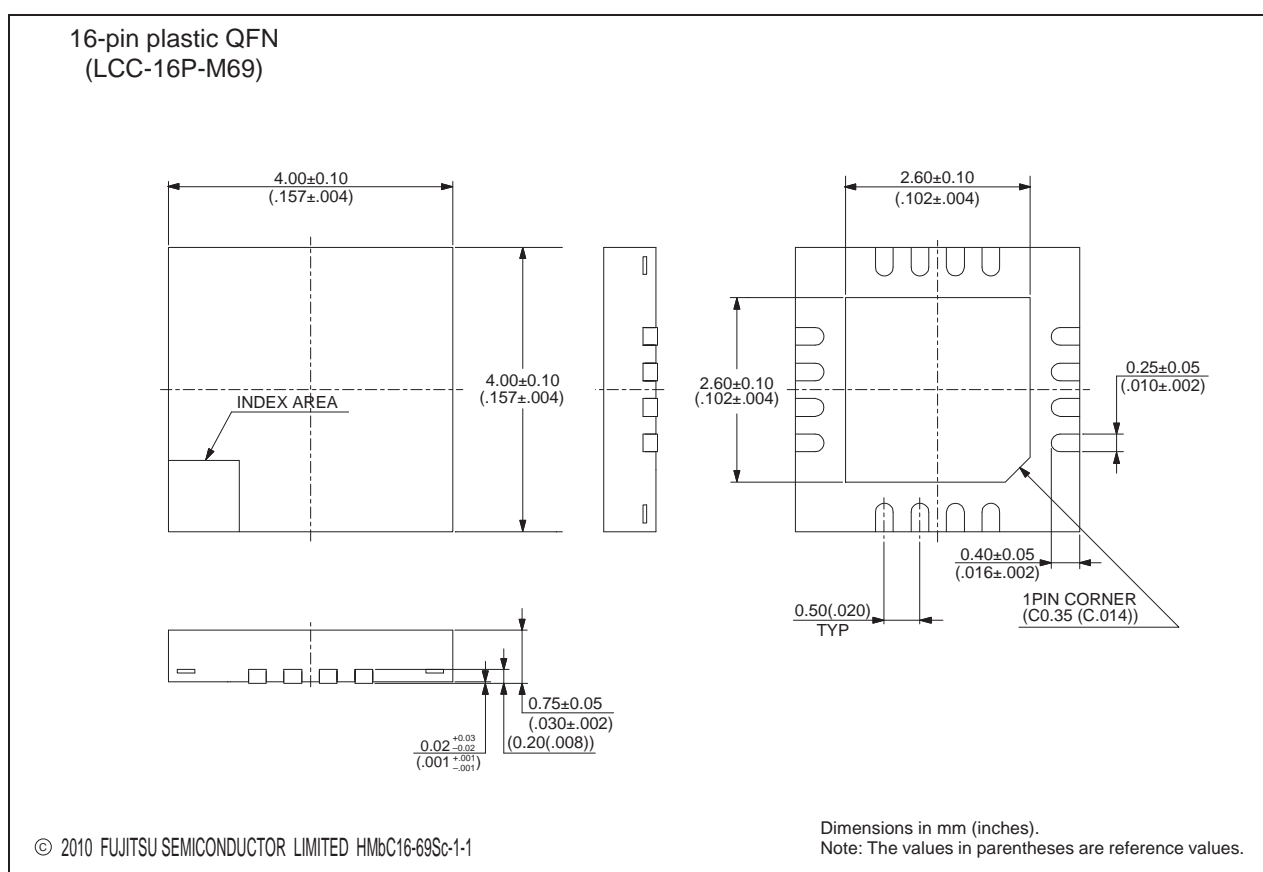
Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max).
 Note 2) *2 : These dimensions do not include resin protrusion.
 Note 3) Pins width and pins thickness include plating thickness.
 Note 4) Pins width do not include tie bar cutting remainder.



© 2003-2010 FUJITSU SEMICONDUCTOR LIMITED F16013S-c-4-8

Dimensions in mm (inches).
 Note: The values in parentheses are reference values.

<p>16-pin plastic QFN</p>  <p>(LCC-16P-M69)</p>	Lead pitch	0.50 mm
	Package width × package length	4.00 mm × 4.00 mm
	Sealing method	Plastic mold
	Mounting height	0.80 mm MAX
	Weight	0.04 g



Please check the latest package dimension at the following URL.
<http://edevic.fujitsu.com/package/en-search/>

MEMO

MEMO

FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,
Kohoku-ku Yokohama Kanagawa 222-0033, Japan

Tel: +81-45-415-5858

<http://jp.fujitsu.com/fsl/en/>

For further information please contact:

North and South America

FUJITSU SEMICONDUCTOR AMERICA, INC.

1250 E. Arques Avenue, M/S 333

Sunnyvale, CA 94085-5401, U.S.A.

Tel: +1-408-737-5600 Fax: +1-408-737-5999

<http://us.fujitsu.com/micro/>

Europe

FUJITSU SEMICONDUCTOR EUROPE GmbH

Pittlerstrasse 47, 63225 Langen, Germany

Tel: +49-6103-690-0 Fax: +49-6103-690-122

<http://emea.fujitsu.com/semiconductor/>

Korea

FUJITSU SEMICONDUCTOR KOREA LTD.

902 Kosmo Tower Building, 1002 Daechi-Dong,

Gangnam-Gu, Seoul 135-280, Republic of Korea

Tel: +82-2-3484-7100 Fax: +82-2-3484-7111

<http://kr.fujitsu.com/fsk/>

Asia Pacific

FUJITSU SEMICONDUCTOR ASIA PTE. LTD.

151 Lorong Chuan,

#05-08 New Tech Park 556741 Singapore

Tel : +65-6281-0770 Fax : +65-6281-0220

<http://sg.fujitsu.com/semiconductor/>

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.

30F, Kerry Parkside, 1155 Fang Dian Road, Pudong District,

Shanghai 201204, China

Tel : +86-21-6146-3688 Fax : +86-21-6146-3660

<http://cn.fujitsu.com/fss/>

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.

10/F., World Commerce Centre, 11 Canton Road,

Tsimshatsui, Kowloon, Hong Kong

Tel : +852-2377-0226 Fax : +852-2376-3269

<http://cn.fujitsu.com/fsp/>

Specifications are subject to change without notice. For further information please contact each office.

All Rights Reserved.

The contents of this document are subject to change without notice.

Customers are advised to consult with sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of FUJITSU SEMICONDUCTOR device; FUJITSU SEMICONDUCTOR does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information.

FUJITSU SEMICONDUCTOR assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of FUJITSU SEMICONDUCTOR or any third party or does FUJITSU SEMICONDUCTOR warrant non-infringement of any third-party's intellectual property right or other right by using such information. FUJITSU SEMICONDUCTOR assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that FUJITSU SEMICONDUCTOR will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Exportation/release of any products described in this document may require necessary procedures in accordance with the regulations of the Foreign Exchange and Foreign Trade Control Law of Japan and/or US export control laws.

The company names and brand names herein are the trademarks or registered trademarks of their respective owners.

Edited: Sales Promotion Department