High-Voltage 1-A Step-Down Switching Regulator

Check for Samples: LM5010

FEATURES

- **Input Voltage Range: 8V to 75V**
- **Valley Current Limit At 1.25A**
- **Switching Frequency Can Exceed 1 MHz**
- **Integrated N-Channel Buck Switch**
- **Integrated Startup Regulator**
- **No Loop Compensation Required**
- **Ultra-Fast Transient Response**
- **Operating Frequency Remains Constant With Load and Line Variations**
- **Maximum Duty Cycle Limited During Startup**
- **Adjustable Output Voltage**
- **Precision 2.5V Feedback Reference**
- **Thermal shutdown**
- **Packages**
  - **10-Pin WSON (4 mm x 4 mm)**
  - **14-Pin HTSSOP**
  - **Both Packages Have Exposed Thermal Pad For Improved Heat Dissipation**

APPLICATIONS

- **High Efficiency Point-Of-Load (POL) Regulator**
- **Non-Isolated Telecommunications Buck Regulator**
- **Secondary High Voltage Post Regulator**
- **Automotive Systems**

DESCRIPTION

The LM5010 Step Down Switching Regulator features all the functions needed to implement a low cost, efficient, buck bias regulator capable of supplying in excess of 1A load current. This high voltage regulator contains an N-Channel Buck Switch, and is available in thermally enhanced 10-pin WSON and 14-pin HTSSOP packages. The hysteretic regulation scheme requires no loop compensation, results in fast load transient response, and simplifies circuit implementation. The operating frequency remains constant with line and load variations due to the inverse relationship between the input voltage and the on-time. The valley current limit detection is set at 1.25A. Additional features include: V_{CC} under-voltage lockout, thermal shutdown, gate drive under-voltage lockout, and maximum duty cycle limiter.

DEVICE INFORMATION

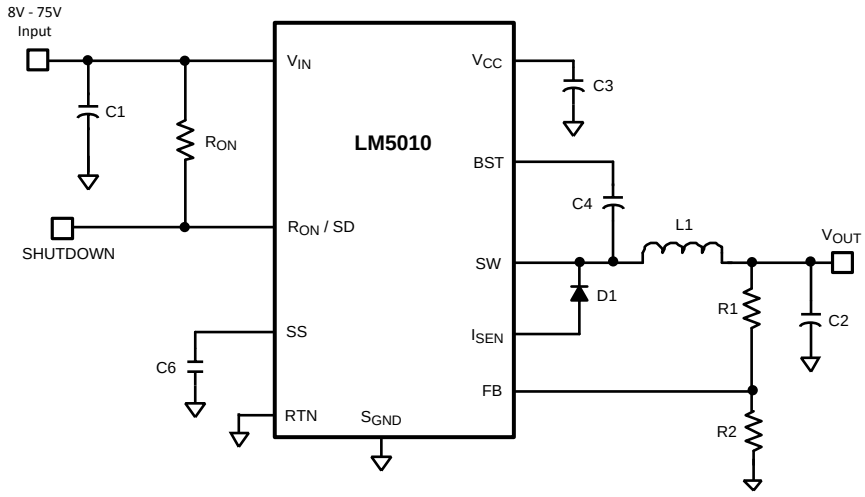
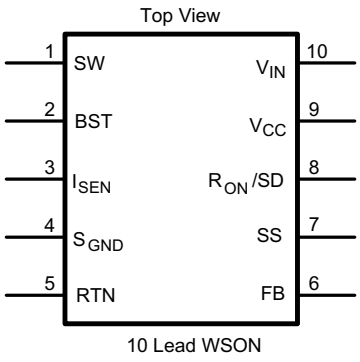
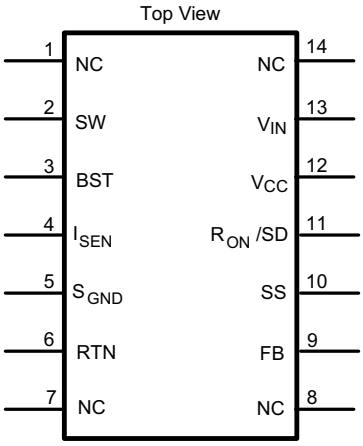


Figure 1. Basic Step-Down Regulator

Connection Diagram



10 Lead WSON



14 Lead HTSSOP

Pin Functions

Table 1. Pin Description

PIN NUMBER		NAME	DESCRIPTION	APPLICATION INFORMATION
WSON-10	HTSSOP-14			
1	2	SW	Switching Node	Internally connected to the buck switch source. Connect to the inductor, free-wheeling diode, and bootstrap capacitor.
2	3	BST	Boost pin for bootstrap capacitor	Connect a 0.022 µF capacitor from SW to this pin. The capacitor is charged from V_{CC} via an internal diode during each off-time.
3	4	I_{SEN}	Current sense	The re-circulating current flows through the internal sense resistor, and out of this pin to the free-wheeling diode. Current limit is nominally set at 1.25A.
4	5	S_{GND}	Sense Ground	Re-circulating current flows into this pin to the current sense resistor.
5	6	RTN	Circuit Ground	Ground for all internal circuitry other than the current limit detection.
6	9	FB	Feedback input from the regulated output	Internally connected to the regulation and over-voltage comparators. The regulation level is 2.5V.
7	10	SS	Softstart	An internal 11.5 µA current source charges an external capacitor to 2.5V, providing the soft start function.
8	11	R_{ON}/SD	On-time control and shutdown	An external resistor from V_{IN} to this pin sets the buck switch on-time. Grounding this pin shuts down the regulator.
9	12	V_{CC}	Output from the startup regulator	Nominally regulates at 7.0V. An external voltage (7.5V-14V) can be applied to this pin to reduce internal dissipation. An internal diode connects V_{CC} to V_{IN}.
10	13	V_{IN}	Input supply voltage	Nominal input range is 8.0V to 75V.
	1, 7, 8, 14	NC	No connection	No internal connection.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

V_{IN} to GND	76V
BST to GND	90V
SW to GND (Steady State)	-1.5V
BST to V_{CC}	76V
BST to SW	14V
V_{CC} to GND	14V
S_{GND} to RTN	-0.3V to +0.3V
SS to RTN	-0.3V to 4V
V_{IN} to SW	76V
Current Out of I_{SEN}	See Text
All Other Inputs to GND	-0.3 to 7V
ESD Rating, Human Body Model (2)	2kV
Storage Temperature Range	-55°C to +150°C
Lead Temperature (Soldering 4 sec) (3)	260°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.
(2) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
(3) For detailed information on soldering plastic HTSSOP and WSON packages, refer to the Packaging Data Book.

Operating Ratings (1)

V_{IN}	8V to 75V
Operating Junction Temperature	−40°C to + 125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{IN} = 48V, R_{ON} = 200kΩ, unless otherwise stated (1) and (2).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC} Regulator						
V_{CC}Reg	V_{CC} regulated output		**6.6**	7	**7.4**	Volts
	V_{IN} - V_{CC}	I_{CC} = 0 mA, F_S < 200 kHz, 7.5V ≤ V_{IN} ≤ 8.0V		1.3		V
	V_{CC} output impedance (0 mA ≤ I_{CC} ≤ 5 mA)	V_{IN} = 8.0V		140		Ω
		V_{IN} = 48V		2.5		
	V_{CC} current limit (3)	V_{CC} = 0V		10		mA
$UVLO_{VCC}$	V_{CC} under-voltage lockout threshold	V_{CC} increasing		5.8		V
	$UVLO_{VCC}$ hysteresis	V_{CC} decreasing		145		mV
	$UVLO_{VCC}$ filter delay	100 mV overdrive		3		µs
	I_{IN} operating current	Non-switching, FB = 3V		650	**850**	µA
	I_{IN} shutdown current	R_{ON}/SD = 0V		95	**200**	µA

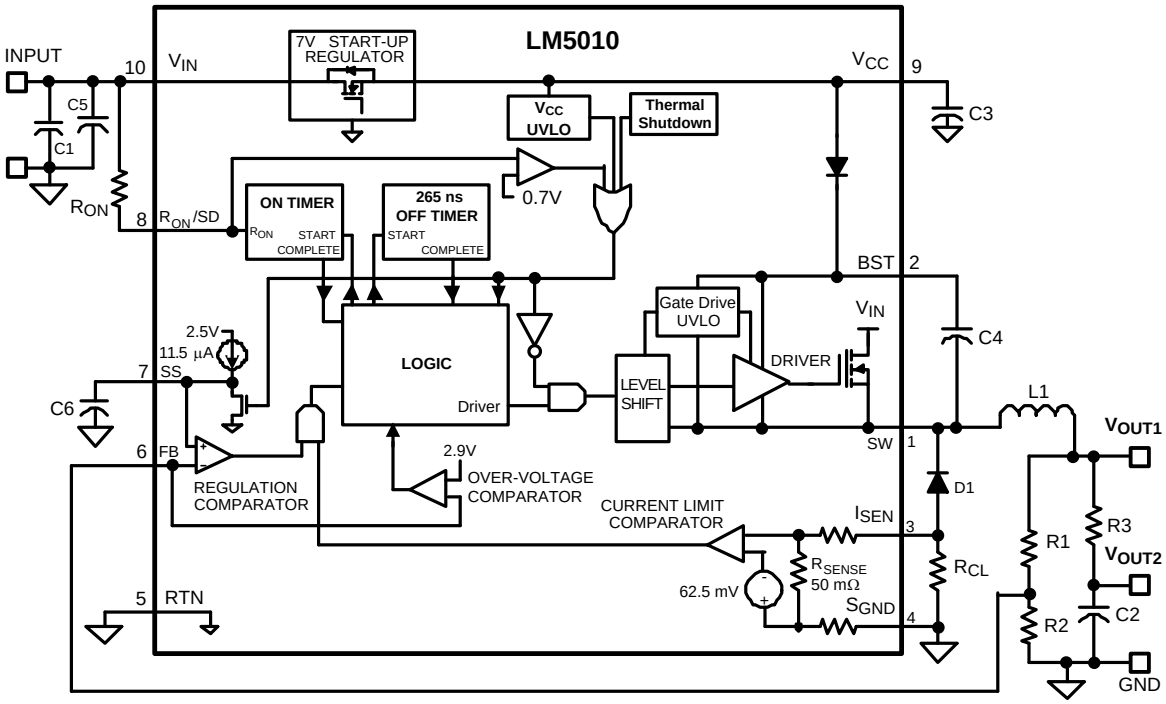
(1) Typical specifications represent the most likely parametric norm at 25°C operation.
(2) All electrical characteristics having room temperature limits are tested during production with T_A = 25°C. All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(3) V_{CC} provides bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

Electrical Characteristics (continued)

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** type apply over full **Operating Junction Temperature range**. V_{IN} = 48V, R_{ON} = 200kΩ, unless otherwise stated (1) and (2).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Switch Characteristics						
Rds(on)	Buck Switch Rds(on)	I_{TEST} = 200 mA		0.35	**0.80**	Ω
$UVLO_{GD}$	Gate Drive UVLO	V_{BST} - V_{SW} Increasing	**3.0**	4.3	**5.0**	V
	$UVLO_{GD}$ hysteresis			440		mV
Softstart Pin						
	Pull-up voltage			2.5		V
	Internal current source			11.5		µA
Current Limit						
I_{LIM}	Threshold	Current out of I_{SEN}	**1**	1.25	**1.5**	A
	Resistance from I_{SEN} to S_{GND}			130		mΩ
	Response time			150		ns
On Timer, R_{ON}/SD Pin						
t_{ON} - 1	On-time	V_{IN} = 10V, R_{ON} = 200 kΩ	**2.1**	2.75	**3.4**	µs
t_{ON} - 2	On-time	V_{IN} = 75V, R_{ON} = 200 kΩ	**290**	390	**490**	ns
	Shutdown threshold	Voltage at R_{ON}/SD rising	**0.35**	0.65	**1.1**	V
	Threshold hysteresis	Voltage at R_{ON}/SD falling		40		mV
Off Timer						
t_{OFF}	Off-time			265		ns
Regulation and Over-Voltage Comparators (FB Pin)						
V_{REF}	FB regulation threshold	SS pin = steady state	**2.445**	2.5	**2.550**	V
	FB over-voltage threshold			2.9		V
	FB bias current			1		nA
Thermal Shutdown						
T_{SD}	Thermal shutdown temperature			175		°C
	Thermal shutdown hysteresis			20		°C
Thermal Resistance						
θ_{JA}	Junction to Ambient	WSON-10 Package		40		°C/W
		HTSSOP-14 Package		40		

TYPICAL APPLICATION CIRCUIT AND BLOCK DIAGRAM



NOTE: Pin numbers are for the WSON-10 package.

Typical Performance Characteristics

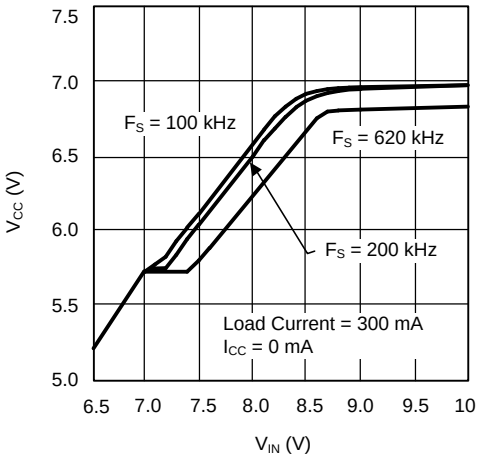


Figure 2. V_{CC} vs V_{IN}

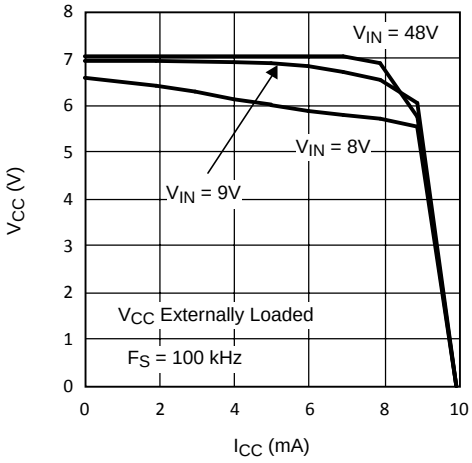


Figure 3. V_{CC} vs I_{CC}

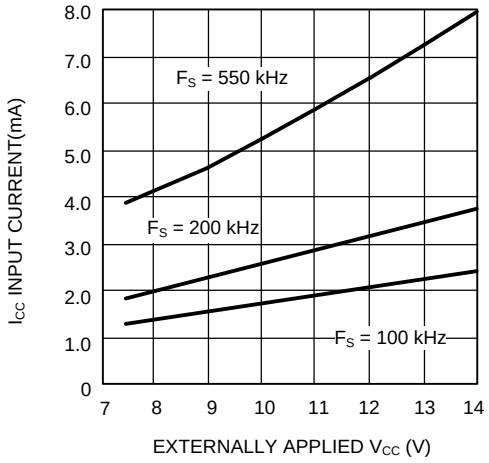


Figure 4. I_{CC} vs Externally Applied V_{CC}

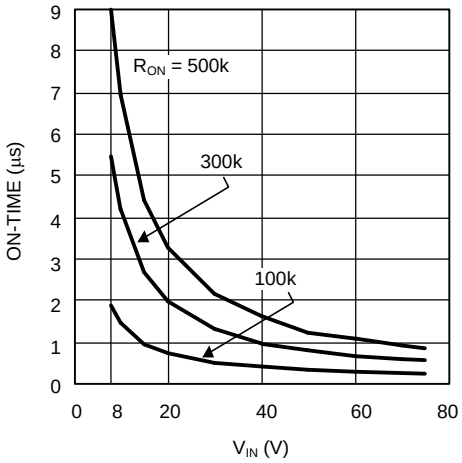


Figure 5. On-Time vs V_{IN} and R_{ON}

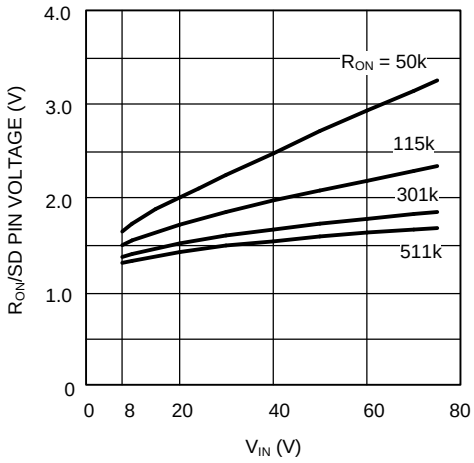


Figure 6. Voltage at R_{ON}/SD Pin

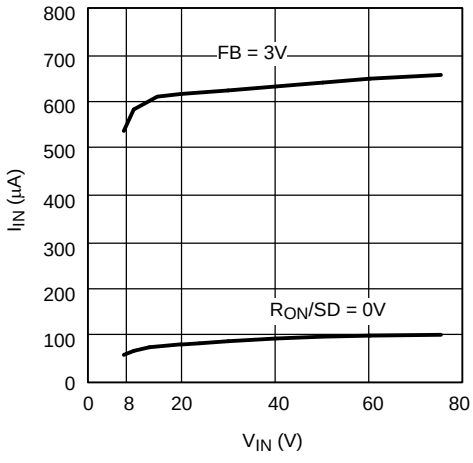


Figure 7. I_{IN} vs V_{IN}

Typical Performance Characteristics (continued)

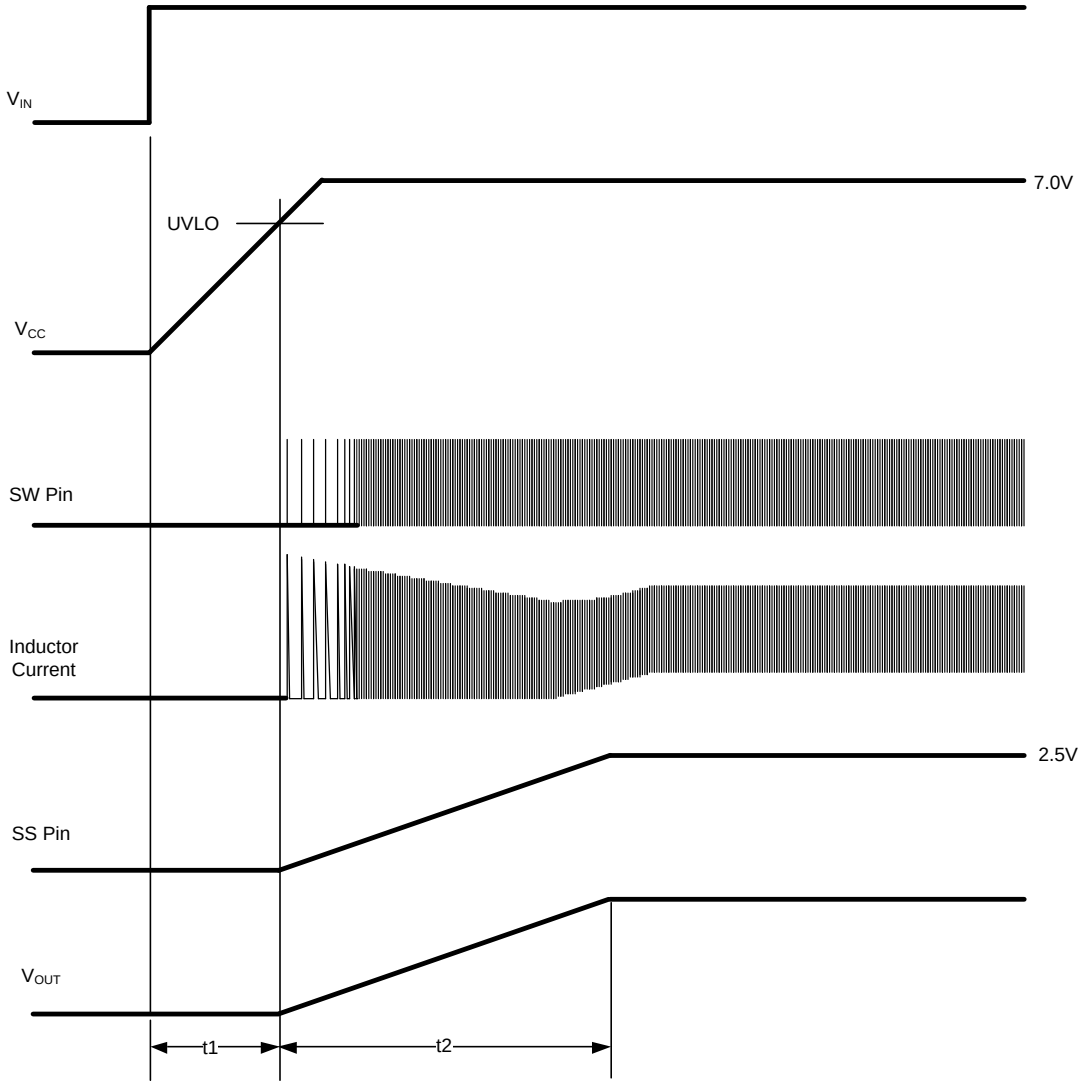


Figure 8. Startup Sequence

FUNCTIONAL DESCRIPTION

The LM5010 Step Down Switching Regulator features all the functions needed to implement a low cost, efficient buck bias power converter capable of supplying in excess of 1A to the load. This high voltage regulator contains an N-Channel buck switch, is easy to implement, and is available in the thermally enhanced WSON-10 and HTSSOP-14 packages. The regulator's operation is based on a hysteretic control scheme, and uses an on-time which varies inversely with V_{IN}. This feature results in the operating frequency remaining relatively constant with load and input voltage variations. The switching frequency can range from 100 kHz to > 1.0 MHz. The hysteretic control requires no loop compensation resulting in very fast load transient response. The valley current limit detection circuit, internally set at 1.25A, holds the buck switch off until the high current level subsides. Typical Application Circuit and Block Diagram shows the functional block diagram. The LM5010 can be applied in numerous applications to efficiently regulate down higher voltages. This regulator is well suited for 48V telecom applications, as well as the new 42V automotive power bus. Implemented as a Point-of-Load regulator following a highly efficient intermediate bus converter can result in high overall system efficiency. Features include: Thermal shutdown, V_{CC} under-voltage lockout, gate drive under-voltage lockout, and maximum duty cycle limit.

Hysteretic Control Circuit Overview

The LM5010 buck DC-DC regulator employs a control scheme based on a comparator and a one-shot on-timer, with the output voltage feedback (FB) compared to an internal reference (2.5V). If the FB voltage is below the reference the buck switch is turned on for a time period determined by the input voltage and a programming resistor (R_{ON}). Following the on-time the switch remains off for 265 ns, or until the FB voltage falls below the reference, whichever is longer. The buck switch then turns on for another on-time period. Typically when the load current increases suddenly, the off-times are temporarily at the minimum of 265 ns. Once regulation is established, the off-time resumes its normal value. The output voltage is set by two external resistors (R1, R2). The regulated output voltage is calculated as follows:

$$V_{OUT} = 2.5V \times (R1 + R2) / R2 \quad (1)$$

Output voltage regulation is based on ripple voltage at the feedback input, requiring a minimum amount of ESR for the output capacitor C2. The LM5010 requires a minimum of 25 mV of ripple voltage at the FB pin. In cases where the capacitor's ESR is insufficient additional series resistance may be required (R3 in Typical Application Circuit and Block Diagram).

When in regulation, the LM5010 operates in continuous conduction mode at heavy load currents and discontinuous conduction mode at light load currents. In continuous conduction mode current always flows through the inductor, never reaching zero during the off-time. In this mode the operating frequency remains relatively constant with load and line variations. The minimum load current for continuous conduction mode is one-half the inductor's ripple current amplitude. The approximate operating frequency is calculated as follows:

$$F_S = \frac{V_{OUT}}{1.18 \times 10^{-10} \times R_{ON}} \quad (2)$$

The buck switch duty cycle is approximately equal to:

$$DC = \frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_{OUT}}{V_{IN}} \quad (3)$$

At low load current, the circuit operates in discontinuous conduction mode, during which the inductor current ramps up from zero to a peak during the on-time, then ramps back to zero before the end of the off-time. The next on-time period starts when the voltage at FB falls below the reference - until then the inductor current remains zero, and the load current is supplied by the output capacitor (C2). In this mode the operating frequency is lower than in continuous conduction mode, and varies with load current. Conversion efficiency is maintained at light loads since the switching losses reduce with the reduction in load and frequency. The approximate discontinuous operating frequency can be calculated as follows:

$$F_S = \frac{V_{OUT}^2 \times L1 \times 1.4 \times 10^{20}}{R_L \times (R_{ON})^2} \quad (4)$$

where R_L = the load resistance.

For applications where lower output voltage ripple is required the output can be taken directly from a low ESR output capacitor as shown in Figure 9. However, R3 slightly degrades the load regulation.

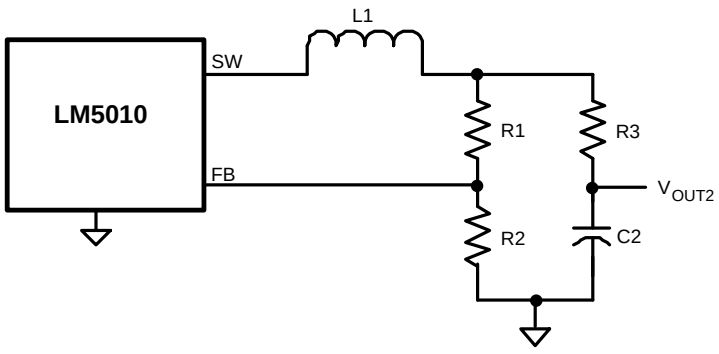


Figure 9. Low Ripple Output Configuration

Start-up Regulator (V_{CC})

The startup regulator is integral to the LM5010. The input pin (V_{IN}) can be connected directly to line voltages up to 75V. The V_{CC} output is regulated at 7.0V, ±6%, and is current limited to 10 mA. Upon power up the regulator sources current into the external capacitor at V_{CC} (C3). With a 0.1 µF capacitor at V_{CC}, approximately 58 µs are required for the V_{CC} voltage to reach the under-voltage lockout threshold (UVLO) of 5.8V (t1 in Figure 8), at which time the buck switch is enabled, and the soft start pin is released to allow the soft start capacitor (C6) to charge up. V_{OUT} then increases to its regulated value as the soft start voltage increases (t2 in Figure 8).

The minimum input operating voltage is determined by the regulator's dropout voltage, the V_{CC} UVLO falling threshold (≅5.65V), and the frequency. When V_{CC} falls below the falling threshold the V_{CC} UVLO activates to shut off the buck switch and ground the soft start pin. If V_{CC} is externally loaded, the minimum input voltage increases since the output impedance at V_{CC} is ≅140Ω at low V_{IN}. See Figure 2 and Figure 3. In applications involving a high value for V_{IN} where power dissipation in the startup regulator is a concern, an auxiliary voltage can be diode connected to the V_{CC} pin (Figure 10). Setting the auxiliary voltage to between 7.5V and 14V shuts off the internal regulator, reducing internal power dissipation. The current required into the V_{CC} pin is shown in Figure 4. Internally a diode connects V_{CC} to V_{IN}.

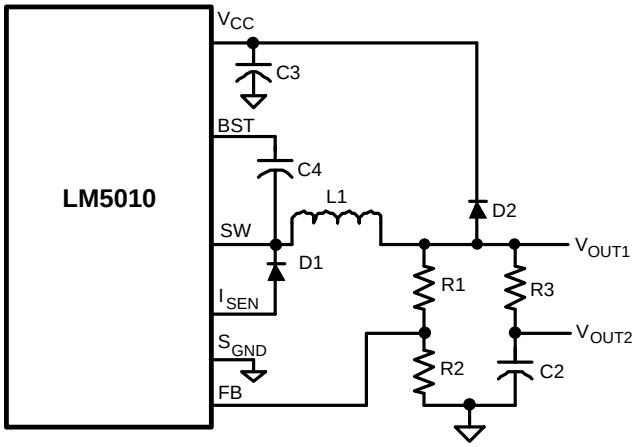


Figure 10. Self Biased Configuration

Regulation Comparator

The feedback voltage at FB is compared to the voltage at the Softstart pin (2.5V, ±2%). In normal operation (the output voltage is regulated) an on-time period is initiated when the voltage at FB falls below 2.5V. The buck switch stays on for the on-time causing the FB voltage to rise above 2.5V. After the on-time period the buck switch stays off until the FB voltage falls below 2.5V. Bias current at the FB pin is less than 5 nA over temperature.

Over-Voltage Comparator

The feedback voltage at FB is compared to an internal 2.9V reference. If the voltage at FB rises above 2.9V the on-time is immediately terminated. This condition can occur if the input voltage, or the output load, change suddenly. The buck switch will not turn on again until the voltage at FB falls below 2.5V.

ON-Time Control

The on-time of the internal switch (see Figure 5) is determined by the R_{ON} resistor and the input voltage (V_{IN}), calculated from the following:

$$t_{ON} = \frac{1.18 \times 10^{-10} \times (R_{ON} + 1.4k)}{V_{IN} - 1.4V} + 67\ ns \quad (5)$$

The inverse relationship of t_{ON} vs. V_{IN} results in a nearly constant frequency as V_{IN} is varied. If the application requires a high frequency the minimum value for t_{ON}, and consequently R_{ON}, is limited by the off-time (265 ns, ±15%) which limits the maximum duty cycle at minimum V_{IN}. The tolerance for Equation 5 is ±25%. Frequencies in excess of 1 MHz are possible with the LM5010.

Shutdown

The LM5010 can be remotely shut down by taking the R_{ON}/SD pin below 0.65V. See Figure 11. In this mode the soft start pin is internally grounded, the on-timer is disabled, and the input current at V_{IN} is reduced (Figure 7). Releasing the R_{ON}/SD pin allows normal operation to resume. When the switch is open, the nominal voltage at R_{ON}/SD is shown in Figure 6.

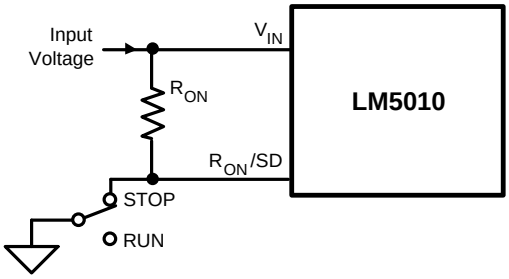


Figure 11. Shutdown Implementation

Current Limit

Current limit detection occurs during the off-time by monitoring the recirculating current through the free-wheeling diode (D1). The detection threshold is 1.25A, ±0.25A. Referring to Typical Application Circuit and Block Diagram, when the buck switch is off the inductor current flows through the load, into S_{GND}, through the sense resistor, out of I_{SEN} and through D1. If that current exceeds the threshold the current limit comparator output switches to delay the start of the next on-time period. The next on-time starts when the current out of I_{SEN} is below the threshold and the voltage at FB is below 2.5V. If the overload condition persists causing the inductor current to exceed the threshold during each on-time, that is detected at the beginning of each off-time. The operating frequency is lower due to longer-than-normal off-times.

Figure 12 illustrates the inductor current waveform. During normal operation the load current is I_O, the average of the ripple waveform. When the load resistance decreases the current ratchets up until the lower peak attempts to exceed the threshold. During the Current Limited portion of Figure 12, the current ramps down to the threshold during each off-time, initiating the next on-time (assuming the voltage at FB is < 2.5V). During each on-time the current ramps up an amount equal to:

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{L1} \tag{6}$$

During this time the LM5010 is in a constant current mode, with an average load current (I_{OCL}) equal to the threshold + ΔI/2.

The “valley current limit” technique allows the load current to exceed the current limit threshold as long as the lower peak of the inductor current is less than the threshold.

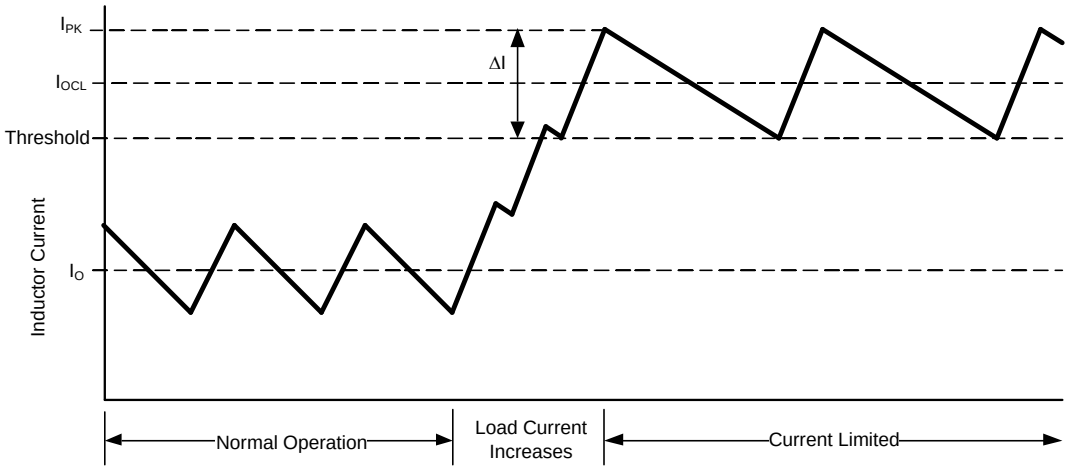


Figure 12. Inductor Current - Current Limit Operation

The current limit threshold can be increased by connecting an external resistor (R_{CL}) between S_{GND} and I_{SEN}. The external resistor typically is less than 1Ω, and its calculation is explained in the Applications Information section.

The peak current out of SW and I_{SEN} must not exceed 3.5A. The average current out of SW must be less than 3A, and the average current out of I_{SEN} must be less than 2A.

N-Channel Buck Switch and Driver

The LM5010 integrates an N-Channel buck switch and associated floating high voltage gate driver. The peak current through the buck switch must not be allowed to exceed 3.5A, and the average current must be less than 3A. The gate driver circuit is powered by the external bootstrap capacitor between BST and SW (C4). During each off-time, the SW pin is at approximately -1V, and C4 is re-charged from V_{CC} through the internal high voltage diode. The minimum off-time of 265 ns ensures a minimum time each cycle to recharge the bootstrap capacitor. A 0.022 µF ceramic capacitor is recommended for C4.

Soft Start

The soft start feature allows the converter to gradually reach a steady state operating point, thereby reducing startup stresses and current surges. Upon turn-on, after V_{CC} reaches the under-voltage threshold (t1 in Figure 8), an internal 11.5 µA current source charges the external capacitor at the Softstart pin to 2.5V (t2 in Figure 8). The ramping voltage at SS (and at the non-inverting input of the regulation comparator) ramps up the output voltage in a controlled manner. This feature keeps the load current from going to current limit during startup, thereby reducing inrush currents.

An internal switch grounds the Softstart pin if V_{CC} is below the under-voltage lockout threshold, if a thermal shutdown occurs, or if the circuit is shutdown using the R_{ON}/SD pin.

Thermal Shutdown

The LM5010 should be operated so the junction temperature does not exceed 125°C. If the junction temperature increases above that, an internal Thermal Shutdown circuit activates (typically) at 175°C, taking the controller to a low power reset state by disabling the buck switch and the on-timer, and grounding the Softstart pin. This feature helps prevent catastrophic failures from accidental device overheating. When the junction temperature reduces below 155°C (typical hysteresis = 20°C), the Softstart pin is released and normal operation resumes.

APPLICATIONS INFORMATION

EXTERNAL COMPONENTS

The procedure for calculating the external components is illustrated with a design example. The circuit in Typical Application Circuit and Block Diagram is to be configured for the following specifications:

- V_{OUT} = 10V
- V_{IN} = 15V to 75V
- F_S = 625 kHz
- Minimum load current = 150 mA
- Maximum load current = 1.0A
- Softstart time = 5 ms

R1 and R2: The ratio of these resistors is calculated from:

$$R1/R2 = (V_{OUT}/2.5V) - 1 \quad (7)$$

R1/R2 calculates to 3.0. The resistors should be chosen from standard value resistors in the range of 1.0 kΩ - 10 kΩ. Values of 3.0 kΩ for R1, and 1.0 kΩ for R2 will be used.

R_{ON}, F_S: R_{ON} sets the on-time, and can be chosen using Equation 2 to set a nominal frequency, or from Equation 5 if the on-time at a particular V_{IN} is important. A higher frequency generally means a smaller inductor and capacitors (value, size and cost), but higher switching losses. A lower frequency means a higher efficiency, but with larger components. If PC board space is tight, a higher frequency is better. The resulting on-time and frequency have a ±25% tolerance. Re-arranging Equation 2,

$$R_{ON} = \frac{10V}{1.18 \times 10^{-10} \times 625\ kHz} = 136\ k\Omega \quad (8)$$

The next larger standard value (137 kΩ) is chosen for R_{ON}, yielding a nominal frequency of 618 kHz.

L1: The inductor value is determined based on the load current, ripple current, and the minimum and maximum input voltage ($V_{IN(min)}$, $V_{IN(max)}$). Refer to Figure 13.

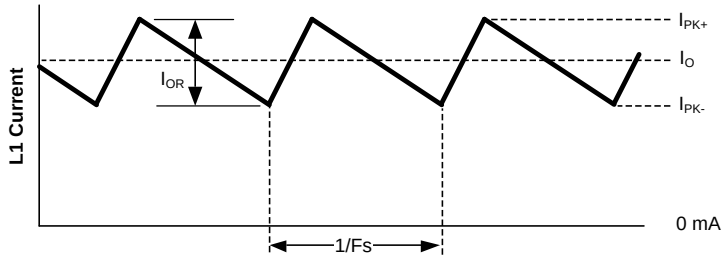


Figure 13. Inductor Current

To keep the circuit in continuous conduction mode, the maximum allowed ripple current is twice the minimum load current, or 300 mAp-p. Using this value of ripple current, the inductor (L1) is calculated using the following:

$$L1 = \frac{V_{OUT1} \times (V_{IN(max)} - V_{OUT1})}{I_{OR} \times F_{S(min)} \times V_{IN(max)}} \quad (9)$$

where $F_{S(min)}$ is the minimum frequency (F_S - 25%).

$$L1 = \frac{10V \times (75V - 10V)}{0.30A \times 463\ kHz \times 75V} = 63\ \mu H \quad (10)$$

This provides a minimum value for L1 - the next higher standard value (100 µH) will be used. L1 must be rated for the peak current (I_{PK+}) to prevent saturation. The peak current occurs at maximum load current with maximum ripple. The maximum ripple is calculated by re-arranging Equation 9 using $V_{IN(max)}$, $F_{S(min)}$, and the minimum inductor value, based on the manufacturer's tolerance. Assume, for this exercise, the inductor's tolerance is ±20%.

$$I_{OR(max)} = \frac{V_{OUT1} \times (V_{IN(max)} - V_{OUT1})}{L1_{MIN} \times F_{S(min)} \times V_{IN(max)}} \tag{11}$$

$$I_{OR(max)} = \frac{10V \times (75V - 10V)}{80\ \mu H \times 463\ kHz \times 75V} = 234\ mAp\text{-}p \tag{12}$$

$$I_{PK+} = 1.0A + 0.234A / 2 = 1.117A \tag{13}$$

R_{CL}: Since it is obvious that the lower peak of the inductor current waveform does not exceed 1.0A at maximum load current (see Figure 13), it is not necessary to increase the current limit threshold. Therefore R_{CL} is not needed for this exercise. For applications where the lower peak exceeds 1.0A, see the section below on increasing the current limit threshold.

C2 and R3: Since the LM5010 requires a minimum of 25 mVp-p of ripple at the FB pin for proper operation, the required ripple at V_{OUT1} is increased by R1 and R2. This necessary ripple is created by the inductor ripple current acting on C2's ESR + R3. First, the minimum ripple current is determined.

$$I_{OR(min)} = \frac{V_{OUT1} \times (V_{IN(min)} - V_{OUT1})}{L1_{MAX} \times F_{S(max)} \times V_{IN(min)}}$$

$$= \frac{10V \times (15V - 10V)}{120\ \mu H \times 772\ kHz \times 15V} = 36\ mA \tag{14}$$

The minimum ESR for C2 is then equal to:

$$ESR_{(min)} = \frac{25\ mV \times (R1 + R2)}{R2 \times I_{OR(min)}} = 2.8\Omega \tag{15}$$

If the capacitor used for C2 does not have sufficient ESR, R3 is added in series as shown in Typical Application Circuit and Block Diagram. C2 should generally be no smaller than 3.3 µF, although that is dependent on the frequency and the allowable ripple amplitude at V_{OUT1}. Experimentation is usually necessary to determine the minimum value for C2, as the nature of the load may require a larger value. A load which creates significant transients requires a larger value for C2 than a non-varying load.

D1: The important parameters are reverse recovery time and forward voltage drop. The reverse recovery time determines how long the current surge lasts each time the buck switch is turned on. The forward voltage drop is significant in the event the output is short-circuited as it is mainly this diode's voltage (plus the voltage across the current limit sense resistor) which forces the inductor current to decrease during the off-time. For this reason, a higher voltage is better, although that affects efficiency. A reverse recovery time of ≅30 ns, and a forward voltage drop of ≅0.75V are preferred. The reverse leakage specification is important as that can significantly affect efficiency. Other types of diodes may have a lower forward voltage drop, but may have longer recovery times, or greater reverse leakage. D1 should be rated for the maximum V_{IN}, and for the peak current when in current limit (I_{PK} in Figure 11) which is equal to:

$$I_{PK} = 1.5A + I_{OR(max)} = 1.734A \tag{16}$$

where 1.5A is the maximum guaranteed current limit threshold, and the maximum ripple current was previously calculated as 234 mAp-p. Note that this calculation is valid only when R_{CL} is not required.

C1: Assuming the voltage supply feeding V_{IN} has a source impedance greater than zero, this capacitor limits the ripple voltage at V_{IN} while supplying most of the switch current during the on-time. At maximum load current, when the buck switch turns on, the current into V_{IN} increases to the lower peak of the output current waveform, ramps up to the peak value, then drops to zero at turn-off. The average current into V_{IN} during this on-time is the load current. For a worst case calculation, C1 must supply this average load current during the maximum on-time. The maximum on-time is calculated using Equation 5, with a 25% tolerance added:

$$t_{ON(max)} = \frac{1.18 \times 10^{-10} \times (137k + 1.4k) \times 1.25}{15V - 1.4V} + 67\ ns = 1.57\ \mu s \quad (17)$$

C1 is calculated from:

$$C1 = \frac{I_O \times t_{ON}}{\Delta V} = \frac{1.0A \times 1.57\ \mu s}{1V} = 1.57\ \mu F \quad (18)$$

where I_O is the load current, and ΔV is the allowable ripple voltage at V_{IN} (1V for this example). Quality ceramic capacitors with a low ESR should be used for C1. To allow for capacitor tolerances and voltage effects, a 2.2 µF capacitor will be used

C3: The capacitor at the V_{CC} pin provides not only noise filtering and stability, but also prevents false triggering of the V_{CC} UVLO at the buck switch on/off transitions. For this reason, C3 should be no smaller than 0.1 µF, and should be a good quality, low ESR, ceramic capacitor. This capacitor also determines the initial startup delay (t1 in Figure 8).

C4: The recommended value for C4 is 0.022 µF. A high quality ceramic capacitor with low ESR is recommended as C4 supplies the surge current to charge the buck switch gate at turn-on. A low ESR also ensures a complete recharge during each off-time.

C5: This capacitor suppresses transients and ringing due to long lead inductance at V_{IN}. A low ESR, 0.1 µF ceramic chip capacitor is recommended, located physically close to the LM5010.

C6: The capacitor at the SS pin determines the soft start time, i.e. the time for the reference voltage at the regulation comparator, and the output voltage, to reach their final value. The time is determined from the following:

$$t_{SS} = \frac{C6 \times 2.5V}{11.5\ \mu A} \quad (19)$$

For a 5 ms soft start time, C6 calculates to 0.022 µF.

FINAL CIRCUIT

The final circuit is shown in Figure 14, and its performance is shown in Figure 15 to Figure 18.

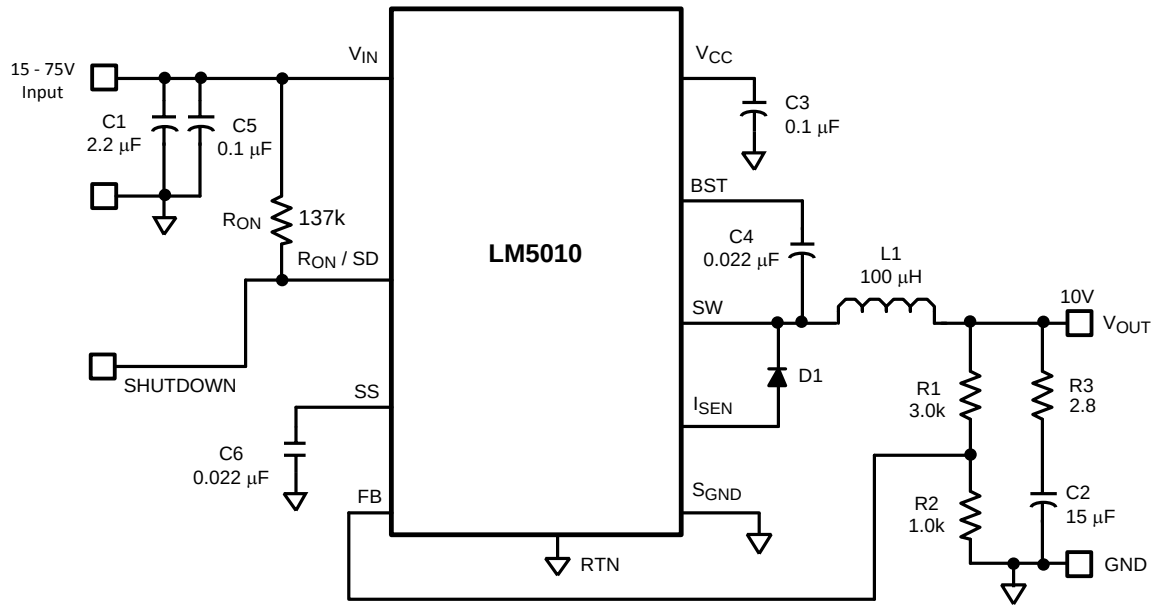


Figure 14. LM5010 Example Circuit

Table 2. Bill of Materials

Item	Description	Part No.	Package	Value
C1	Ceramic Capacitor	TDK C4532X7R2A225M	1812	2.2 µF, 100V
C2	Ceramic Capacitor	TDK C4532X7R1E156M	1812	15 µF, 25V
C3	Ceramic Capacitor	Kemet C0805C104K4RAC	0805	0.1 µF, 16V
C4, C6	Ceramic Capacitor	Kemet C0805C223K4RAC	0805	0.022 µF, 16V
C5	Ceramic Capacitor	TDK C2012X7R2A104M	0805	0.1 µF, 100V
D1	Ultra fast diode	Central Semi CMR2U-01	SMB	100V, 2A
L1	Inductor	TDK SLF10145	10.1 x 10.1	100 µH
R1	Resistor	Vishay CRCW08053001F	0805	3.0 kΩ
R2	Resistor	Vishay CRCW08051001F	0805	1.0 kΩ
R3	Resistor	Vishay CRCW08052R80F	0805	2.8 Ω
R_{ON}	Resistor	Vishay CRCW08051373F	0805	137 kΩ
U1	Switching regulator	LM5010		

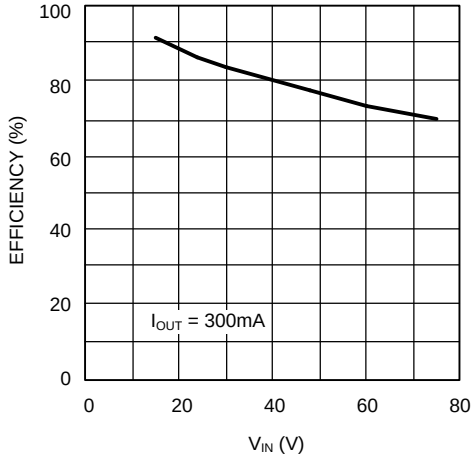


Figure 15. Efficiency vs V_{IN}
Circuit of Figure 14

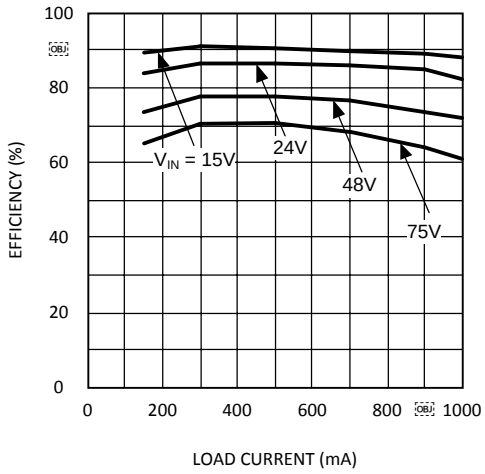


Figure 16. Efficiency vs Load Current and V_{IN}
Circuit of Figure 14

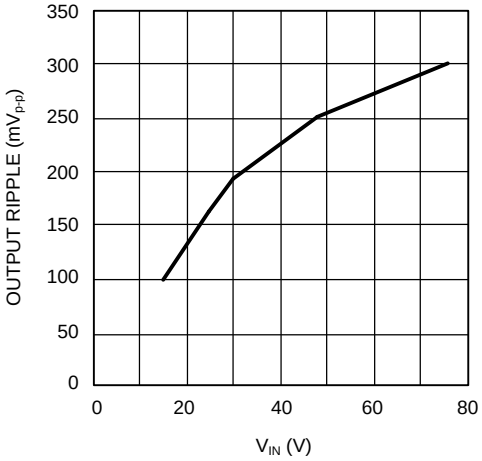


Figure 17. Output Voltage Ripple vs V_{IN}
Circuit of Figure 14

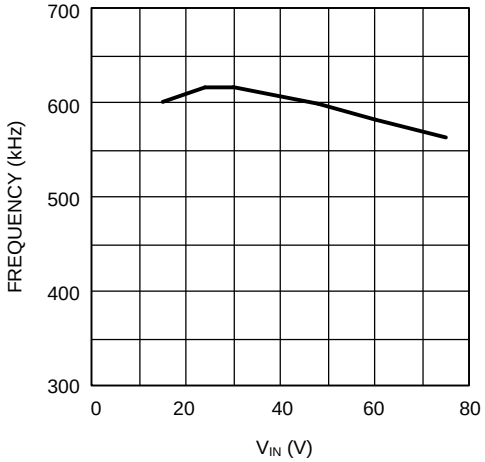


Figure 18. Frequency vs V_{IN}
Circuit of Figure 14

INCREASING THE CURRENT LIMIT THRESHOLD

The current limit threshold is nominally 1.25A, with a minimum guaranteed value of 1.0A. If, at maximum load current, the lower peak of the inductor current (I_{PK-} in Figure 13) exceeds 1.0A, resistor R_{CL} must be added between S_{GND} and I_{SEN} to increase the current limit threshold to equal or exceed that lower peak current. This resistor diverts some of the recirculating current from the internal sense resistor so that a higher current level is needed to switch the internal current limit comparator. I_{PK-} is calculated from:

$$I_{PK-} = I_{O(max)} - \frac{I_{OR(min)}}{2} \tag{20}$$

where $I_{O(max)}$ is the maximum load current, and $I_{OR(min)}$ is the minimum ripple current calculated using Equation 14. R_{CL} is calculated from:

$$R_{CL} = \frac{1.0A \times 0.11\Omega}{I_{PK-} - 1.0A} \tag{21}$$

where 0.11Ω is the minimum value of the internal resistance from S_{GND} to I_{SEN}. The next smaller standard value resistor should be used for R_{CL}. With the addition of R_{CL} it is necessary to check the average and peak current values to ensure they do not exceed the LM5010 limits. At maximum load current the average current through the internal sense resistor is:

$$I_{AVE} = \frac{I_{O(max)} \times R_{CL} \times (V_{IN(max)} - V_{OUT})}{(R_{CL} + 0.11\Omega) \times V_{IN(max)}} \tag{22}$$

If I_{AVE} is less than 2.0A no changes are necessary. If it exceeds 2.0A, R_{CL} must be reduced. The upper peak of the inductor current (I_{PK+}), at maximum load current, is calculated using the following:

$$I_{PK+} = I_{O(max)} + \frac{I_{OR(max)}}{2} \tag{23}$$

where $I_{OR(max)}$ is calculated using Equation 11. If I_{PK+} exceeds 3.5A , the inductor value must be increased to reduce the ripple amplitude. This will necessitate recalculation of $I_{OR(min)}$, I_{PK-}, and R_{CL}.

When the circuit is in current limit, the upper peak current out of the SW pin is

$$I_{PK+(CL)} = \frac{1.5A \times (150\ m\Omega + R_{CL})}{R_{CL}} + I_{OR(MAX)} \tag{24}$$

The inductor L1 and diode D1 must be rated for this current.

PC BOARD LAYOUT

The LM5010 regulation, over-voltage, and current limit comparators are very fast, and will respond to short duration noise pulses. Layout considerations are therefore critical for optimum performance. The layout must be as neat and compact as possible, and all the components must be as close as possible to their associated pins. The current loop formed by D1, L1, C2, and the S_{GND} and I_{SEN} pins should be as small as possible. The ground connection from C2 to C1 should be as short and direct as possible. If it is expected that the internal dissipation of the LM5010 will produce high junction temperatures during normal operation, good use of the PC board's ground plane can help considerably to dissipate heat. The exposed pad on the IC package bottom can be soldered to a ground plane, and that plane should both extend from beneath the IC, and be connected to exposed ground plane on the board's other side using as many vias as possible. The exposed pad is internally connected to the IC substrate.

The use of wide PC board traces at the pins, where possible, can help conduct heat away from the IC. The four No Connect pins on the HTSSOP package are not electrically connected to any part of the IC, and may be connected to ground plane to help dissipate heat from the package. Judicious positioning of the PC board within the end product, along with the use of any available air flow (forced or natural convection) can help reduce the junction temperature.

REVISION HISTORY

Changes from Revision E (February 2013) to Revision F **Page**

- Changed layout of National Data Sheet to TI format 16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5010MH	NRND	HTSSOP	PWP	14	94	TBD	Call TI	Call TI	-40 to 125	L5010 MH	
LM5010MH/NOPB	ACTIVE	HTSSOP	PWP	14	94	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5010 MH	Samples
LM5010MHX/NOPB	ACTIVE	HTSSOP	PWP	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5010 MH	Samples
LM5010SD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00057B	Samples
LM5010SDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L00057B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

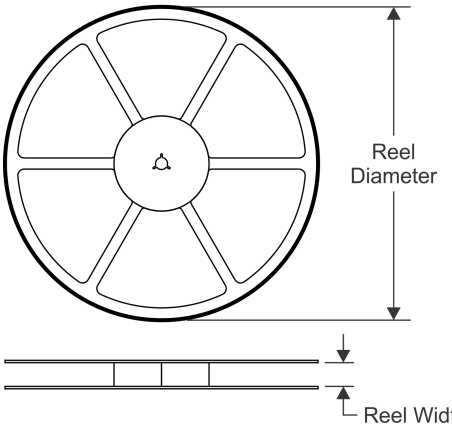
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

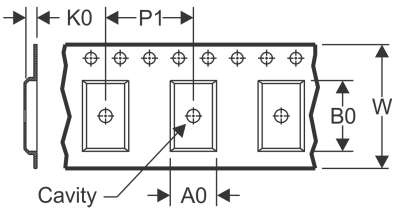
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

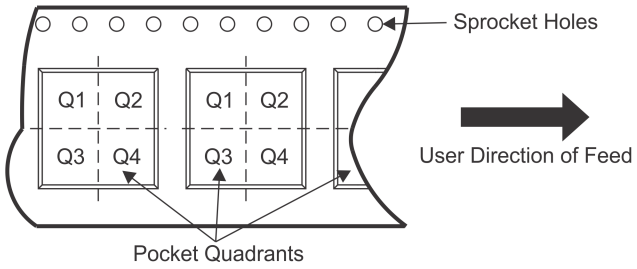


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

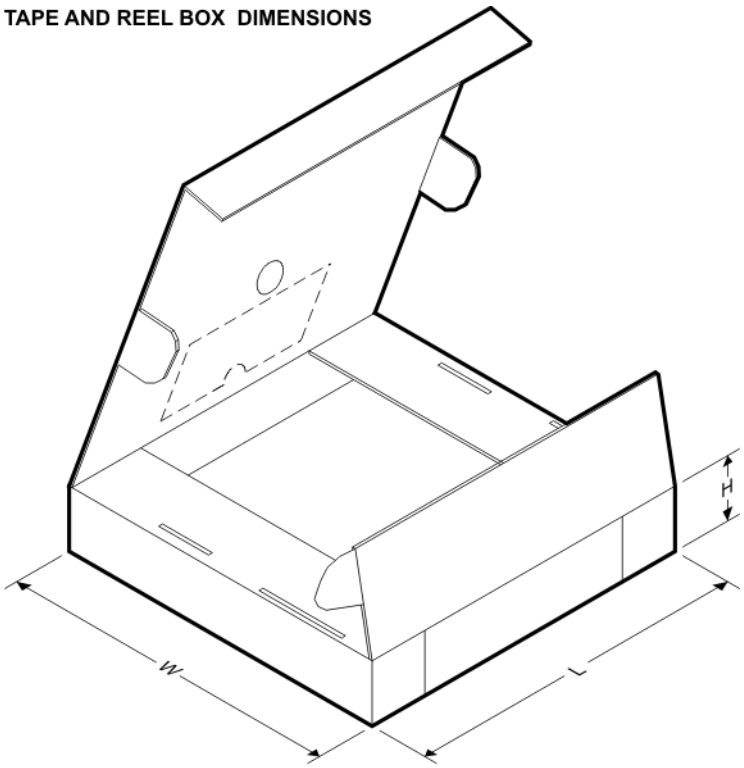
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5010MHX/NOPB	HTSSOP	PWP	14	2500	330.0	12.4	6.95	8.3	1.6	8.0	12.0	Q1
LM5010SD/NOPB	WSON	DPR	10	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5010SDX/NOPB	WSON	DPR	10	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

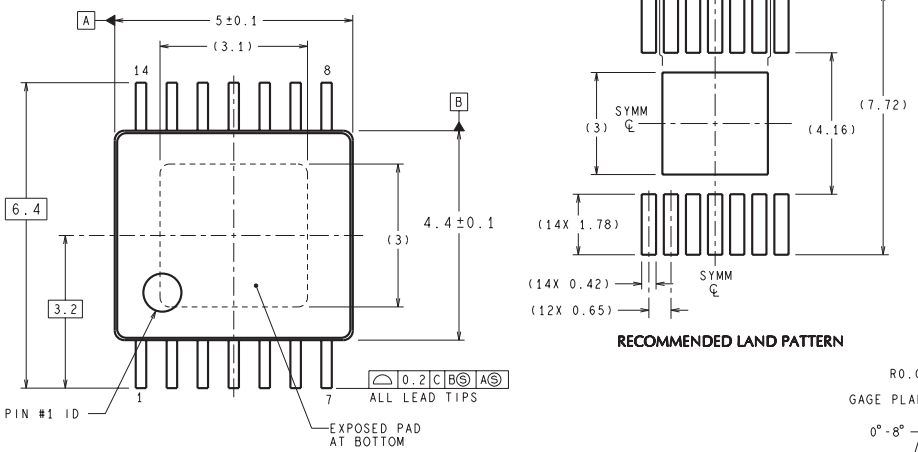
TAPE AND REEL BOX DIMENSIONS



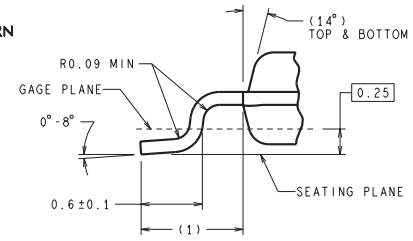
*All dimensions are nominal

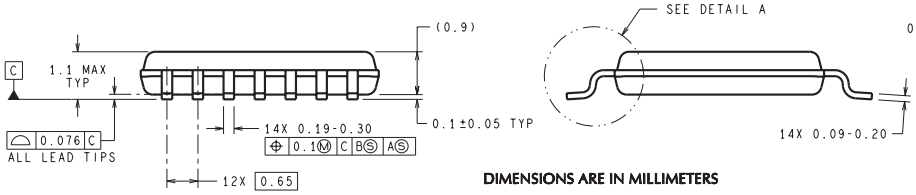
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5010MHX/NOPB	HTSSOP	PWP	14	2500	367.0	367.0	35.0
LM5010SD/NOPB	WSON	DPR	10	1000	210.0	185.0	35.0
LM5010SDX/NOPB	WSON	DPR	10	4500	367.0	367.0	35.0

PWP0014A



RECOMMENDED LAND PATTERN





DIMENSIONS ARE IN MILLIMETERS

MXA14A (Rev A)

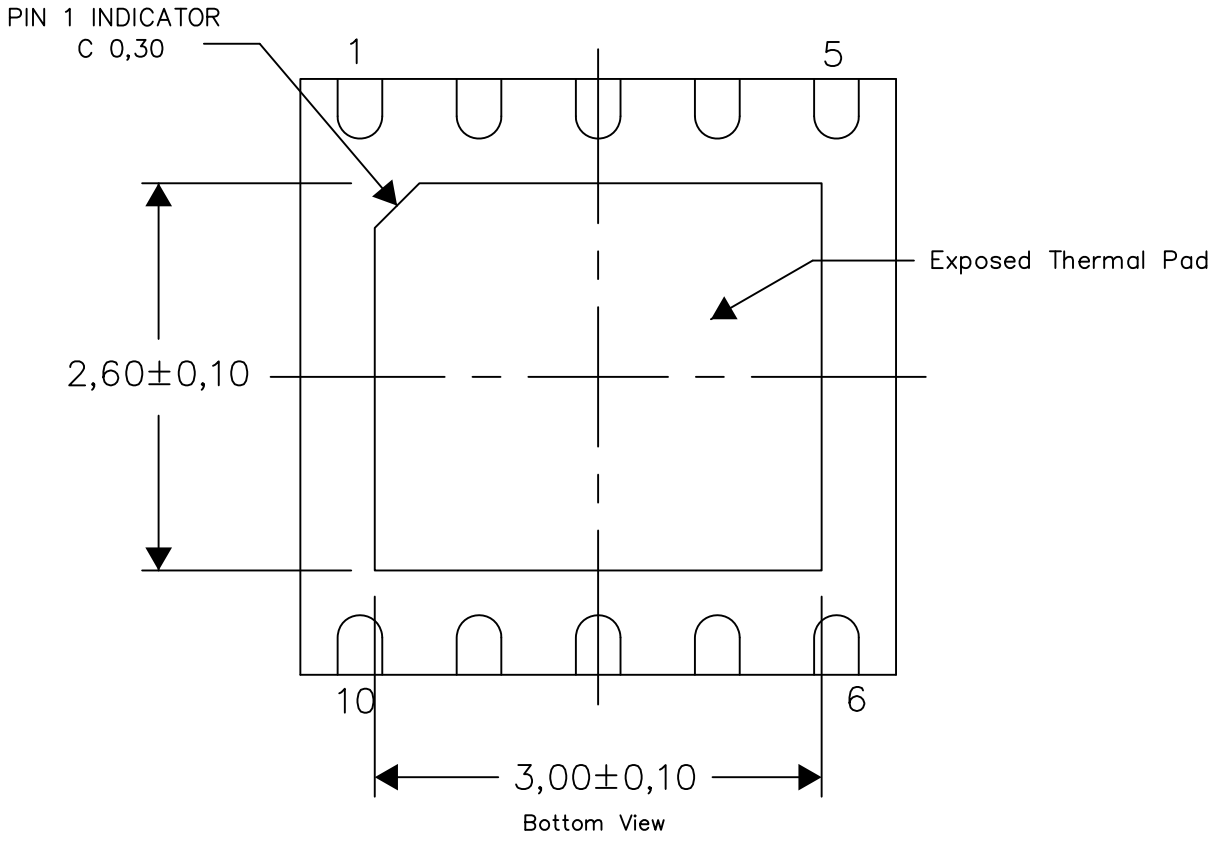
DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

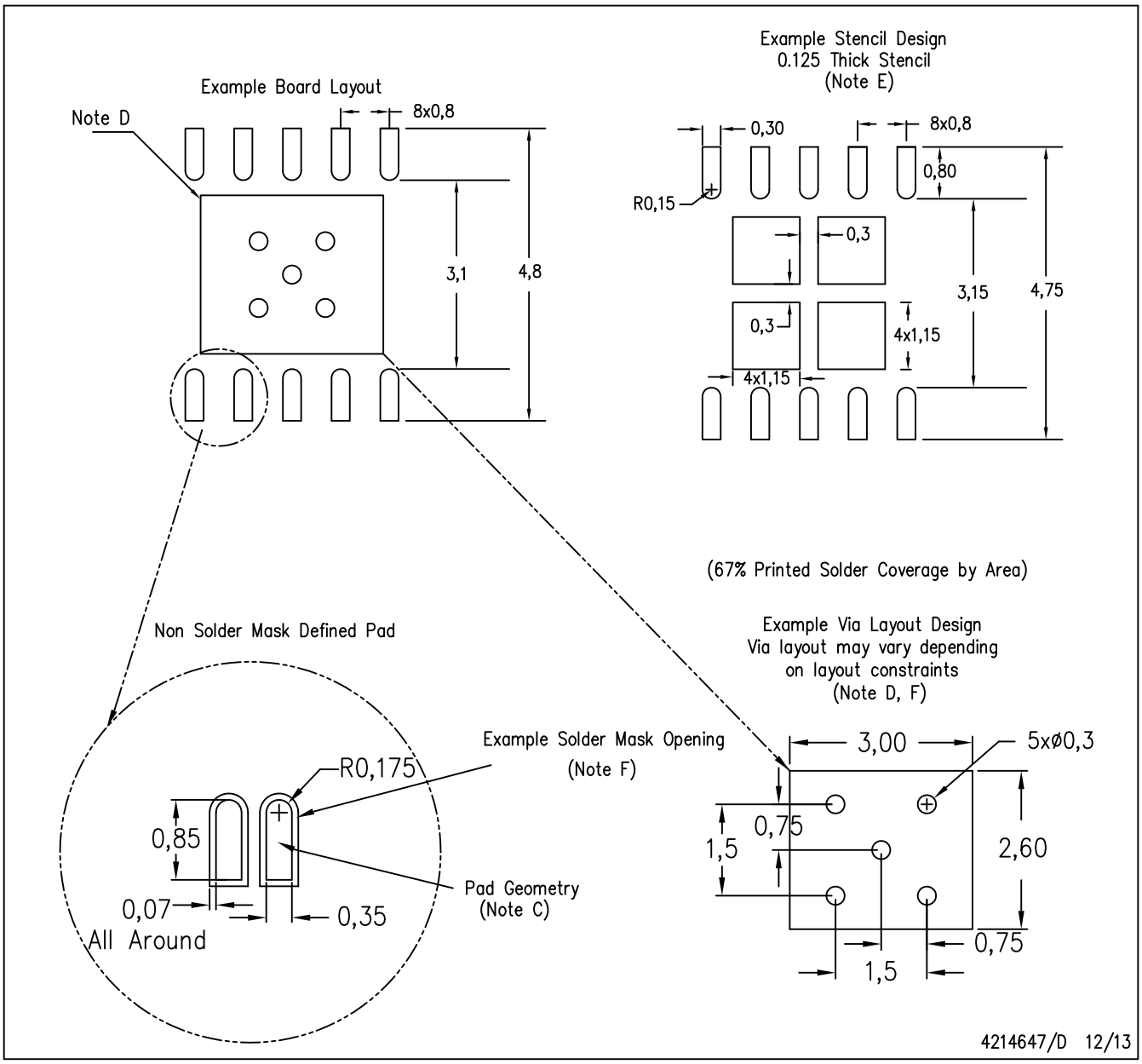


Exposed Thermal Pad Dimensions

4211551/C 12/13

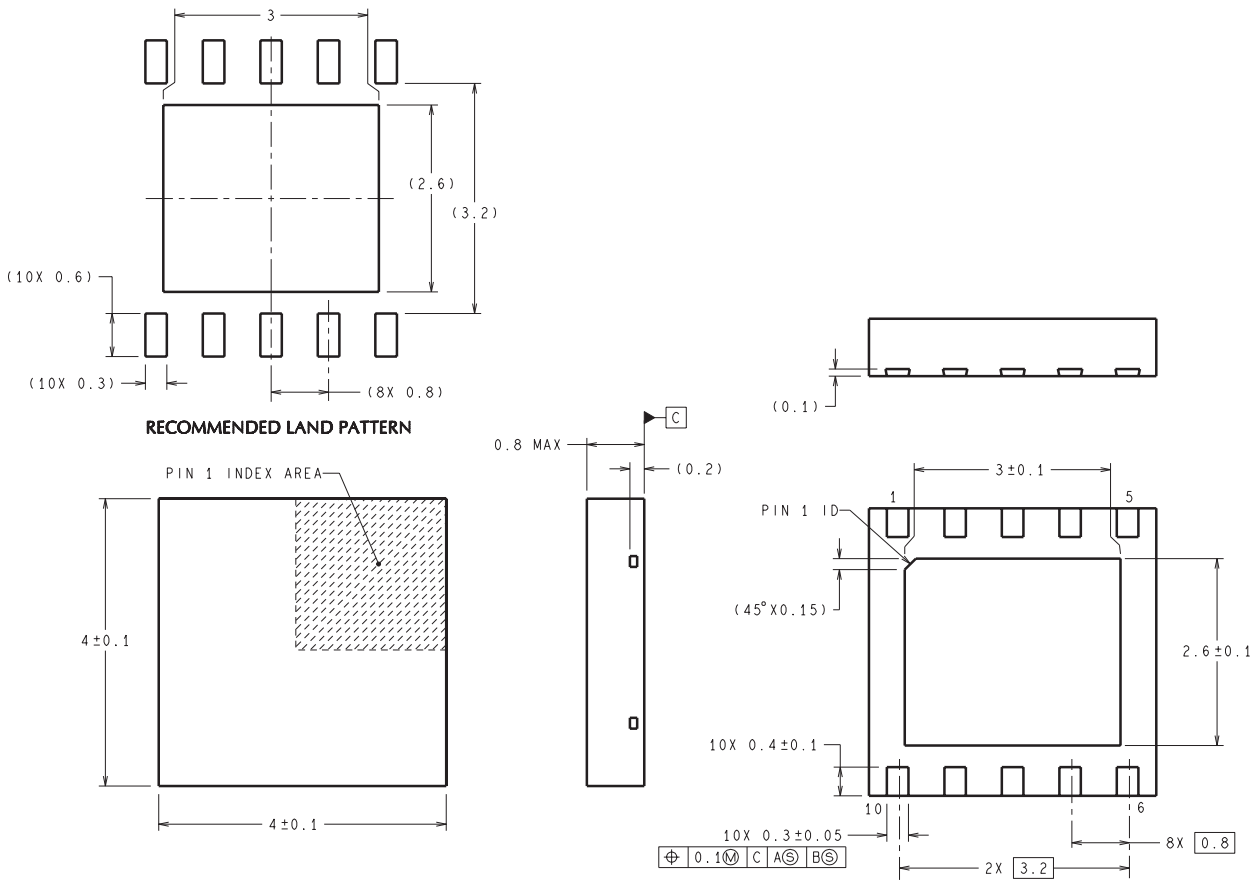
NOTES: All linear dimensions are in millimeters

DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DPR0010A



DIMENSIONS ARE IN MILLIMETERS

SDC10A (Rev A)

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