# TPS56x200 4.5 V to 17 V Input, 2A/3A Synchronous Step-Down Voltage Regulator in SOT-23

## 1 Features

- D-CAP2™ Mode Control with 650-kHz Switching Frequency
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- Integrated 122-mΩ and 72-mΩ FETs ('562200)
- Integrated 68-mΩ and 39-mΩ FETs ('563200)
- Advanced Eco-mode™ Pulse-skip
- Low Shutdown Current Less than 10 µA
- 1% Feedback Voltage Accuracy (25°C)
- Startup from Pre-Biased Output Voltage
- Cycle-By-Cycle Hiccup Over-current Limit
- Non-latch OVP, UVLO and TSD Protections
- Fixed Soft Start: 1 ms

## 2 Applications

- Digital TV Power Supply
- High Definition Blu-ray Disc™ Players
- Networking Home Terminal
- Digital Set Top Box (STB)

## 3 Description

The TPS562200 and TPS563200 are simple, easy-to-use, 2 A and 3 A synchronous step-down (buck) converters in SOT-23 package.

The devices are optimized to operate with minimum external component counts and also optimized to achieve low standby current.

These switch mode power supply (SMPS) devices employ D-CAP2 mode control providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

TPS562200 and TPS563200 operate in Advanced Eco-mode, which maintains high efficiency during light load operation. The devices are available in a 6-pin 1.6 x 2.9mm SOT (DDC) package, and specified from –40°C to 85°C of ambient temperature.

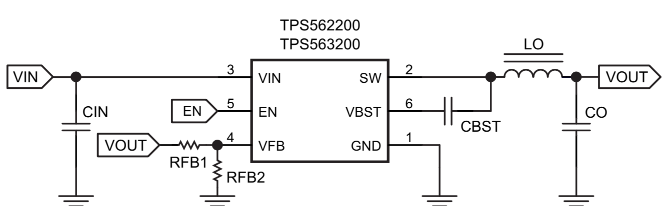
**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS562200 | SOT (6) | 1.60mm x 2.90mm |
| TPS563200(2) | | |

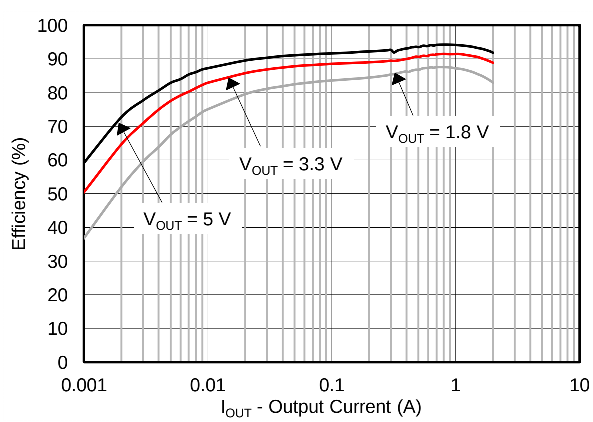
(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) Product Preview

## 4 Simplified Schematic




**TPS562200 Efficiency**



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# 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (January 2014) to Revision B** — **Page**

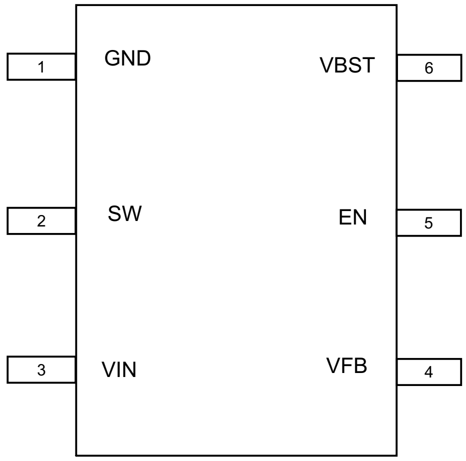
- Changed the data sheet title From: 4.5 V to 17 V Input, 2A Synchronous Step-Down.. To: 4.5 V to 17 V Input, 2A/3A Synchronous Step-Down.. ..... 1
- Changed the datasheet to the new Ti format ..... 1
- Changed device number From: TPS563209 To TPS563200 ..... 1
- Added Feature: Integrated 68-mΩ and 39-mΩ FETs ('563200) ..... 1
- Changed Feature From: 2% Feedback Voltage Accuracy (25°C) To: 1% Feedback Voltage Accuracy (25°C) ..... 1
- Added the Timing Requirements table ..... 5
- Added Table 1 ..... 13
- Changed Table 2 ..... 13
- Deleted sentence following Table 2 "For higher output voltages, additional phase boost can be achieved by adding a feed forward capacitor (C7) in parallel with R2." ..... 14
- Added Application Information for the TPS563200 device ..... 17
- Added Table 3 ..... 17

**Changes from Original (January 2014) to Revision A** — **Page**

- Changed the device status From: Product Preview To: Production ..... 1

# 6 Pin Configuration and Functions

**TPS562200, TPS563200**
**DDC Package**
**Top View**




## Pin Functions

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | NUMBER | |
| GND | 1 | Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point. |
| SW | 2 | Switch node connection between high-side NFET and low-side NFET. |
| VIN | 3 | Input voltage supply pin. The drain terminal of high-side power NFET. |
| VFB | 4 | Converter feedback input. Connect to output voltage with feedback resistor divider. |
| EN | 5 | Enable input control. Active high and must be pulled up to enable the device. |
| VBST | 6 | Supply input for the high-side NFET gate drive circuit. Connect a 0.1µF capacitor between VBST and SW pins. |

# 7 Specifications

## 7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | VALUE MIN | VALUE MAX | UNIT |
|---|---|---|---|---|
| Input voltage range | VIN, EN | –0.3 | 19 | V |
| | VBST | –0.3 | 25 | V |
| | VBST (10 ns transient) | –0.3 | 27 | V |
| | VBST (vs SW) | –0.3 | 6.5 | V |
| | VFB | –0.3 | 6.5 | V |
| | SW | –2 | 19 | V |
| | SW (10 ns transient) | –3.5 | 21 | V |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –55 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | –2 | 2 | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | –500 | 500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Supply input voltage range | | 4.5 | 17 | V |
| $V_I$ | Input voltage range | VBST | –0.1 | 23 | V |
| | | VBST (10 ns transient) | –0.1 | 26 | |
| | | VBST(vs SW) | –0.1 | 6 | |
| | | EN | –0.1 | 17 | |
| | | VFB | –0.1 | 5.5 | |
| | | SW | –1.8 | 17 | |
| | | SW (10 ns transient) | –3.5 | 20 | |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

## 7.4 Thermal Information

| THERMAL METRIC (1) | | TPS562200 DDC (6 PINS) | TPS563200 DDC (6 PINS) | UNITS |
|---|---|---|---|---|
| $R_{θJA}$ | Junction-to-ambient thermal resistance | 109.2 | 87.9 | °C/W |
| $R_{θJCtop}$ | Junction-to-case (top) thermal resistance | 44.5 | 42.2 | |
| $R_{θJB}$ | Junction-to-board thermal resistance | 57.3 | 13.6 | |
| $ψ_{JT}$ | Junction-to-top characterization parameter | 2.3 | 1.9 | |
| $ψ_{JB}$ | Junction-to-board characterization parameter | 60.4 | 13.3 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

over operating free-air temperature range, VIN = 12V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | |
| $I_{(VIN)}$ | Operating – non-switching supply current | $V_{IN}$ current, $T_A$ = 25°C, EN = 5V, $V_{FB}$ = 0.8 V | TPS562200 | | 230 | 330 | μA |
| | | | TPS563200 | | 190 | 290 | μA |
| $I_{(VINSDN)}$ | Shutdown supply current | $V_{IN}$ current, $T_A$ = 25°C, EN = 0 V | | | 3 | 10 | μA |
| **LOGIC THRESHOLD** | | | | | | | |
| $V_{EN(H)}$ | EN high-level input voltage | EN | | 1.6 | | | V |
| $V_{EN(L)}$ | EN low-level input voltage | EN | | | | 0.6 | V |
| $R_{EN}$ | EN pin resistance to GND | $V_{EN}$ = 12 V | | 225 | 450 | 900 | kΩ |
| **$V_{FB}$ VOLTAGE AND DISCHARGE RESISTANCE** | | | | | | | |
| $V_{FB(TH)}$ | $V_{FB}$ threshold voltage | $T_A$ = 25°C, $V_O$ = 1.05 V, $I_O$ = 10mA, Eco-mode™ operation | | | 772 | | mV |
| | | $T_A$ = 25°C, $V_O$ = 1.05 V, continuous mode operation | | 758 | 765 | 772 | mV |
| $I_{(VFB)}$ | $V_{FB}$ input current | $V_{FB}$ = 0.8V, $T_A$ = 25°C | | | 0 | ±0.1 | μA |
| **MOSFET** | | | | | | | |
| $R_{DS(on)h}$ | High side switch resistance | $T_A$ = 25°C, $V_{BST}$ – SW = 5.5 V | TPS562200 | | 122 | | mΩ |
| | | | TPS563200 | | 68 | | mΩ |
| $R_{DS(on)l}$ | Low side switch resistance | $T_A$ = 25°C | TPS562200 | | 72 | | mΩ |
| | | | TPS563200 | | 39 | | mΩ |
| **CURRENT LIMIT** | | | | | | | |
| $I_{ocl}$ | Current limit (1) | DC current, $V_{OUT}$ = 1.05 V, $L_{OUT}$ = 2.2 μF | TPS562200 | 2.5 | 3.2 | 4.3 | A |
| | | | TPS563200 | 3.5 | 4.2 | 5.3 | A |
| **THERMAL SHUTDOWN** | | | | | | | |
| $T_{SDN}$ | Thermal shutdown threshold (1) | Shutdown temperature | | | 155 | | °C |
| | | Hysteresis | | | 35 | | °C |
| **OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION** | | | | | | | |
| $V_{OVP}$ | Output OVP threshold | OVP Detect (L > H) | | | 125% | | |
| $V_{UVP}$ | Output Hiccup threshold | Hiccup detect (H > L) | | | 65% | | |
| $t_{UVPEN}$ | Output Hiccup enable delay | Relative to soft-start time | | | x1.7 | | |
| **UVLO** | | | | | | | |
| UVLO | UVLO threshold | Wake up VIN voltage | | 3.45 | 3.75 | 4.05 | V |
| | | Hysteresis VIN voltage | | 0.13 | 0.32 | 0.55 | V |

(1) Not production tested

## 7.6 Timing Requirements

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ON-TIME TIMER CONTROL** | | | | | | |
| $t_{ON}$ | On time | $V_{IN}$ = 12 V, $V_O$ = 1.05 V | | 150 | | ns |
| $t_{OFF(MIN)}$ | Minimum off time | $T_A$ = 25°C, $V_{FB}$ = 0.5 V | | 260 | 310 | ns |
| **SOFT START** | | | | | | |
| $t_{ss}$ | Soft-start time | Internal soft-start time | 0.7 | 1 | 1.3 | ms |

## 7.7 Typical Characteristics TPS562200

$V_{IN}$ = 12 V (unless otherwise noted).

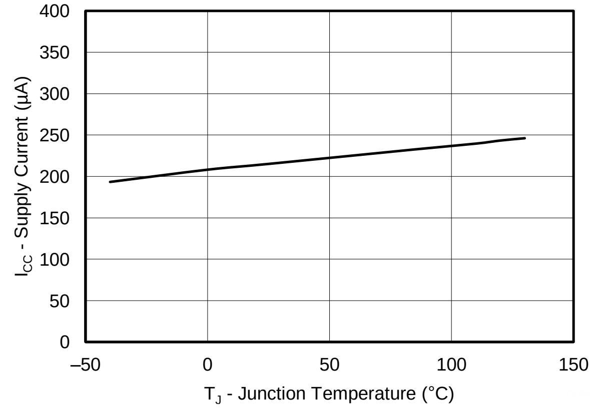
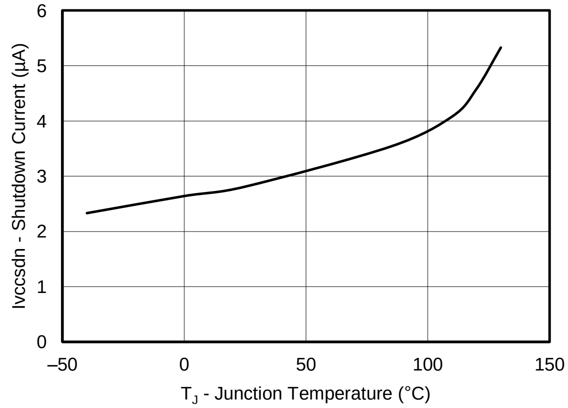
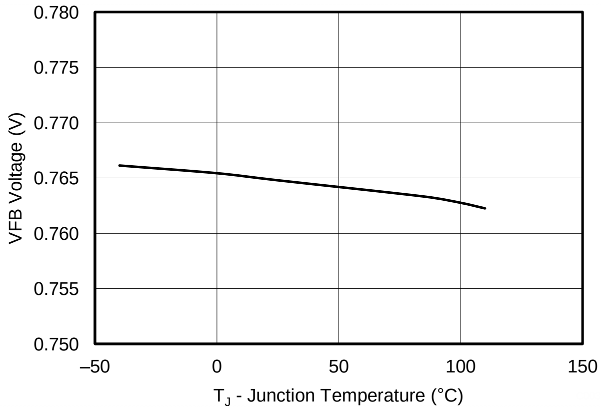



Figure 1. Supply Current vs Junction Temperature




EN = 0 V

Figure 2. VIN Shutdown Current vs Junction Temperature




$I_O$ = 1 A

Figure 3. VFB Voltage vs Junction Temperature

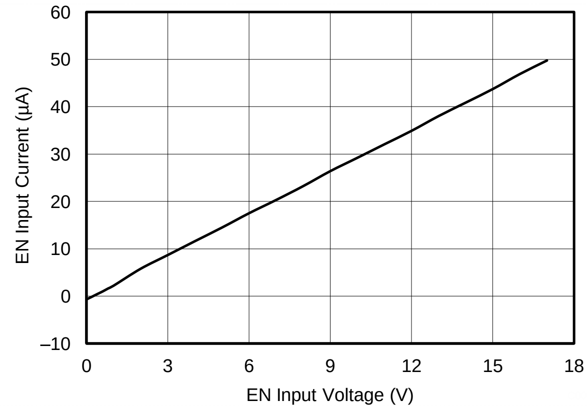



Figure 4. EN Current vs EN Voltage

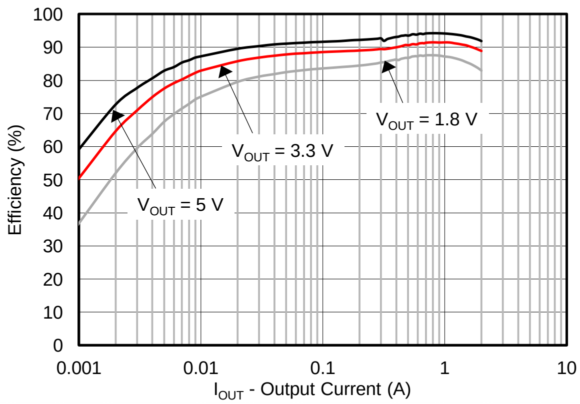



Figure 5. Efficiency vs Output Current

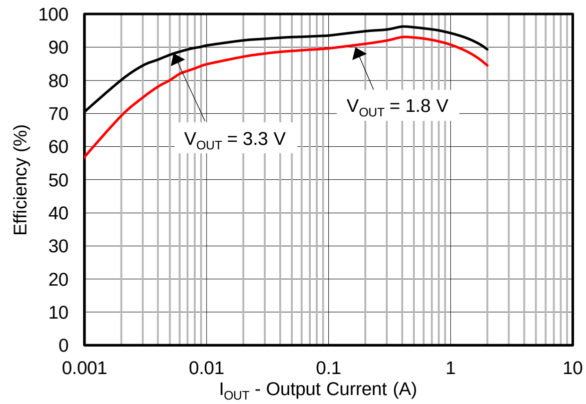



Figure 6. Efficiency vs Output Current ($V_{IN}$ = 5 V)

## Typical Characteristics TPS562200 (continued)

$V_{IN}$ = 12 V (unless otherwise noted).

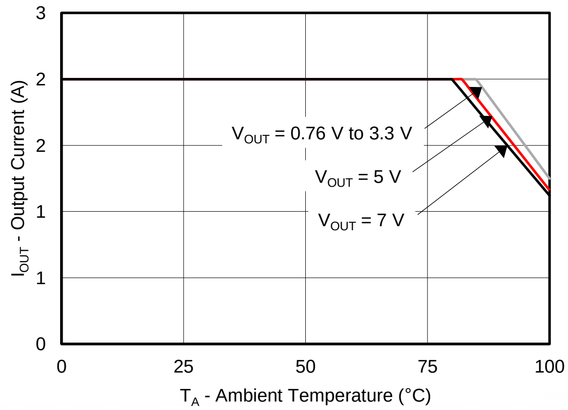
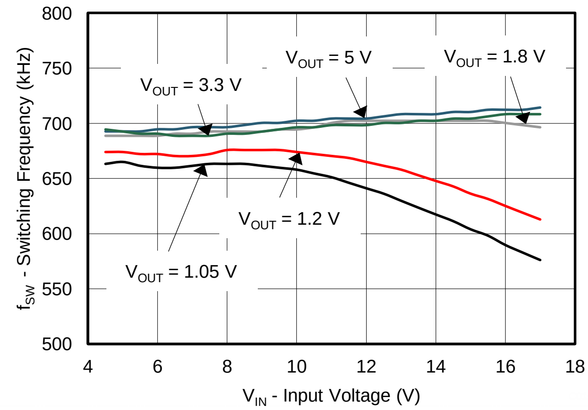



**Figure 7. Output Current vs Ambient Temperature**




$I_{OUT}$ = 500 mA

**Figure 8. Switching Frequency vs Input Voltage**

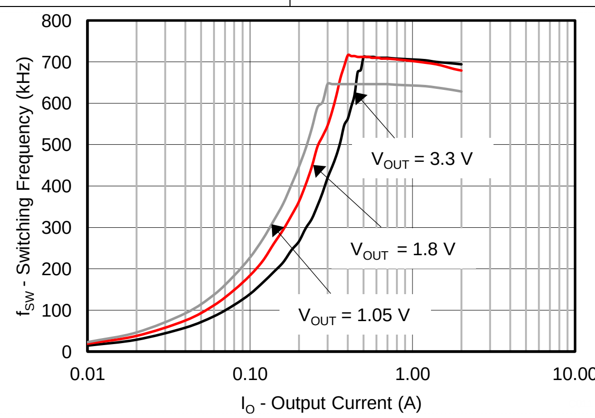



**Figure 9. Switching Frequency vs Output Current**

## 7.8 Typical Characteristics TPS563200

$V_{IN}$ = 12 V (unless otherwise noted).

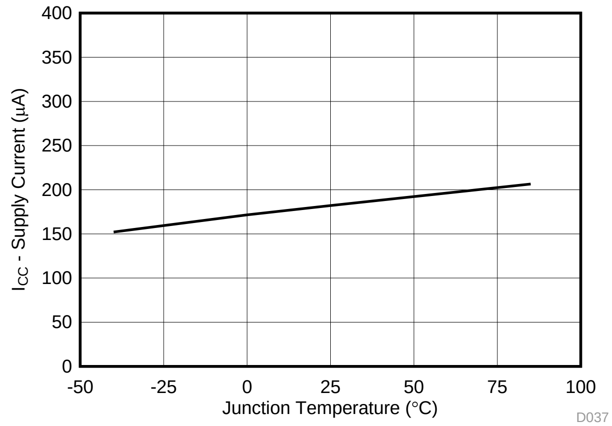
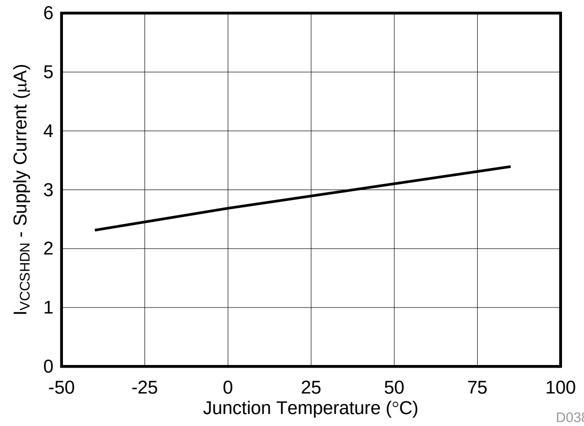
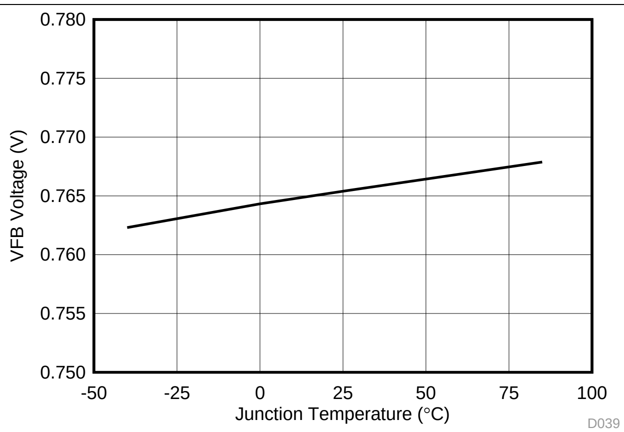



**Figure 10. Supply Current vs Junction Temperature**




EN = 0 V

**Figure 11. VIN Shutdown Current vs Junction Temperature**




$I_O$ = 1 A

**Figure 12. VFB Voltage vs Junction Temperature**

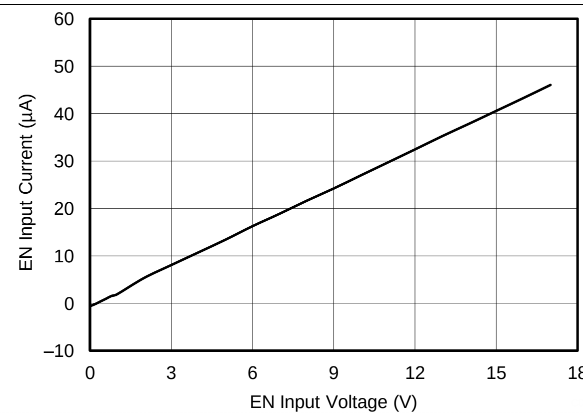



**Figure 13. EN Current vs EN Voltage**

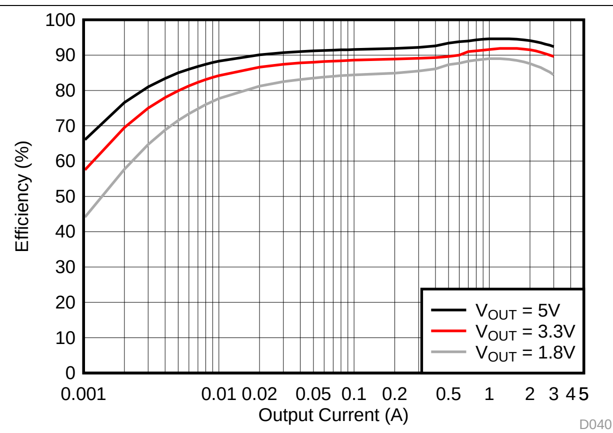



**Figure 14. Efficiency vs Output Current**

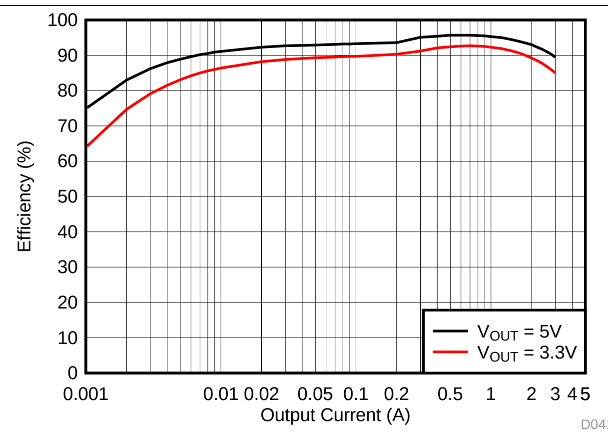



**Figure 15. Efficiency vs Output Current ($V_{IN}$ = 5 V)**

## Typical Characteristics TPS563200 (continued)

$V_{IN}$ = 12 V (unless otherwise noted).

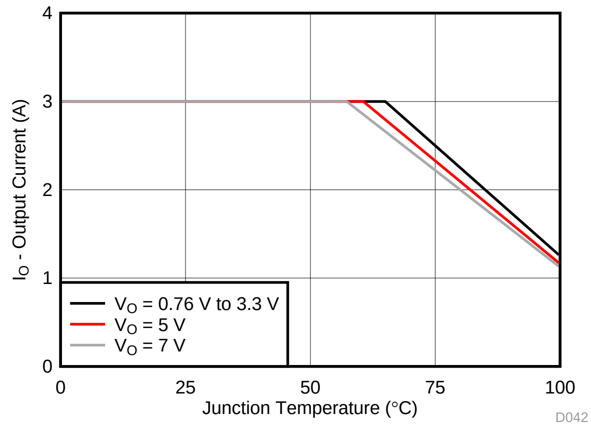



**Figure 16. Output Current vs Ambient Temperature**

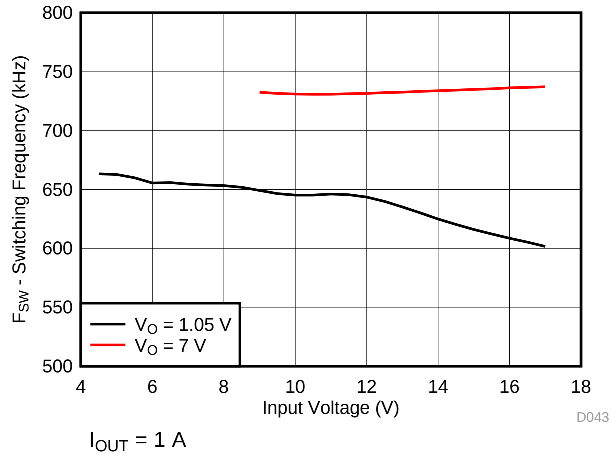



**Figure 17. Switching Frequency vs Input Voltage**

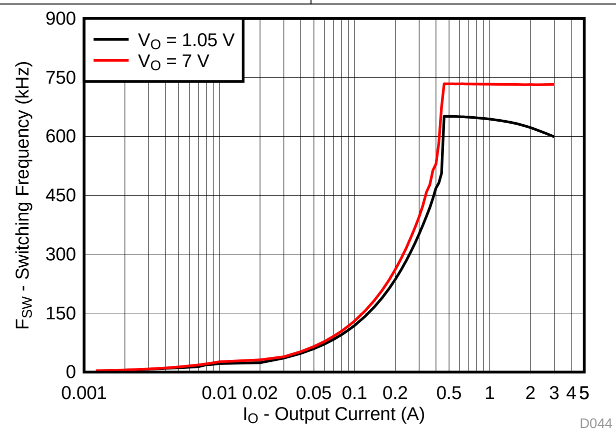



**Figure 18. Switching Frequency vs Output Current**

# 8 Detailed Description

## 8.1 Overview

The TPS562200 and TPS563200 are 2-A and 3-A synchronous step-down converters. The proprietary D-CAP2™mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2™ mode control can reduce the output capacitance required to meet a specific level of performance.

## 8.2 Functional Block Diagrams

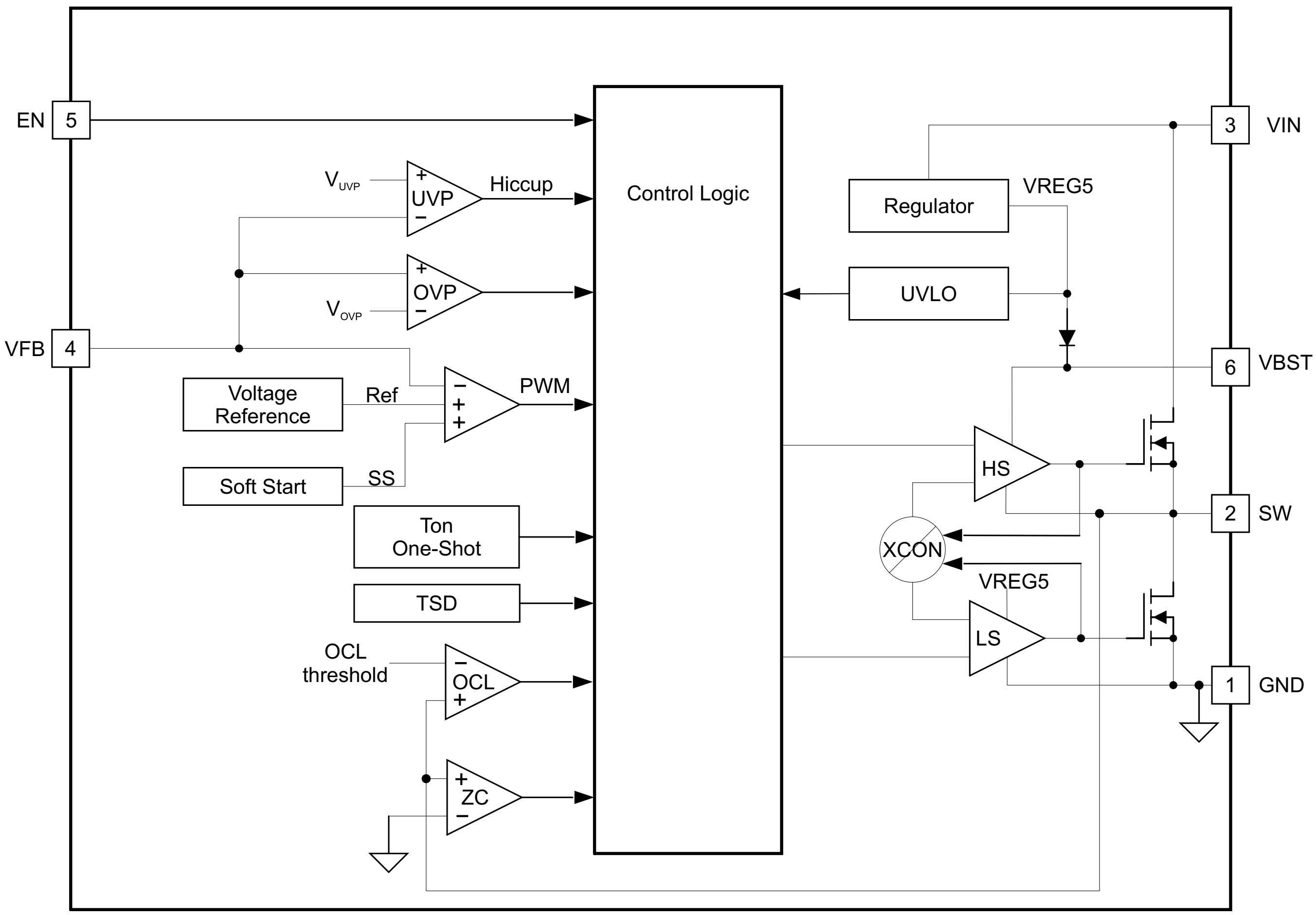



Figure 19. Functional Block Diagram: TPS562200 and TPS563200

## 8.3 Feature Description

### 8.3.1 The Adaptive On-Time Control and PWM Operation

The main control loop of the TPS562200 and TPS563200 are adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. The D-CAP2™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot duration is set proportional to the converter input voltage, $V_{IN}$, and inversely proportional to the output voltage, $V_O$, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

### 8.3.2 Advanced Eco-Mode™ Control

The TPS562200 and TPS563200 are designed with Advanced Eco-mode™ to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}} \tag{1}$$

### 8.3.3 Soft Start and Pre-Biased Soft Start

The TPS562200 and TPS563200 have an internal 1 ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator. If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage VFB. This scheme ensures that the converters ramp up smoothly into regulation point.

### 8.3.4 Current Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by $V_{IN}$, $V_{OUT}$, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current $I_{OUT}$. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL threshold is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. Then, the device shuts down after the UVP delay time (typically 14 µs) and re-start after the hiccup time (typically 12 ms).

## Feature Description (continued)

When the overcurrent condition is removed, the output voltage returns to the regulated value.

### 8.3.5 Over Voltage Protection

TPS562200 and TPS563200 detect overvoltage condition by monitoring the feedback voltage (VFB). When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and both the high-side MOSFET driver and the low-side MOSFET driver turn off. This function is non-latch operation.

### 8.3.6 UVLO Protection

Undervoltage lock out protection (UVLO) monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

### 8.3.7 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 155°C), the device is shut off. This is a non-latch protection

## 8.4 Device Functional Modes

### 8.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS562200 and TPS563200 can operate in their normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS562200 and TPS563200 operate at a quasi-fixed frequency of 650 kHz.

### 8.4.2 Eco-mode Operation

When the TPS562200 and TPS563200 are in the normal CCM operating mode and the switch current falls to 0 A, the TPS562200 and TPS563200 begin operating in pulse skipping eco-mode. Each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VFB voltage falls below the eco-mode threshold voltage. As the output current decreases the perceived time between switching pulses increases.

### 8.4.3 Standby Operation

When the TPS562200 and TPS563200 are operating in either normal CCM or eco-mode, they may be placed in standby by asserting the EN pin low.

# 9 Application and Implementation

## 9.1 Application Information

The TPS562200 and TPS563200 are typically used as step down converters, which convert a voltage from 4.5V - 17V to a lower voltage. Webench software is available to aid in the design and analysis of circuits

## 9.2 Typical Applications

### 9.2.1 TPS562200 4.5-V to 17-V Input, 1.05-V Output Converter

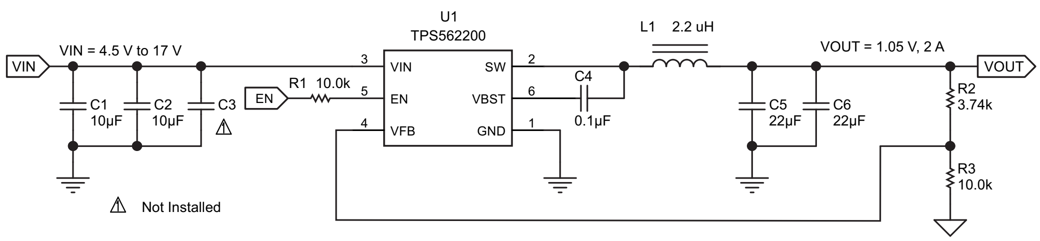



**Figure 20. TPS562200 1.05V/2A Reference Design**

#### *9.2.1.1 Design Requirements*

To begin the design process, the user must know a few application parameters:

**Table 1. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Input voltage range | 4.5 V to 17V |
| Output voltage | 1.05V |
| Output current | 2A |
| Output voltage ripple | 20mVpp |

#### *9.2.1.2 Detailed Design Procedures*

##### 9.2.1.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 2 to calculate $V_{OUT}$.

To improve efficiency at light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.765 \times \left(1 + \frac{R2}{R3}\right) \tag{2}$$

##### 9.2.1.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{3}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 1.

**Table 2. TPS562200 Recommended Component Values**

| Output Voltage (V) | R2 (kΩ) | R3 (kΩ) | L1 (µH) TPS562200 | | | C8 + C9 (µF) |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| 1 | 3.09 | 10.0 | 1.5 | 2.2 | 4.7 | 20 - 68 |
| 1.05 | 3.74 | 10.0 | 1.5 | 2.2 | 4.7 | 20 - 68 |
| 1.2 | 5.76 | 10.0 | 1.5 | 2.2 | 4.7 | 20 - 68 |
| 1.5 | 9.53 | 10.0 | 1.5 | 2.2 | 4.7 | 20 - 68 |
| 1.8 | 13.7 | 10.0 | 1.5 | 2.2 | 4.7 | 20 - 68 |
| 2.5 | 22.6 | 10.0 | 2.2 | 3.3 | 4.7 | 20 - 68 |
| 3.3 | 33.2 | 10.0 | 2.2 | 3.3 | 4.7 | 20 - 68 |
| 5 | 54.9 | 10.0 | 3.3 | 4.7 | 4.7 | 20 - 68 |
| 6.5 | 75 | 10.0 | 3.3 | 4.4 | 4.7 | 20 - 68 |

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 4, Equation 5 and Equation 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for $f_{SW}$.

Use 650 kHz for $f_{SW}$. Make sure the chosen inductor is rated for the peak current of Equation 5 and the RMS current of Equation 6.

$$I_{lP-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \tag{4}$$

$$I_{lPEAK} = I_O + \frac{I_{lP-P}}{2} \tag{5}$$

$$I_{LO(RMS)} = \sqrt{I_O^{\,2} + \frac{1}{12} I_{lP-P}^{\,2}} \tag{6}$$

For this design example, the calculated peak current is 2.34 A and the calculated RMS current is 2.01 A. The inductor used is a TDK CLF7045T-2R2N with a peak current rating of 5.5-A and an RMS current rating of 4.3-A

The capacitor value and ESR determines the amount of output voltage ripple. The device is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 µF to 68 µF. Use Equation 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \tag{7}$$

For this design two TDK C3216X5R0J226M 22 µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286 A and each output capacitor is rated for 4 A.

#### 9.2.1.2.3 Input Capacitor Selection

The device requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1 µF capacitor(C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

#### 9.2.1.2.4 Bootstrap Capacitor Selection

A 0.1 µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

#### 9.2.1.3 *Application Curves*

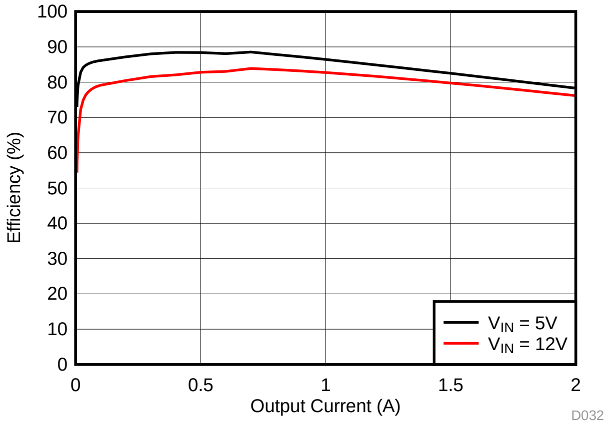



**Figure 21. TPS562200 Efficiency**

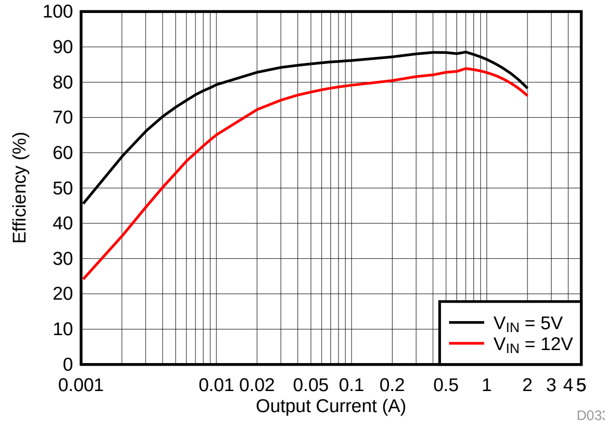



**Figure 22. TPS562200 Light Load Efficiency**

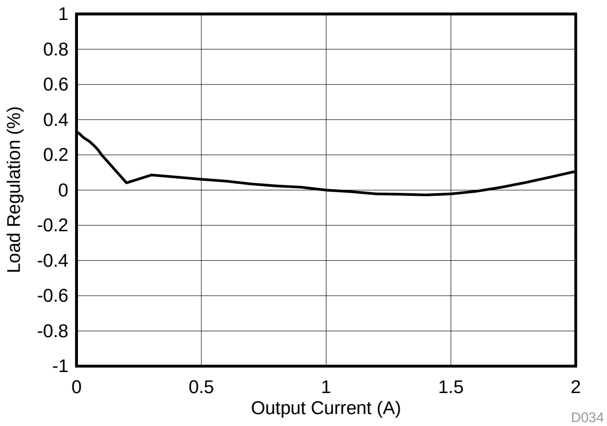



**Figure 23. TPS562200 Load Regulation, $V_I$ = 5 V**

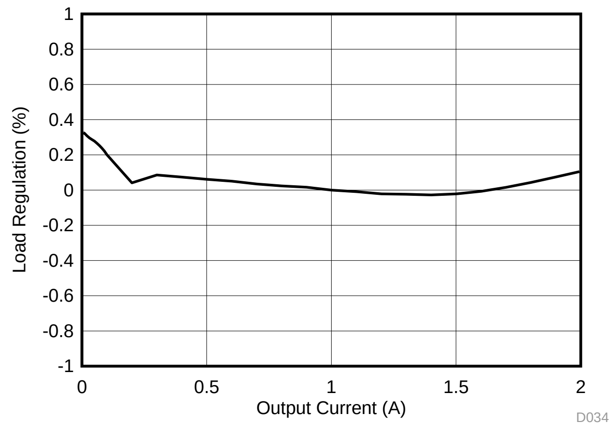



**Figure 24. TPS562200 Load Regulation, $V_I$ = 12 V**

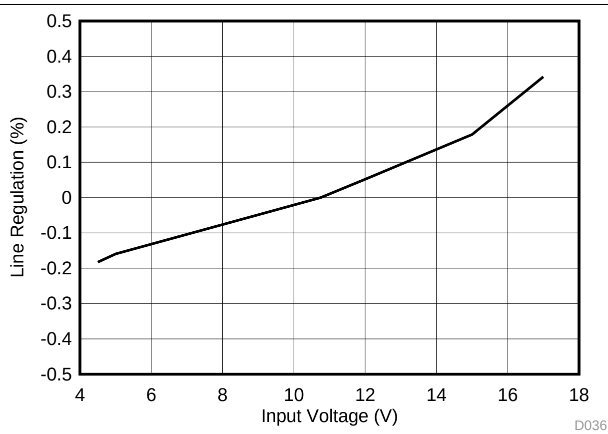



**Figure 25. TPS562200 Line Regulation**

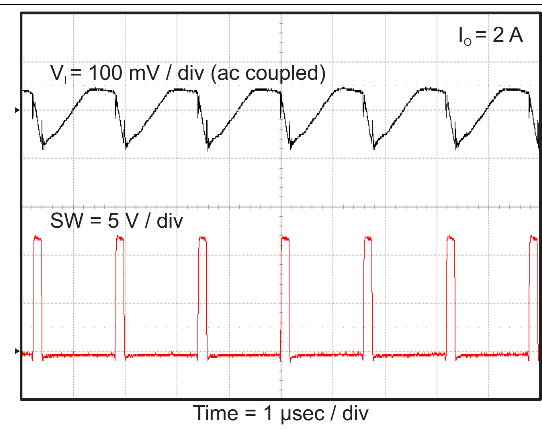



**Figure 26. TPS562200 Input Voltage Ripple**

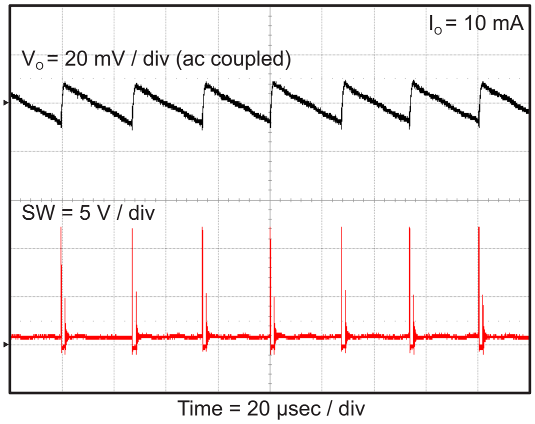



**Figure 27. TPS562200 Output Voltage Ripple**

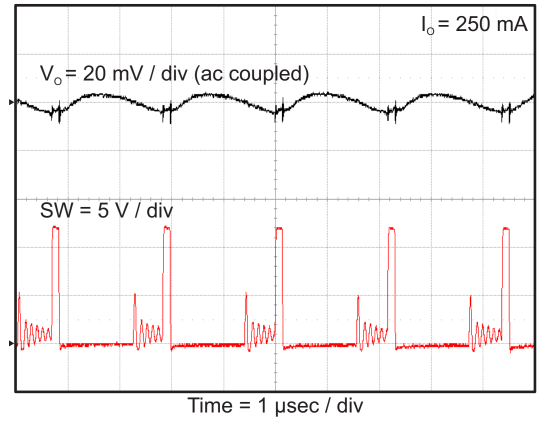



**Figure 28. TPS562200 Output Voltage Ripple**

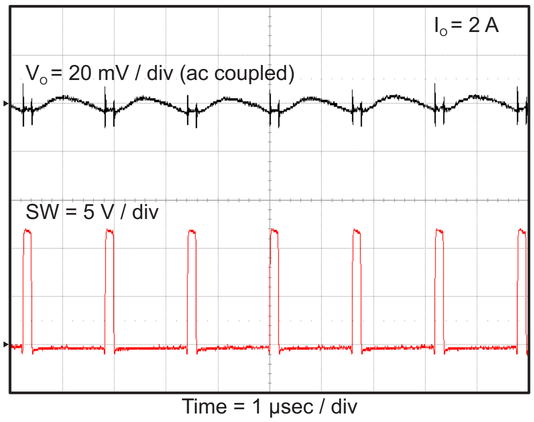



**Figure 29. TPS562200 Output Voltage Ripple**

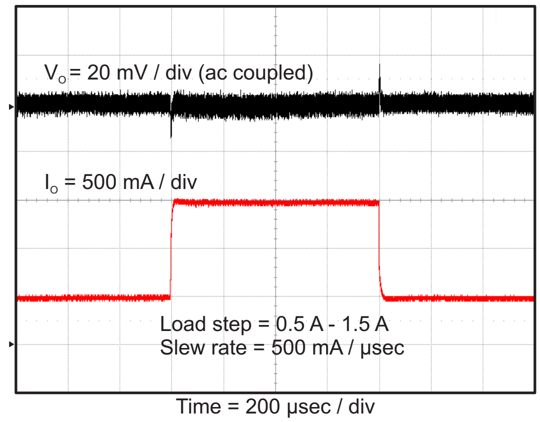



**Figure 30. TPS562200 Transient Response**

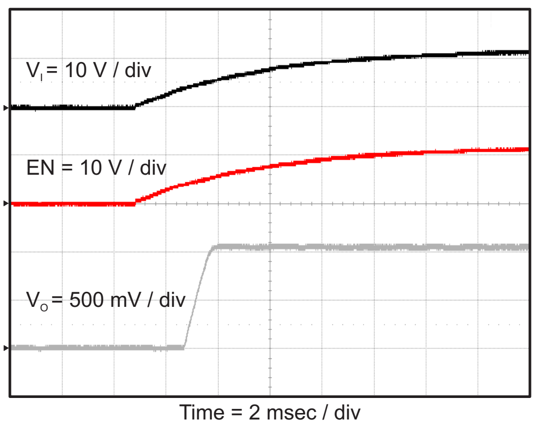



**Figure 31. TPS562200 Start Up Relative to $V_I$**

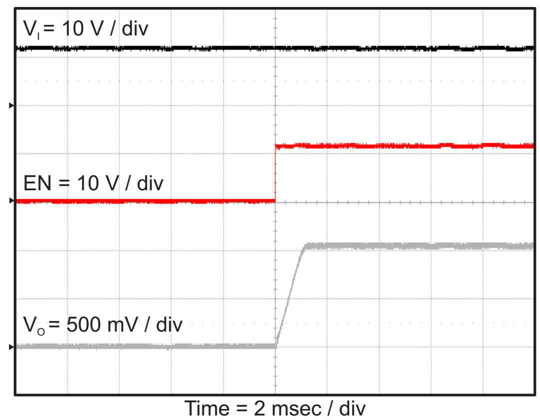



**Figure 32. TPS562200 Start Up Relative to EN**

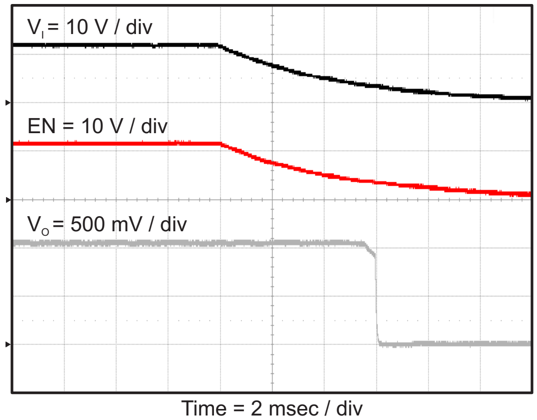


**Figure 33. TPS562200 Shut Down Relative to $V_I$**

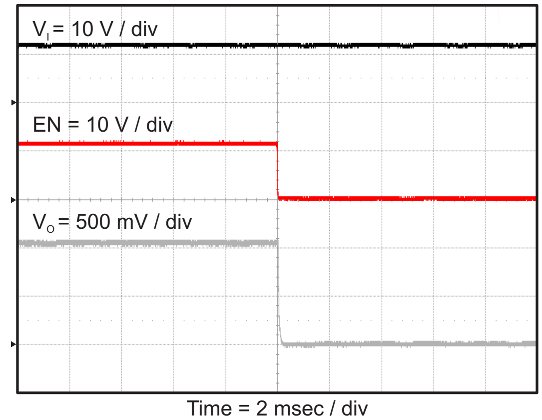


**Figure 34. TPS562200 Shut Down Relative to EN**

### 9.2.2 TPS563200 4.5-V to 17-V Input, 1.05-V Output Converter

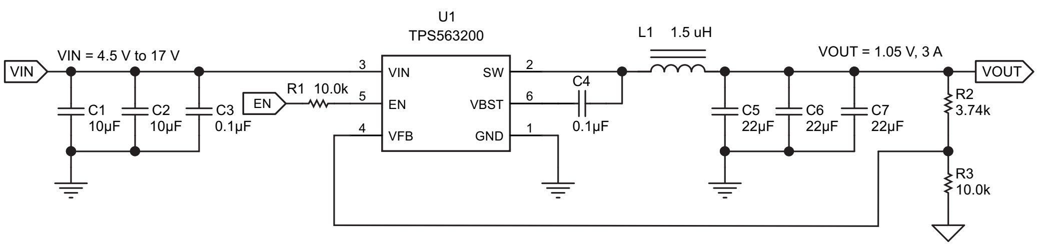


**Figure 35. TPS563200 1.05V/3A Reference Design**

#### *9.2.2.1 Design Requirements*

To begin the design process, the user must know a few application parameters:

**Table 3. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Input voltage range | 4.5 V to 17V |
| Output voltage | 1.05V |
| Output current | 3A |
| Output voltage ripple | 20mVpp |

#### *9.2.2.2 Detailed Design Procedures*

The detailed design procedure for TPS563200 is the same as for TPS562200 except for inductor selection.

#### 9.2.2.2.1 Output Filter Selection

**Table 4. TPS563200 Recommended Component Values**

| Output Voltage (V) | R2 (kΩ) | R3 (kΩ) | L1 (µH) TPS563200 | | | C8 + C9 (µF) |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| 1 | 3.09 | 10.0 | 1.0 | 1.5 | 4.7 | 20 - 68 |
| 1.05 | 3.74 | 10.0 | 1.0 | 1.5 | 4.7 | 20 - 68 |
| 1.2 | 5.76 | 10.0 | 1.0 | 1.5 | 4.7 | 20 - 68 |
| 1.5 | 9.53 | 10.0 | 1.0 | 1.5 | 4.7 | 20 - 68 |
| 1.8 | 13.7 | 10.0 | 1.5 | 2.2 | 4.7 | 20 - 68 |
| 2.5 | 22.6 | 10.0 | 1.5 | 2.2 | 4.7 | 20 - 68 |
| 3.3 | 33.2 | 10.0 | 1.5 | 2.2 | 4.7 | 20 - 68 |
| 5 | 54.9 | 10.0 | 2.2 | 3.3 | 4.7 | 20 - 68 |
| 6.5 | 75 | 10.0 | 2.2 | 3.3 | 4.7 | 20 - 68 |

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 8, Equation 9 and Equation 10. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for $f_{SW}$.

Use 650 kHz for $f_{SW}$. Make sure the chosen inductor is rated for the peak current of Equation 9 and the RMS current of Equation 10.

$$I_{lP-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (8)$$

$$I_{lPEAK} = I_O + \frac{I_{lP-P}}{2} \quad (9)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{lP-P}^2} \quad (10)$$

For this design example, the calculated peak current is 3.505 A and the calculated RMS current is 3.014 A. The inductor used is a TDK CLF7045T-1R5N with a peak current rating of 7.3-A and an RMS current rating of 4.9-A

### *9.2.2.3 Application Curves*

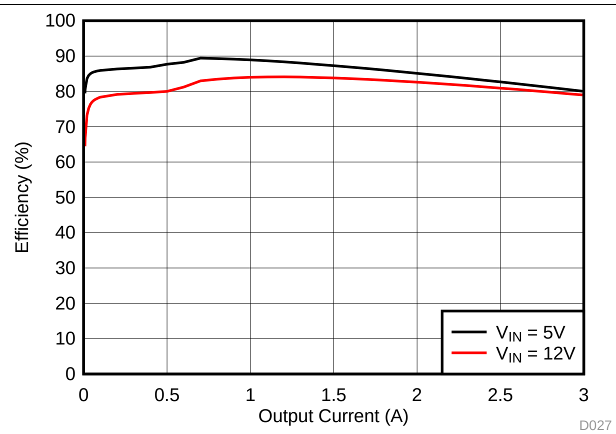



**Figure 36. TPS563200 Efficiency**

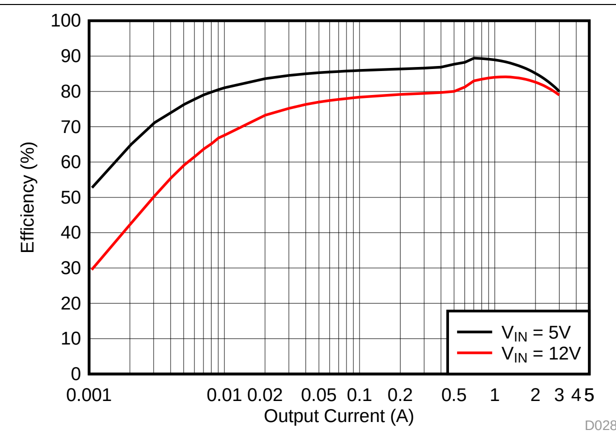



**Figure 37. TPS563200 Light Load Efficiency**

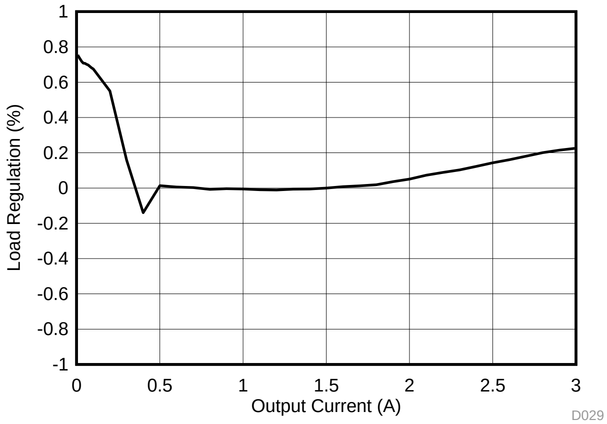



**Figure 38. TPS563200 Load Regulation, $V_I$ = 5 V**

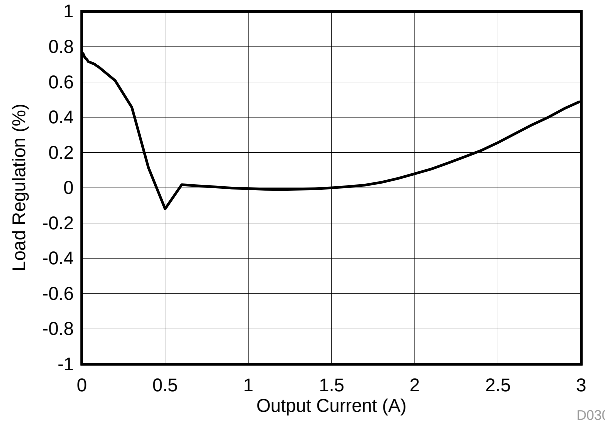



**Figure 39. TPS563200 Load Regulation, $V_I$ = 12 V**

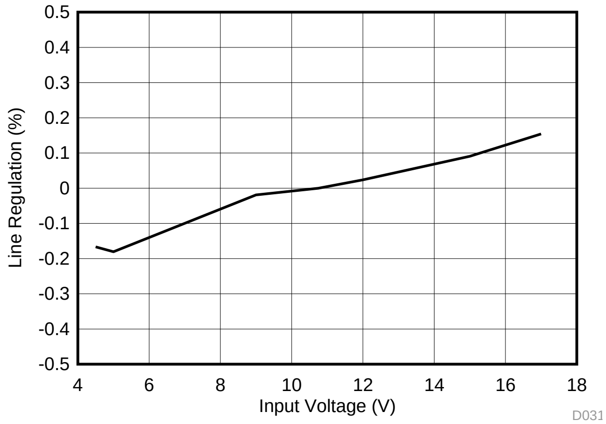



**Figure 40. TPS563200 Line Regulation**

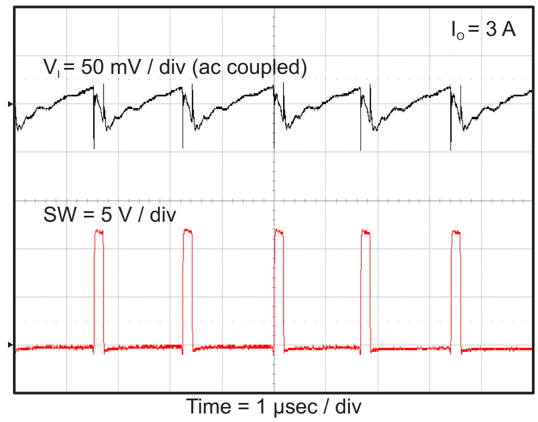



**Figure 41. TPS563200 Input Voltage Ripple**

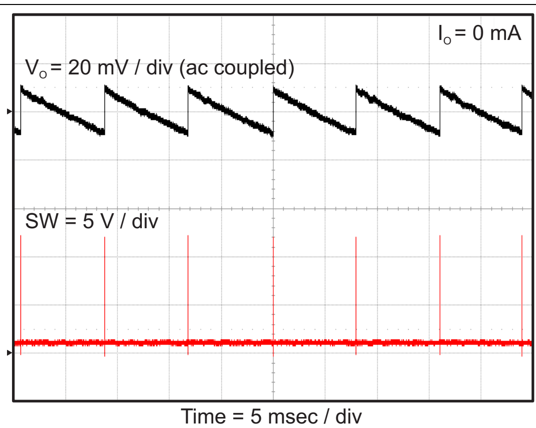



**Figure 42. TPS563200 Output Voltage Ripple**

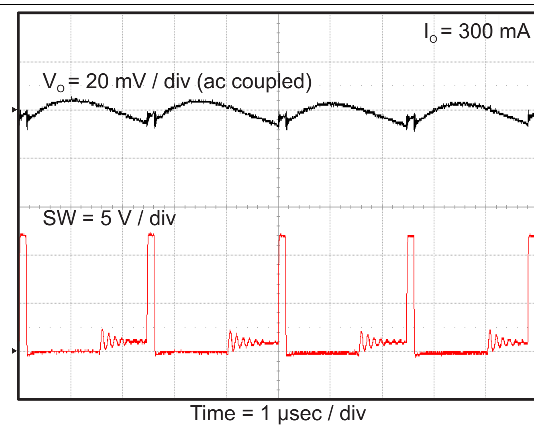



**Figure 43. TPS563200 Output Voltage Ripple**

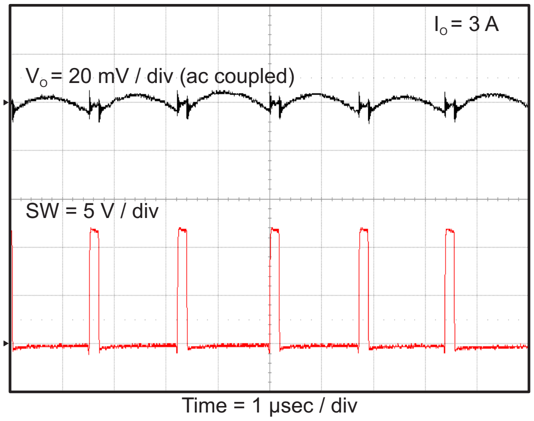



**Figure 44. TPS563200 Output Voltage Ripple**

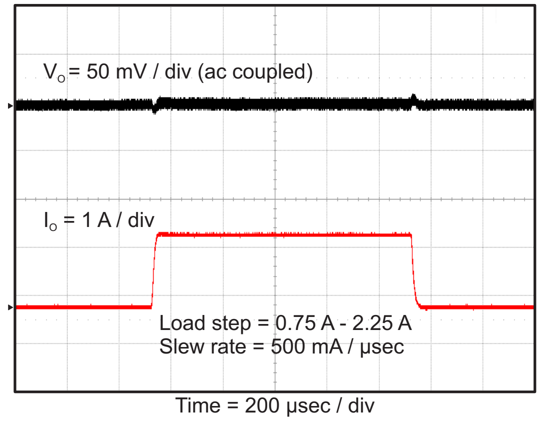



**Figure 45. TPS563200 Transient Response**

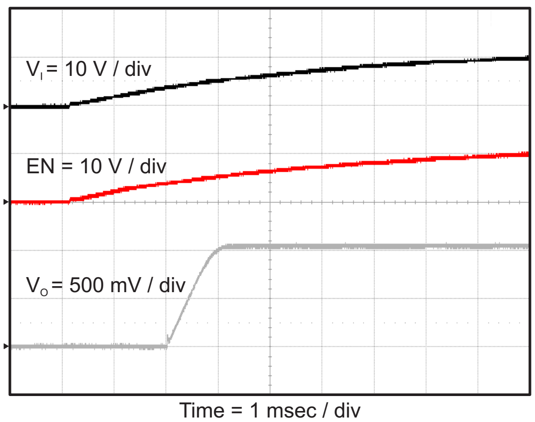



**Figure 46. TPS563200 Start Up Relative to $V_I$**

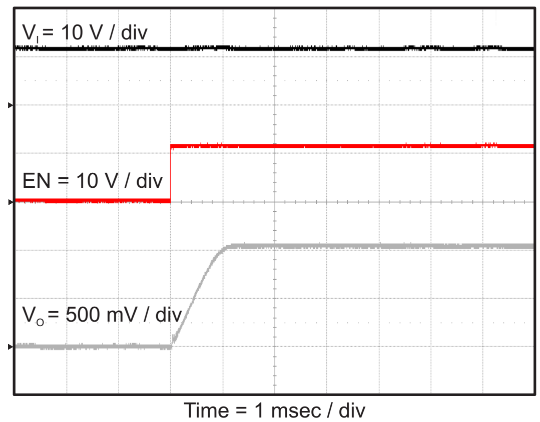



**Figure 47. TPS563200 Start Up Relative to EN**

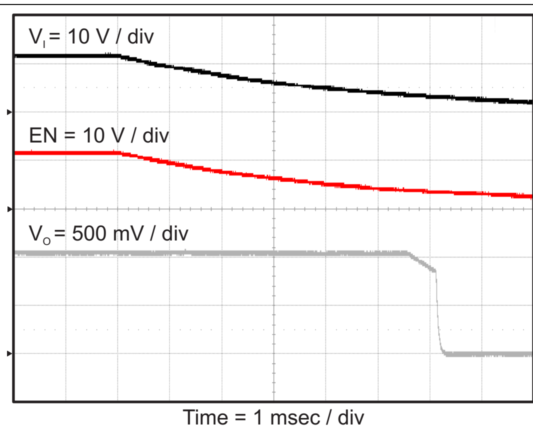



**Figure 48. TPS563200 Shut Down Relative to $V_I$**

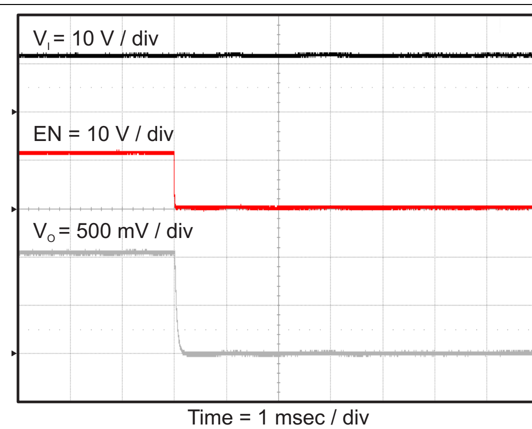



**Figure 49. TPS563200 Shut Down Relative to EN**

## 10 Power Supply Recommendations

The TPS562200 and TPS563200 are designed to operate from input supply voltage in the range of 4.5V to 17V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 65%. Using that criteria, the minimum recommended input voltage is $V_O$ / 0.65.

# 11 Layout

## 11.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

## 11.2 Layout Example

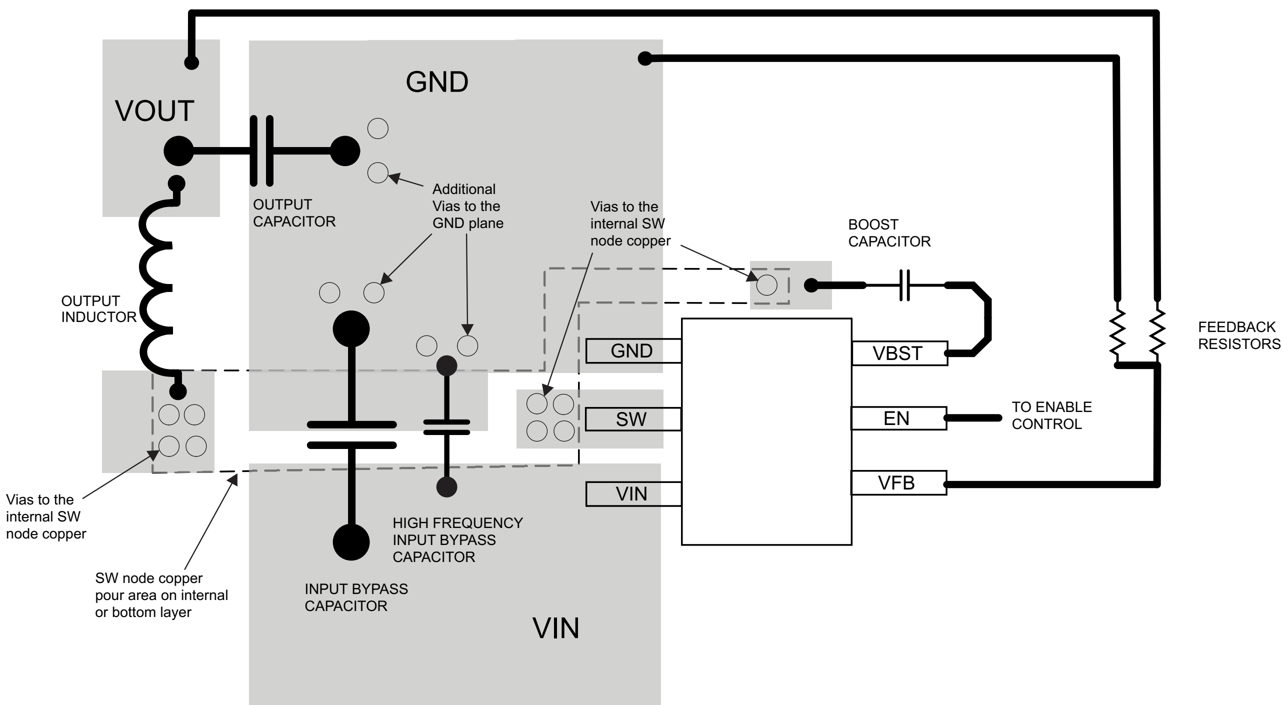



**Figure 50. Typical Layout**

# 12 Device and Documentation Support

## 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 5. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TPS562200 | Click here | Click here | Click here | Click here | Click here |
| TPS563200 | Click here | Click here | Click here | Click here | Click here |

## 12.2 Trademarks

D-CAP2, Eco-mode are trademarks of Texas Instruments.
Blu-ray Disc is a trademark of Blu-ray Disc Association.

## 12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS562200DDCR | ACTIVE | SOT | DDC | 6 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | 200 | Samples |
| TPS562200DDCT | ACTIVE | SOT | DDC | 6 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | 200 | Samples |
| TPS563200DDCR | ACTIVE | SOT | DDC | 6 | 3000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | 320 | Samples |
| TPS563200DDCT | ACTIVE | SOT | DDC | 6 | 250 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 85 | 320 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

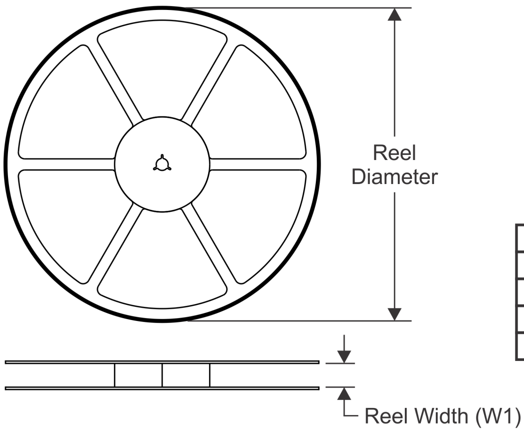
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

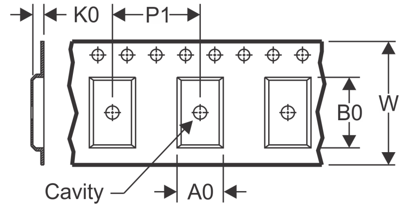
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

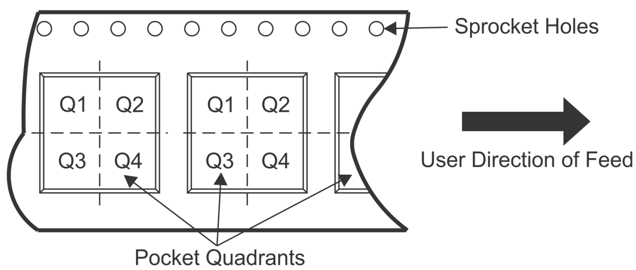



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

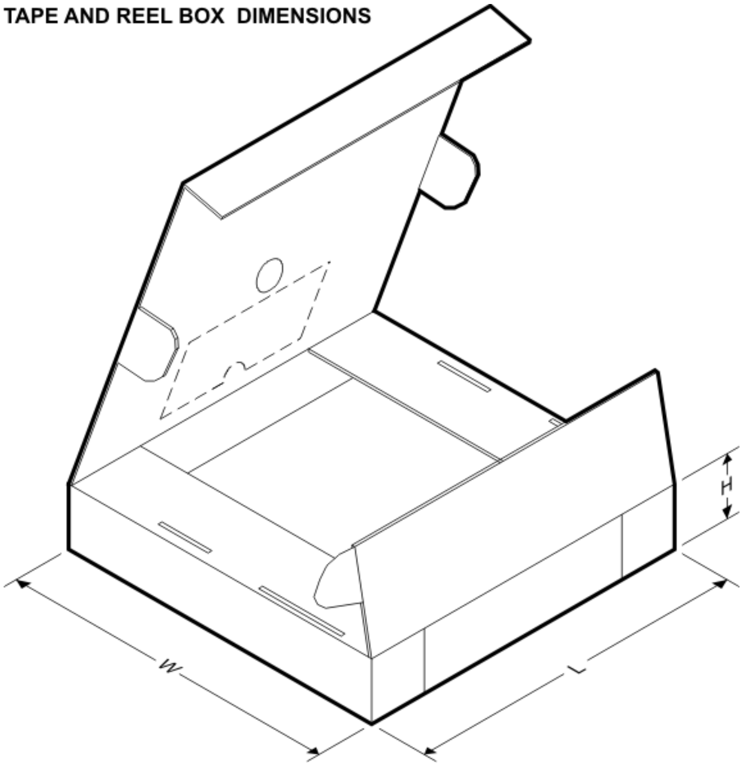
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS562200DDCR | SOT | DDC | 6 | 3000 | 180.0 | 9.5 | 3.17 | 3.1 | 1.1 | 4.0 | 8.0 | Q3 |
| TPS562200DDCT | SOT | DDC | 6 | 250 | 180.0 | 9.5 | 3.17 | 3.1 | 1.1 | 4.0 | 8.0 | Q3 |
| TPS563200DDCR | SOT | DDC | 6 | 3000 | 180.0 | 9.5 | 3.17 | 3.1 | 1.1 | 4.0 | 8.0 | Q3 |
| TPS563200DDCT | SOT | DDC | 6 | 250 | 180.0 | 9.5 | 3.17 | 3.1 | 1.1 | 4.0 | 8.0 | Q3 |

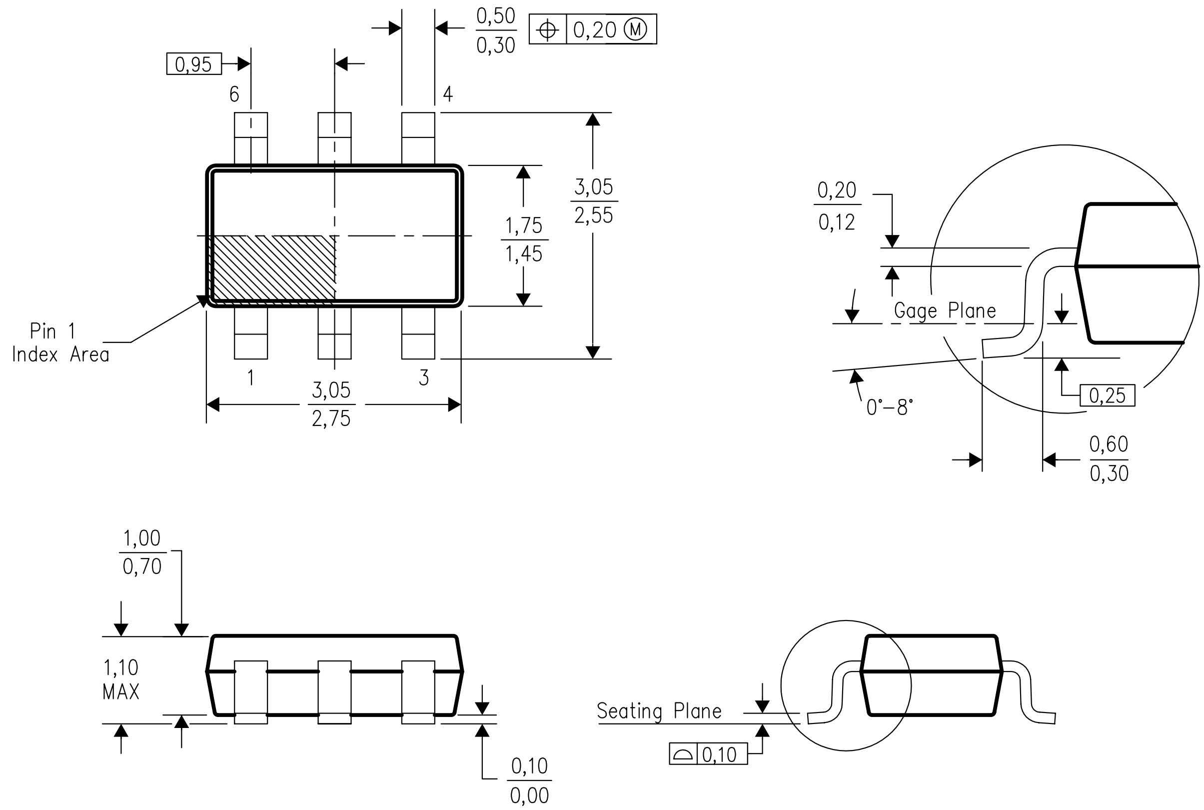
## TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS562200DDCR | SOT | DDC | 6 | 3000 | 184.0 | 184.0 | 19.0 |
| TPS562200DDCT | SOT | DDC | 6 | 250 | 184.0 | 184.0 | 19.0 |
| TPS563200DDCR | SOT | DDC | 6 | 3000 | 184.0 | 184.0 | 19.0 |
| TPS563200DDCT | SOT | DDC | 6 | 250 | 184.0 | 184.0 | 19.0 |

DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

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