LP2985-N Micropower 150-mA Low-Noise Ultra-Low-Dropout Regulator in SOT-23 and DSBGA Packages Designed for Use with Very Low ESR Output Capacitors

1 Features

- Input Voltage Range: 2.5 V to 16 V
- Ultra Low-Dropout Voltage
- Ensured 150 mA Output Current
- Smallest Possible Size (SOT-23 and DSBGA 0.5-mm Pitch Packages)
- Requires Minimum External Components
- Stable With Low-ESR Output Capacitor
- < 1 µA Quiescent Current When Shut Down
- Low Ground Pin Current at All Loads
- Output Voltage Accuracy 1% (A Grade)
- High Peak Current Capability
- Low Z_{OUT}: 0.3 Ω Typical (10 Hz to 1 MHz)
- Overtemperature and Overcurrent Protection
- −40°C to 125°C Junction Temperature Range
- Custom Voltages Available

2 Applications

- Cellular Phone
- Palmtop and Laptop Computer
- Personal Digital Assistant (PDA)
- Camcorder, Personal Stereo, Camera

3 Description

The LP2985-N low noise linear regulator delivers up to 150-mA output current and only requires 300-mV dropout voltage of input to output. Using an optimized VIP (Vertically Integrated PNP) process, the LP2985-N delivers unequaled performance for all battery-powered designs. The LP2985-N device provides 1% tolerance precision output voltage with only 75 µA quiescent current at 1 mA load and 850 µA at 150 mA load. By adding a 10-nF bypass capacitor, the output noise can be reduced to 30 μV_{RMS} in a 30-kHz bandwidth.

The LP2985-N is designed to work with a ceramic output capacitor with equivalent series resistance (ESR) as low as 5 mΩ. The devices are available with fixed output voltage from 2.5 V to 6.1 V. Contact Texas Instrument Sales for specific voltage option needs.

The smallest SOT-23 and DSBGA packages are available for absolute minimum board space.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE
LP2985-N	SOT-23 (5)	2.90 mm x 1.60 mm (NOM)
	DSBGA (5)	1.159 mm x 0.981 mm (MAX)
		1.464 mm x 1.095 mm (MAX)

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

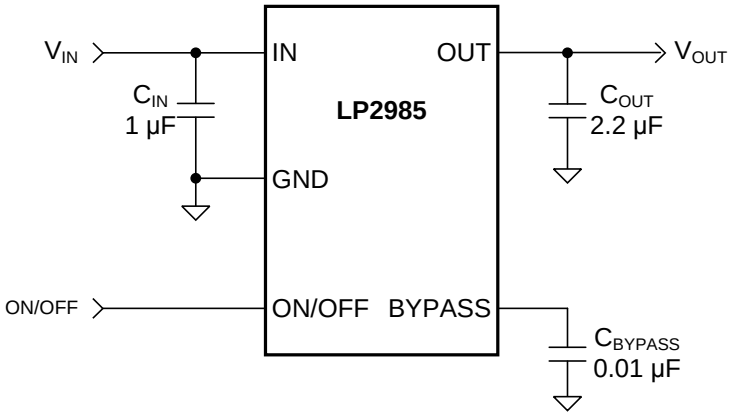


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision W (September 2014) to Revision X — **Page**

- Changed pin names in text and app circuit drawing "VOUT" and "VIN" to "OUT" and "IN"; replace *Handling Ratings* with *ESD Ratings*; update *Thermal Values* ... 1
- Changed footnote 1 to *Ab Max* table per new format ... 5
- Changed location of storage temperature range from *Handling Ratings* to *Ab Max* table ... 5
- Added required *Application Information* section ... 15

Changes from Revision V (April 2013) to Revision W — **Page**

- Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision U (April 2013) to Revision V — **Page**

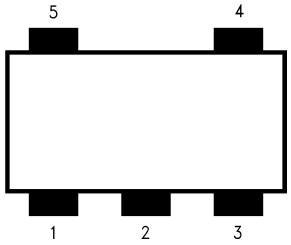
- Changed layout of National Data Sheet to TI format ... 23

5 Device Comparison Table

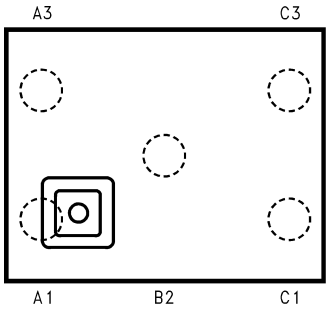
DEVICE NUMBER	PACKAGE	VOLTAGE OPTION (V)
LP2985-N	SOT-23	2.5
		2.6
		2.7
		2.8
		2.9
		3.0
		3.1
		3.2
		3.3
		3.6
		3.8
		4.0
		4.5
		5.0
		5.7
		6.1
	DSBGA (YPB)	2.5
		2.6
		2.7
		2.8
		2.9
		3.0
		3.3
		5.0
	DSBGA (YZR)	3.3

6 Pin Configuration and Functions

DBV Package
5 Pin SOT-23
Top View



YPB and YZR Packages
5-Pin DSBGA
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SOT-23	DSBGA		
IN	1	C3	I	Input voltage
GND	2	A1	—	Common ground (device substrate)
ON/OFF	3	A3	I	Logic high enable input
BYPASS	4	B2	I/O	Bypass capacitor for low noise operation
OUT	5	C1	O	Regulated output voltage

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Operating junction temperature	–40	125	°C
Lead Temp. (Soldering, 5 sec.)		260	°C
Power dissipation(3)	Internally Limited		
Input supply voltage (survival)	–0.3	16	V
Input supply voltage (operating)	2.5	16	V
Shutdown input voltage (survival)	–0.3	16	V
Output voltage (survival, See(4))	–0.3	9	V
I_{OUT} (survival)	Short Circuit Protected		
Input-output voltage (survival, see(5))	–0.3	16	V
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J_MAX}, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using:

$$P_{MAX} = \frac{T_{J\_MAX} - T_A}{R_{\theta JA}}$$

Where the value of $R_{\theta JA}$ for the SOT-23 package is 175.7°C/W in a typical PC board mounting and 180°C/W for YZR type DSBGA package or 178.8°C/W for YPB type DSBGA package.
Exceeding the maximum allowable dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.

(4) For 12V option, output voltage survival: –0.3 to +16 V. If used in a dual-supply system where the regulator load is returned to a negative supply, the LP2985-N output must be diode-clamped to ground.

(5) The output PNP structure contains a diode between the IN to OUT pins that is normally reverse-biased. Reversing the polarity from IN to OUT will turn on this diode.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except 3 and 4 (SOT-23) All pins except A3 and B2 (DSBGA)	±1000	V
			Pins 1, 2, and 5 (SOT-23) Pins A1, C1, and C3 (DSBGA)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply input voltage	3.1(1)	16	V
$V_{ON/OFF}$	ON/OFF input voltage	0	V_{IN}	V
I_{OUT}	Output current		150	mA
T_J	Operating junction temperature	–40	125	°C

(1) Recommended minimum V_{IN} is the greater of 3.1 V or V_{OUT}(max) + rated dropout voltage (max) for operating load current.

7.4 Thermal Information

THERMAL METRIC[1]		LP2985-N			UNIT
		SOT-23	DSBGA (YZR)	DSBGA (YPB)	
		5 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	175.7	180	178.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78	1	2.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	30.8	109.3	146.3	
ψ_{JT}	Junction-to-top characterization parameter	2.8	7.1	1.9	
ψ_{JB}	Junction-to-board characterization parameter	30.3	109.3	146.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Unless otherwise specified: $V_{IN} = V_O(NOM) + 1$ V, $I_L = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 4.7$ µF, $V_{ON/OFF} = 2$ V, $T_J = 25°C$.[1]

PARAMETER		TEST CONDITIONS	TYP	LP2985AI-X.X[2]		LP2985I-X.X[2]		UNIT
				MIN	MAX	MIN	MAX	
ΔV_O	Output voltage tolerance	$I_L = 1$ mA		−1	1	–1.5	1.5	$\%V_{NOM}$
		1 mA ≤ I_L ≤ 50 mA		−1.5	1.5	–2.5	2.5	
		1 mA ≤ I_L ≤ 50 mA, –40°C ≤ T_J ≤ 125°C		−2.5	2.5	–3.5	3.5	
		1 mA ≤ I_L ≤ 150 mA		−2.5	2.5	–3	3	
		1 mA ≤ I_L ≤ 150 mA, –40°C ≤ T_J ≤ 125°C		−3.5	3.5	–4	4	
$\Delta V_O/\Delta V_{IN}$	Output voltage	$V_O(NOM)+1$ V ≤ V_{IN} ≤ 16 V	0.007		0.014		0.014	%/V
	Line regulation	$V_O(NOM)+1$ V ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C			0.032		0.032	
$V_{IN}–V_O$	Dropout voltage[3]	$I_L = 0$	1		3		3	mV
		$I_L = 0$, –40°C ≤ T_J ≤ 125°C			5		5	
		$I_L = 1$ mA	7		10		10	
		$I_L = 1$ mA, –40°C ≤ T_J ≤ 125°C			15		15	
		$I_L = 10$ mA	40		60		60	
		$I_L = 10$ mA, –40°C ≤ T_J ≤ 125°C			90		90	
		$I_L = 50$ mA	120		150		150	
		$I_L = 50$ mA, –40°C ≤ T_J ≤ 125°C			225		225	
		$I_L = 150$ mA	280		350		350	
		$I_L = 150$ mA, –40°C ≤ T_J ≤ 125°C			575		575	

(1) Exposing the DSBGA device to direct sunlight will cause misoperation. See *DSBGA Light Sensitivity* for additional information.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(3) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1 V differential.

Electrical Characteristics (continued)

Unless otherwise specified: $V_{IN} = V_O(NOM) + 1$ V, $I_L = 1$ mA, $C_{IN} = 1$ µF, $C_{OUT} = 4.7$ µF, $V_{ON/OFF} = 2$ V, $T_J = 25°C$.[1]

PARAMETER		TEST CONDITIONS	TYP	LP2985AI-X.X[2]		LP2985I-X.X[2]		UNIT
				MIN	MAX	MIN	MAX	
I_{GND}	Ground pin current	$I_L = 0$	65		95		95	µA
		$I_L = 0$, –40°C ≤ T_J ≤ 125°C			125		125	
		$I_L = 1$ mA	75		110		110	
		$I_L = 1$ mA, –40°C ≤ T_J ≤ 125°C			170		170	
		$I_L = 10$ mA	120		220		220	
		$I_L = 10$ mA, –40°C ≤ T_J ≤ 125°C			400		400	
		$I_L = 50$ mA	350		600		600	
		$I_L = 50$ mA, –40°C ≤ T_J ≤ 125°C			1000		1000	
		$I_L = 150$ mA	850		1500		1500	
		$I_L = 150$ mA, –40°C ≤ T_J ≤ 125°C			2500		2500	
		$V_{ON/OFF}$ < 0.3 V	0.01		0.8		0.8	
		$V_{ON/OFF}$ < 0.15 V, –40°C ≤ T_J ≤ 125°C	0.05		2		2	
$V_{ON/OFF}$	ON/OFF input voltage[4]	High = O/P ON	1.4					V
		High = O/P ON, –40°C ≤ T_J ≤ 125°C		1.6		1.6		
		Low = O/P OFF	0.55					
		Low = O/P OFF, –40°C ≤ T_J ≤ 125°C			0.15		0.15	
$I_{ON/OFF}$	ON/OFF input current	$V_{ON/OFF} = 0$	0.01					µA
		$V_{ON/OFF} = 0$, –40°C ≤ T_J ≤ 125°C			−2		−2	
		$V_{ON/OFF} = 5$ V	5					
		$V_{ON/OFF} = 5$ V, –40°C ≤ T_J ≤ 125°C			15		15	
e_n	Output noise voltage (RMS)	BW = 300 Hz to 50 kHz,						µV
		$C_{OUT} = 10$ µF	30					
		$C_{BYPASS} = 10$ nF						
$\Delta V_O/\Delta V_{IN}$	Ripple rejection	f = 1 kHz, $C_{BYPASS} = 10$ nF	45					dB
		$C_{OUT} = 10$ µF						
$I_O(SC)$	Short circuit current	$R_L = 0$ (Steady State)[5]	400					mA
$I_O(PK)$	Peak output current	$V_{OUT} \geq V_o(NOM)$ –5%	350					mA

(4) The ON/OFF input must be properly driven to prevent possible misoperation. For details, refer to *ON/OFF Input Operation*.
(5) The LP2985-N has foldback current limiting which allows a high peak current when $V_{OUT} > 0.5$ V, and then reduces the maximum output current as V_{OUT} is forced to ground (see *Typical Characteristics* curves).

7.6 Typical Characteristics

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to V_{IN}.

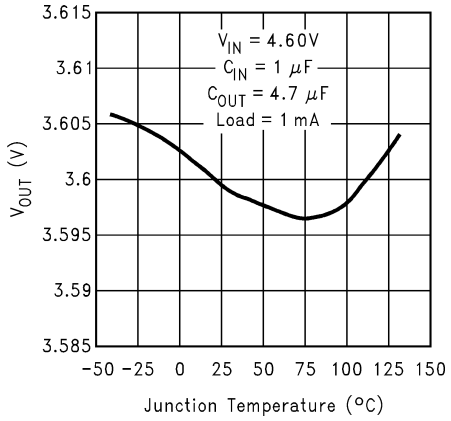


Figure 1. V_{OUT} vs Temperature

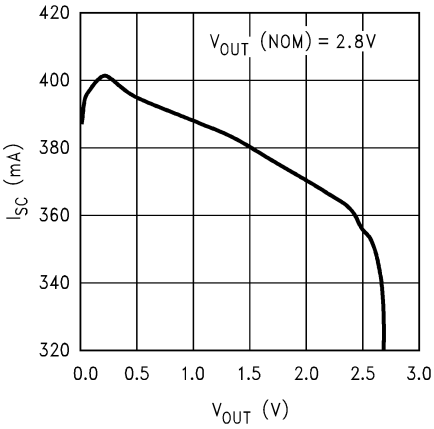


Figure 2. Short Circuit Current vs Output Voltage

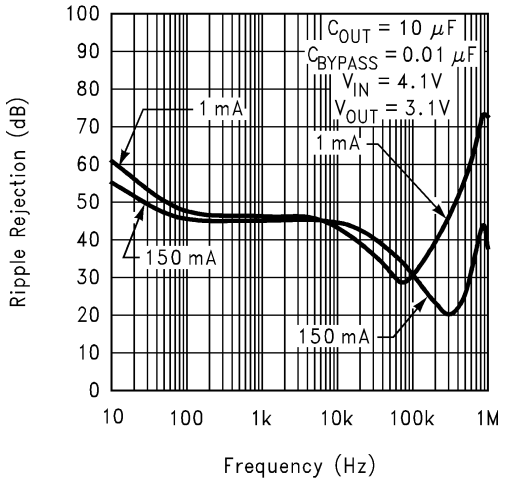


Figure 3. Ripple Rejection

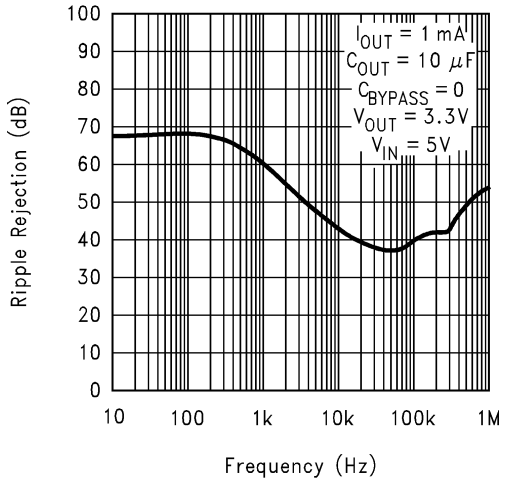


Figure 4. Ripple Rejection

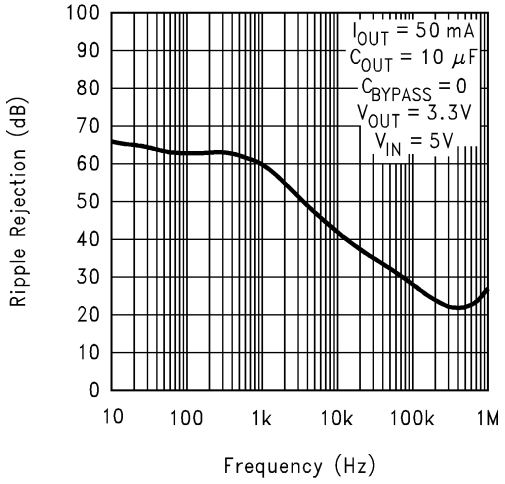


Figure 5. Ripple Rejection

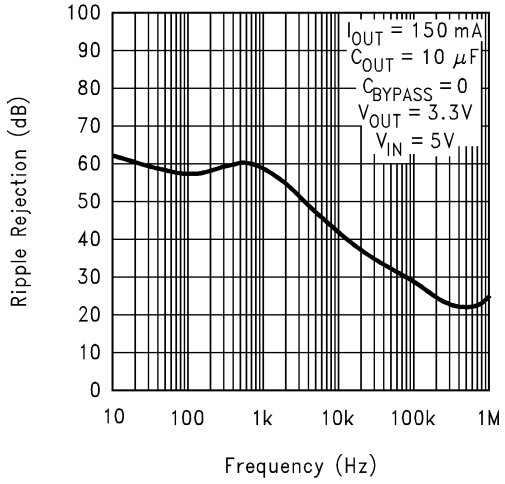


Figure 6. Ripple Rejection

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to V_{IN}.

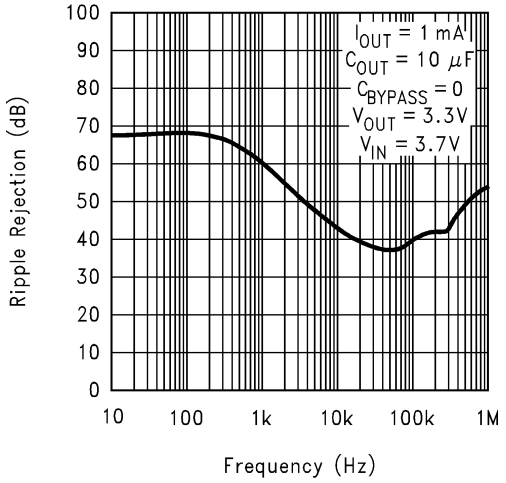


Figure 7. Ripple Rejection

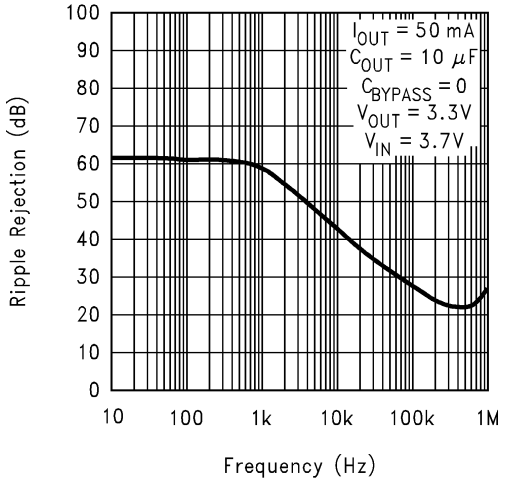


Figure 8. Ripple Rejection

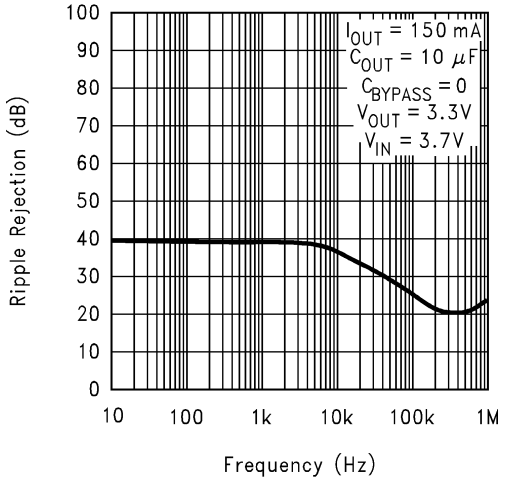


Figure 9. Ripple Rejection

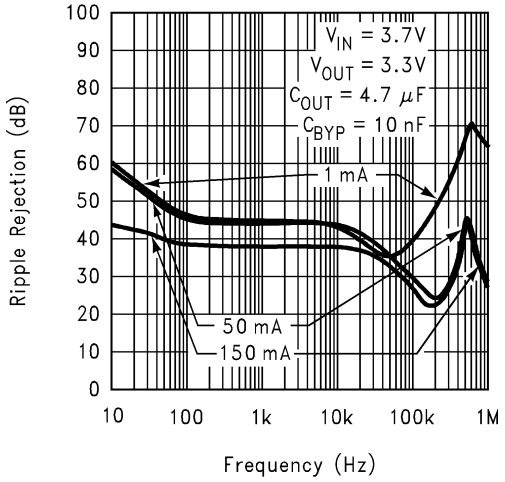


Figure 10. Ripple Rejection

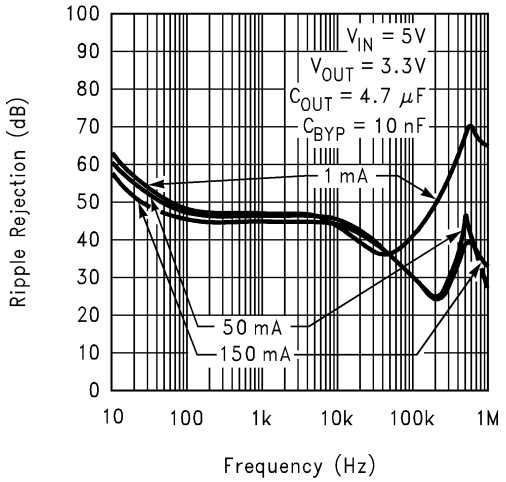


Figure 11. Ripple Rejection

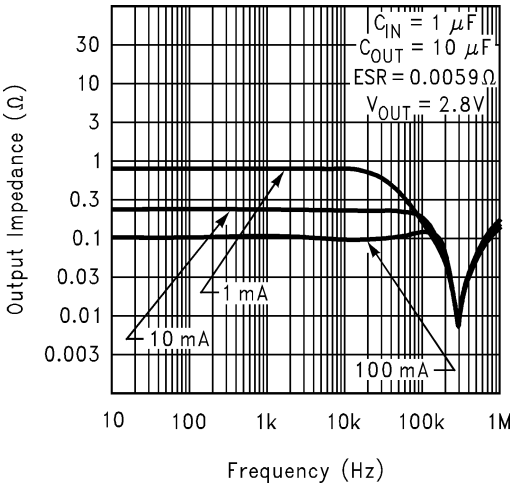


Figure 12. Output Impedance vs Frequency

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to V_{IN}.

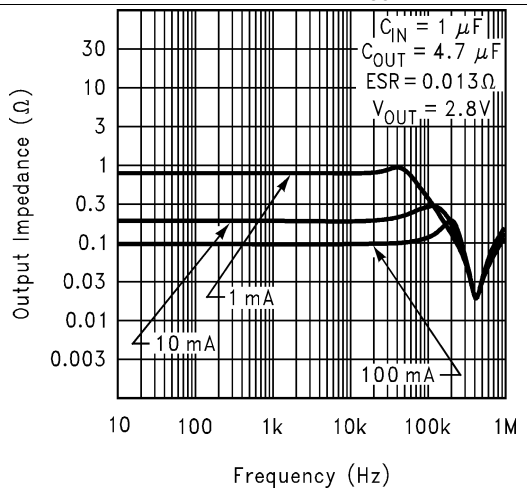


Figure 13. Output Impedance vs Frequency

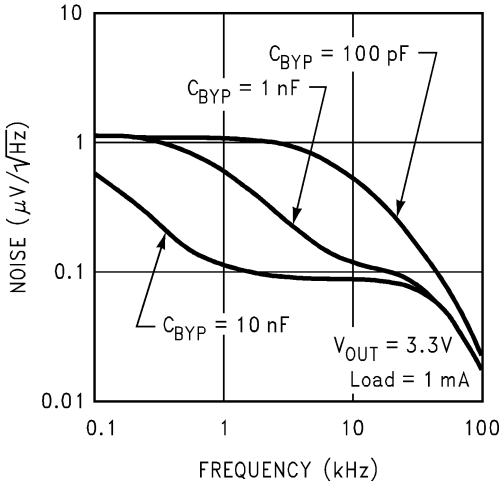


Figure 14. Output Noise Density

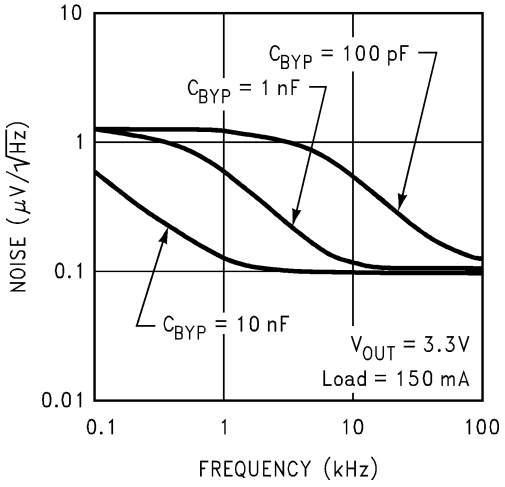


Figure 15. Output Noise Density

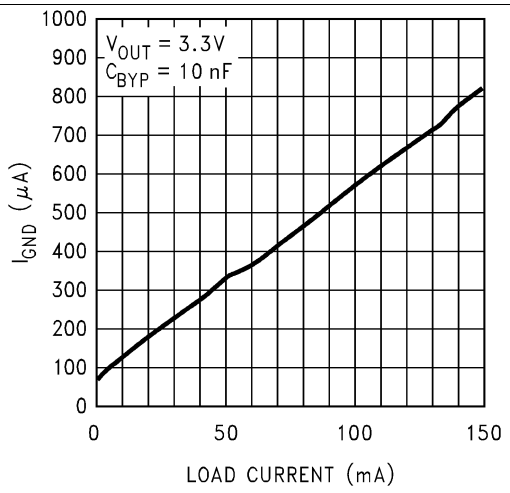


Figure 16. Ground Pin vs Load Current

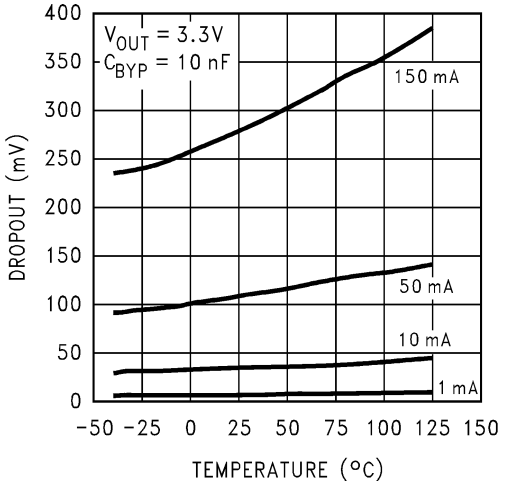


Figure 17. Dropout Voltage vs Temperature

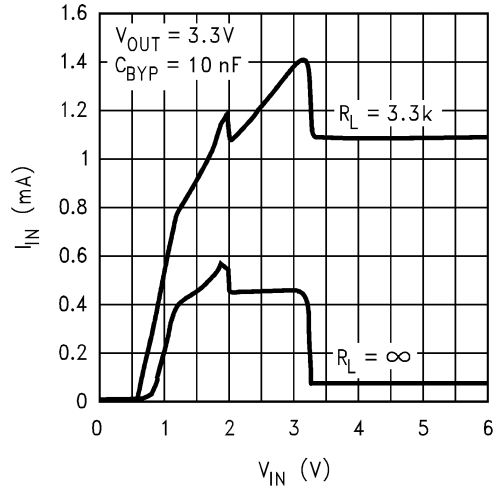


Figure 18. Input Current vs Pin

Typical Characteristics (continued)

Unless otherwise specified: C_{IN} = 1 µF, C_{OUT} = 4.7 µF, V_{IN} = $V_{OUT(NOM)}$ + 1, T_A = 25°C, ON/$\overline{OFF}$ pin is tied to V_{IN}.

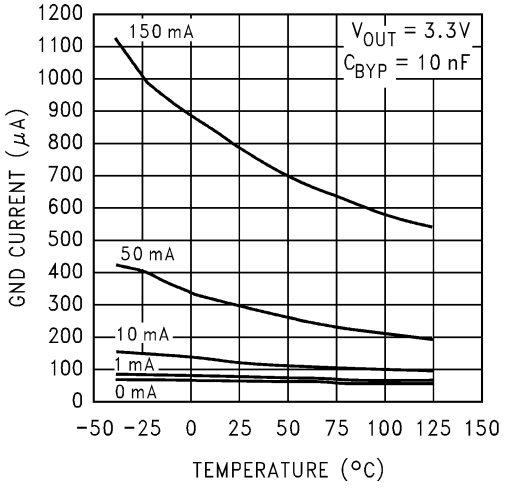


Figure 19. GND Pin Current vs Temperature

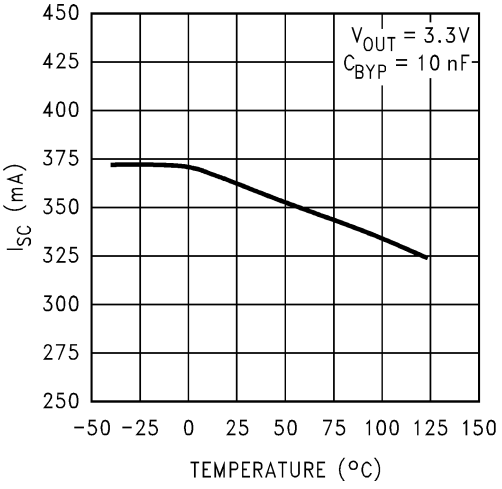


Figure 20. Instantaneous Short Circuit Current

8 Detailed Description

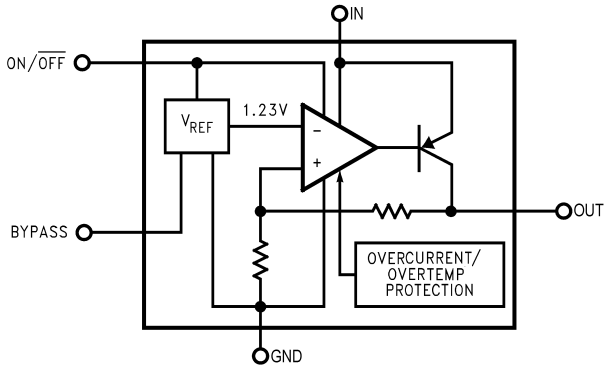
8.1 Overview

The LP2985-N family of fixed-output, ultra-low-dropout and low-noise regulators offers exceptional, cost-effective performance for battery-powered applications. Available in output voltages from 2.5 V to 5 V, the family has an output tolerance of 1% for the A version (1.5% for the non-A version) and is capable of delivering 150-mA continuous load current. Standard regulator features, such as overcurrent and overtemperature protection, are also included.

Using an optimized Vertically Integrated PNP (VIP) process, the LP2985-N contains several features to facilitate battery powered designs:

- Multiple voltage options
- Low dropout voltage, typical dropout of 300 mV at 150 mA load current and 7 mV at 1 mA load.
- Low quiescent current and low ground current, typically 850-µA at 150 mA load, and 75-µA at 1-mA load.
- A shutdown feature is available, allowing the regulator to consume only 0.01-uA typically when the ON/$\overline{\text{OFF}}$ pin is pulled low.
- Over Temperature Protection and Over Current Protection circuitry is designed to safeguard the device during unexpected conditions
- Enhanced Stability: The LP2985-N is stable with output capacitor ESR as low as 5-mΩ, which allows the use of ceramic capacitors on the output.
- Low noise: A BYPASS pin allows for low-noise operation, with a typical output noise of 30 μV_{RMS}, with the use of a 10-nF bypass capacitor.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Multiple Voltage Options

In order to meet different application's requirement, the LP2985-N family provide multiple fixed output options from 2.5 V to 6.1 V. Please consult factory for custom voltages.

8.3.2 Output Voltage Accuracy

Output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent. This accuracy error includes the errors introduced by the internal reference and the load and line regulation across the full range of rated load and line operating conditions over temperature, unless otherwise specified by the *Electrical Characteristics*. Output voltage accuracy also accounts for all variations between manufacturing lots.

Feature Description (continued)

8.3.3 Ultra-Low Dropout Voltage

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage ($V_{DO} = V_{IN} – V_{OUT}$), where the main current pass-FET is fully on in the ohmic region of operation and is characterized by the classic $R_{DS(ON)}$ of the FET. V_{DO} indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary. If the input falls below this V_{DO} limit ($V_{IN} < V_{OUT} + V_{DO}$), then the output voltage decreases in order to follow the input voltage.

8.3.4 Low Ground Current

LP2985-N uses a vertical PNP process which allows for quiescent currents that are considerably lower than those associated with traditional lateral PNP regulators, typically 850 µA at150 mA load, and 75 µA at 1-mA load.

8.3.5 Sleep Mode

When pull ON/OFF pin to low level, LP2985-N will enter sleep mode, and less than 2-µA quiescent current is consumed. This function is designed for the application which needs a sleep mode to effectively enhance battery life cycle.

8.3.6 Internal Protection Circuitry

8.3.6.1 Short Circuit Protection (Current Limit)

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output.

A fold back feature limits the short-circuit current to protect the regulator from damage under all load conditions. If V_{OUT} is forced below 0 V before EN goes high and the load current required exceeds the fold back current limit, the device may not start up correctly.

8.3.6.2 Thermal Protection

The LP2985-N contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. The thermal time-constant of the semiconductor die is fairly short, and thus the output cycles on and off at a high rate when thermal shutdown is reached until the power dissipation is reduced.

The internal protection circuitry of the LP2985-N is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades its reliability.

8.3.7 Enhanced Stability

The LP2985-N is designed specifically to work with ceramic output capacitors, utilizing circuitry which allows the regulator to be stable across the entire range of output current with an output capacitor whose ESR is as low as 5 mΩ. For output capacitor requirement, please refer to *Output Capacitor*.

8.3.8 Low Noise

The LP2985-N includes a low-noise reference ensuring minimal noise during operation because the internal reference is normally the dominant term in noise analysis. Further noise reduction can be achieved by adding an external bypass bapacitor between the BYPASS pin and the GND pin.

8.4 Device Functional Modes

8.4.1 Operation with $V_{OUT(TARGET)} + 0.6\ V \geq V_{IN} > 16\ V$

The device operate if the input voltage is equal to, or exceeds $V_{OUT(TARGET)}$ + 0.6 V. At input voltages below the minimum V_{IN} requirement, the devices do not operate correctly and output voltage may not reach target value.

Device Functional Modes (continued)

8.4.2 Operation With ON/$\overline{\text{OFF}}$ Control

If the voltage on the ON/$\overline{\text{OFF}}$ pin is less than 0.15 V, the device is disabled, and in this state shutdown current does not exceed 2 µA. Raising ON/$\overline{\text{OFF}}$ above 1.6 V initiates the start-up sequence of the device.

9 Application and Implementation

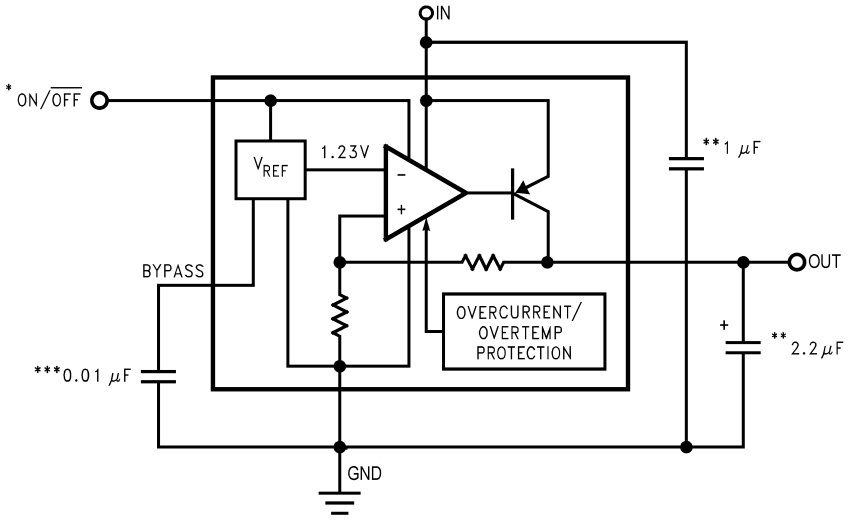
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LP2985-N is a linear voltage regulator operating from 2.5 V to 16 V on the input and regulates voltages between 2.5 V to 6.1 V with 1% accuracy and 150-mA maximum output current. Efficiency is defined by the ratio of output voltage to input voltage because the LP2985-N is a linear voltage regulator. To achieve high efficiency, the dropout voltage (V_{IN} – V_{OUT}) must be as small as possible, thus requiring a very-low-dropout LDO. Successfully implementing an LDO in an application depends on the application requirements. If the requirements are simply input voltage and output voltage, compliance specifications (such as internal power dissipation or stability) must be verified to ensure a solid design. If timing, start-up, noise, power supply rejection ratio (PSRR), or any other transient specification is required, then the design becomes more challenging.

9.2 Typical Application



*ON/$\overline{OFF}$ input must be actively terminated. Tie to V_{IN} if this function is not to be used.
**Minimum capacitance is shown to ensure stability (may be increased without limit). Ceramic capacitor required for output (see *Output Capacitor*).
***Reduces output noise (may be omitted if application is not noise critical). Use ceramic or film type with very low leakage current (see *Noise Bypass Capacitor*).

Figure 21. Typical Application Schematic

9.2.1 Design Requirements

DESIGN PARAMETERS	VALUE
Input voltage	4.3 V, ±10% provided by the DC-DC converter switching at 1 MHz
Output voltage	3.3 V, ±5%
Output current	150 mA (maximum), 1 mA (minimum)
RMS noise, 300 Hz to 50 kHz	< 50 μV_{RMS}
PSRR at 1 kHz	> 40 dB

9.2.2 Detailed Design Procedure

At 150-mA loading, the dropout of the LP2985-N has 575-mV maximum dropout over temperature, thus an 1000-mV headroom is sufficient for operation over both input and output voltage accuracy. The efficiency of the LP2985-N in this configuration is V_{OUT} / V_{IN} = 76.7%. To achieve the smallest form factor, the SOT-23 package is selected.

Input and output capacitors are selected in accordance with the *Capacitor Characteristics* section. Ceramic capacitances of 1 µF for the input and one 2.2-µF capacitor for the output are selected. With an efficiency of 76.7% and a 150 mA maximum load, the internal power dissipation is 150-mW, which corresponds to a 26°C junction temperature rise for the SOT-23 package. With an 85°C maximum ambient temperature, the junction temperature is at 111°C. To minimize noise, a bypass capacitance (C_{BYPASS}) of 0.01 µF is selected.

9.2.2.1 External Capacitors

Like any low-dropout regulator, the LP2985-N requires external capacitors for regulator stability. These capacitors must be correctly selected for good performance.

9.2.2.1.1 Input Capacitor

An input capacitor whose capacitance is ≥ 1 µF is required between the LP2985-N input and ground (the amount of capacitance may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

NOTE

Tantalum capacitors can suffer catastrophic failure due to surge current when connected to a low-impedance source of power (like a battery or very large capacitor). If a Tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will be ≥ 1 µF over the entire operating temperature range.

9.2.2.1.2 Output Capacitor

The LP2985-N is designed specifically to work with ceramic output capacitors, utilizing circuitry which allows the regulator to be stable across the entire range of output current with an output capacitor whose ESR is as low as 5 mΩ. It may also be possible to use Tantalum or film capacitors at the output, but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

The output capacitor must meet the requirement for minimum amount of capacitance and also have an ESR value which is within the stable range. Curves are provided which show the stable ESR range as a function of load current (see Figure 22).

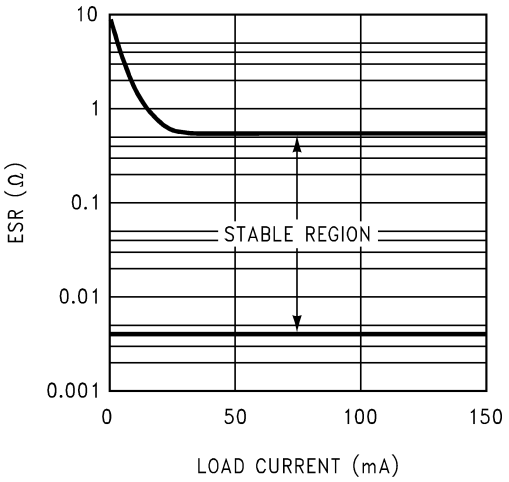


Figure 22. ESR Graph

NOTE

The output capacitor must maintain its ESR within the stable region over the full operating temperature range of the application to assure stability.

The LP2985-N requires a minimum of 2.2 µF on the output (output capacitor size can be increased without limit).

It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. It should be noted that ceramic capacitors can exhibit large changes in capacitance with temperature (see *Capacitor Characteristics*). The output capacitor must be located not more than 1 cm from the output pin and returned to a clean analog ground.

9.2.2.1.3 Noise Bypass Capacitor

Connecting a 10 nF capacitor to the BYPASS pin significantly reduces noise on the regulator output. It should be noted that the capacitor is connected directly to a high-impedance circuit in the bandgap reference.

Because this circuit has only a few microamperes flowing in it, any significant loading on this node will cause a change in the regulated output voltage. For this reason, DC leakage current through the noise bypass capacitor must never exceed 100 nA, and should be kept as low as possible for best output voltage accuracy.

The types of capacitors best suited for the noise bypass capacitor are ceramic and film. High-quality ceramic capacitors with either NPO or COG dielectric typically have very low leakage. 10 nF polypropolene and polycarbonate film capacitors are available in small surface-mount packages and typically have extremely low leakage current.

9.2.2.2 Capacitor Characteristics

The LP2985-N was designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the 2.2 µF to 4.7 µF range, ceramics are the least expensive and also have the lowest ESR values (which makes them best for eliminating high-frequency noise). The ESR of a typical 2.2 µF ceramic capacitor is in the range of 10 mΩ to 20 mΩ, which easily meets the ESR limits required for stability by the LP2985-N.

One disadvantage of ceramic capacitors is that their capacitance can vary with temperature. Most large value ceramic capacitors (≥ 2.2 µF) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

This could cause problems if a 2.2 µF capacitor were used on the output since it will drop down to approximately 1 µF at high ambient temperatures (which could cause the LM2985 to oscillate). If Z5U or Y5V capacitors are used on the output, a minimum capacitance value of 4.7 µF must be observed.

A better choice for temperature coefficient in ceramic capacitors is X7R, which holds the capacitance within ±15%. Unfortunately, the larger values of capacitance are not offered by all manufacturers in the X7R dielectric.

Tantalum capacitors are less desirable than ceramics for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1 µF to 4.7 µF range.

Another important consideration is that Tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a Tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value.

It should also be noted that the ESR of a typical Tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

9.2.2.3 ON/$\overline{\text{OFF}}$ Input Operation

The LP2985-N is shut off by driving the ON/OFF input low, and turned on by pulling it high. If this feature is not to be used, the ON/$\overline{\text{OFF}}$ input should be tied to V_{IN} to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the ON/$\overline{\text{OFF}}$ input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed in the *Electrical Characteristics* section under $V_{ON/OFF}$. To prevent mis-operation, the turn-on (and turn-off) voltage signals applied to the ON/OFF input must have a slew rate which is ≥ 40 mV/µs.

CAUTION

The regulator output voltage cannot be ensured if a slow-moving AC (or DC) signal is applied that is in the range between the specified turn-on and turn-off voltages listed under the electrical specification $V_{ON/OFF}$ (see *Electrical Characteristics*).

9.2.2.4 Reverse Input-Output Voltage

The PNP power transistor used as the pass element in the LP2985-N has an inherent diode connected between the regulator output and input. During normal operation (where the input voltage is higher than the output) this diode is reverse-biased).

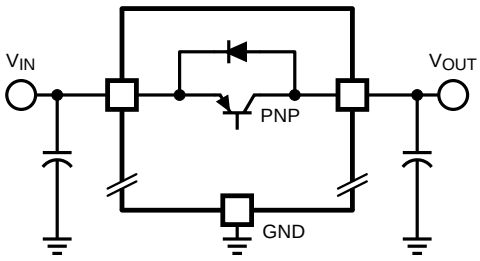


Figure 23. Reverse Current Path

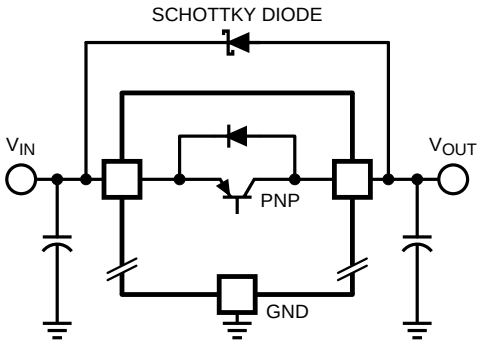


Figure 24. Reverse Current Protection

However, if the output is pulled above the input, this diode will turn ON and current will flow into the regulator output. In such cases, a parasitic SCR can latch which will allow a high current to flow into V_{IN} (and out the ground pin), which can damage the part.

In any application where the output may be pulled above the input, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN}, anode on V_{OUT}), to limit the reverse voltage across the LP2985-N to 0.3 V (see *Absolute Maximum Ratings*).

9.2.3 Application Curves

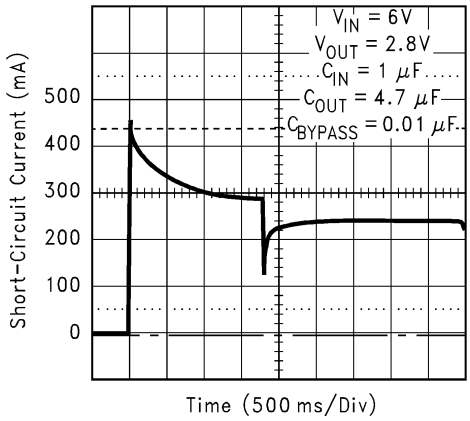


Figure 25. Short-Circuit Current

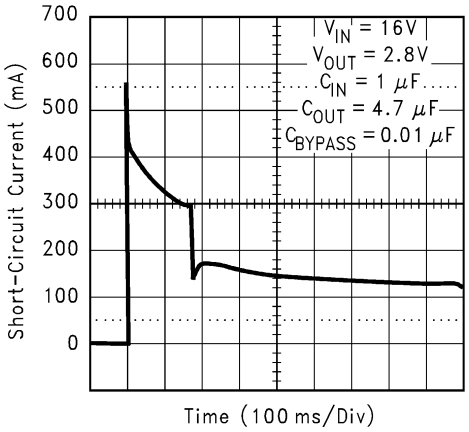


Figure 26. Short-Circuit Current

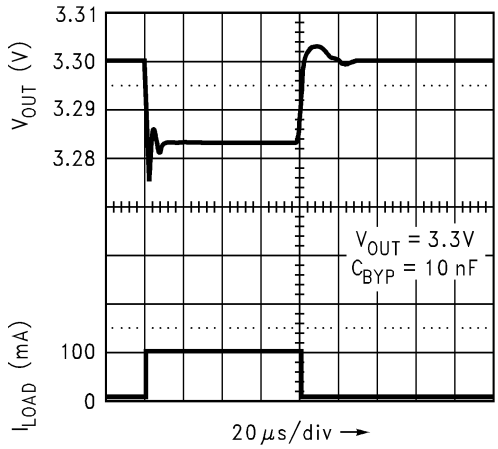


Figure 27. Load Transient Response

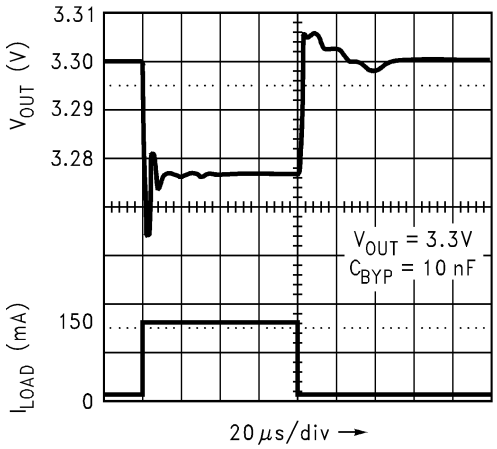


Figure 28. Load Transient Response

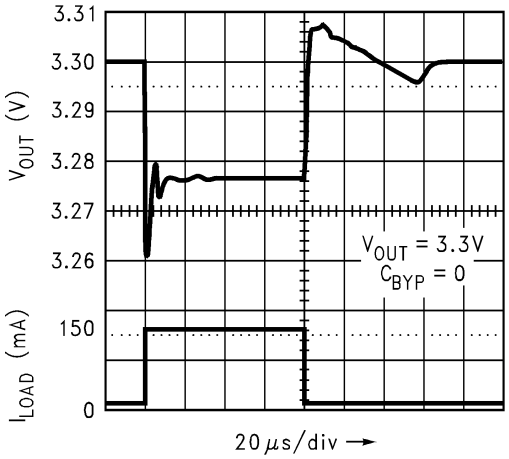


Figure 29. Load Transient Response

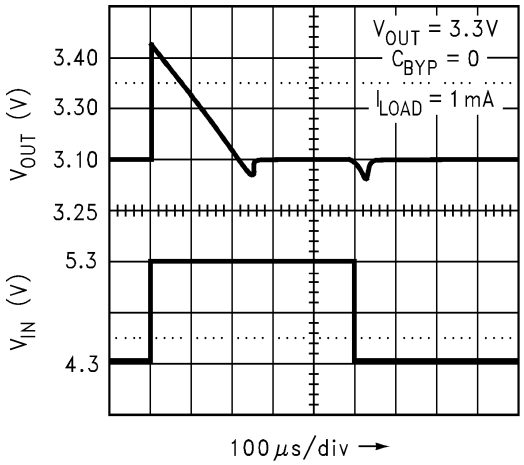


Figure 30. Line Transient Response

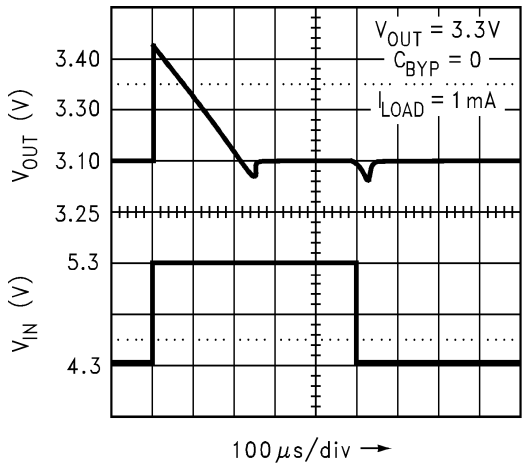


Figure 31. Line Transient Response

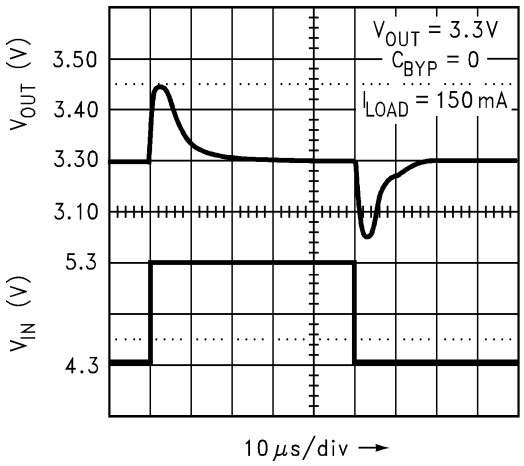


Figure 32. Line Transient Response

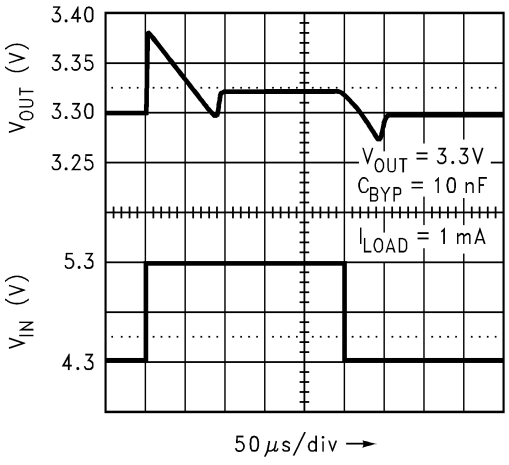


Figure 33. Line Transient Response

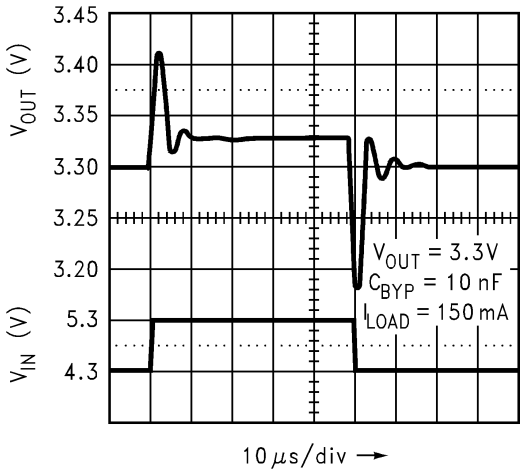


Figure 34. Line Transient Response

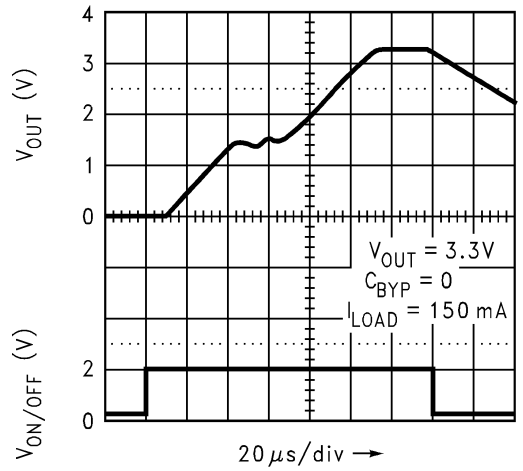


Figure 35. Turn-On Time

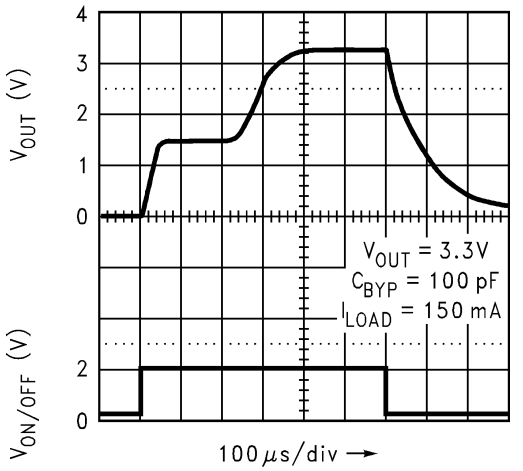


Figure 36. Turn-On Time

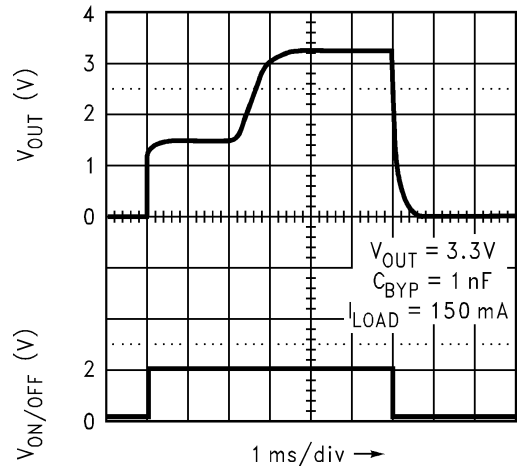


Figure 37. Turn-On Time

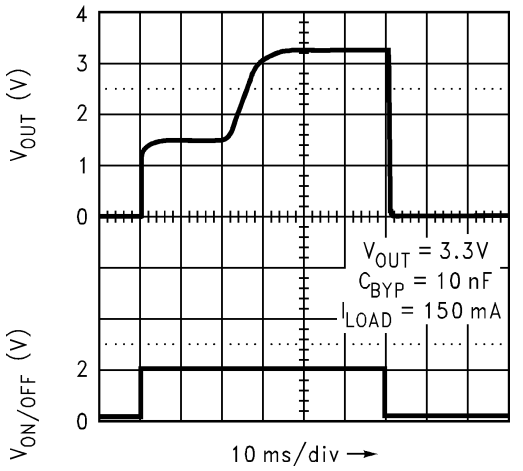


Figure 38. Turn-On Time

10 Power Supply Recommendations

The LP2985-N is designed to operate from an input voltage supply range between V_{IN} of 2.5 V and 16 V. (Recommended minimum V_{IN} is the greater of 3.1 V or $V_{OUT(max)}$ + rated dropout voltage (max) for operating load current.) The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help to improve the output noise performance.

11 Layout

11.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

11.2 Layout Example

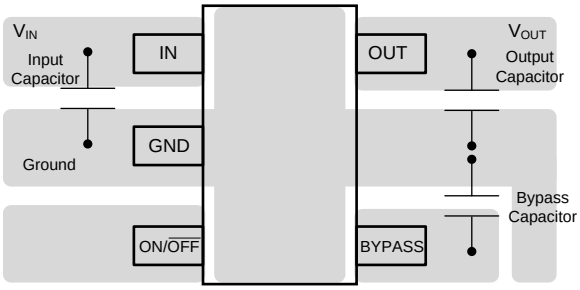


Figure 39. LP2985 SOT-23 Package Typical Layout

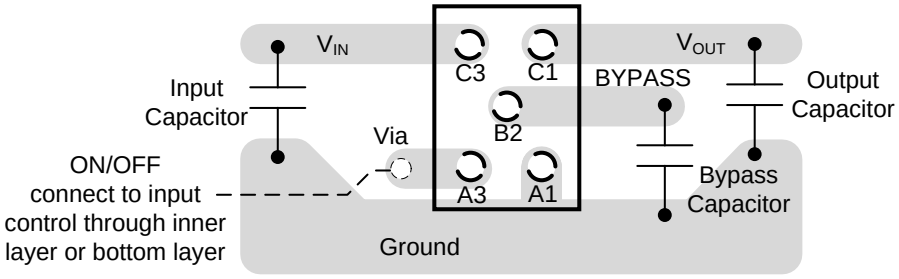


Figure 40. LP2985 DSBGA Package Typical Layout

11.3 DSBGA Mounting

The DSBGA package requires specific mounting techniques which are detailed in *AN-1112 DSBGA Wafer Level Chip Scale Package* (SNVA009). Referring to the section *Surface Mount Technology (SMT) Assembly Considerations*, it should be noted that the pad style which must be used with the 5-pin package is the NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

11.4 DSBGA Light Sensitivity

Exposing the DSBGA device to direct sunlight will cause misoperation of the device. Light sources such as Halogen lamps can also affect electrical performance if brought near to the device.

The wavelengths which have the most detrimental effect are reds and infra-reds, which means that the fluorescent lighting used inside most buildings has very little effect on performance. A DSBGA test board was brought to within 1 cm of a fluorescent desk lamp and the effect on the regulated output voltage was negligible, showing a deviation of less than 0.1% from nominal.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

AN-1112 DSBGA Wafer Level Chip Scale Package (SNVA009)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

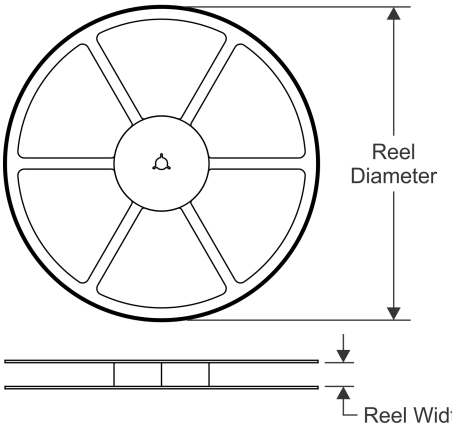
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

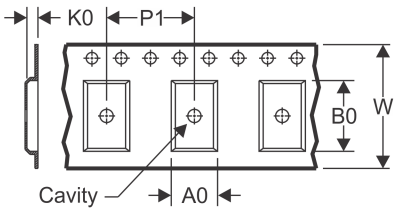
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

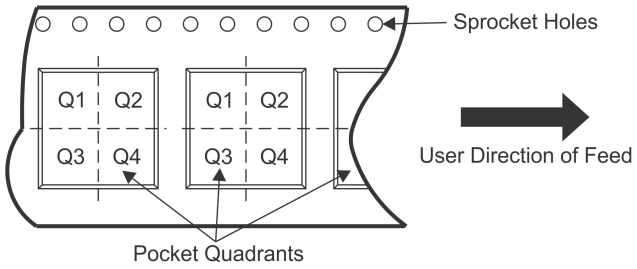


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

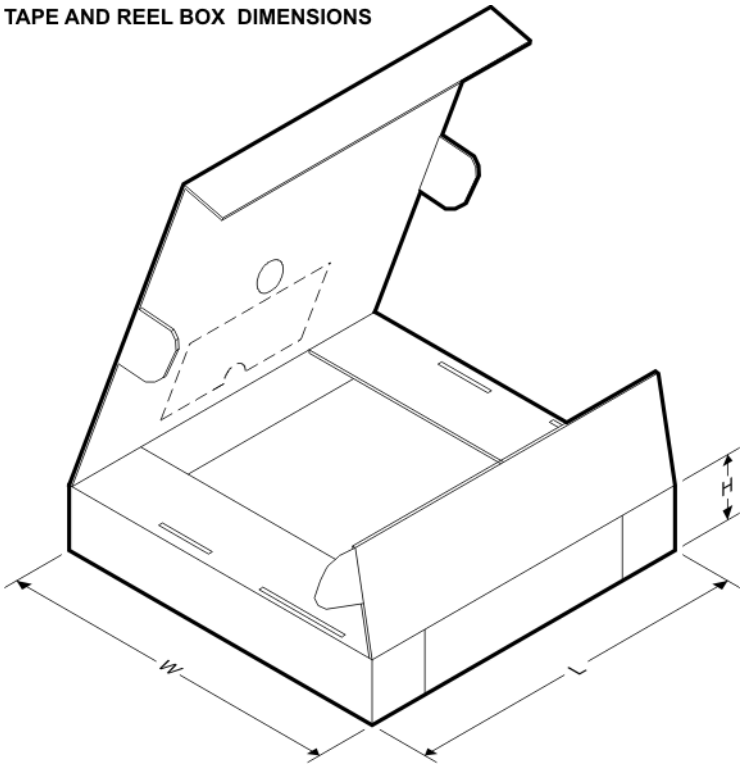
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2985AIM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-2.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-2.8	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-2.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-2.9/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.6	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.6/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-4.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-4.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-5.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-5.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2985AIM5-6.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-2.5	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-2.6/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-2.7/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-2.9/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.3	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.6/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-4.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-4.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-5.0	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-5.7/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-6.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AITL-3.3/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LP2985AITLX-3.3/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LP2985AITP-2.6/NOPB	DSBGA	YPB	5	250	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985AITP-2.7/NOPB	DSBGA	YPB	5	250	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985AITP-2.8/NOPB	DSBGA	YPB	5	250	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985AITP-2.9/NOPB	DSBGA	YPB	5	250	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985AITP-3.0/NOPB	DSBGA	YPB	5	250	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985AITP-3.3/NOPB	DSBGA	YPB	5	250	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985AITP-5.0/NOPB	DSBGA	YPB	5	250	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985AITPX-2.5/NOPB	DSBGA	YPB	5	3000	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985AITPX-2.6/NOPB	DSBGA	YPB	5	3000	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985AITPX-2.7/NOPB	DSBGA	YPB	5	3000	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985AITPX-2.8/NOPB	DSBGA	YPB	5	3000	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985AITPX-2.9/NOPB	DSBGA	YPB	5	3000	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985AITPX-3.0/NOPB	DSBGA	YPB	5	3000	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985AITPX-3.3/NOPB	DSBGA	YPB	5	3000	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985AITPX-5.0/NOPB	DSBGA	YPB	5	3000	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985IM5-2.5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.9/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2985IM5-3.2/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.6	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.6/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.8	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-4.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
LP2985IM5-4.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-5.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-5.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
LP2985IM5-5.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-6.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-2.7/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-2.9/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-3.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-3.6/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-3.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-4.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-4.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-5.0	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-5.7/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-6.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985ITL-3.3/NOPB	DSBGA	YZR	5	250	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LP2985ITLX-3.3/NOPB	DSBGA	YZR	5	3000	178.0	8.4	1.14	1.47	0.76	4.0	8.0	Q1
LP2985ITP-2.5/NOPB	DSBGA	YPB	5	250	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985ITP-2.6/NOPB	DSBGA	YPB	5	250	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985ITP-2.7/NOPB	DSBGA	YPB	5	250	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985ITP-2.8/NOPB	DSBGA	YPB	5	250	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985ITP-2.9/NOPB	DSBGA	YPB	5	250	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985ITP-3.0/NOPB	DSBGA	YPB	5	250	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985ITP-3.3/NOPB	DSBGA	YPB	5	250	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985ITP-5.0/NOPB	DSBGA	YPB	5	250	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985ITPX-2.6/NOPB	DSBGA	YPB	5	3000	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985ITPX-2.7/NOPB	DSBGA	YPB	5	3000	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985ITPX-2.8/NOPB	DSBGA	YPB	5	3000	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985ITPX-2.9/NOPB	DSBGA	YPB	5	3000	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985ITPX-3.0/NOPB	DSBGA	YPB	5	3000	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2985ITPX-3.3/NOPB	DSBGA	YPB	5	3000	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1
LP2985ITPX-5.0/NOPB	DSBGA	YPB	5	3000	178.0	8.4	1.02	1.19	0.66	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

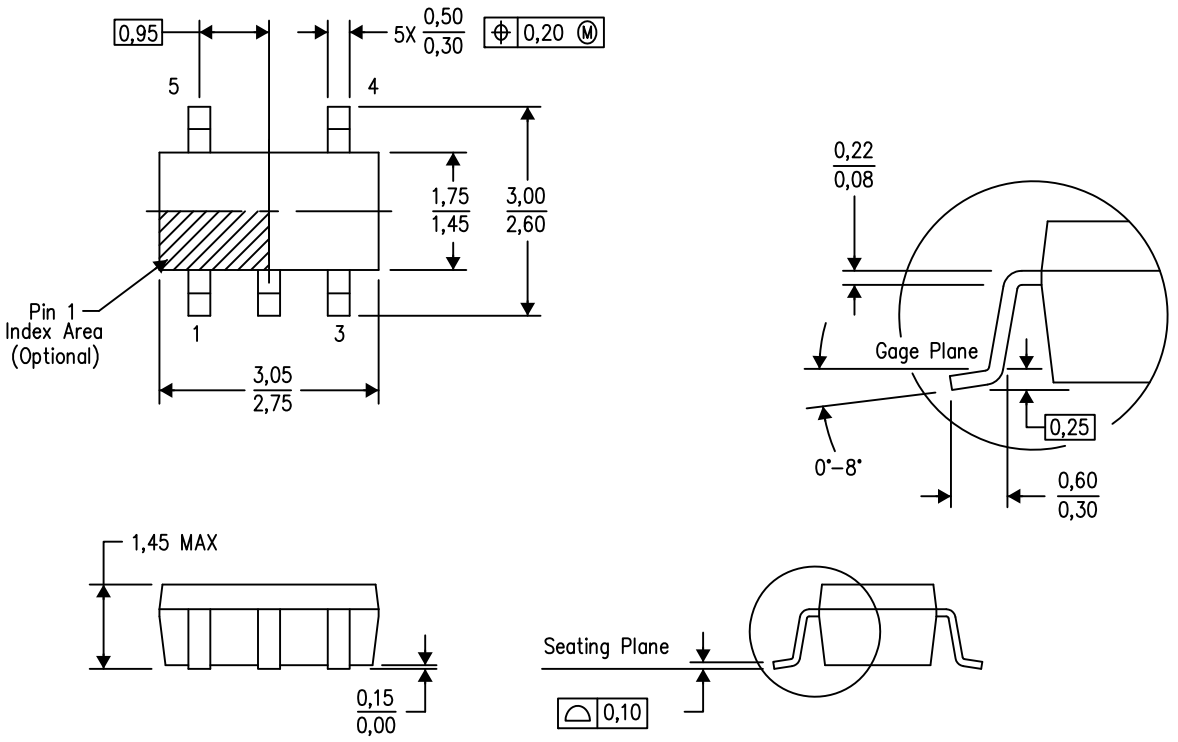
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2985AIM5-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-2.7/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-2.8	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-2.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-2.9/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-3.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-3.1/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-3.6	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-3.6/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-3.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-4.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-4.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2985AIM5-5.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-5.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-5.7/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5-6.1/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985AIM5X-2.5	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-2.6/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-2.7/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-2.9/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.1/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.3	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.6/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-4.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-4.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-5.0	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-5.7/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-6.1/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AITL-3.3/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP2985AITLX-3.3/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP2985AITP-2.6/NOPB	DSBGA	YPB	5	250	210.0	185.0	35.0
LP2985AITP-2.7/NOPB	DSBGA	YPB	5	250	210.0	185.0	35.0
LP2985AITP-2.8/NOPB	DSBGA	YPB	5	250	210.0	185.0	35.0
LP2985AITP-2.9/NOPB	DSBGA	YPB	5	250	210.0	185.0	35.0
LP2985AITP-3.0/NOPB	DSBGA	YPB	5	250	210.0	185.0	35.0
LP2985AITP-3.3/NOPB	DSBGA	YPB	5	250	210.0	185.0	35.0
LP2985AITP-5.0/NOPB	DSBGA	YPB	5	250	210.0	185.0	35.0
LP2985AITPX-2.5/NOPB	DSBGA	YPB	5	3000	210.0	185.0	35.0
LP2985AITPX-2.6/NOPB	DSBGA	YPB	5	3000	210.0	185.0	35.0
LP2985AITPX-2.7/NOPB	DSBGA	YPB	5	3000	210.0	185.0	35.0
LP2985AITPX-2.8/NOPB	DSBGA	YPB	5	3000	210.0	185.0	35.0
LP2985AITPX-2.9/NOPB	DSBGA	YPB	5	3000	210.0	185.0	35.0
LP2985AITPX-3.0/NOPB	DSBGA	YPB	5	3000	210.0	185.0	35.0
LP2985AITPX-3.3/NOPB	DSBGA	YPB	5	3000	210.0	185.0	35.0
LP2985AITPX-5.0/NOPB	DSBGA	YPB	5	3000	210.0	185.0	35.0
LP2985IM5-2.5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-2.7/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-2.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-2.9/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2985IM5-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.1/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.2/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.3/NOPB	SOT-23	DBV	5	1000	223.0	191.0	35.0
LP2985IM5-3.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.6	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.6/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.8	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-3.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-4.0/NOPB	SOT-23	DBV	5	1000	223.0	191.0	35.0
LP2985IM5-4.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-5.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-5.0/NOPB	SOT-23	DBV	5	1000	223.0	191.0	35.0
LP2985IM5-5.7/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5-6.1/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP2985IM5X-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-2.7/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-2.9/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-3.1/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-3.6/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-3.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-4.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-4.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-5.0	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-5.0/NOPB	SOT-23	DBV	5	3000	223.0	191.0	35.0
LP2985IM5X-5.7/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-6.1/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985ITL-3.3/NOPB	DSBGA	YZR	5	250	210.0	185.0	35.0
LP2985ITLX-3.3/NOPB	DSBGA	YZR	5	3000	210.0	185.0	35.0
LP2985ITP-2.5/NOPB	DSBGA	YPB	5	250	210.0	185.0	35.0
LP2985ITP-2.6/NOPB	DSBGA	YPB	5	250	210.0	185.0	35.0
LP2985ITP-2.7/NOPB	DSBGA	YPB	5	250	210.0	185.0	35.0
LP2985ITP-2.8/NOPB	DSBGA	YPB	5	250	210.0	185.0	35.0
LP2985ITP-2.9/NOPB	DSBGA	YPB	5	250	210.0	185.0	35.0
LP2985ITP-3.0/NOPB	DSBGA	YPB	5	250	210.0	185.0	35.0
LP2985ITP-3.3/NOPB	DSBGA	YPB	5	250	210.0	185.0	35.0
LP2985ITP-5.0/NOPB	DSBGA	YPB	5	250	210.0	185.0	35.0
LP2985ITPX-2.6/NOPB	DSBGA	YPB	5	3000	210.0	185.0	35.0
LP2985ITPX-2.7/NOPB	DSBGA	YPB	5	3000	210.0	185.0	35.0
LP2985ITPX-2.8/NOPB	DSBGA	YPB	5	3000	210.0	185.0	35.0
LP2985ITPX-2.9/NOPB	DSBGA	YPB	5	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2985ITPX-3.0/NOPB	DSBGA	YPB	5	3000	210.0	185.0	35.0
LP2985ITPX-3.3/NOPB	DSBGA	YPB	5	3000	210.0	185.0	35.0
LP2985ITPX-5.0/NOPB	DSBGA	YPB	5	3000	210.0	185.0	35.0

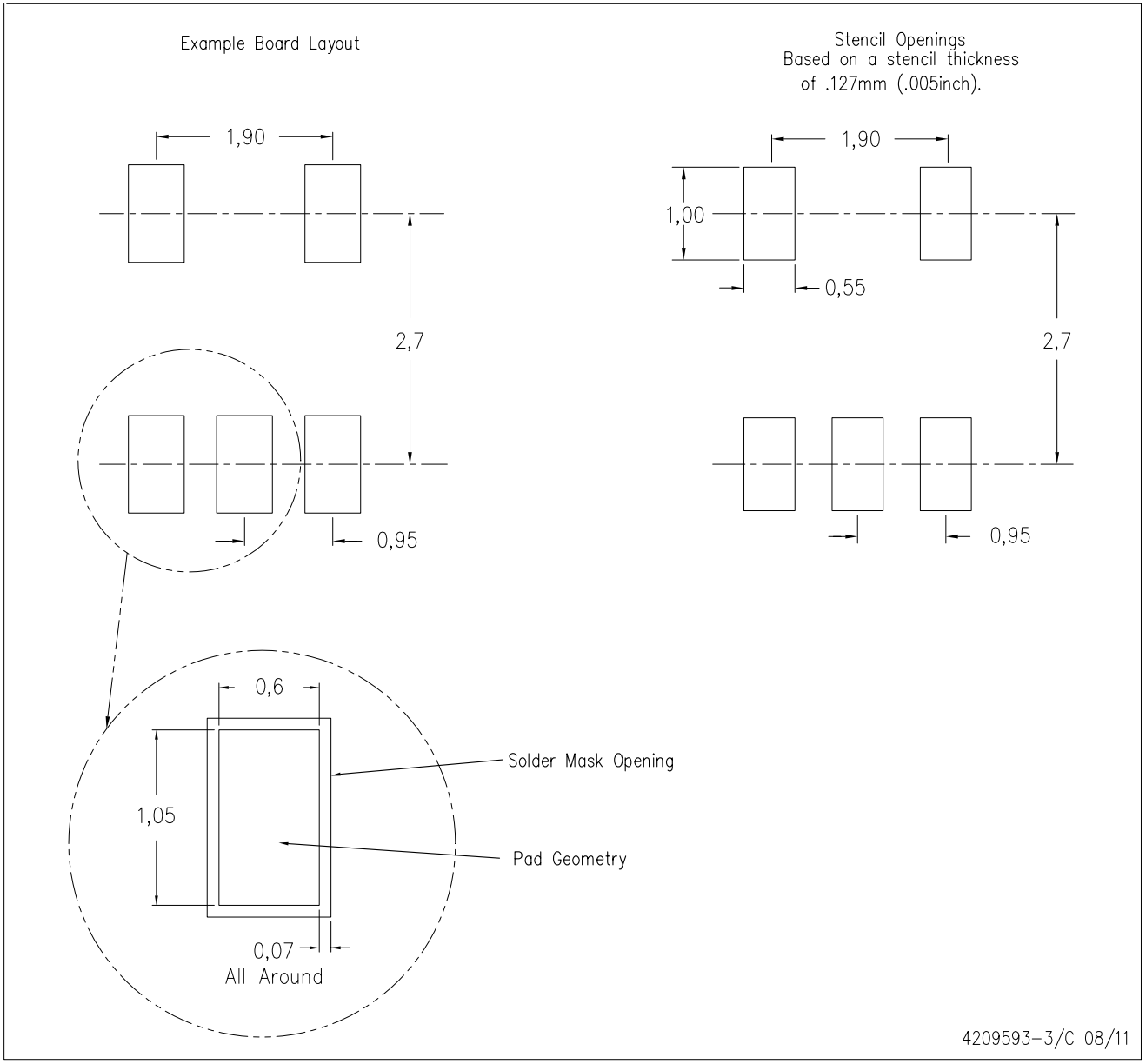
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

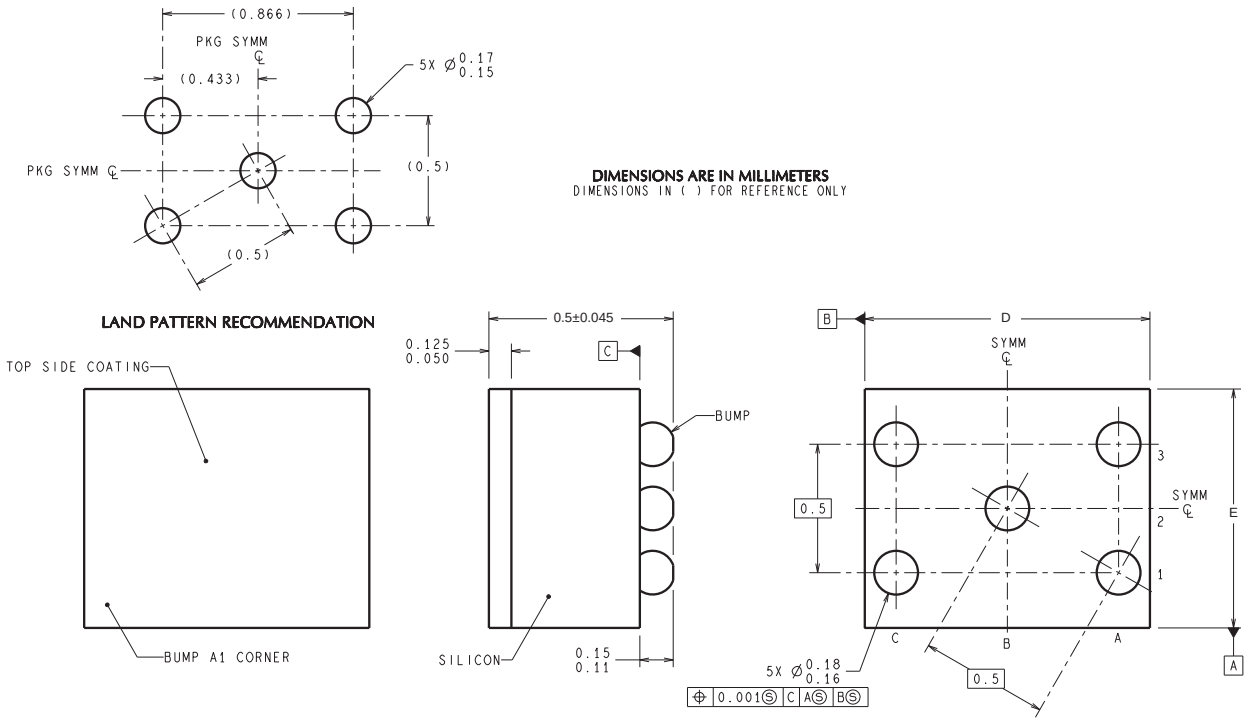
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

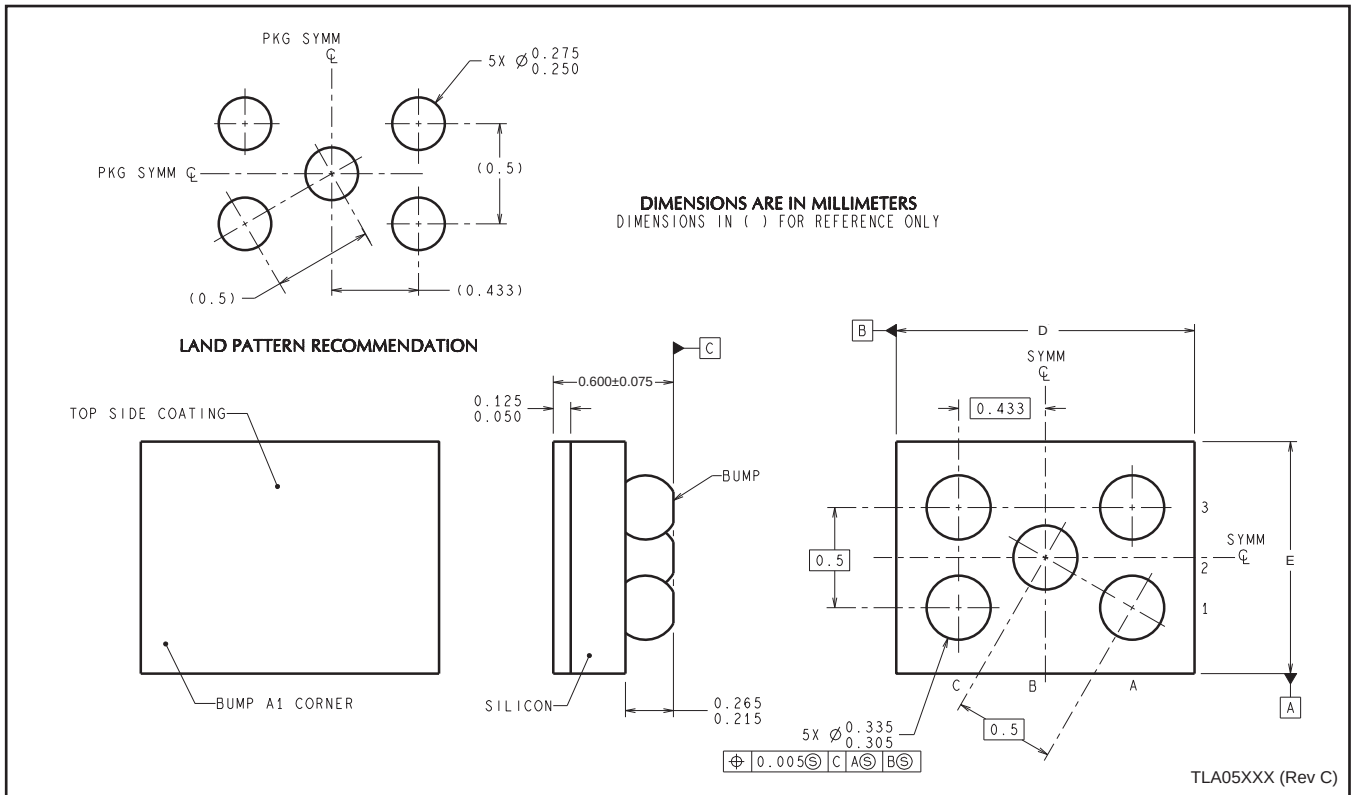
YPB0005



4215098/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

YZR0005



4215043/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265