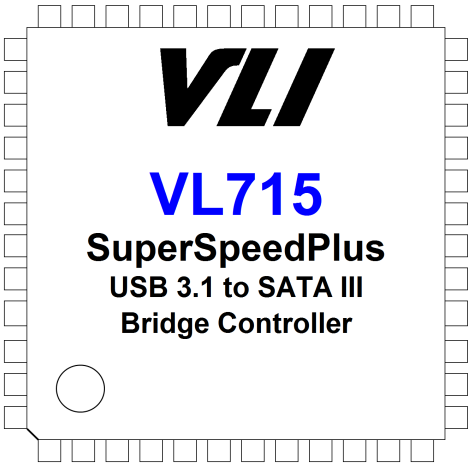
VIA Labs, Inc.

# Data Sheet

VL715
USB3.1 to SATA 6Gb/s
Bridge Controller

May 12, 2015
Revision 0.85



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# Revision History

| Rev | Date | Initial | Note |
|---|---|---|---|
| 0.8 | 11/11/2014 | HC | Preliminary release |
| 0.85 | 05/12/2015 | HC | Update GPIO driving spec, add GPIO7 with PWM |

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# Product Features

**VL715**

USB3.1 to SATA 6Gb/s Bridge Controller

- **SuperSpeedPlus USB (10Gb/s) and High-Speed USB (480Mb/s)**
  - Compliant to Universal Serial Bus 3.1 Specification Revision 1.0
  - Compliant to Universal Serial Bus Specification Revision 2.0
  - Mass Storage Class Bulk-Only Transport (BOT)
  - USB Attached SCSI Protocol (UASP) for streaming
  - Integrated in-house SuperSpeedPlus PHY and USB2.0 PHY
- **Serial ATA 6Gb/s, 3Gb/s and 1.5Gb/s**
  - Compliant to Serial ATA Specification Revision 3.1
  - Integrated in-house SATA 6Gb/s PHY
  - RBC command conversion for ATA device
  - MMC-2 command pass-through to ATAPI
  - Support 48-bit LBA
  - Support multiple LUN
- **Fast 8051 Macro cell 80C32-Compatible Microcontroller**
  - Standard 1T 8051 instruction set
- **Built-in Voltage Regulators**
  - 5.0V to 3.3V LDO
  - 5.0V to 1.2V switching DC-DC
- **GPIOs for Special Function Usage**
  - 7 GPIOs in QFN48 and QFN44 for customer special usage
  - 2 dedicated BUSY/POWER LED indicators
- **Misc**
  - Support device power down function
  - Support external SPI flash for firmware upgrade
- **Software**
  - Support Microsoft Windows 8, Windows 7, Vista, XP
  - Support Mac OS 10.X
  - Support various Linux kernels
- **Physical**
  - QFN 48L green package (6x6x0.85 mm)
  - QFN 44L green package (6x5x0.85 mm)
- **Certification**
  - USB-IF SuperSpeedPlus Certified: TBD

## VL715 System Overview

VIA Lab's VL715 is a high performance, low power single chip USB 3.1 to SATA 6Gb/s bridge controller designed for new generation external storage devices that connecting Hard Disk Drive (HDD), Solid-State Drive (SSD), and Optical Disc Drive (ODD). Its integrated in-house USB 3.1 PHY enables VL715 to run in USB SuperSpeedPlus, Super-Speed, High-Speed, and Full-Speed modes. Supporting USB mass storage class Bulk-Only Transport (BOT), VL715 based devices can work on Windows 8, Windows 7, Vista, XP, Mac OS X and various Linux kernels without additional driver. Besides Bulk-Only Transport, VL715 also support USB Attached SCSI Protocol (UASP) that allowing mass storage command queuing and out of order data transfers to further enhance read/write performance. Its integrated in-house SATA 6Gb/s host controller can work with all SATA based storage devices and can connect at SATA 6Gb/s, SATA 3Gb/s, or SATA 1.5Gb/s automatically.

Built-in all required linear and switching voltage regulators, highly integrated VL715 work perfectly with single power input from USB 5V bus power to save customer BOM cost. 7 GPIO pins are available for push button, operation LEDs, device power down control, and other special usage. The SPI interface can support external flash for firmware upgrades or additional software enhancements. VL715 is pin to pin compatibility to its predecessor VL711 which can keep using the same PCB design. VL715 is available in QFN 48L (6x6x0.85 mm) and QFN 44L (6x5x0.85 mm) green packages to fit small form-factor design.



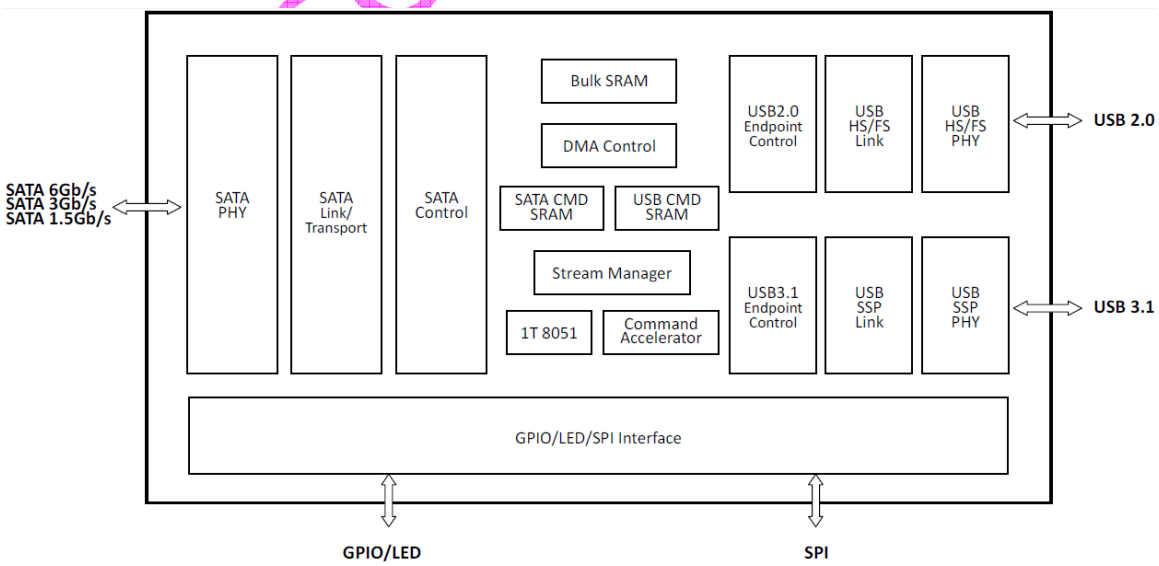



**Figure 1 – VL715 Block Diagram**

## Pinout

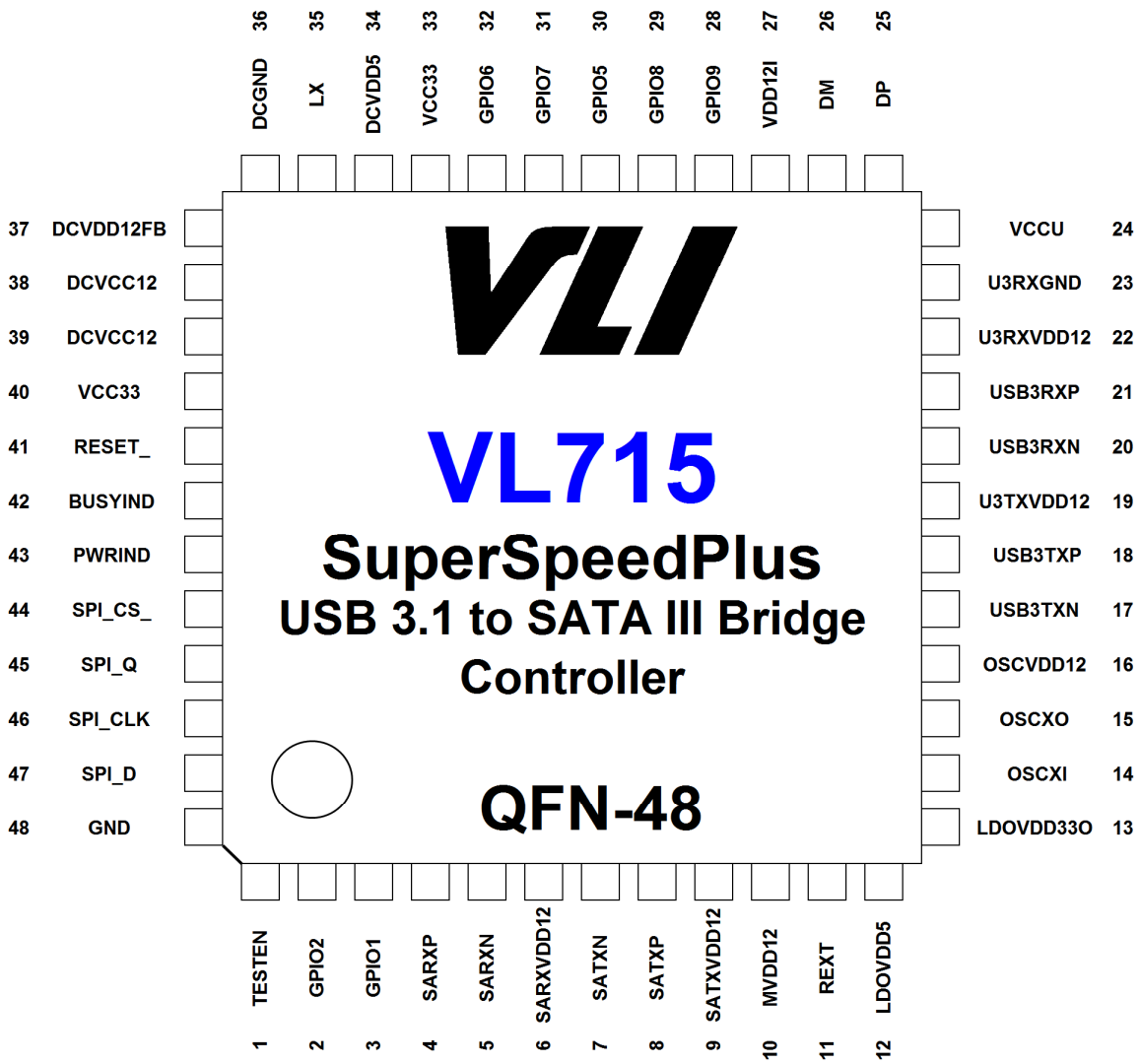



**Figure 2 – VL715 QFN-48 Pin Diagram**

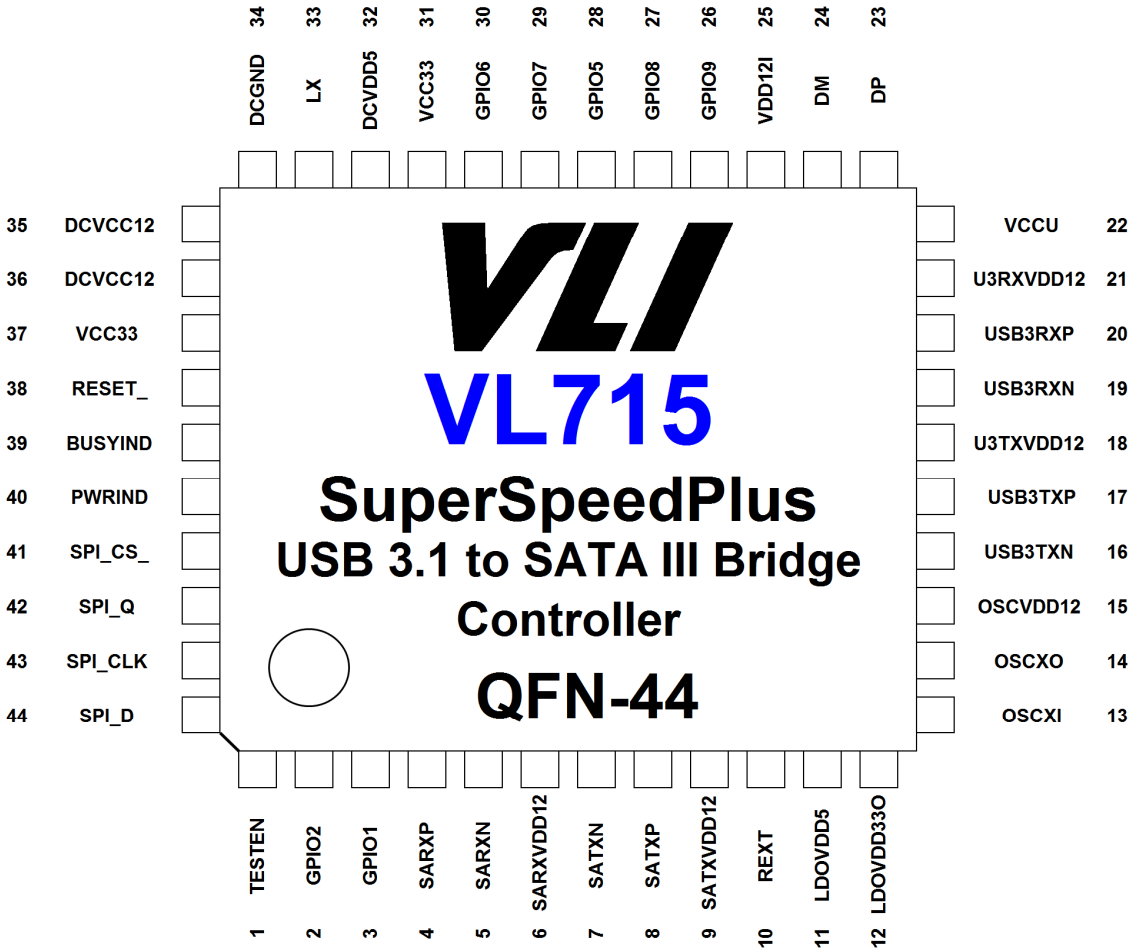



**Figure 3 – VL715 QFN-44 Pin Diagram**

# Pin List

**Table 1 – VL715 QFN-48 Pin List**

| Pin | Pin Name | Pin | Pin Name |
|---|---|---|---|
| 1 | TESTEN | 25 | DP |
| 2 | GPIO2 | 26 | DM |
| 3 | GPIO1 | 27 | VDD12I |
| 4 | SARXP | 28 | GPIO9 |
| 5 | SARXN | 29 | GPIO8 |
| 6 | SARXVDD12 | 30 | GPIO5 |
| 7 | SATXN | 31 | GPIO7 |
| 8 | SATXP | 32 | GPIO6 |
| 9 | SATXVDD12 | 33 | VCC33 |
| 10 | MVDD12 | 34 | DCVDD5 |
| 11 | REXT | 35 | LX |
| 12 | LDOVDD5 | 36 | DCGND |
| 13 | LDOVDD33O | 37 | DCVDD12FB |
| 14 | OSCXI | 38 | DCVCC12 |
| 15 | OSCXO | 39 | DCVCC12 |
| 16 | OSCVDD12 | 40 | VCC33 |
| 17 | USB3TXN | 41 | RESET_ |
| 18 | USB3TXP | 42 | BUSYIND |
| 19 | U3TXVDD12 | 43 | PWRIND |
| 20 | USB3RXN | 44 | SPI_CS_ |
| 21 | USB3RXP | 45 | SPI_Q |
| 22 | U3RXVDD12 | 46 | SPI_CLK |
| 23 | U3RXGND | 47 | SPI_D |
| 24 | VCCU | 48 | DGND |

**Table 2 – VL715 QFN-44 Pin List**

| Pin | Pin Name | Pin | Pin Name |
|---|---|---|---|
| 1 | TESTEN | 23 | DP |
| 2 | GPIO2 | 24 | DM |
| 3 | GPIO1 | 25 | VDD12I |
| 4 | SARXP | 26 | GPIO9 |
| 5 | SARXN | 27 | GPIO8 |
| 6 | SARXVDD12 | 28 | GPIO5 |
| 7 | SATXN | 29 | GPIO7 |
| 8 | SATXP | 30 | GPIO6 |
| 9 | SATXVDD12 | 31 | VCC33 |
| 10 | REXT | 32 | DCVDD5 |
| 11 | LDOVDD5 | 33 | LX |
| 12 | LDOVDD33O | 34 | DCGND |
| 13 | OSCXI | 35 | DCVCC12 |
| 14 | OSCXO | 36 | DCVCC12 |
| 15 | OSCVDD12 | 37 | VCC33 |
| 16 | USB3TXN | 38 | RESET_ |
| 17 | USB3TXP | 39 | BUSYIND |
| 18 | U3TXVDD12 | 40 | PWRIND |
| 19 | USB3RXN | 41 | SPI_CS_ |
| 20 | USB3RXP | 42 | SPI_Q |
| 21 | U3RXVDD12 | 43 | SPI_CLK |
| 22 | VCCU | 44 | SPI_D |

# Pin Descriptions

**Signal Type Definition**

| Name | Type | Signal Description |
|---|---|---|
| Input | I | A standard input-only signal |
| Output | O | A standard active driver |
| Input/Output | I/O | A bi-directional signal |
| Analog bias | $A_{BIAS}$ | Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network |
| Power | PWR | A power pin |
| Ground | GND | A ground pin |

**Serial ATA Interface**

| Pin Name | QFN48 | QFN44 | I/O | Signal Description |
|---|---|---|---|---|
| SARXP | 4 | 4 | I | SATA Port Differential Receive Data + |
| SARXN | 5 | 5 | I | SATA Port Differential Receive Data - |
| SATXP | 8 | 8 | O | SATA Port Differential Transmit Data + |
| SATXN | 7 | 7 | O | SATA Port Differential Transmit Data - |
| SATXVDD12 | 9 | 9 | PWR | Analog 1.2V |
| SARXVDD12 | 6 | 6 | PWR | Analog 1.2V |

**USB 3.1 Interface**

| Pin Name | QFN48 | QFN44 | I/O | Signal Description |
|---|---|---|---|---|
| USB3RXP | 21 | 20 | I | USB 3.1 Port Differential Receive Data + |
| USB3RXN | 20 | 19 | I | USB 3.1 Port Differential Receive Data - |
| USB3TXP | 18 | 17 | O | USB 3.1 Port Differential Transmit Data + |
| USB3TXN | 17 | 16 | O | USB 3.1 Port Differential Transmit Data - |
| U3RXVDD12 | 22 | 21 | PWR | Analog 1.2V |
| U3TXVDD12 | 19 | 18 | PWR | Analog 1.2V |
| U3RXGND | 23 | — | GND | USB3 RX ground |

**USB 2.0 Interface**

| Pin Name | QFN48 | QFN44 | I/O | Signal Description |
|---|---|---|---|---|
| DP | 25 | 23 | I/O | USB 2.0 Bus Data Plus (D+) |
| DM | 26 | 24 | I/O | USB 2.0 Bus Data Minus (D–) |
| VCCU | 24 | 22 | PWR | Analog 3.3V |

**Serial EEPROM Interface**

| Pin Name | QFN48 | QFN44 | I/O | Signal Description |
|---|---|---|---|---|
| SPI_CS_ | 44 | 41 | O | Serial Flash Chip Enable |
| SPI_D | 47 | 44 | O | Serial Flash Data Input |
| SPI_Q | 45 | 42 | I | Serial Flash Data Output |
| SPI_CLK | 46 | 43 | O | Serial Flash Clock |

**Analog Command Block**

| Pin Name | QFN48 | QFN44 | I/O | Signal Description |
|---|---|---|---|---|
| OSCXI | 14 | 13 | I | 25M crystal input |
| OSCXO | 15 | 14 | O | 25M crystal output |
| REXT | 11 | 10 | $A_{BIAS}$ | Connect to external resistor |
| LDOVDD5 | 12 | 11 | PWR | 5.0V voltage input for 5V to 3.3V LDO |
| LDOVDD33O | 13 | 12 | O | 3.3V voltage output for 5V to 3.3V LDO |
| DCVDD5 | 34 | 32 | PWR | 5.0V voltage input for DC2DC regulator |
| LX | 35 | 33 | O | 1.2V voltage output for DC2DC regulator |
| DCGND | 36 | 34 | GND | Ground for DC2DC regulator |
| DCVDD12FB | 37 | — | I | 1.2V feedback for DC2DC regulator |
| DCVCC12 | 38 | 35 | PWR | 1.2V voltage input for core power |
| DCVCC12 | 39 | 36 | PWR | 1.2V voltage input for core power |
| MVDD12 | 10 | — | PWR | Master analog 1.2V |
| OSCVDD12 | 16 | 15 | PWR | Oscillator analog 1.2V |

**General Purpose I/O and Miscellaneous**

| Pin Name | QFN48 | QFN44 | I/O | Signal Description |
|---|---|---|---|---|
| BUSYIND | 42 | 39 | O | Busy LED Indicator, including PWM<br>Typical Low Level Output Current $I_{OL}$ = 22.6mA @ 0.4V (max);<br>Typical High Level Output Current $I_{OH}$ = 39.6mA @ 2.4V (min) |
| PWRIND | 43 | 40 | O | Power LED Indicator, including PWM<br>Typical Low Level Output Current $I_{OL}$ = 22.6mA @ 0.4V (max);<br>Typical High Level Output Current $I_{OH}$ = 39.6mA @ 2.4V (min) |
| RESET_ | 41 | 38 | I | External Chip Reset |
| GPIO_1 | 3 | 3 | I/O | General Purpose I/O ($I_{OL}$ = 22.6mA @ 0.4V; $I_{OH}$ = 39.6mA @ 2.4V in output mode)<br>Default: Device power down control |
| GPIO_2 | 2 | 2 | I/O | General Purpose I/O, including PWM ($I_{OL}$ = 22.6mA @ 0.4V; $I_{OH}$ = 39.6mA @ 2.4V in output mode)<br>Default: USB3.1/USB2.0 mode indicator |
| GPIO_5 | 30 | 28 | I/O | General Purpose I/O ($I_{OL}$ = 22.6mA @ 0.4V; $I_{OH}$ = 39.6mA @ 2.4V in output mode)<br>Default: Push button trigger pin |
| GPIO_6 | 32 | 30 | I/O | General Purpose I/O ($I_{OL}$ = 22.6mA @ 0.4V; $I_{OH}$ = 39.6mA @ 2.4V in output mode)<br>Default: USB cable power detect |
| GPIO_7 | 31 | 29 | I/O | General Purpose I/O, including PWM ($I_{OL}$ = 22.6mA @ 0.4V; $I_{OH}$ = 39.6mA @ 2.4V in output mode)<br>Default: Device write protect control |
| GPIO_8 | 29 | 27 | I/O | General Purpose I/O ($I_{OL}$ = 22.6mA @ 0.4V; $I_{OH}$ = 39.6mA @ 2.4V in output mode)<br>Default: Push button status indicator |
| GPIO_9 | 28 | 26 | I/O | General Purpose I/O ($I_{OL}$ = 22.6mA @ 0.4V; $I_{OH}$ = 39.6mA @ 2.4V in output mode)<br>Default: EEPROM chip select & LED blinking mode select |

**Test Pin**

| Pin Name | QFN48 | QFN44 | I/O | Signal Description |
|---|---|---|---|---|
| TESTEN | 1 | 1 | I | Test Mode Enable<br>Do not connect for normal operation.<br>Internal pull down |

**Power and Ground**

| Pin Name | QFN48 | QFN44 | I/O | Signal Description |
|---|---|---|---|---|
| DGND | 48 | — | GND | Ground |
| VCC33 | 33, 40 | 31, 37 | PWR | Digital IO power 3.3V |
| VDD12I | 27 | 25 | PWR | Digital Core power 1.2V |

# Electrical Specification

### Absolute Maximum Rating

| Symbol | Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| $T_{STG}$ | Storage Temperature | -55 | 125 | °C | — |
| $T_A$ | Ambient Temperature | 0 | 70 | °C | — |
| $V_{DD33}$ | Power Supply Voltage | -0.5 | 3.69 | V | — |
| $V_{DD50}$ | Input Voltage | -0.5 | 5.5 | V | — |
| $V_O$ | Output Voltage at any output | -0.5 | VCC+ 0.5 | V | — |
| $V_{ESD}$ | Electrostatic Discharge | — | 2 | kV | Human Body Model |

Note: Stress above conditions may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described.

### Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC33}$ | Digital IO power 3.3V | 3.0 | 3.3 | 3.6 | V |
| LDOVDD5 | 5V to 3.3V LDO 5V Power Input | 4.5 | 5 | 5.5 | V |
| DCVDD5 | 5V to 1.2V DC2DC 5V Power Input | 4.5 | 5 | 5.5 | V |
| $V_{DD12I}$ | Digital Core power 1.2V | 1.08 | 1.2 | 1.36 | V |
| DGND | Ground | — | 0 | — | V |

### General IO DC Characteristics

| Symbol | Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.30 | 0.8 | V | — |
| $V_{IH}$ | Input High Voltage | 2.0 | 3.6 | V | — |
| $V_{OL}$ | Output Low Voltage | — | 0.4 | V | IOL=15.8mA |
| $V_{OH}$ | Output High Voltage | 2.4 | — | V | IOH=26.5mA |
| $I_{IL}$ | Input Leakage Current | — | +/-10 | μA | 0<VIN<VCC |
| $I_{OZ}$ | Tristate Leakage Current | — | +/-10 | μA | 0<VOUT<VCC |

### Internal 5V to 1.2V DC/DC Converter

| Parameter | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|
| Input Voltage | 4.5 | 5.0 | 5.5 | V | |
| Output Voltage | 1.14 | 1.2 | 1.26 | V | |
| Max. Output Current | | TBD | TBD | mA | |
| Output Voltage Tolerance | | +/- 5% | | | |

### Internal 5V to 3.3V LDO Regulator

| Parameter | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|
| Input Voltage | 4.5 | 5.0 | 5.5 | V | |

| | | | | |
|---|---|---|---|---|
| Output Voltage | 3.135 | 3.3 | 3.465 | V |
| Max. Output Current | | TBD | TBD | mA |
| Output Voltage Tolerance | | +/- 5% | | |

**External Crystal Electrical Characteristics**

Please refer to the Figure 4.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| FL | Normal Frequency | | 25 | | MHz |
| | Oscillation Mode | | Fundamental | | |
| | Frequency Tolerance | -30 | | 30 | ppm |
| | Aging | -5 | | 5 | ppm |
| CL | Loading Capacitance | | 20 | | pf |
| C0 | Shunt Capacitance | 1 | 3 | 7 | pf |
| Rr | Effective Resistance | | | 50 | ohms |

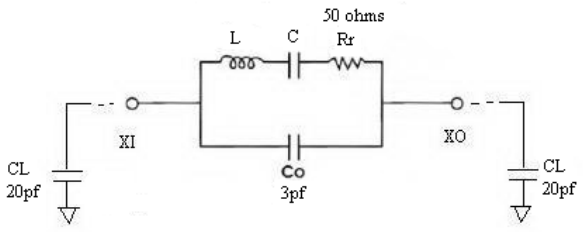



**Figure 4 – 25MHz Crystal equivalent circuit and spec requirement**

**USB Full Speed DC/AC Characteristics**

| Symbol | Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| $V_{FSIH}$ | Full-speed Input High | 2.0 | | V | — |
| $V_{FSIL}$ | Full-speed Input Low | | 0.8 | V | — |
| $V_{FSCM}$ | Differential Common Mode Voltage | 0.8 | 2.5 | V | — |
| $V_{FSOL}$ | Full-speed Output Low | 0.0 | 0.3 | V | — |
| $V_{FSOH}$ | Full-speed Output High | 2.8 | 3.6 | V | — |
| $T_{FSR}$ | Full-speed Rise Time | 4 | 20 | ns | — |
| $T_{FSF}$ | Full-speed Fall Time | 4 | 20 | ns | — |
| $V_{FSCRS}$ | Full-speed Output Signal Crossover Voltage | 1.3 | 2.0 | V | — |

**USB High Speed DC/AC Characteristics**

| Symbol | Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| $V_{HSSQ}$ | High-speed squelch detection threshold | 100 | 150 | mV | — |
| $V_{HSCM}$ | High-speed data signaling common mode voltage | -50 | 500 | mV | — |
| $V_{HSOI}$ | High-speed idle level | -10 | 10 | mV | — |
| $V_{HSOH}$ | High-speed data high | 360 | 440 | mV | — |

| | | | | | |
|---|---|---|---|---|---|
| $V_{HSOL}$ | High-speed data low | -10 | 10 | mV | — |
| $V_{CHIRPJ}$ | Chirp J level | 700 | 1100 | mV | — |
| $V_{CHIRPK}$ | Chirp K level | -900 | -500 | mV | — |
| $Z_{HSDRV}$ | Drive output resistance | 40.5 | 49.5 | Ω | — |
| $T_{HSR}$ | High-speed Rise Time | 500 | | ps | — |
| $T_{HSF}$ | High-speed Fall Time | 500 | | ps | — |

## USB SuperSpeedPlus TX RX Characteristics

TBD

### USB Super Speed TX Characteristics

| Symbol | Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| $V_{TX-DIFF-PP}$ | Differential p-p Tx swing | 0.8 | 1.2 | V | — |
| $V_{TX-DE-RATIO}$ | Tx de-emphasis | 3.0 | 4.0 | dB | — |
| $R_{TX-DIFF-DC}$ | DC differential impedance | 72 | 120 | Ω | — |
| $V_{TX-RCV-DETECT}$ | The Voltage Change allowed during Receiver Detection | | 0.6 | V | — |
| $T_{TX-EYE}$ | Transmitter Eye | 0.625 | | UI | — |
| $T_{TX-DJ-DD}$ | Tx Deterministic Jitter | | 0.205 | UI | — |
| $R_{TX-DC}$ | Transmitter DC Common Mode Impedance | 18 | 30 | Ω | — |
| $V_{TX-DC-CM}$ | Transmitter DC Common Mode Voltage | 0 | 2.2 | V | — |
| $V_{TX-CM-AC-PP-ACTIVE}$ | Tx AC Common Mode Voltage Active | | 100 | mV | — |
| $V_{TX-IDLE-DIFF-AC-pp}$ | Electrical Idle Differential P-P Output Voltage | 0 | 10 | mV | — |
| $V_{TX-IDLE-DIFF-DC}$ | DC Electrical Idle Differential Output Voltage | 0 | 10 | mV | — |

### USB Super Speed RX Characteristics (5.0 GT/s)

| Symbol | Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| UI | Unit Interval | 199.94 | 200.06 | ps | UI does not account for SSC caused variations |
| $R_{RX-DC}$ | Receiver DC common mode impedance | 18 | 30 | Ω | DC impedance limits are needed to guarantee Receiver detect<br>Measured with respect to ground over a voltage of 500mV maximum |
| $R_{RX-DIFF-DC}$ | DC differential impedance | 72 | 120 | Ω | |
| $Z_{RX-HIGH-IMP-DC-POS}$ | DC Input CM Input Impedance for V>0 during Reset or power down | 25k | | Ω | Rx DC CM impedance with the Rx terminations not powered, measured over the range 0 – 500mv with respect to ground |

| | | | | | |
|---|---|---|---|---|---|
| $V_{RX-LFPS-DET-DIFF_{p-p}}$ | LFPS Detect Threshold | 100 | 300 | mV | Below the minimum is noise<br>Must wake up above the maximum |
| $V_{RX-DIFF-PP-POST-EQ}$ | Differential Rx peak-to-peak voltage | 30 | | mV | Measured after the Rx EQ function (Section 6.8.2) |
| $t_{RX-TJ}$ | Max Rx inherent timing error | | 0.45 | UI | Measured after the Rx EQ function (Section 6.8.2) |
| $t_{RX-DJ-DD}$ | Max Rx inherent deterministic timing error | | 0.3 | UI | Maximum Rx inherent deterministic timing error |
| $C_{RX-PARASITIC}$ | Rx input capacitance for return loss | | 1.1 | pf | |
| $V_{RX-CM-AC-P}$ | Rx AC common mode voltage | | 150 | mV Peak | Measured at Rx pins into a pair of 50Ω terminations into ground<br>Includes Tx and channel conversion, AC range up to 5 GHz |
| $V_{RX-CM-DC-ACTIVE-IDLE-DELTA-P}$ | Rx AC common mode voltage during the U1 to U0 transition | | 200 | mV Peak | Measured at Rx pins into a pair of 50Ω terminations into ground<br>Includes Tx and channel conversion, AC range up to 5 GHz |

**SATA TX Characteristics**

| Symbol | Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| $Z_{diffTX}$ | TX Pair Differential Impedance | 85 | 115 | Ohm | |
| $Z_{s-eTX}$ | TX Single-Ended Impedance | 40 | | | |
| $RL_{DD11,TX}$ | TX Differential Mode Return Loss (150MHz-300MHz) | 14 | | dB | |
| | TX Differential Mode Return Loss (300MHz-600MHz) | 8 | | dB | |
| | TX Differential Mode Return Loss (600MHz-1.2GHz) | 6 | | dB | |
| | TX Differential Mode Return Loss (1.2GHz-2.4GHz) | 6 | | dB | |
| | TX Differential Mode Return Loss (2.4GHz-3.0GHz) | 3 | | dB | |
| | TX Differential Mode Return Loss (3.0GHz-5.0GHz) | 1 | | dB | Only for Gen2i |
| $RL_{DD11,TX}$ | TX Differential Mode Return Loss Start for slope for Gen3 | Min at 300MHz is 14 | | dB | |

| | | | | | |
|---|---|---|---|---|---|
| | Slope of TX Differential Mode Return Loss for Gen3 | -13 | | dB/dec | |
| | TX Differential Mode Return Loss Max Frequency for Gen3 | | Max is 3 | GHz | |
| $RL_{CC11,TX}$ | TX Common Mode Return Loss (150MHz-300MHz) | 8 | | dB | |
| | TX Common Mode Return Loss (300MHz-600MHz) | 5 | | dB | |
| | TX Common Mode Return Loss (600MHz-1.2GHz) | 2 | | dB | |
| | TX Common Mode Return Loss (1.2GHz-2.4GHz) | 1 | | dB | |
| | TX Common Mode Return Loss (2.4GHz-3.0GHz) | 1 | | dB | |
| | TX Common Mode Return Loss (3.0GHz-5.0GHz) | 1 | | dB | Only for Gen2i |
| $RL_{DC11,TX}$ | TX Impedance Balance (150MHz-300MHz) | 30 | | dB | |
| | TX Impedance Balance (300MHz-600MHz) | 20 | | dB | |
| | TX Impedance Balance (600MHz-1.2GHz) | 10 | | dB | |
| | TX Impedance Balance (1.2GHz-2.4GHz) | 10 | | dB | |
| | TX Impedance Balance (2.4GHz-3.0GHz) | 4/10 | | dB | For Gen3i is 10dB |
| | TX Impedance Balance (3.0GHz-5.0GHz) | 4 | | dB | |
| | TX Impedance Balance (5.0GHz-6.5GHz) | 4 | | | Only for Gen3i |
| $V_{diffTX}$ | TX Differential Output Voltage | 400 | 600 | mVppd | For Gen1 |
| | TX Differential Output Voltage | 400 | 700 | mVppd | For Gen2 |
| | TX Differential Output Voltage | 200 | 900 | mVppd | For Gen3 |
| $UI_{VminTX}$ | TX Minimum Voltage Measurement Interval | 0.45 | 0.55 | UI | |
| $t_{20-80TX}$ | TX Rise/Fall Time | 100 | 273 | ps | For Gen1 |
| | TX Rise/Fall Time | 67 | 136 | ps | For Gen2 |
| | TX Rise/Fall Time | 33 | 80 | ps | For Gen3 |
| $t_{skewTX}$ | TX Differential Skew | | 20 | ps | |
| $V_{cm,acTX}$ | TX AC Common Mode Voltage | | 50 | mVp-p | |
| | TX AC Common Mode Voltage 3 GHz Max | | 26 | dBmV(rms) | For Gen3 |
| | TX AC Common Mode Voltage 6 GHz Max | | 30 | dBmV(rms) | For Gen3 |
| $D_{vdiffOOB}$ | OOB Differential Delta | | 25 | mV | |
| $D_{vcmOOB}$ | OOB Common Mode Delta | | 50 | mV | |
| $R/F_{bal}$ | TX Rise/Fall Imbalance | | 20 | % | Only for Gen2 |
| $Amp_{bal}$ | TX Amplitude Imbalance | | 30 | % | Only for Gen2 |

| | | | | | |
|---|---|---|---|---|---|
| | TJ at Connector Clk-Data fBAUD/500 JTF Defined | | 0.37 | UI | For Gen1/Gen2 |
| | DJ at Connector Clk-Data fBAUD/500 JTF Defined | | 0.19 | UI | For Gen1/Gen2 |
| | Jitter Transfer Function Bandwidth (D24.3,high pass -3dB) | 1.1 | 3.1 | MHz | For Gen1/Gen2 |
| | Jitter Transfer Function Peaking | | 3.5 | dB | For Gen1/Gen2 |
| | Jitter Transfer Function Low Frequency Attenuation | 69 | 75 | db | For Gen1/Gen2 |
| | Jitter Transfer Function Bandwidth (D24.3,high pass -3dB) | 2.2 | 6.2 | MHz | For Gen3 |
| | Jitter Transfer Function Peaking | | 3.5 | dB | For Gen3 |
| | Jitter Transfer Function Low Frequency Attenuation | 35.2 | 41.2 | db | For Gen3 |
| | TJ(10-12)before and after CIC,Clk-Data JTF Defined | | 0.52 | UI | For Gen3 |
| | TJ(10-6)before and after CIC,Clk-Data JTF Defined | | 0.46 | UI | For Gen3 |

**SATA RX Characteristics**

| Symbol | Parameter | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| $V_{diffRX}$ | Gen1 RX Differential Input Voltage | 240 | 600 | mVppd | |
| | Gen2 RX Differential Input Voltage | 240 | 750 | | |
| | Gen3 RX Differential Input Voltage | 240 | 1000 | | |
| $t_{20\text{-}80RX}$ | Gen1 RX Rise/Fall time | 100 | 273 | ps | |
| | Gen2 RX Rise/Fall time | 67 | 136 | | |
| | Gen2 RX Rise/Fall time | 62 | 75 | | |
| $t_{skewRX}$ | Gne2 RX Differential Skew | | 50 | Ps | |
| | Gen3 RX Differential Skew | | 30 | | |
| $V_{cm,acRX}$ | RX AC Common Mode Voltage | | 100 | mVppd | |
| $f_{cm,acRX}$ | RX AC Common Mode Frequency | 2 | 200 | MHz | |
| | Gen1 TJ at Connector, Data-Data, 5UI | | 0.43 | UI | |
| | Gen1 DJ at Connector, Data-Data, 5UI | | 0.25 | UI | |
| | Gen1 TJ at Connector, Data-Data, 250UI | | 0.6 | UI | |
| | Gen1 TJ at Connector, Data-Data, 250UI | | 0.35 | UI | |
| | Gen2 TJ at Connector, Clk-Data, $f_{BAUD}/10$ | | 0.46 | UI | |
| | Gen2 DJ at Connector, Clk-Data, $f_{BAUD}/10$ | | 0.35 | UI | |
| | Gen2 TJ at Connector, Clk-Data, $f_{BAUD}/500$ | | 0.60 | UI | |

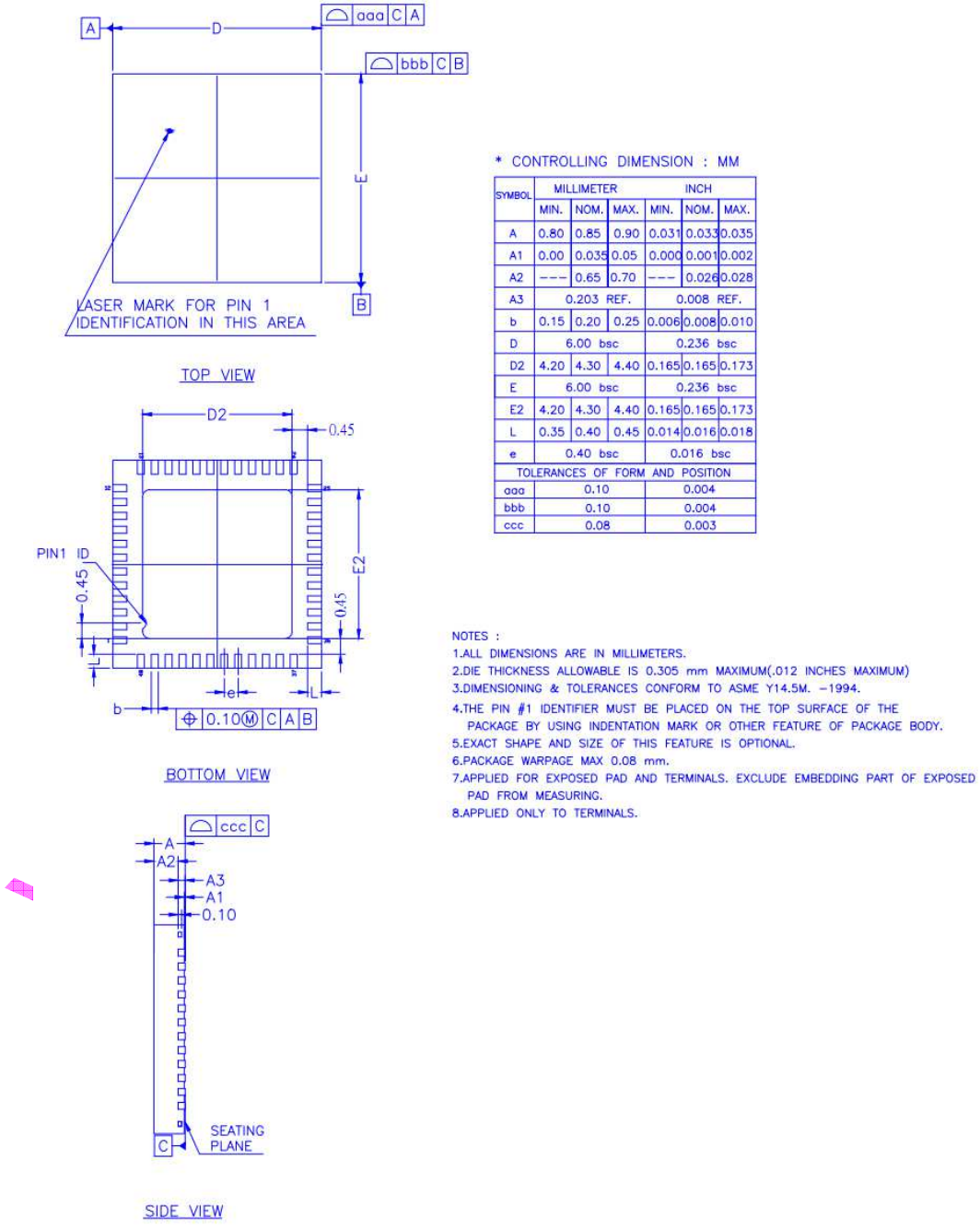
| | | | | |
|---|---|---|---|---|
| | Gen2 DJ at Connector, Clk-Data, $f_{BAUD}/500$ | | 0.42 | UI |
| Gen3 TJ after CIC | Clk-Data JTF Defined | | 0.60 | UI |
| Gen3 RJ before CIC | MFTP Clk-Data JTF Defined | | 0.60 | |
| $Z_{diffRX}$ | RX Pair Differential Impedance | 85 | 115 | Ohm |
| $Z_{s\text{-}eRX}$ | RX single-ended Impedance | 40 | | Ohm |
| $RL_{DD11,RX}$ | Gen2i/m RX Differential Mode Return Loss (150MHz-300MHz) | 18 | | dB |
| | Gen2i/m RX Differential Mode Return Loss (300MHz-600MHz) | 14 | | dB |
| | Gen2i/m RX Differential Mode Return Loss (600MHz-1.2GHz) | 10 | | dB |
| | Gen2i/m RX Differential Mode Return Loss (1.2GHz-2.4GHz) | 8 | | dB |
| | Gen2i/m RX Differential Mode Return Loss (2.4GHz-3.0GHz) | 3 | | dB |
| | Gen2i/m RX Differential Mode Return Loss (3.0GHz-5.0GHz) | 1 | | dB |
| | Gen3i RX Differential Mode Return Loss (min @ 300MHz) | | 18 | dB |
| | Gen3i Slop of RX Differential Mode Return Loss | -13 | | dB/dec |
| | Gen3i RX Differential Mode Return Loss max frequency | | 6.0 | GHz |
| $RL_{CC11}$ | Gen2i/m RX Common Mode Return Loss (150MHz-300MHz) | 5 | | dB |
| | Gen2i/m RX Common Mode Return Loss (300MHz-600MHz) | 5 | | dB |
| | Gen2i/m RX Common Mode Return Loss (600MHz-1.2GHz) | 2 | | dB |
| | Gen2i/m RX Common Mode Return Loss (1.2GHz-2.4GHz) | 1 | | dB |
| | Gen2i/m RX Common Mode Return Loss (2.4GHz-3.0GHz) | 1 | | dB |
| | Gen2i/m RX Common Mode Return Loss (3.0GHz-5.0GHz) | 1 | | dB |
| $V_{thresh}$ | Gen1 OOB Signal Detection Threshold | 50 | 200 | mVppd |
| | Gen2/3 OOB Signal Detection Threshold | 75 | 200 | mVppd |
| $UI_{OOB}$ | UI During OOB Signaling | 646.67 | 686.67 | ps |
| | COMINIT/COMRESET/COMWAKE Transmit Burst Length | 160 | 160 | $UI_{OOB}$ |
| | COMINIT/COMRESET Transmit Gap Length | 480 | 480 | $UI_{OOB}$ |
| | COMWAKE Transmit Gap Length | 160 | 160 | $UI_{OOB}$ |
| | COMWAKE Gap Detection Window | 55 | 175 | ns |

| | | | | |
|---|---|---|---|---|
| | COMINIT/COMRESET Gap Detection Window | 175 | 525 | ns |

# Package Mechanical Specifications

**QFN-48 Pb-free Maximum Temperature for IR Reflow**

| Parameter | Value | Unit |
|---|---|---|
| Maximum Temperature Tp | 250 | °C |
| Max Time within 5°C of Tp | 30 | seconds |




* CONTROLLING DIMENSION : MM

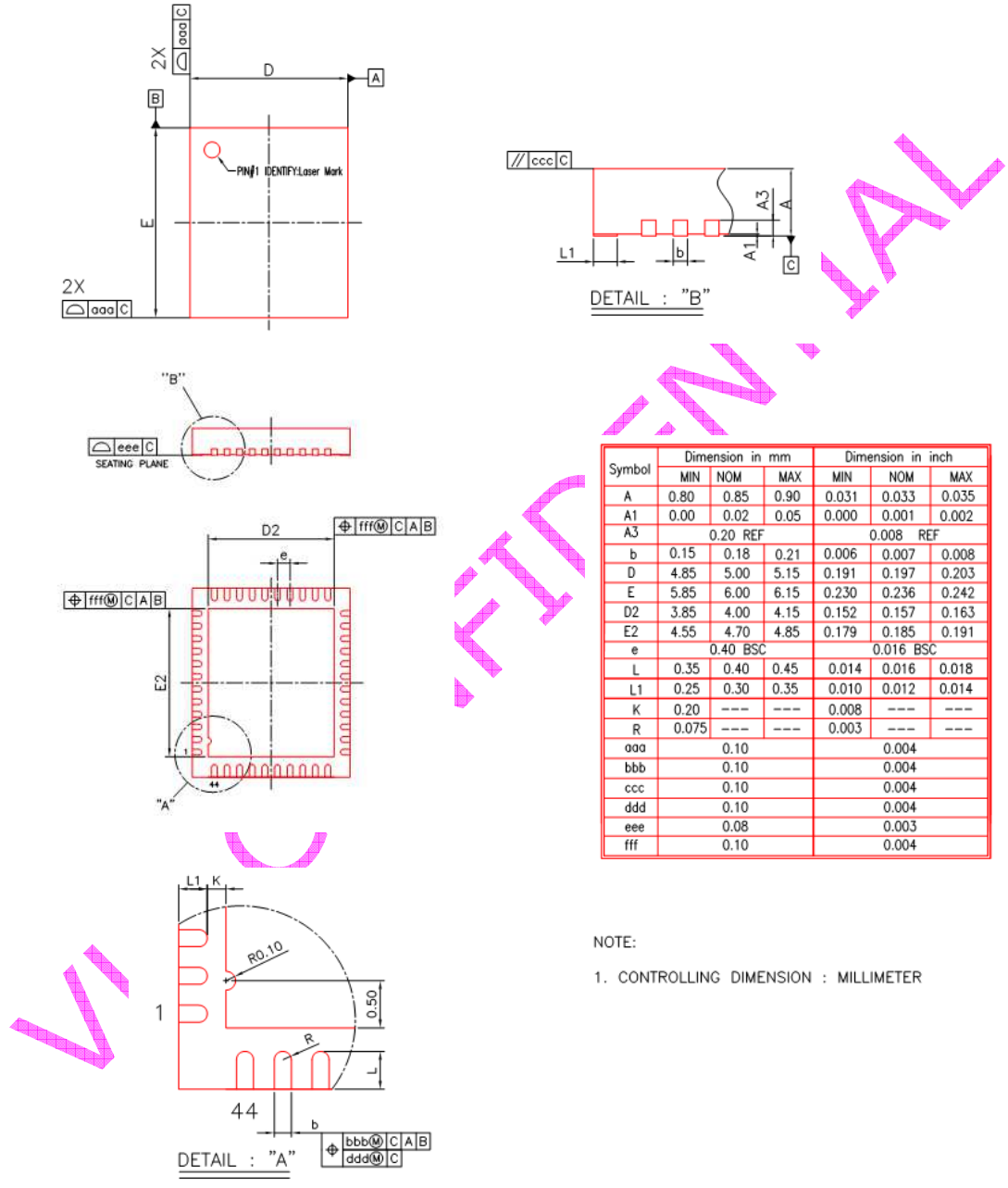
| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.80 | 0.85 | 0.90 | 0.031 | 0.033 | 0.035 |
| A1 | 0.00 | 0.035 | 0.05 | 0.000 | 0.001 | 0.002 |
| A2 | --- | 0.65 | 0.70 | --- | 0.026 | 0.028 |
| A3 | 0.203 REF. | | | 0.008 REF. | | |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | 6.00 bsc | | | 0.236 bsc | | |
| D2 | 4.20 | 4.30 | 4.40 | 0.165 | 0.165 | 0.173 |
| E | 6.00 bsc | | | 0.236 bsc | | |
| E2 | 4.20 | 4.30 | 4.40 | 0.165 | 0.165 | 0.173 |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| e | 0.40 bsc | | | 0.016 bsc | | |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | 0.10 | | | 0.004 | | |
| bbb | 0.10 | | | 0.004 | | |
| ccc | 0.08 | | | 0.003 | | |

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.

**Figure 5 – QFN 48L 6x6x0.85 mm Mechanical Specification**

**QFN-44 Pb-free Maximum Temperature for IR Reflow**

| Parameter | Value | Unit |
|---|---|---|
| Maximum Temperature Tp | 250 | °C |
| Max Time within 5°C of Tp | 30 | seconds |




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.80 | 0.85 | 0.90 | 0.031 | 0.033 | 0.035 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| A3 | | 0.20 REF | | | 0.008 REF | |
| b | 0.15 | 0.18 | 0.21 | 0.006 | 0.007 | 0.008 |
| D | 4.85 | 5.00 | 5.15 | 0.191 | 0.197 | 0.203 |
| E | 5.85 | 6.00 | 6.15 | 0.230 | 0.236 | 0.242 |
| D2 | 3.85 | 4.00 | 4.15 | 0.152 | 0.157 | 0.163 |
| E2 | 4.55 | 4.70 | 4.85 | 0.179 | 0.185 | 0.191 |
| e | | 0.40 BSC | | | 0.016 BSC | |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| L1 | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| K | 0.20 | --- | --- | 0.008 | --- | --- |
| R | 0.075 | --- | --- | 0.003 | --- | --- |
| aaa | | 0.10 | | | 0.004 | |
| bbb | | 0.10 | | | 0.004 | |
| ccc | | 0.10 | | | 0.004 | |
| ddd | | 0.10 | | | 0.004 | |
| eee | | 0.08 | | | 0.003 | |
| fff | | 0.10 | | | 0.004 | |

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

**Figure 6 – QFN 44L 6x5x0.85 mm Mechanical Specification**

## Package Top Side Marking

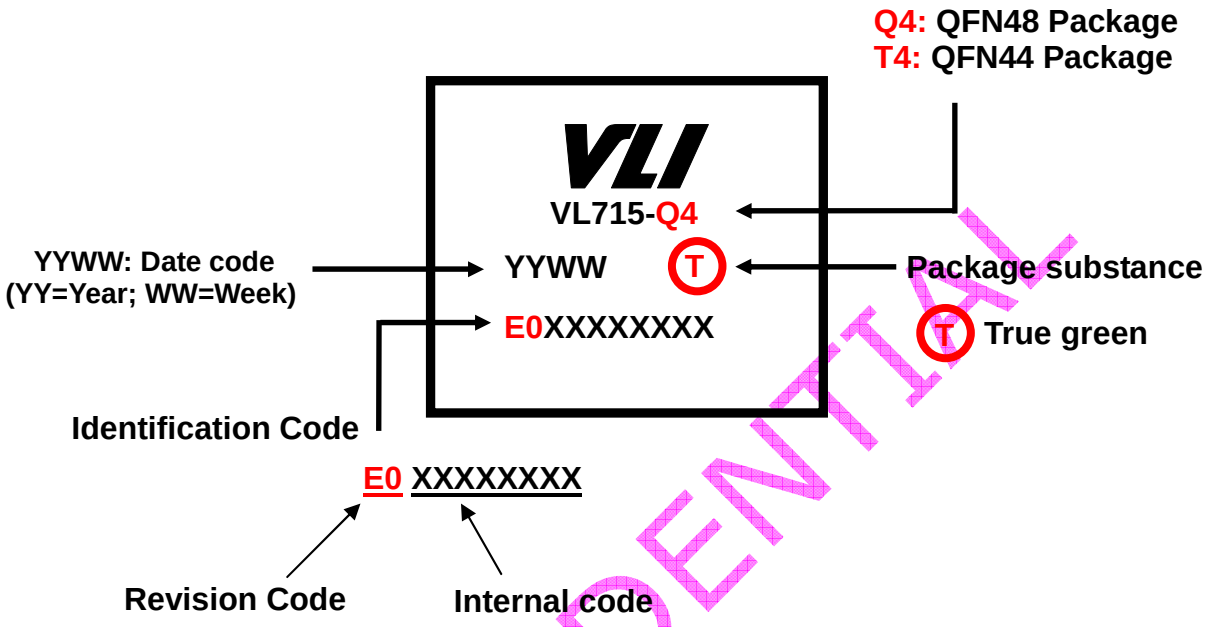



**Figure 7 – VL715 Package Top Side Marking**



## Ordering Information

| Part Number | Description | Package |
|---|---|---|
| VL715-Q4 | USB3.1 to SATA 6Gb/s bridge | 48-pin QFN (6x6mm) |
| VL715-T4 | USB3.1 to SATA 6Gb/s bridge | 44-pin QFN (6x5mm) |

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