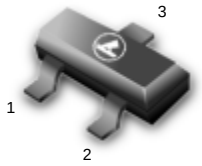
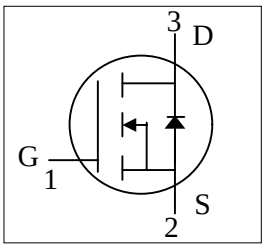
20V N-Channel Enhancement-Mode MOSFET

LN2302LT1G



SOT– 23 (TO–236AB)



●APPLICATIONS

1)High Density Cell Design For Ultra Low On-Resistance

Improved Shoot-Through FOM

2)We declare that the material of product compliant with RoHS requirements and Halogen Free

●FEATURES

V_{DS}= 20V

$R_{DS(ON)}$, Vgs@4.5V, Ids@2.8A = 60mΩ

$R_{DS(ON)}$, Vgs@2.5V, Ids@2.0A = 115mΩ

●DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LN2302LT1G	N02	3000/Tape&Reel
LN2302LT3G	N02	10000/Tape&Reel

●MAXIMUM RATINGS(Ta = 25℃)

Parameter		Symbol	Limits	Unit
Drain−to−Source Voltage		V_{DSS}	20	V
Gate−to−Source Voltage		V_{GS}	±8	V
Continuous Drain Current		I_D	2.3	A
Pulsed Drain Current (Note1)		I_{DM}	8	A
Maximum Power Dissipation	T_A = 25°C	P_D	0.9	W
	T_A = 75°C		0.57	
Operating and Storage Temperature Range		T_J, Tstg	–55 to +150	°C
Junction to Ambient Thermal Resistance(PCB mounted)(Note 2)		$R_{\theta JA}$	145	°C/W

1. Repetitive Rating: Pulse width limited by the Maximum junction temperation

2. 1-in2 2oz Cu PCB board

●ELECTRICAL CHARACTERISTICS (Ta= 25℃)

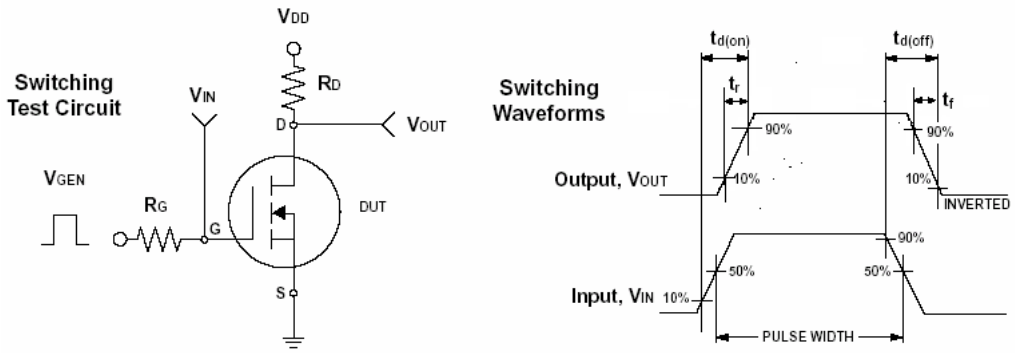
STATIC

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	20	–	–	V	V_{GS} = 0 V, I_D = 250 μA
Gate Threshold Voltage	$V_{GS(TH)}$	0.6	0.95	1.2	V	V_{GS} = V_{DS}, I_D = 250 μA
Zero Gate Voltage Drain Current	I_{DSS}	–	–	-1	μA	VDS=9.6V, VGS=0V
Gate−to−Source Leakage Current	I_{GSS}	–	–	±100	nA	V_{DS} = 0 V, V_{GS} = ±8 V
Drain−to−Source On Resistance	$R_{DS(on)}$	–	40	60	mΩ	V_{GS} = 4.5 V, I_D =2.8 A
		–	50	115	mΩ	V_{GS} = 2.5 V, I_D = 2 A
Forward Diode Voltage	V_{SD}			1.2	V	V_{GS} = 0 V, I_{SD} = -1.6A
Forward Transconductance	g_{FS}	–	6.5	–	S	V_{DS} = 5.0 V, I_D = 4 A

DYNAMIC(Note 3)

Input Capacitance	Ciss	–	427.12	–	pF	V_{GS} = 0 V, f = 1.0 MHz, V_{DS}= 6 V
Output Capacitance	Coss	–	80.56	–		
Reverse Transfer Capacitance	Crss	–	57.00	–		
Total Gate Charge	Q_G	–	3.69	–	nC	V_{GS} =4.5 V,V_{DS} = 6 V I_D = 2.8 A
Gate−to−Source Gate Charge	Q_{GS}	–	0.70	–		
Gate−to−Drain Charge	Q_{GD}	–	1.06	–		
Turn−On Delay Time	td(on)	–	6.16	–	ns	V_{DD} = 6V, R_L = 6Ω I_D = 1A, V_{GEN} = 4.5V R_G = 6Ω
Rise Time	tr	–	7.56	–		
Turn−Off Delay Time	td(off)	–	16.61	–		
Fall Time	tf	–	4.07	–		

3.Pulse test: pulse width ≦ 300us, duty cycle≦ 2%



LN2302LT1G

ELECTRICAL CHARACTERISTIC CURVES

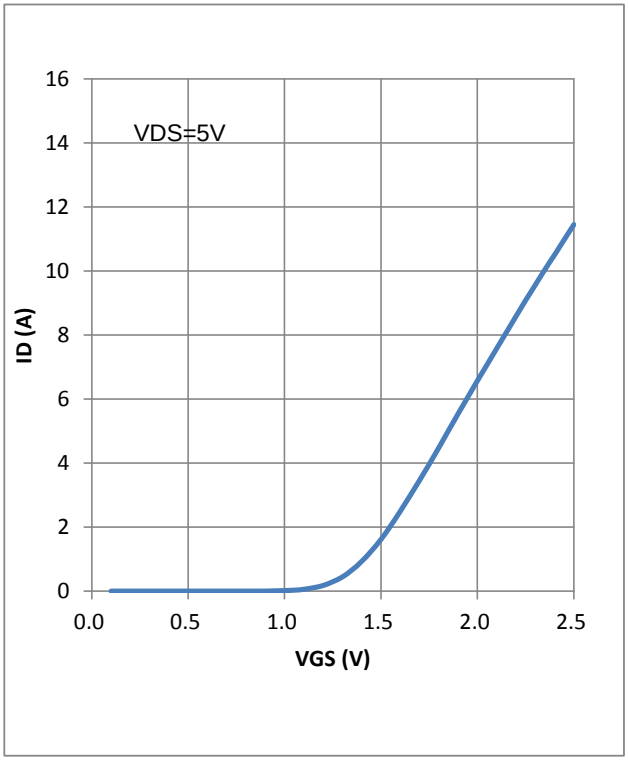


FIG.1 Transfer Characteristics

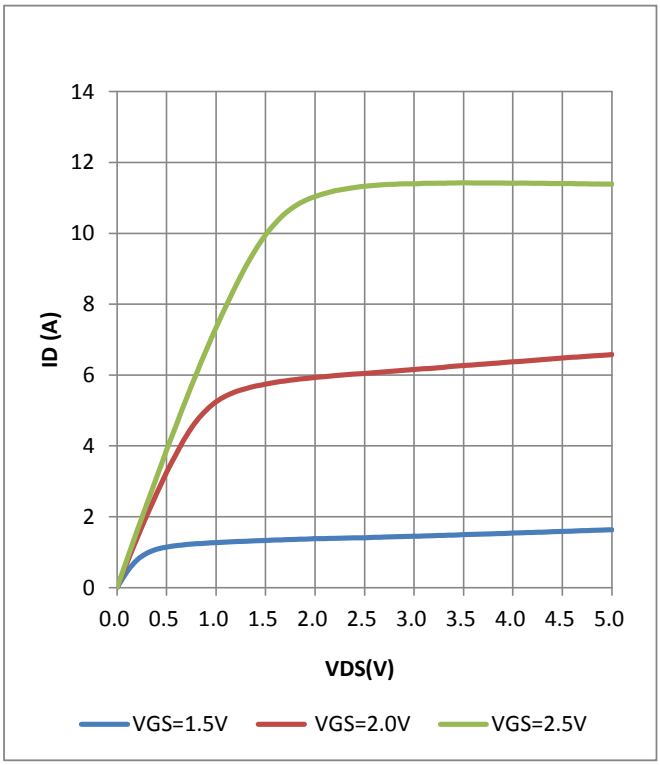


FIG.2 On-Region Characteristics

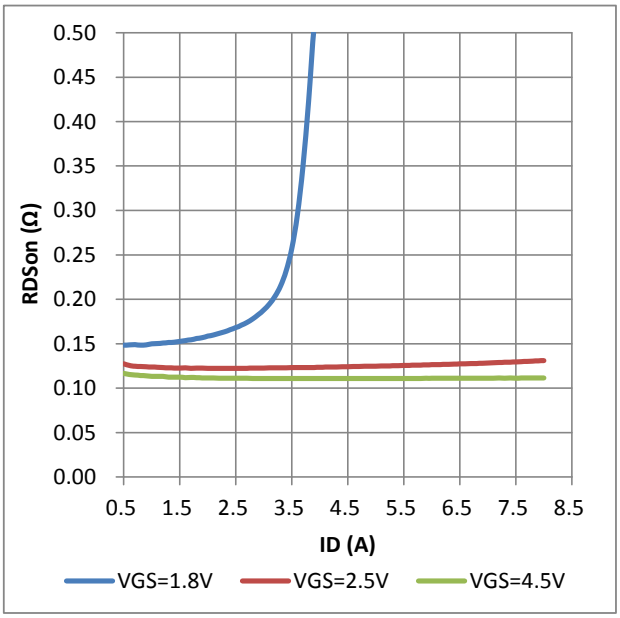


FIG.3 On-Resistance vs. Drain Current

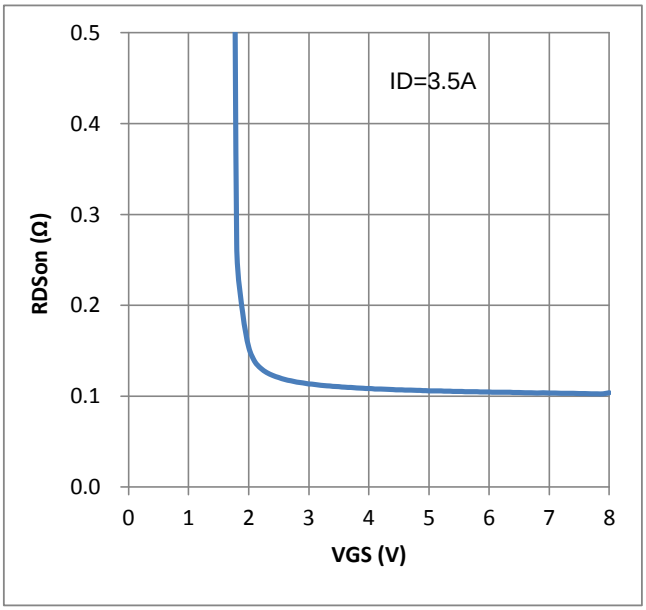


FIG.4 On-Resistance vs. Gate-to-Source Voltage

ELECTRICAL CHARACTERISTIC CURVES

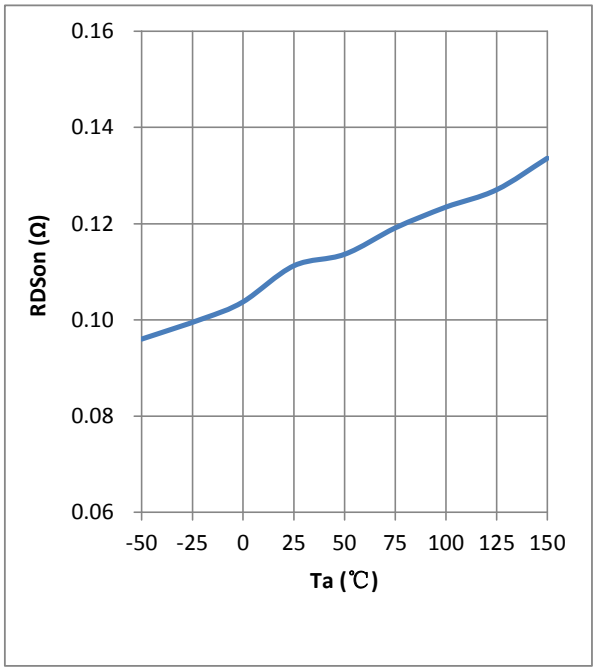


FIG.7 On-Resistance vs. Junction Temperature

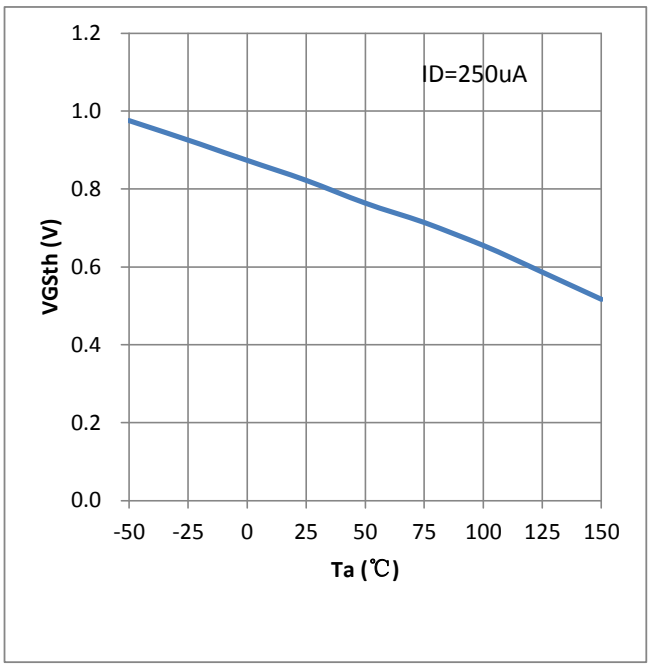
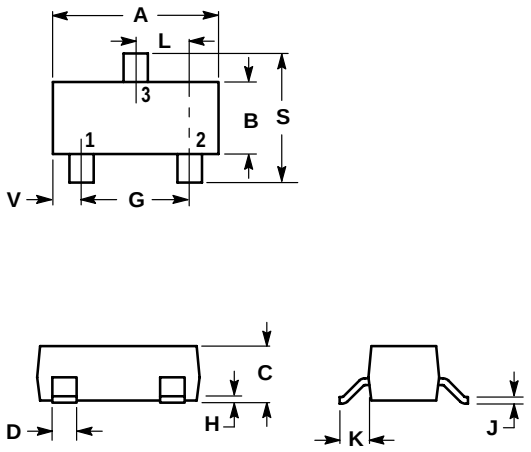


FIG.8 VTH vs. Junction Temperature

LN2302LT1G

SOT–23



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60