

74HC138; 74HCT138

3-to-8 line decoder/demultiplexer; inverting

Rev. 6 — 28 December 2015

Product data sheet

1. General description

The 74HC138; 74HCT138 decodes three binary weighted address inputs (A0, A1 and A2) to eight mutually exclusive outputs ($\bar{Y}0$ to $\bar{Y}7$). The device features three enable inputs ($\bar{E}1$, $\bar{E}2$ and E3). Every output will be HIGH unless $\bar{E}1$ and $\bar{E}2$ are LOW and E3 is HIGH. This multiple enable function allows easy parallel expansion to a 1-of-32 (5 to 32 lines) decoder with just four '138' ICs and one inverter. The '138' can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Complies with JEDEC standard no. 7A
- Input levels:
 - ◆ For 74HC138: CMOS level
 - ◆ For 74HCT138: TTL level
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|---|--------|--|----------|
| | Temperature range | Name | Description | Version |
| 74HC138D | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74 HCT138D | | | | |
| 74HC138DB | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SSOP16 | plastic shrink small outline package; 16 leads; body width 5.3 mm | SOT338-1 |
| 74HCT138DB | | | | |



Table 1. Ordering information ...continued

| Type number | Package | | | Version |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74HC138PW | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74HCT138PW | | | | |
| 74HC138BQ | -40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |
| 74HCT138BQ | | | | |

4. Functional diagram

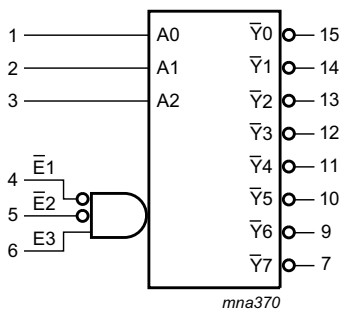


Fig 1. Logic symbol

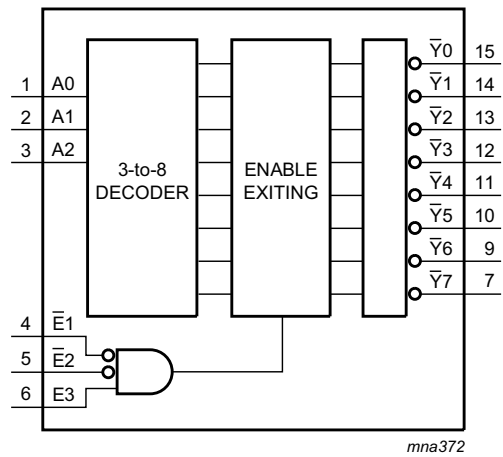


Fig 2. Functional diagram

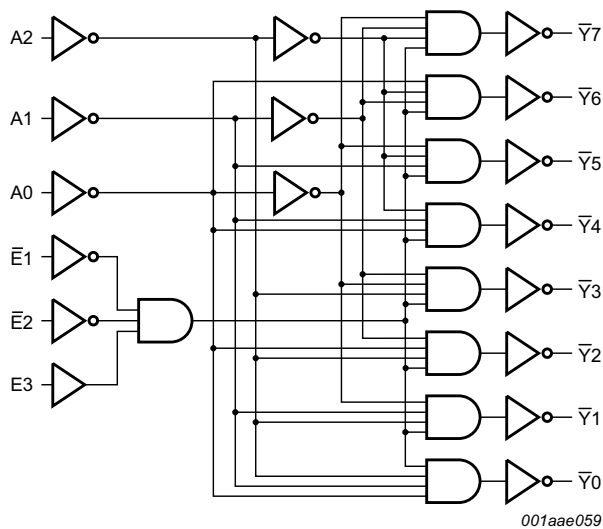
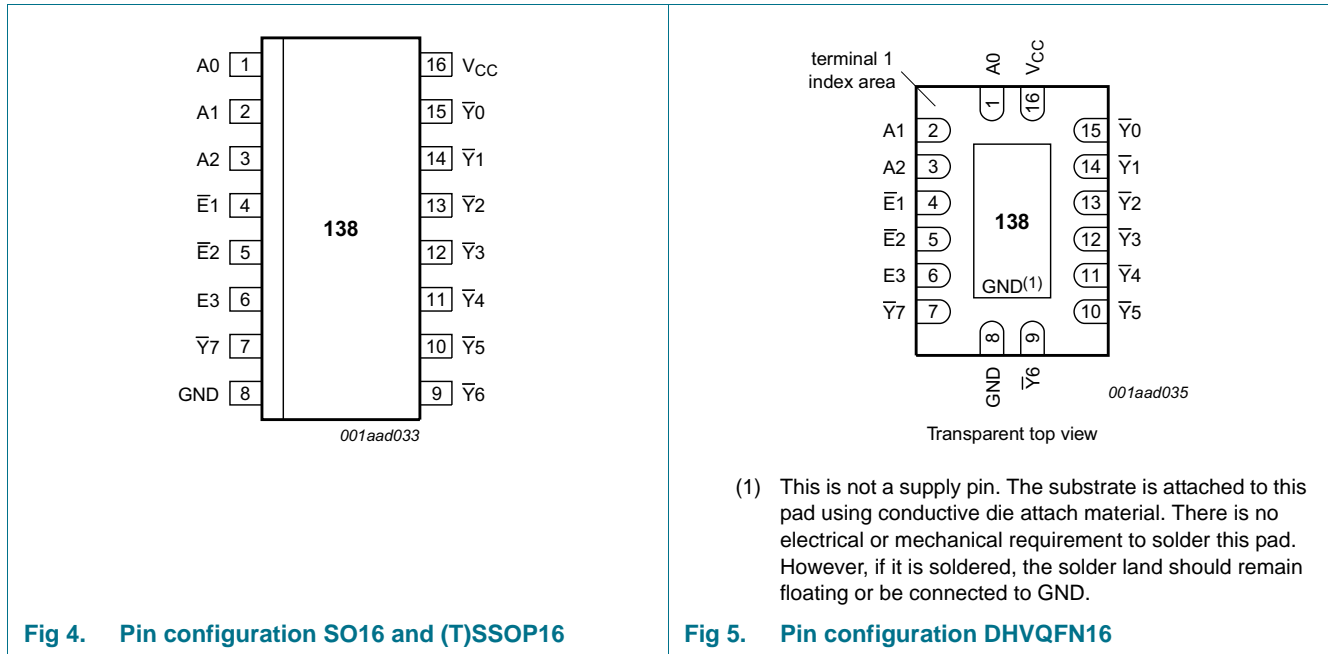


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--|------------------------------|--|
| A0, A1, A2 | 1, 2, 3 | address input A0, A1, A2 |
| $\bar{E}1, \bar{E}2$ | 4, 5 | enable input $\bar{E}1, \bar{E}2$ (active LOW) |
| E3 | 6 | enable input E3 (active HIGH) |
| $\bar{Y}0, \bar{Y}1, \bar{Y}2, \bar{Y}3, \bar{Y}4, \bar{Y}5, \bar{Y}6, \bar{Y}7$ | 15, 14, 13, 12, 11, 10, 9, 7 | output $\bar{Y}0, \bar{Y}1, \bar{Y}2, \bar{Y}3, \bar{Y}4, \bar{Y}5, \bar{Y}6, \bar{Y}7$ (active LOW) |
| GND | 8 | ground (0 V) |
| V _{CC} | 16 | positive supply voltage |

6. Functional description

Table 3. Function table^[1]

| Control | | | Input | | | Output | | | | | | | |
|------------|------------|----|-------|----|----|------------|------------|------------|------------|------------|------------|------------|------------|
| $\bar{E}1$ | $\bar{E}2$ | E3 | A2 | A1 | A0 | $\bar{Y}7$ | $\bar{Y}6$ | $\bar{Y}5$ | $\bar{Y}4$ | $\bar{Y}3$ | $\bar{Y}2$ | $\bar{Y}1$ | $\bar{Y}0$ |
| H | X | X | X | X | X | H | H | H | H | H | H | H | H |
| X | H | X | | | | | | | | | | | |
| X | X | L | | | | | | | | | | | |
| L | L | H | L | L | L | H | H | H | H | H | H | H | L |
| | | | L | L | H | H | H | H | H | H | H | L | H |
| | | | L | H | L | H | H | H | H | H | L | H | H |
| | | | L | H | H | H | H | H | H | L | H | H | H |
| | | | H | L | L | H | H | H | L | H | H | H | H |
| | | | H | L | H | H | H | L | H | H | H | H | H |
| | | | H | H | L | H | L | H | H | H | H | H | H |
| | | | H | H | H | H | H | L | H | H | H | H | H |

- [1] H = HIGH voltage level;
 L = LOW voltage level;
 X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|--------------------------|--|------|----------|------|
| V_{CC} | supply voltage | | -0.5 | +7 | V |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ | - | ± 20 | mA |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ | - | ± 20 | mA |
| I_O | output current | $V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$ | - | ± 25 | mA |
| I_{CC} | quiescent supply current | | - | 50 | mA |
| I_{GND} | ground current | | -50 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | SO16 package [1] | - | 500 | mW |
| | | SSOP16 package [2] | - | 500 | mW |
| | | TSSOP16 package [2] | - | 500 | mW |
| | | DHVQFN16 package [3] | - | 500 | mW |

- [1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
 [2] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
 [3] For DHVQFN16 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | 74HC138 | | | 74HCT138 | | | Unit |
|------------------|-------------------------------------|-------------------------|---------|------|-----------------|----------|------|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | V _{CC} = 6.0 V | - | - | 83 | - | - | - | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | T _{amb} = -40 °C to +85 °C | | T _{amb} = -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|--|--------------------------|------|------|-------------------------------------|------|--------------------------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC138 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| | | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | T _{amb} = -40 °C to +85 °C | | T _{amb} = -40 °C to +125 °C | | Unit |
|------------------|---------------------------|--|--------------------------|------|------|-------------------------------------|-------|--------------------------------------|-------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| C _I | input capacitance | | - | 3.5 | - | | | | | pF |
| 74HCT138 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -20 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 20 μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| ΔI _{CC} | additional supply current | V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A | | | | | | | | |
| | | per input pin; A _n inputs | - | 150 | 540 | - | 675 | - | 735 | μA |
| | | per input pin; \overline{E}_n inputs | - | 125 | 450 | - | 562.5 | - | 612.5 | μA |
| | | per input pin; E ₃ input | - | 100 | 360 | - | 450 | - | 490 | μA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 8](#).

| Symbol | Parameter | Conditions | $T_{amb} = 25\text{ °C}$ | | | $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$ | | $T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ | | Unit |
|-------------------------|-------------------------------|--|--------------------------|-----|-----|---|-----|--|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC138 | | | | | | | | | | |
| t_{pd} | propagation delay | An to \bar{Y}_n ; see Figure 6 ^[1] | | | | | | | | |
| | | $V_{CC} = 2.0\text{ V}$ | - | 41 | 150 | - | 190 | - | 225 | ns |
| | | $V_{CC} = 4.5\text{ V}$ | - | 15 | 30 | - | 38 | - | 45 | ns |
| | | $V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$ | - | 12 | - | - | - | - | - | ns |
| | | $V_{CC} = 6.0\text{ V}$ | - | 12 | 26 | - | 33 | - | 38 | ns |
| | | E3 to \bar{Y}_n ; see Figure 6 ^[1] | | | | | | | | |
| | | $V_{CC} = 2.0\text{ V}$ | - | 47 | 150 | - | 190 | - | 225 | ns |
| | | $V_{CC} = 4.5\text{ V}$ | - | 17 | 20 | - | 38 | - | 45 | ns |
| | | $V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$ | - | 14 | - | - | - | - | - | ns |
| | | $V_{CC} = 6.0\text{ V}$ | - | 14 | 26 | - | 33 | - | 38 | ns |
| | | \bar{E}_n to \bar{Y}_n ; see Figure 7 ^[1] | | | | | | | | |
| | | $V_{CC} = 2.0\text{ V}$ | - | 47 | 150 | - | 190 | - | 225 | ns |
| | | $V_{CC} = 4.5\text{ V}$ | - | 17 | 20 | - | 38 | - | 45 | ns |
| | | $V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$ | - | 14 | - | - | - | - | - | ns |
| $V_{CC} = 6.0\text{ V}$ | - | 14 | 26 | - | 33 | - | 38 | ns | | |
| t_t | transition time | \bar{Y}_n ; see Figure 6 and Figure 7 ^[2] | | | | | | | | |
| | | $V_{CC} = 2.0\text{ V}$ | - | 19 | 75 | - | 95 | - | 110 | ns |
| | | $V_{CC} = 4.5\text{ V}$ | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | $V_{CC} = 6.0\text{ V}$ | - | 6 | 13 | - | 16 | - | 19 | ns |
| C_{PD} | power dissipation capacitance | $C_L = 50\text{ pF}; f = 1\text{ MHz}; V_i = \text{GND to } V_{CC}$ ^[3] | - | 67 | - | - | - | - | - | pF |

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 8](#).

| Symbol | Parameter | Conditions | $T_{amb} = 25\text{ °C}$ | | | $T_{amb} = -40\text{ °C to }+85\text{ °C}$ | | $T_{amb} = -40\text{ °C to }+125\text{ °C}$ | | Unit |
|-----------------|-------------------------------|---|--------------------------|-----|-----|--|-----|---|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HCT138 | | | | | | | | | | |
| t_{pd} | propagation delay | An to \bar{Y}_n ; see Figure 6 ^[1] | | | | | | | | |
| | | $V_{CC} = 4.5\text{ V}$ | - | 20 | 35 | - | 44 | - | 53 | ns |
| | | $V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$ | - | 17 | - | - | - | - | - | ns |
| | | E3 to \bar{Y}_n ; see Figure 6 ^[1] | | | | | | | | |
| | | $V_{CC} = 4.5\text{ V}$ | - | 18 | 40 | - | 50 | - | 60 | ns |
| | | $V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$ | - | 19 | - | - | - | - | - | ns |
| | | \bar{E}_n to \bar{Y}_n ; see Figure 7 ^[1] | | | | | | | | |
| | | $V_{CC} = 4.5\text{ V}$ | - | 19 | 40 | - | 50 | - | 60 | ns |
| | | $V_{CC} = 5\text{ V}; C_L = 15\text{ pF}$ | - | 19 | - | - | - | - | ns | |
| t_t | transition time | \bar{Y}_n ; see Figure 6 and Figure 7 ^[2] | | | | | | | | |
| | | $V_{CC} = 4.5\text{ V}$ | - | 7 | 15 | - | 19 | - | 22 | ns |
| C_{PD} | power dissipation capacitance | $C_L = 50\text{ pF}; f = 1\text{ MHz}; V_i = \text{GND to } V_{CC} - 1.5\text{ V}$ ^[3] | - | 67 | - | - | - | - | - | pF |

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_t is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

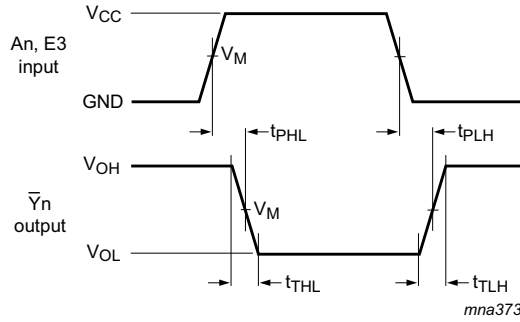
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

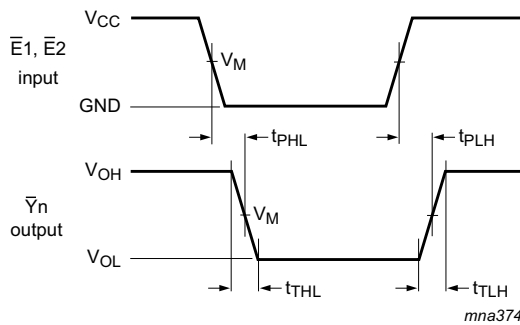
11. Waveforms



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Propagation delay input (A_n) and enable input (E_3) to output (\bar{Y}_n) and transition time output (\bar{Y}_n)



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Propagation delay enable input (\bar{E}_n) to output (\bar{Y}_n) and transition time output (\bar{Y}_n)

Table 8. Measurement points

| Type | Input | Output |
|----------|-------------|-------------|
| | V_M | V_M |
| 74HC138 | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74HCT138 | 1.3 V | 1.3 V |

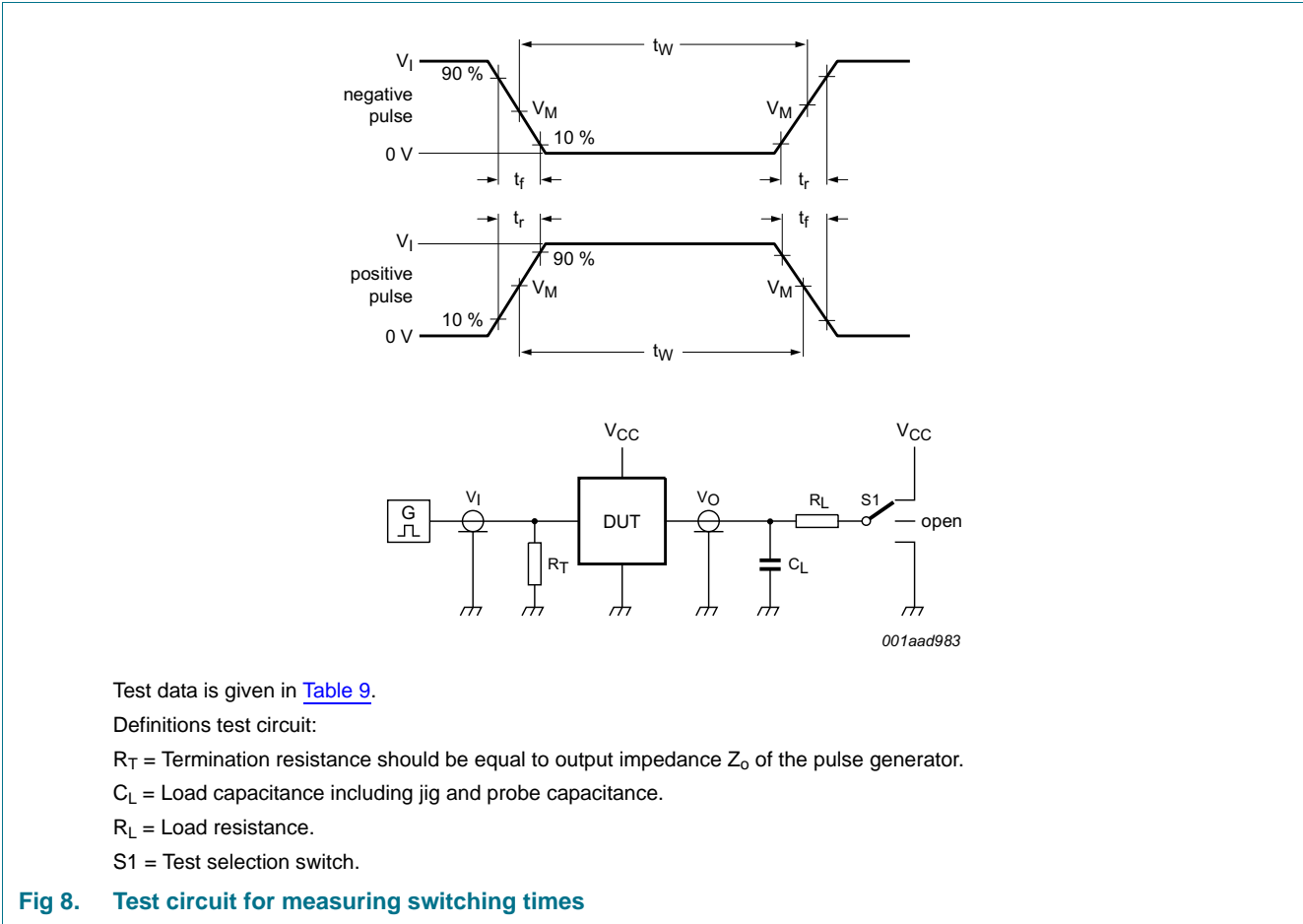


Table 9. Test data

| Type | Input | | Load | | S1 position | | |
|----------|----------|------------|--------------|--------------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 74HC138 | V_{CC} | 6 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |
| 74HCT138 | 3 V | 6 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

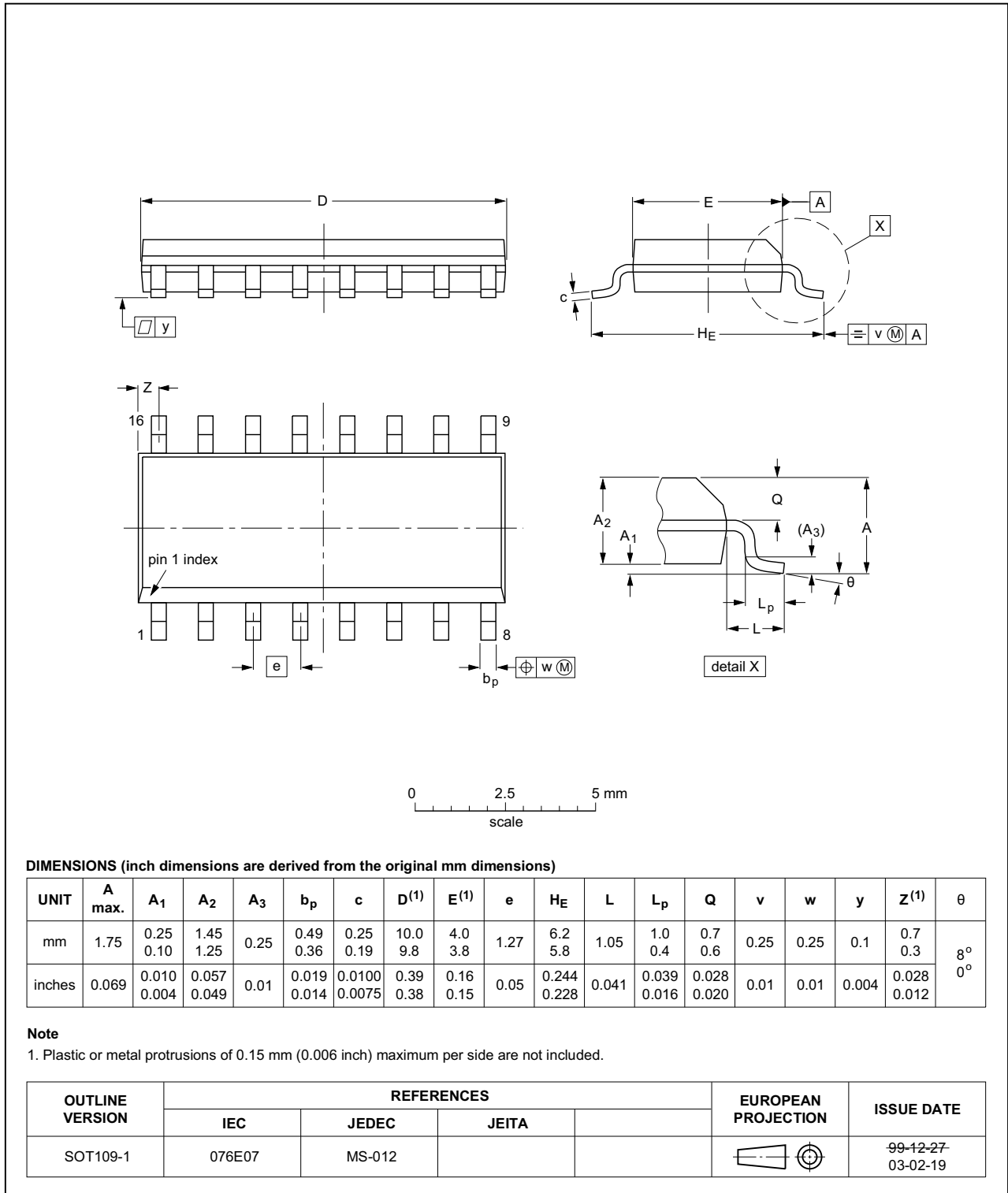


Fig 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

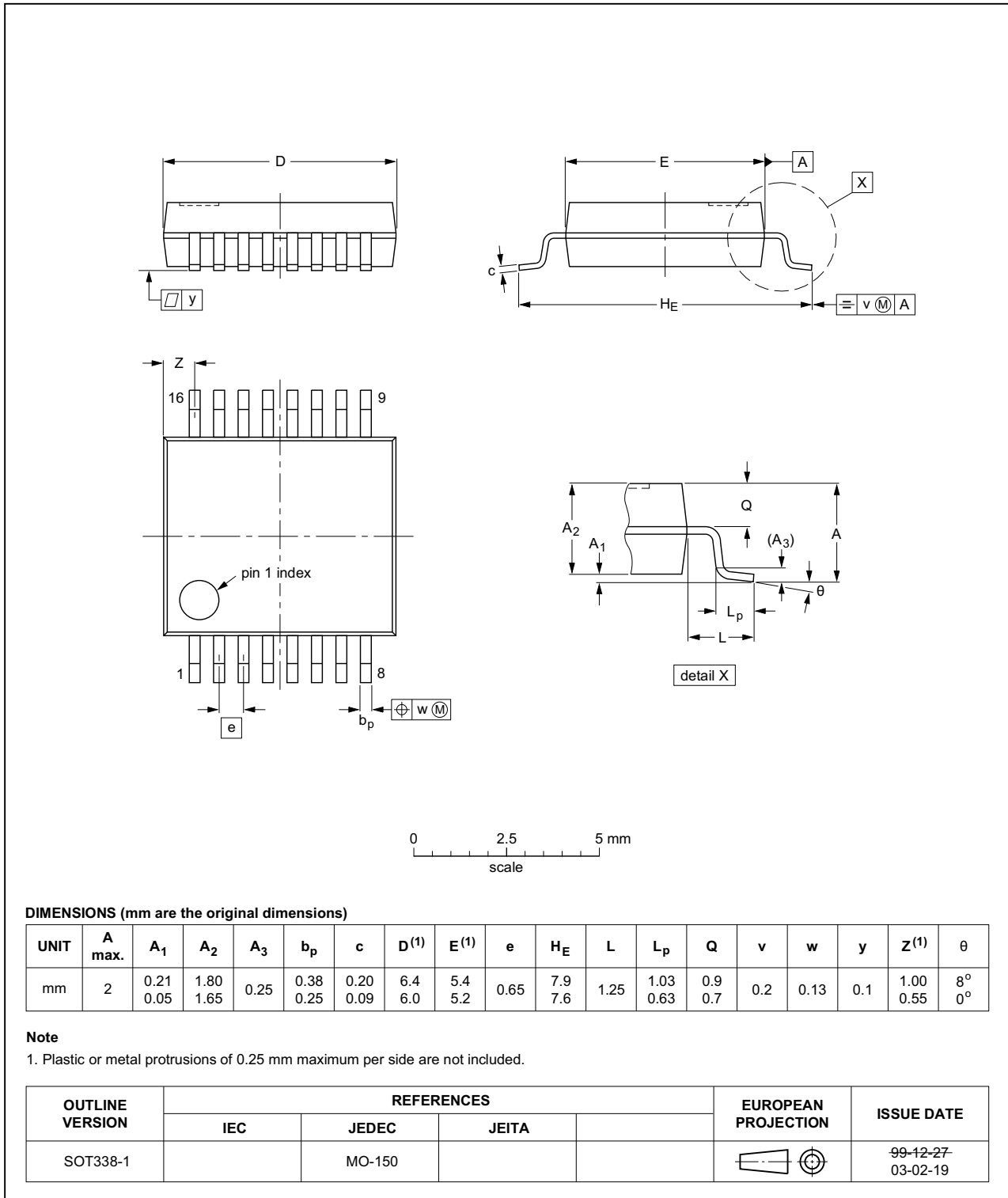


Fig 10. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

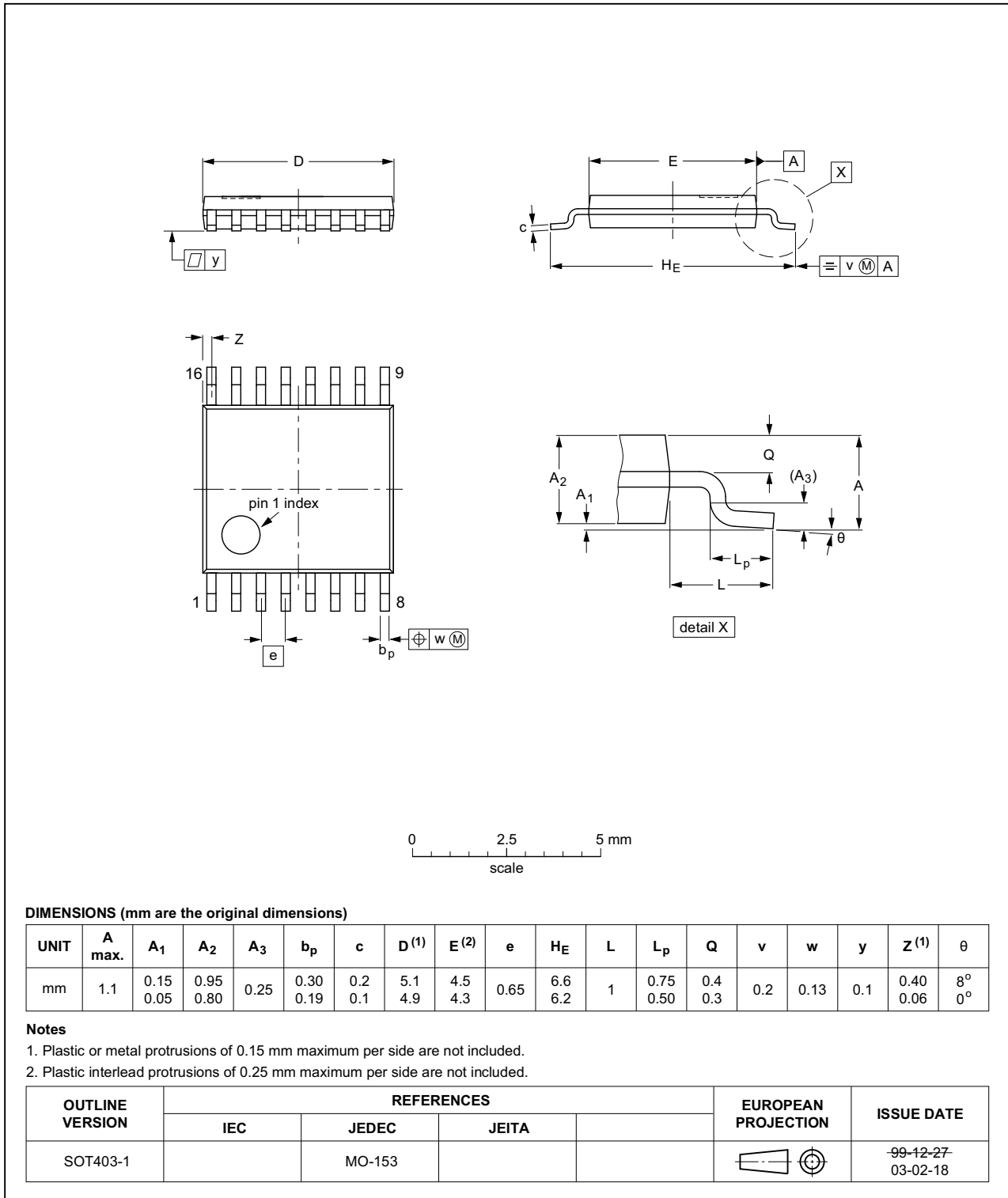


Fig 11. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

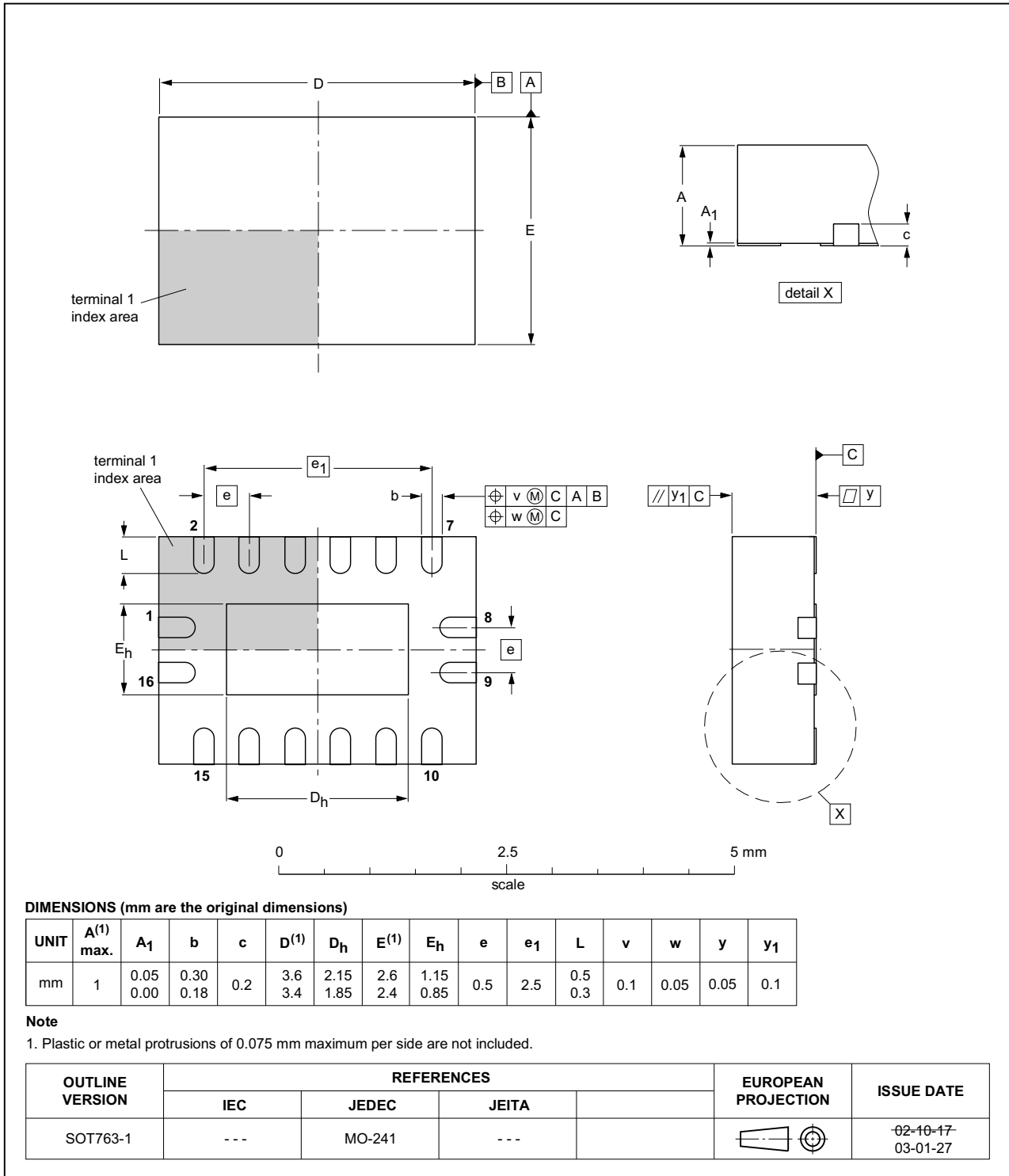


Fig 12. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |
| MM | Machine Model |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------------|--|-----------------------|---------------|---------------------|
| 74HC_HCT138 v.6 | 20151228 | Product data sheet | - | 74HC_HCT138 v.5 |
| Modifications: | <ul style="list-style-type: none"> Type numbers 74HC138N and 74HCT138N (SOT38-4) removed. | | | |
| 74HC_HCT138 v.5 | 20150126 | Product data sheet | - | 74HC_HCT138 v.4 |
| Modifications: | <ul style="list-style-type: none"> Table 6: OFF-state output current removed because device has no 3-state outputs. Table 7: Power dissipation capacitance condition for 74HCT138 is corrected. | | | |
| 74HC_HCT138 v.4 | 20120627 | Product data sheet | - | 74HC_HCT138 v.3 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. SOT38-1 changed to SOT38-4. | | | |
| 74HC_HCT138 v.3 | 20051223 | Product data sheet | - | 74HC_HCT138_CNV v.2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Section 3 "Ordering information", Section 5 "Pinning information" and Section 12 "Package outline": Added DHVQFN package information Section 9 "Static characteristics": Added from the family specification | | | |
| 74HC_HCT138_CNV v.2 | 19970827 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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