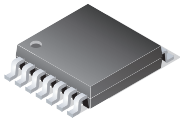
DirectPath™，具有可调节增益的 2VRMS 音频线路驱动器

查询样片: DRV632



特性

- 立体声 **DirectPath™** 音频线路驱动器
  - 在由 **3.3V** 电源供电时，**2Vrms** 进入 **10kΩ** 负载
- 在 **2Vrms** 进入 **10kΩ** 负载时，低总谐波失真 **(THD)+N < 0.01%**
- 高信噪比 **(SNR)**，**> 90dB**
- 可支持 **600Ω** 输出负载
- 差分输入和单端输出
- 由外部增益设定电阻器实现的可调增益
- 低直流偏移，**< 1mV**
- 接地基准输出免除了对于隔直流电容器的需要
  - 减小电路板面积
  - 降低组件成本
  - 改善 **THD+N** 性能
  - 未出现因输出电容器所导致的低频响应性能下降
- 短路保护功能
- 瞬时杂音**(**喀哒声和噼啪声**)**抑制电路
- 外部欠压静音
- 用于实现无杂音音频打开**/**关闭控制的有源静音控制功能
- 节省空间的薄型小外形尺寸 **(TSSOP)** 封装

应用范围

- 机顶盒
- **Blu-ray Disc™**，**DVD** 播放器
- 液晶 **(LCD)** 和等离子 **(PDP)** 电视
- 迷你型**/**微型组合音响系统
- 声卡
- 笔记本电脑

说明

DRV632 是一款 $2V_{RMS}$ 无杂音立体声线路驱动器，此驱动器设计用于去除输出隔直流电容器，以减少组件数目及成本。 对于那些将尺寸和成本作为关键设计参数的单电源电子产品，该器件是理想的选择。

DRV632 的设计运用了 TI 的 DirectPath™ 专利技术，能够在 3.3V 电源电压供电时驱动 $2V_{RMS}$ 进入一个 10kΩ 负载。 此器件具有差分输入，并采用外部增益设置电阻器以支持 ±1V/V 至 ±10V/V 的增益范围，而且可为每个通道单独配置增益。 线路输出具有 ±8kV IEC 静电放电 (ESD) 保护，因而只需要使用一个简单的电阻器-电容器 ESD 保护电路即可。 DRV632 具有针对无杂音音频打开/关闭控制的内置有源静音控制功能。 DRV632 具有一个外部欠压检测器，该欠压检测器在电源被移除时将输出静音，从而确保了无杂音的关断操作。

与产生 $2V_{RMS}$ 输出的传统方法相比，在音频产品中使用 DRV632 能够大幅度地减少组件数量。 DRV632 既不需要采用一个高于 3.3V 的电源来产生其 $5.6V_{pp}$ 输出，也不需要一个分离轨电源。 DRV632 内部集成了电荷泵以产生一个负电源轨，此负电源轨可提供一个良好的无杂音接地偏置 $2V_{RMS}$ 输出。

DRV632 采用 14 引脚 TSSOP 封装。

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE	DESCRIPTION
–40°C to 85°C	DRV632PW	14-Pin

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range

		VALUE	UNIT
	Supply voltage, VDD to GND	–0.3 to 4	V
V_I	Input voltage	V_{SS} – 0.3 to VDD + 0.3	V
R_L	Minimum load impedance – line outputs – OUTL, OUTR	600	Ω
	$\overline{\text{Mute}}$ to GND, UVP to GND	–0.3 to VDD + 0.3	V
T_J	Maximum operating junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature range	–40 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV632 PW 14 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	130	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	49	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	63	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	62	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	n/a	°C/W

(1) 有关传统和全新热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 （文献号：ZHCA543）。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的规定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然对流条件下的结至环境热阻抗。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结至电路板的热阻。
(5) 结至顶部的特征参数，(ψ_{JT})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(6) 结至电路板的特征参数，(ψ_{JB})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到了内容接近的说明。

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
VDD	Supply voltage	DC supply voltage	3	3.3	3.6	V
R_L	Load impedance		0.6	10		kΩ
V_{IL}	Low-level input voltage	$\overline{Mute}$		40		% of VDD
V_{IH}	High-level input voltage	$\overline{Mute}$		60		% of VDD
T_A	Operating free-air temperature		–40	25	85	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage	VDD = 3.3 V		0.5	1	mV
PSRR	Power-supply rejection ratio			80		dB
V_{OH}	High-level output voltage	VDD = 3.3 V	3.1			V
V_{OL}	Low-level output voltage	VDD = 3.3 V			–3.05	V
V_{UVP_EX}	External UVP detect voltage			1.25		V
$V_{UVP\_EX\_HYSTERESIS}$	External UVP detect hysteresis current			5		µA
f_{CP}	Charge pump switching frequency		200	300	400	kHz
$\|I_{IH}\|$	High-level input current, $\overline{Mute}$	VDD = 3.3 V, V_{IH} = VDD			1	µA
$\|I_{IL}\|$	Low-level input current, $\overline{Mute}$	VDD = 3.3 V, V_{IL} = 0 V			1	µA
I_{DD}	Supply current	VDD = 3.3 V, no load, $\overline{Mute}$ = VDD	5	14	25	mA
		VDD = 3.3 V, no load, $\overline{Mute}$ = GND, disabled		14		

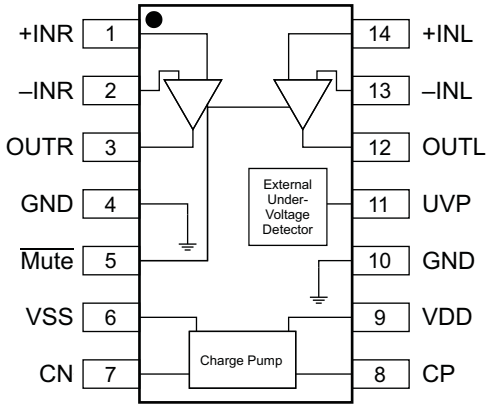
OPERATING CHARACTERISTICS

VDD = 3.3 V, R_{DL} = 10 kΩ, R_{FB} = 30 kΩ, R_{IN} = 15 kΩ, T_A = 25°C, Charge pump: C_P = 1 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage, outputs in phase	THD+N = 1%, VDD = 3.3 V, f = 1 kHz, R_L = 10 kΩ	2	2.4		V_{rms}
THD+N	Total harmonic distortion plus noise	V_O = 2 V_{RMS}, f = 1 kHz		0.002%		
SNR	Signal-to-noise ratio(1)	A-weighted		105		dB
DNR	Dynamic range	A-weighted		105		dB
V_N	Noise voltage	A-weighted		11		µV
Z_O	Output Impedance when muted	$\overline{Mute}$ = GND		110		mΩ
	Input-to-output attenuation when muted	$\overline{Mute}$ = GND		80		dB
	Crosstalk—L to R, R to L	V_O = 1 V_{rms}		–110		dB
I_{LIMIT}	Current limit			25		mA

(1) SNR is calculated relative to 2-Vrms output.

PW PACKAGE
(TOP VIEW)

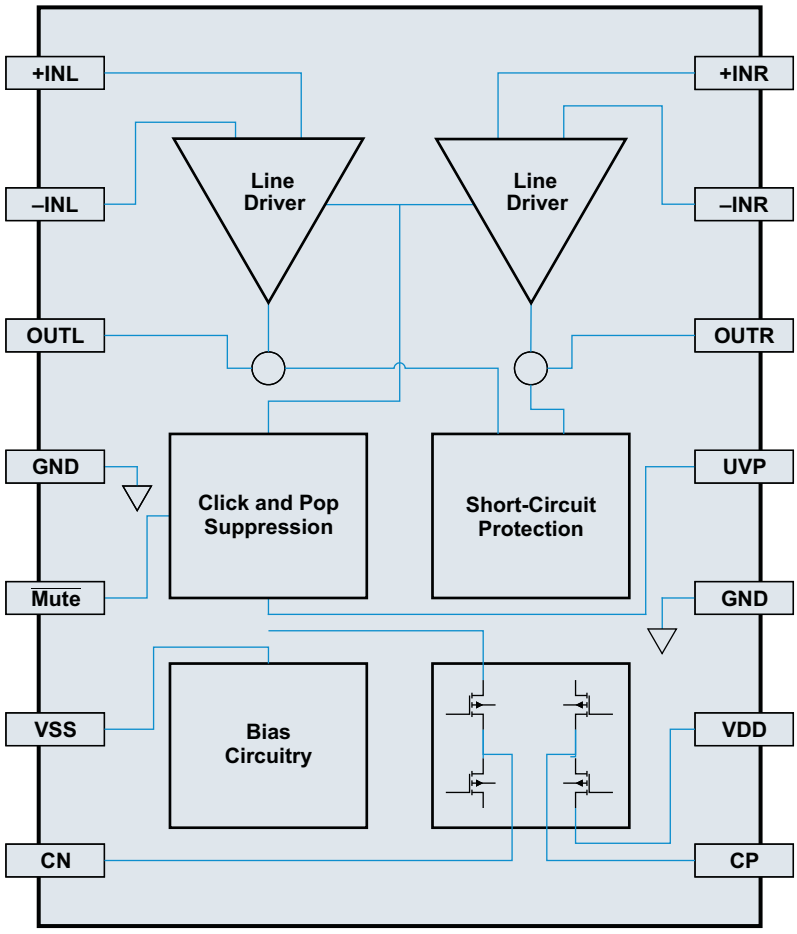


PIN FUNCTIONS

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
CN	7	I/O	Charge-pump flying capacitor negative connection
CP	8	I/O	Charge-pump flying capacitor positive connection
GND	4, 10	P	Ground
–INL	13	I	Left-channel OPAMP negative input
+INL	14	I	Left-channel OPAMP positive input
–INR	2	I	Right-channel OPAMP negative input
+INR	1	I	Right-channel OPAMP positive input
$\overline{\text{Mute}}$	5	I	Mute, active-low
OUTL	12	O	Left-channel OPAMP output
OUTR	3	O	Right-channel OPAMP output
UVP	11	I	Undervoltage protection, internal pullup; unconnected if UVP function is unused.
VDD	9	P	Positive supply
VSS	6	P	Supply voltage

(1) I = input, O = output, P = power

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

VDD = 3.3 V , T_A = 25°C, $C_{(PUMP)}$ = $C_{(VSS)}$ = 1 µF , C_{IN} = 2.2 µF, R_{IN} = 15 kΩ, R_{fb} = 30 kΩ, R_{OUT} = 32 Ω, C_{OUT} = 1 nF (unless otherwise noted)

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE

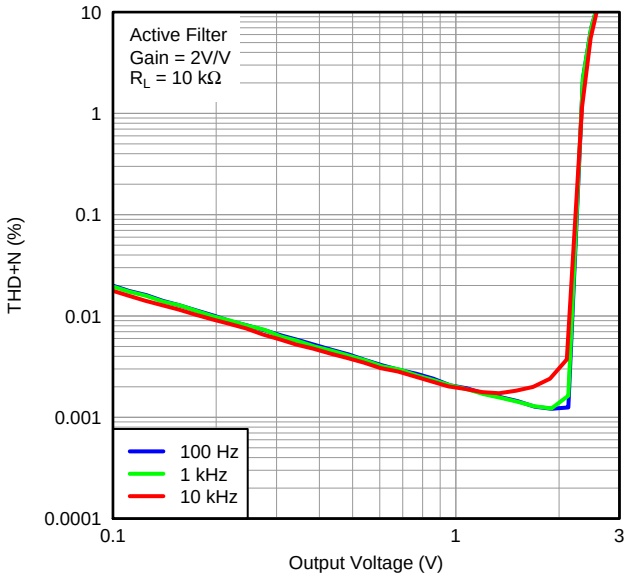


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE

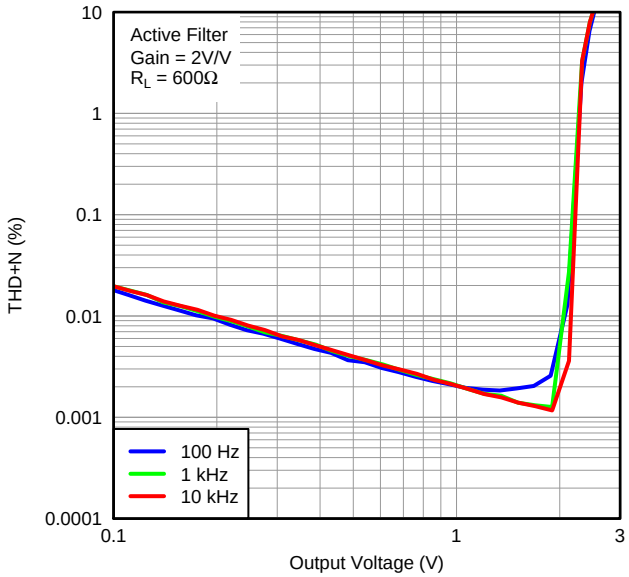


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

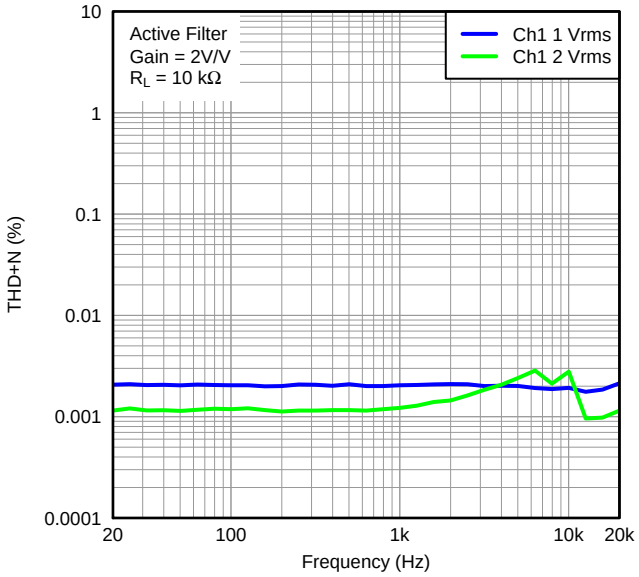


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

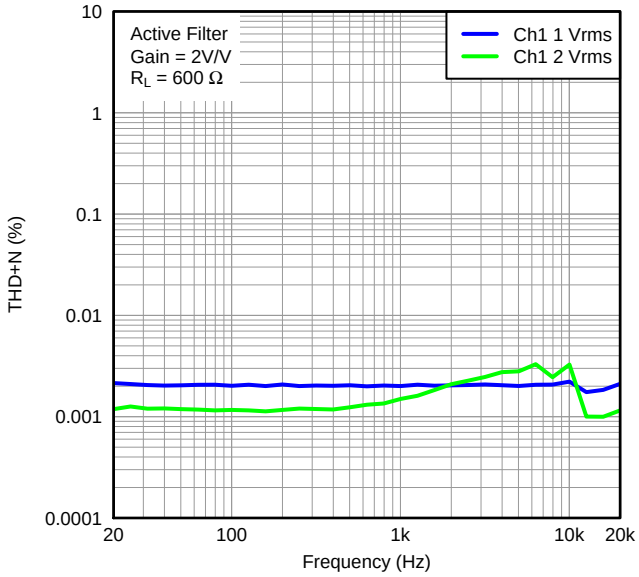


Figure 4.

TYPICAL CHARACTERISTICS (continued)

VDD = 3.3 V , T_A = 25°C, $C_{(PUMP)}$ = $C_{(VSS)}$ = 1 µF , C_{IN} = 2.2 µF, R_{IN} = 15 kΩ, R_{fb} = 30 kΩ, R_{OUT} = 32 Ω, C_{OUT} = 1 nF (unless otherwise noted)

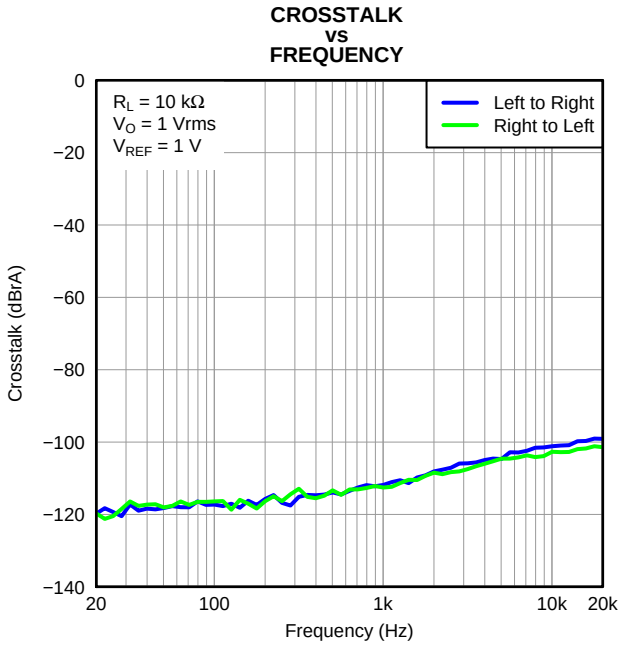


Figure 5.

APPLICATION INFORMATION

LINE DRIVER AMPLIFIERS

Single-supply line-driver amplifiers typically require dc-blocking capacitors. The top drawing in Figure 6 illustrates the conventional line-driver amplifier connection to the load and output signal. DC blocking capacitors are often large in value. The line load (typical resistive values of 600 Ω to 10 kΩ) combines with the dc blocking capacitors to form a high-pass filter. Equation 1 shows the relationship between the load impedance (R_L), the capacitor (C_O), and the cutoff frequency (f_C).

$$f_c = \frac{1}{2\pi R_L C_O} \tag{1}$$

C_O can be determined using Equation 2, where the load impedance and the cutoff frequency are known.

$$C_O = \frac{1}{2\pi R_L f_c} \tag{2}$$

If f_C is low, the capacitor must then have a large value because the load resistance is small. Large capacitance values require large package sizes. Large package sizes consume PCB area, stand high above the PCB, increase cost of assembly, and can reduce the fidelity of the audio output signal.

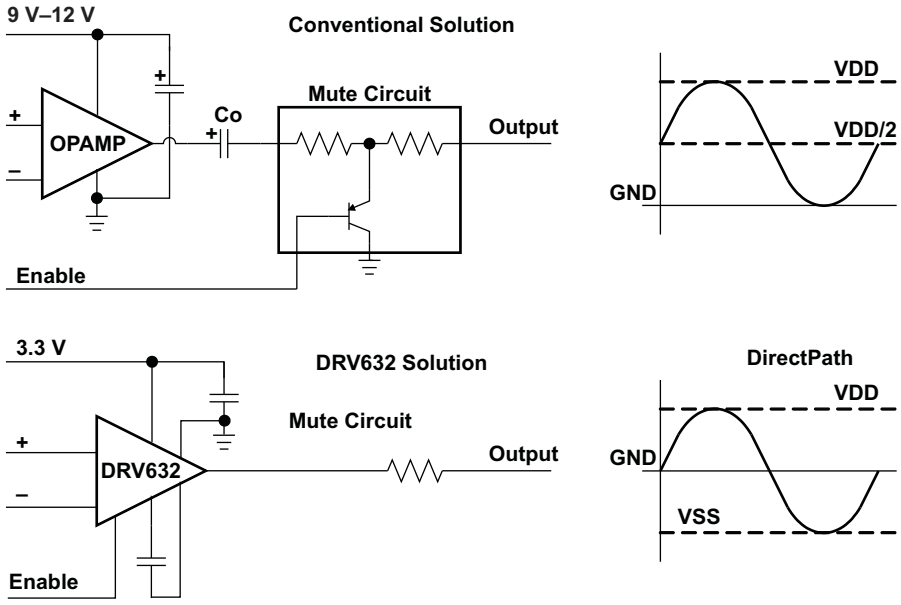


Figure 6. Conventional and DirectPath Line Drivers

The DirectPath amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail. Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split-supply mode. The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. Combining this with the built-in click and pop reduction circuit, the DirectPath amplifier requires no output dc blocking capacitors. The bottom block diagram and waveform of Figure 6 illustrate the ground-referenced line-driver architecture. This is the architecture of the DRV632.

CHARGE-PUMP FLYING CAPACITOR AND PVSS CAPACITOR

The charge-pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge-pump capacitor in order to allow maximum charge transfer. Low-ESR capacitors are an ideal selection, and a value of 1 µF is typical. Capacitor values that are smaller than 1 µF can be used, but the maximum output voltage may be reduced and the device may not operate to specifications. If the DRV632 is used in highly noise-sensitive circuits, it is recommended to add a small LC filter on the VDD connection.

DECOUPLING CAPACITORS

The DRV632 is a DirectPath line-driver amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good, low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 µF, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the DRV632 is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10-µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

GAIN-SETTING RESISTOR RANGES

The gain-setting resistors, R_{IN} and R_{fb}, must be chosen so that noise, stability, and input capacitor size of the DRV632 are kept within acceptable limits. Voltage gain is defined as R_{fb} divided by R_{IN}.

Selecting values that are too low demands a large input ac-coupling capacitor, C_{IN}. Selecting values that are too high increases the noise of the amplifier. Table 1 lists the recommended resistor values for different inverting-input gain settings.

Table 1. Recommended Resistor Values

GAIN	INPUT RESISTOR VALUE, R_{IN}	FEEDBACK RESISTOR VALUE, R_{fb}
–1 V/V	10 kΩ	10 kΩ
–1.5 V/V	8.2 kΩ	12 kΩ
–2 V/V	15 kΩ	30 kΩ
–10 V/V	4.7 kΩ	47 kΩ

USING THE DRV632 AS A SECOND-ORDER FILTER

Several audio DACs used today require an external low-pass filter to remove out-of-band noise. This is possible with the DRV632, as it can be used like a standard operational amplifier. Several filter topologies can be implemented, both single-ended and differential. In Figure 7, multi-feedback (MFB) with differential input and single-ended input are shown.

An ac-coupling capacitor to remove dc content from the source is shown; it serves to block any dc content from the source and lowers the dc gain to 1, helping to reduce the output dc offset to a minimum.

The component values can be calculated with the help of the TI FilterPro™ program available on the TI Web site at:

http://focus.ti.com/docs/toolsw/folders/print/filterpro.html.

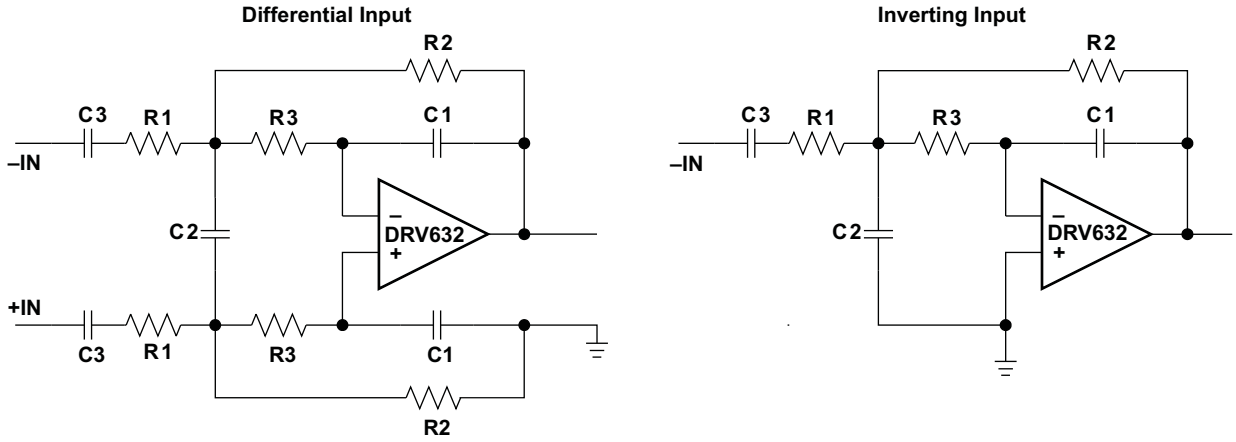


Figure 7. Second-Order Active Low-Pass Filter

The resistor values should have a low value for obtaining low noise, but should also have a high enough value to get a small-size ac-coupling capacitor. With the proposed values of R1 = 15 kΩ, R2 = 30 kΩ, and R3 = 43 kΩ, a dynamic range (DYR) of 106 dB can be achieved with a 1-µF input ac-coupling capacitor.

INPUT-BLOCKING CAPACITORS

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the DRV632. These capacitors block the dc portion of the audio source and allow the DRV632 inputs to be properly biased to provide maximum performance.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using Equation 3. For this calculation, the capacitance used is the input-blocking capacitor, and the resistance is the input resistor chosen from Table 1; then the frequency and/or capacitance can be determined when one of the two values is given.

It is recommended to use electrolytic capacitors or high-voltage-rated capacitors as input blocking capacitors to ensure minimal variation in capacitance with input voltages. Such variation in capacitance with input voltages is commonly seen in ceramic capacitors and can increase low-frequency audio distortion.

$$f_{cIN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad or \quad C_{IN} = \frac{1}{2\pi f_{cIN} R_{IN}} \tag{3}$$

DRV632 UVP OPERATION

The shutdown threshold at the UVP pin is 1.25 V. The customer must use a resistor divider to obtain the shutdown threshold and hysteresis desired for a particular application. The customer-selected thresholds can be determined as follows:

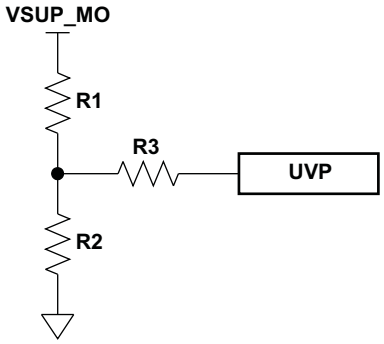
EXTERNAL UNDERVOLTAGE DETECTION

External undervoltage detection can be used to mute/shut down the DRV632 before an input device can generate a pop.

The shutdown threshold at the UVP pin is 1.25 V. The user selects a resistor divider to obtain the shutdown threshold and hysteresis for the specific application. The thresholds can be determined as follows:

V_{UVP} = (1.25 – 6 µA × R3) × (R1 + R2) / R2
Hysteresis = 5 µA × R3 × (R1 + R2) / R2

For example, to obtain V_{UVP} = 3.8 V and 1-V hysteresis, we can use R1 = 3 kΩ, R2 = 1 kΩ, and R3 = 50 kΩ.



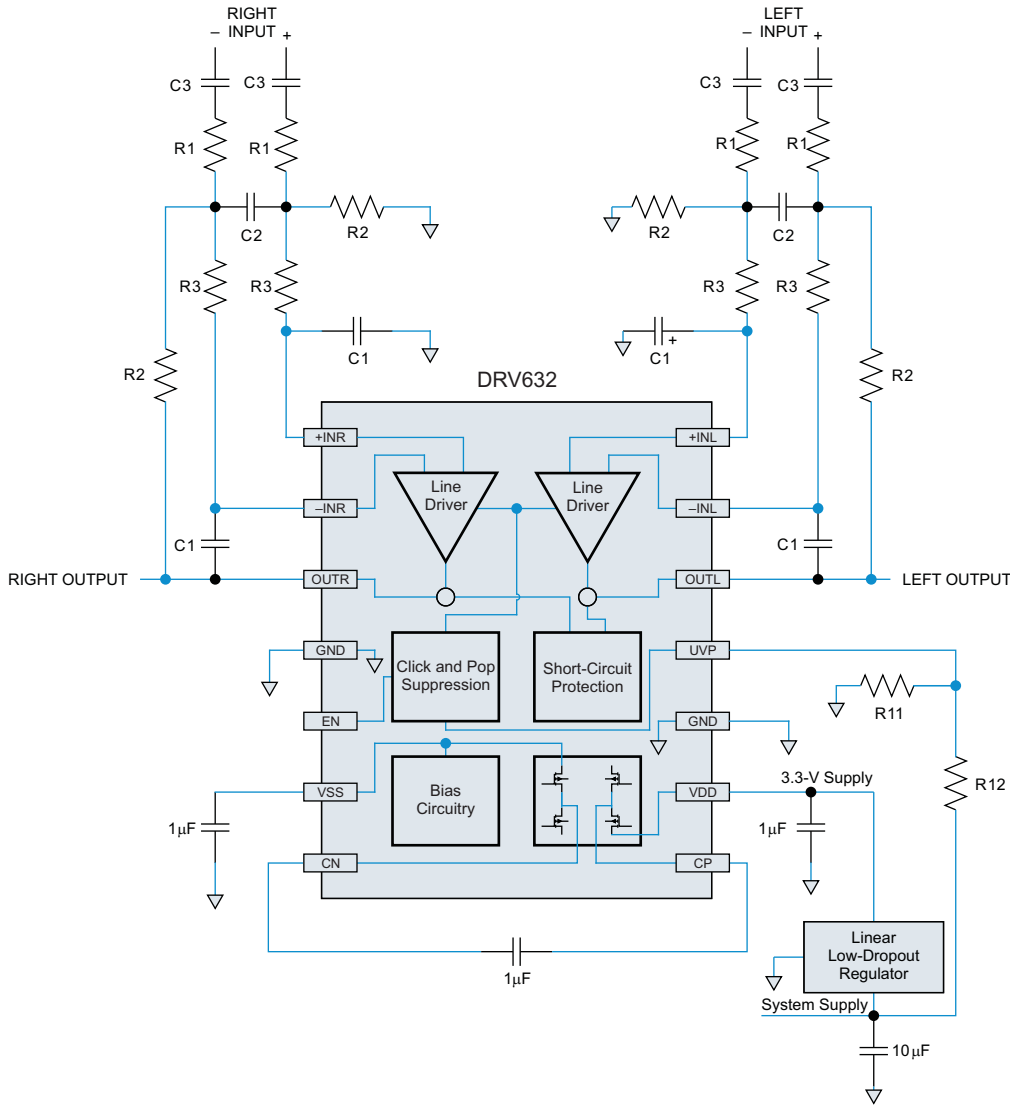
LAYOUT RECOMMENDATIONS

A proposed layout for the DRV632 can be seen in the DRV632EVM User's Guide, and the Gerber files can be downloaded from http://www.ti.com. To access this information, open the DRV632 product folder and look in the Tools and Software folder.

GAIN-SETTING RESISTORS

The gain-setting resistors, R_{IN} and R_{fb}, must be placed close to pins 13 and 17, respectively, to minimize capacitive loading on these input pins and to ensure maximum stability of the DRV632. For the recommended PCB layout, see the DRV632EVM User's Guide.

APPLICATION CIRCUIT



R1 = 15 kΩ, R2 = 30 kΩ, R3 = 43 kΩ, C1 = 47 pF, C2 = 180 pF

Differential-input, single-ended output, second-order filter

REVISION HISTORY

Changes from Original (January 2011) to Revision A **Page**

- Deleted min value for SNR and DNR in *OPERATING CHARACTERISTICS* table 3
- Changed description of UVP in *PIN FUNCTIONS* table 4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV632PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV632	Samples
DRV632PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV632	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

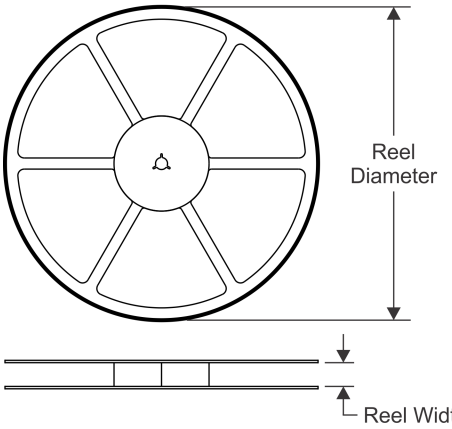
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

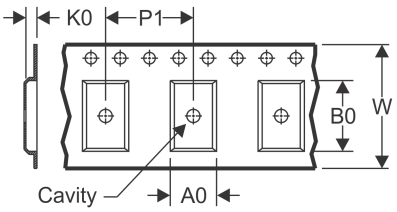
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

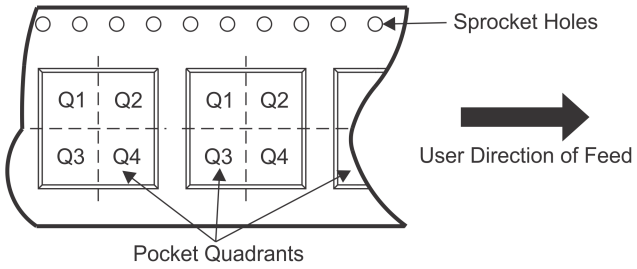


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

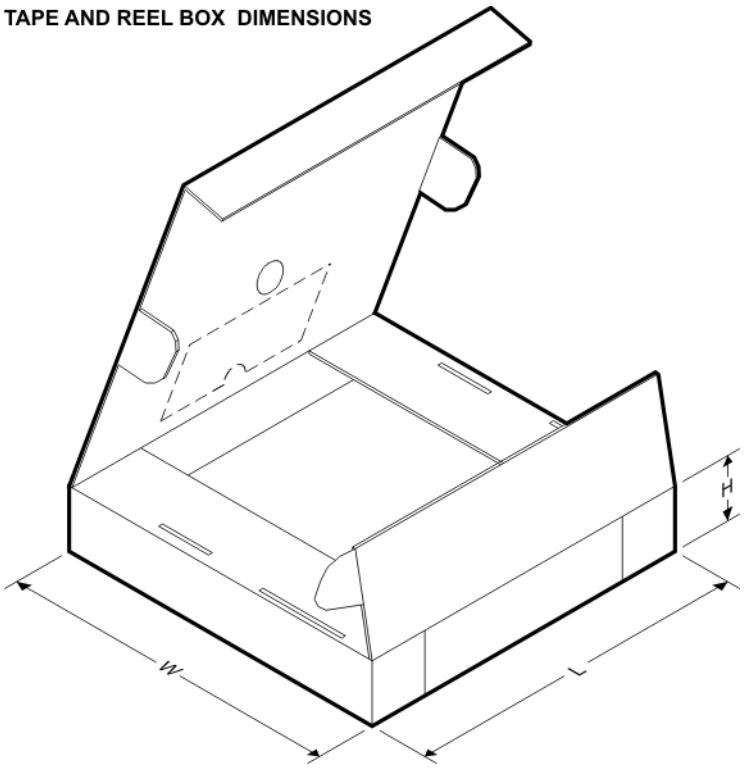
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV632PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

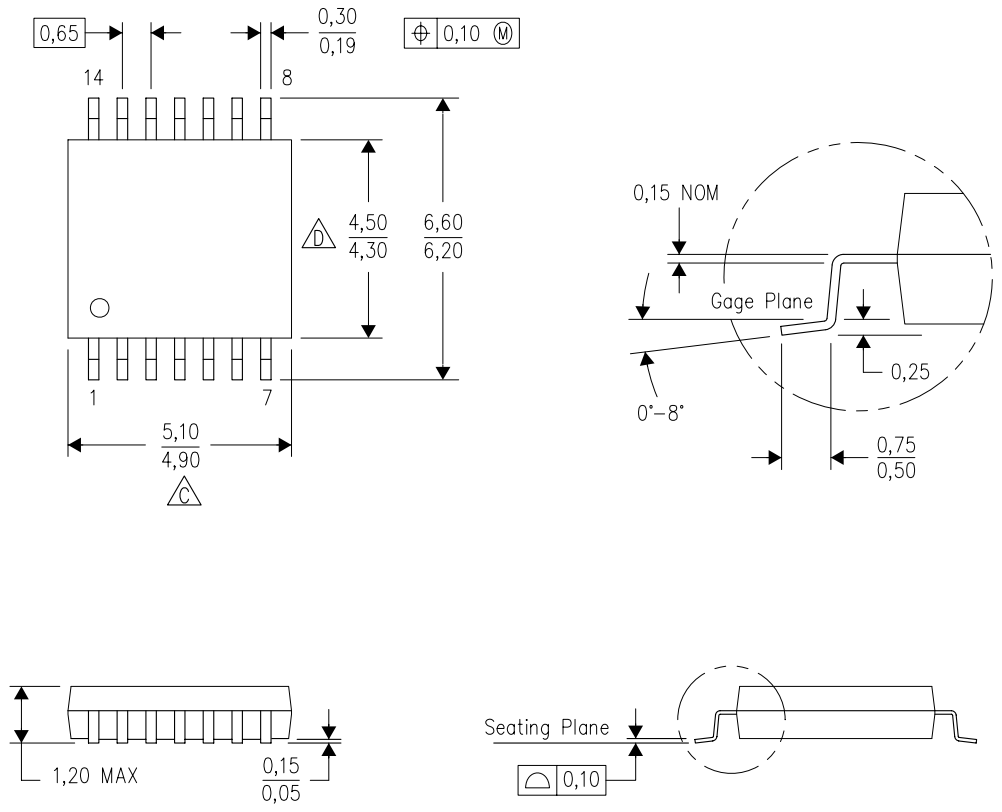
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV632PWR	TSSOP	PW	14	2000	367.0	367.0	38.0

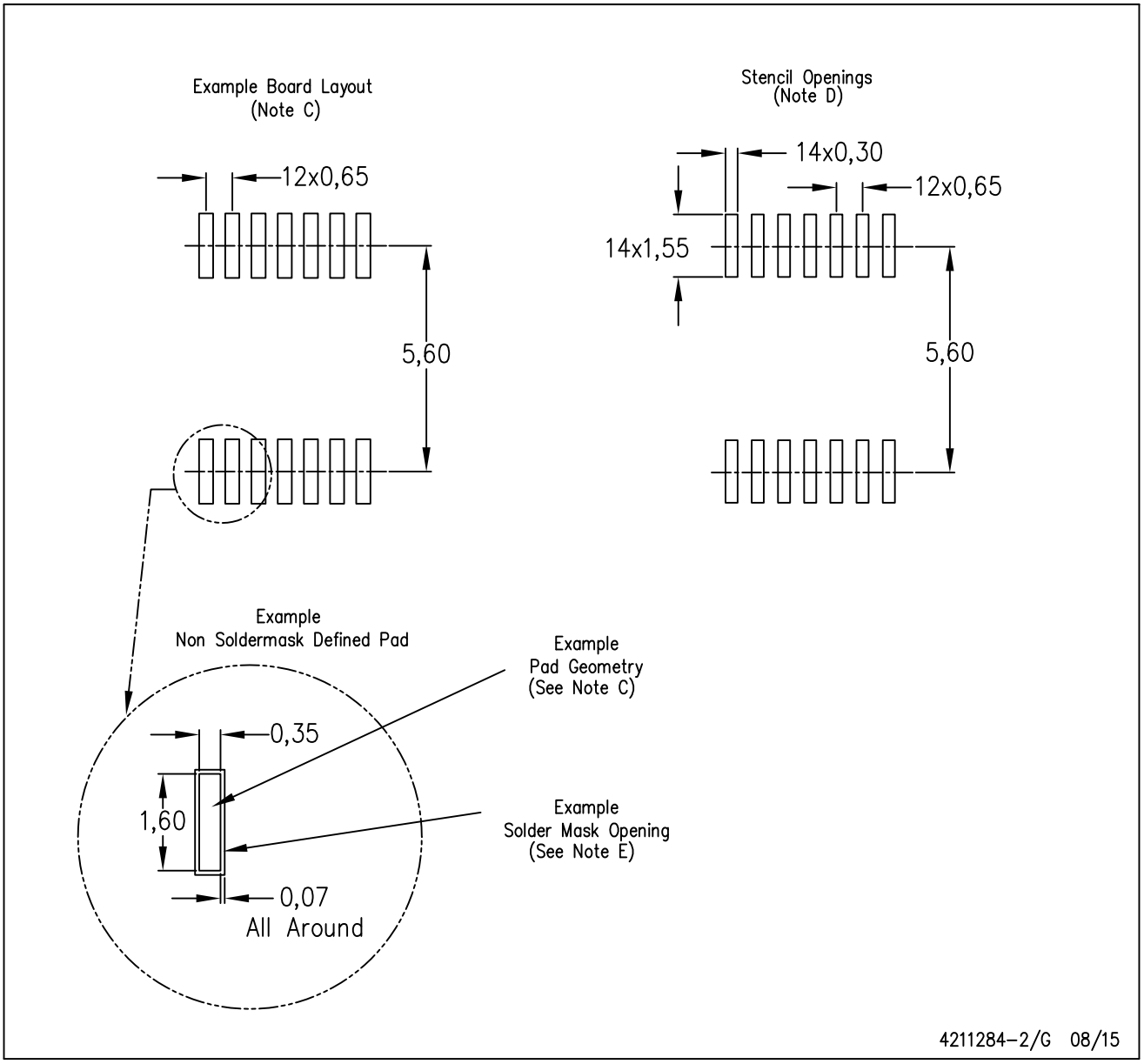
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265