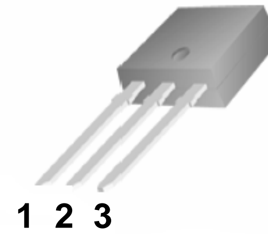
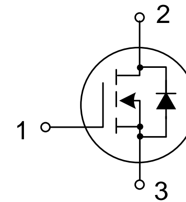
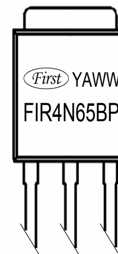
Advanced N-Ch Power MOSFET

PIN Connection TO-251(I-PAK)





Marking Diagram



Y = Year
A = Assembly Location
WW = Work Week
FIR4N65BP = Specific Device Code

General Description

FIR4N65BPGis an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

Features

- 4A,650V,$R_{DS(on)}$（typ）=2.3Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

Absolute Maximum Ratings (Ta = 25°C unless otherwise noted; reference only)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Drain Current	T_C=25°C	I_D	4.0	A
	T_C=100°C		2.8	
Drain Current Pulsed		I_{DM}	16	A
Power Dissipation(T_C=25°C)		P_D	77	W
-Derate above 25°C			0.62	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	202	mJ
Operation Junction Temperature Range		T_J	-55～+150	°C
Storage Temperature Range		T_{stg}	-55～+150	°C

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Thermal Characteristics

Characteristics	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.62	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	110	°C/W

Electrical Characteristics (Ta = 25°C unless otherwise noted; reference only)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	25 °C, V_{GS}=0V, I_D=250μA	650	--	--	V
		125°C, V_{GS}=0V, I_D=250μA	650	--	--	V
Drain-Source Leakage Current	I_{DSS}	25 °C, V_{DS}=650V, V_{GS}=0V	--	--	10	uA
		125°C, V_{DS}=650V, V_{GS}=0V	--	--	50	uA
		150°C, V_{DS}=650V, V_{GS}=0V	--	--	100	uA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=2A	--	2.3	2.7	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ	395.9	514.67	669.07	pF
Output Capacitance	C_{oss}		--	55.83	--	
Reverse Transfer Capacitance	C_{rss}		--	2.46	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=325V,I_D=4.0A, R_G=25Ω (Note 2,3)	--	13.80	--	ns
Turn-on Rise Time	t_r		--	26.60	--	
Turn-off Delay Time	$t_{d(off)}$		--	34.00	--	
Turn-off Fall Time	t_f		--	27.87	--	
Total Gate Charge	Q_g	V_{DS}=520V,I_D=4.0A, V_{GS}=10V (Note 2,3)	--	11.94	--	nC
Gate-Source Charge	Q_{gs}		--	3.23	--	
Gate-Drain Charge	Q_{gd}		--	4.99	--	

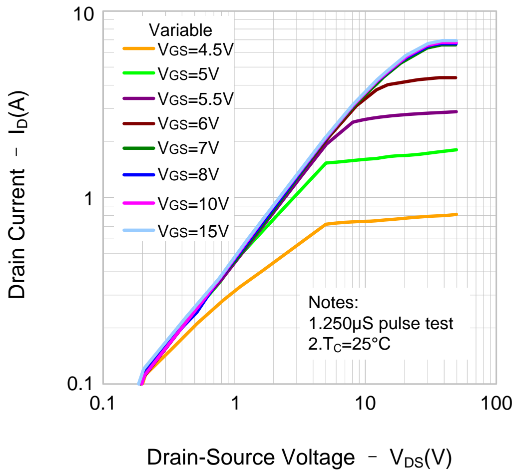
Source-Drain Diode Ratings And Characteristics

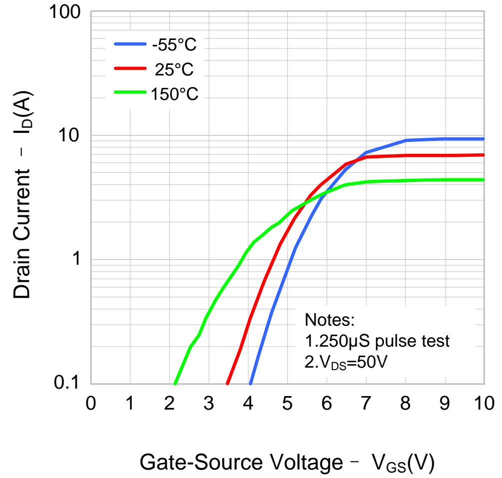
Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	4.0	A
Pulsed Source Current	I_{SM}		--	--	16	
Diode Forward Voltage	V_{SD}	I_S=4.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=4.0A,V_{GS}=0V, dI_F/dt=100A/μs	--	431.00	--	ns
Reverse Recovery Charge	Q_{rr}		--	2.09	--	μC

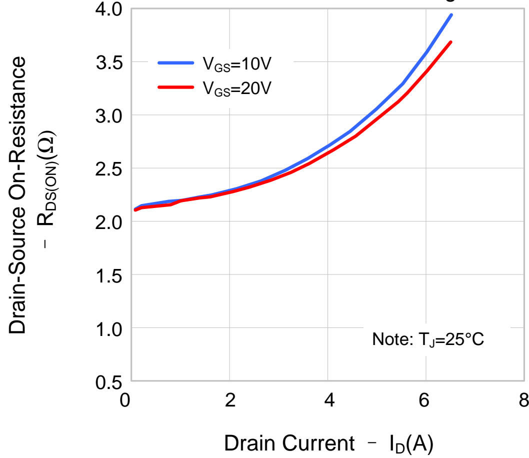
Notes:

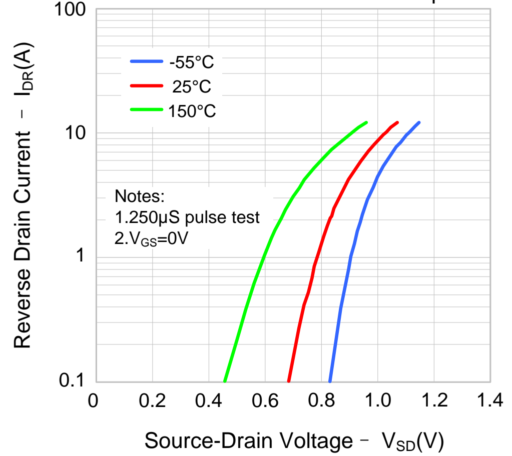
1. L=30mH,I_{AS}=3.36A,V_{DD}=100V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

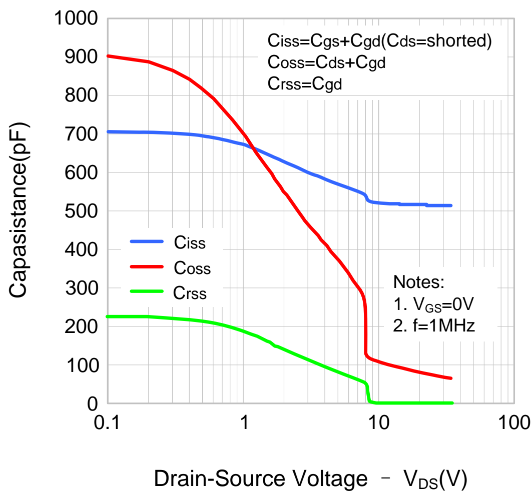
Typical Characteristics

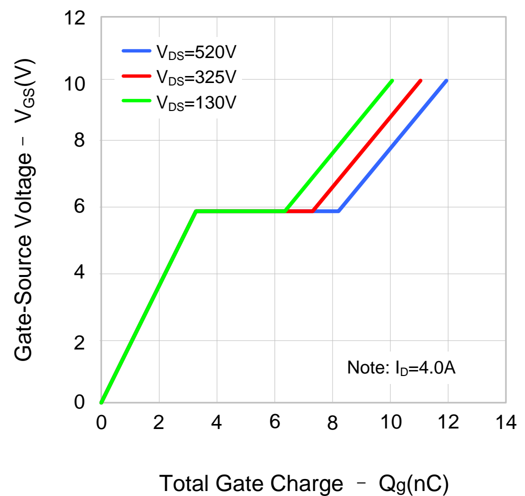












Typical Characteristics(Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

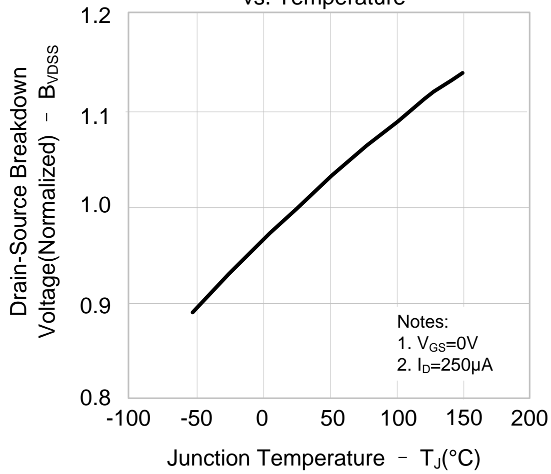


Figure 8. On-resistance Variation vs. Temperature

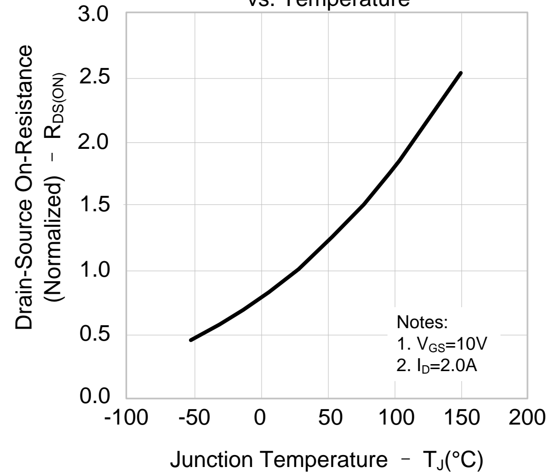


Figure 9 . Max. Safe Operating Area(FIR4N65BPG)

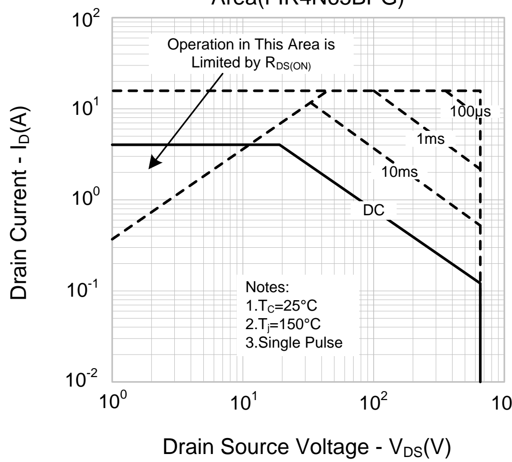
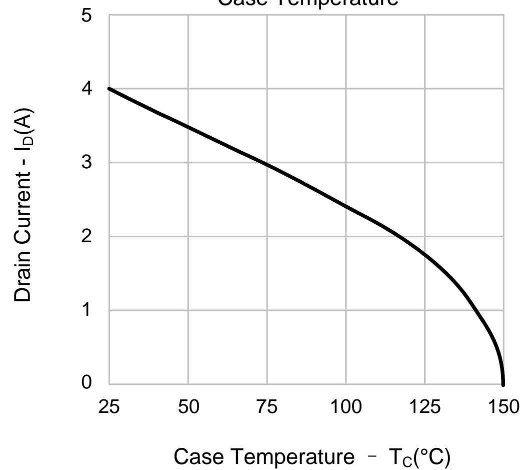
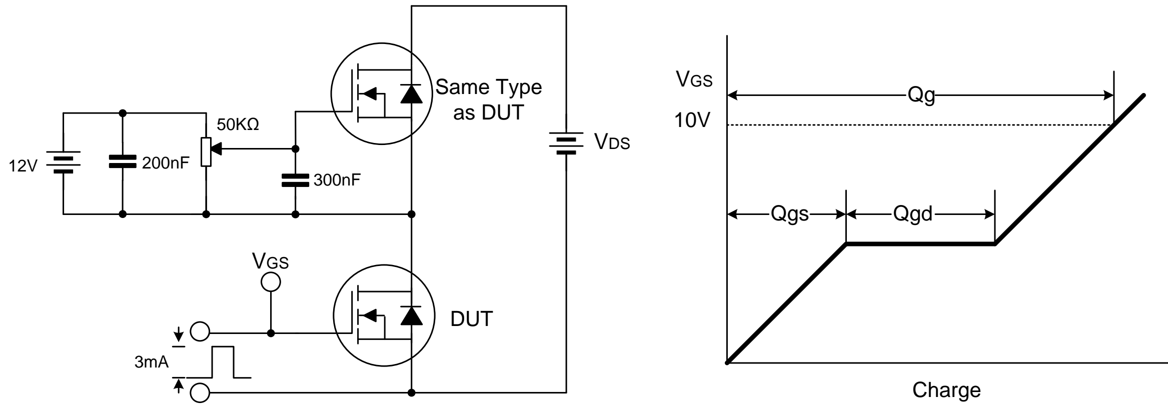


Figure 10. Maximum Drain Current vs. Case Temperature

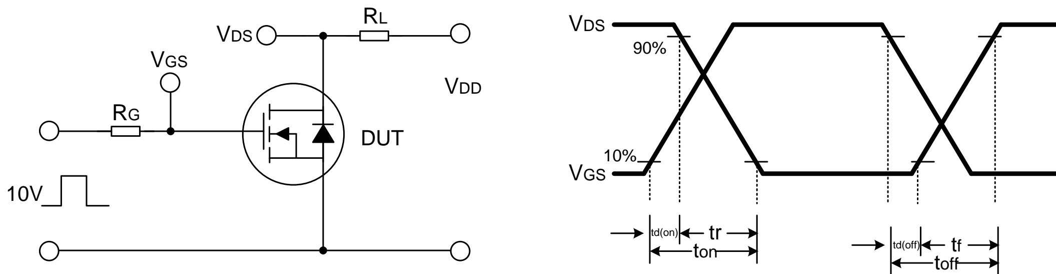


Typical Test Circuit

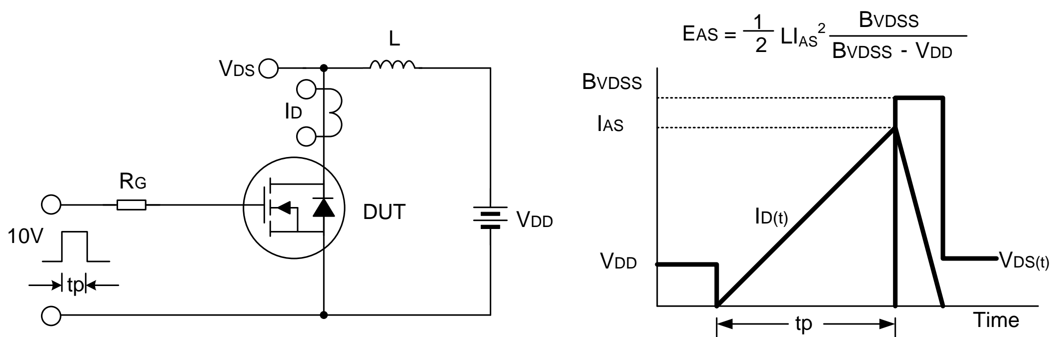
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

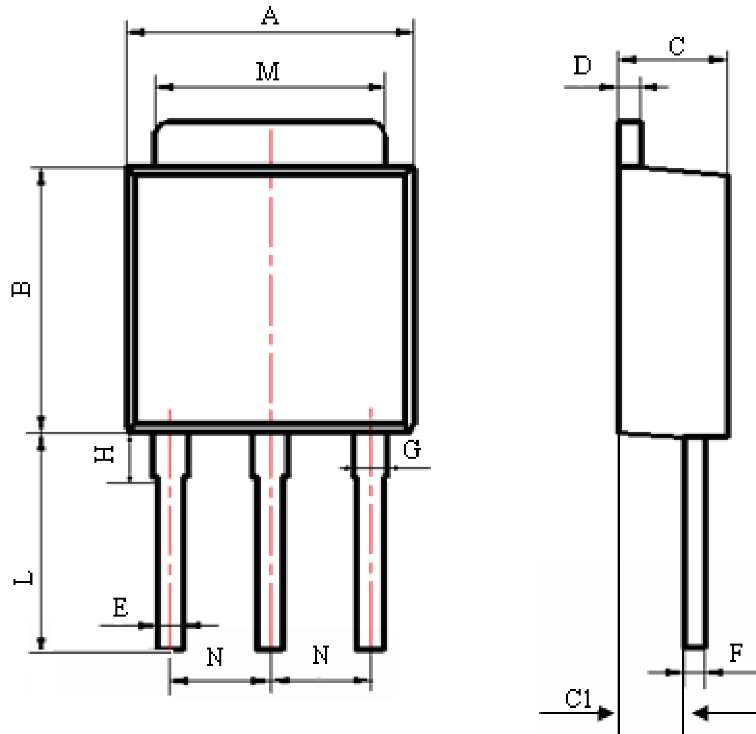


Unclamped Inductive Switching Test Circuit & Waveform



Package Information

TO-251(IPAK)



Items	Values(mm)	
	MIN	MAX
A	6.30	6.80
B	5.20	6.20
C	2.10	2.50
C1	0.85	1.25
D	0.40	0.60
E	0.50	0.70
F	0.40	0.60
G	0.70	0.90
H	1.60	2.40
L	3.50	4.50
M	5.10	5.50
N	2.09	2.49