36V Single Supply, Precision RRO Op-amps With 7MHz Bandwidth

Features

- **Low Offset Voltage: 150μV Maximum**
- **Low Drift: ±0.9μV/°C**
- **Wide Supply Range: 2.7V to 36V**
- **Gain-bandwidth Product: 7MHz**
- **High Slew Rate: 20V/μs**
- **High EMIRR: 84dB at 900MHz**
- **High Common-Mode Rejection: 126dB**
- **High Power Supply Rejection: 130dB**
- **Low Input Bias Current: 3pA Typical**
- **Below-Ground (V-) Input Capability to -0.3V**
- **Rail-to-Rail Output Voltage Range**
- **Pb-Free Packages are Available**
- **–40°C to 125°C Operation Range**
- **Robust 3kV – HBM and 2kV – CDM ESD Rating**

Applications

- Transducer Amplifier
- Bridge Amplifier
- Photodiode Pre-amp
- I/V Converter
- Temperature Measurements
- Strain Gage Amplifier
- Medical Instrumentation

Description

The TP1271/TP1272/TP1274 series are Precision EMI Hardened, high-voltage CMOS op-amps featuring EMIRR of 84dB at 900MHz. TP127X series op amps could operate from ±1.35V to ±18V supplies with excellent performance, They offer very low offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection.

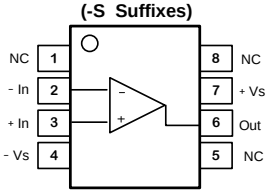
The TP127X are unity gain stable with 100pF capacitive load with a wide 7MHz bandwidth, 20V/μs high slew rate, which makes the device appropriate for I/V converters.

These op amps are ideal for various applications, including process control, industrial and instrumentation equipment, active filtering, data conversion, buffering, and power control and monitoring. Additionally, the TP127X is EMI hardened to minimize any interference, so they are ideal for EMI sensitive application.

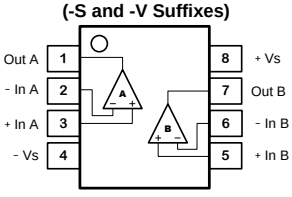
The TP1271 is single channel version available in 8-pin SOIC and 5-pin SOT23 package. The TP1272 is dual channel version available in 8-pin SOIC and MSOP package. The TP1274 is quad channel version available in 14-pin SOIC and TSSOP package.

Pin Configuration (Top View)

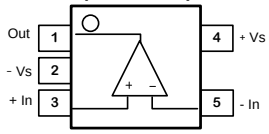
TP1271
8-Pin SOIC
(-S Suffixes)



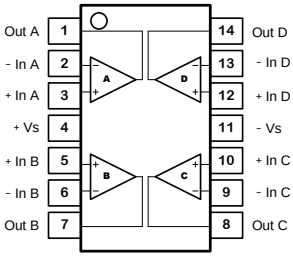
TP1272
8-Pin SOIC/MSOP
(-S and -V Suffixes)



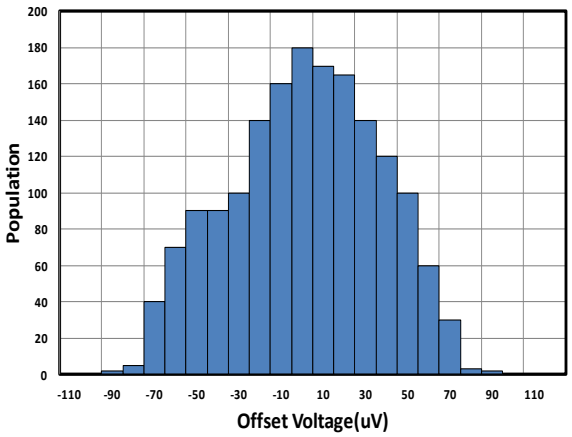
TP1271
5-Pin SOT23
(-T Suffixes)



TP1274
14-Pin SOIC/TSSOP
(-S and -T Suffixes)



Offset Voltage Production Distribution



Order Information

Model Name	Order Number	Package	Transport Media, Quantity	Marking Information
TP1271	TP1271-SR	8-Pin SOIC	Tape and Reel, 4,000	D41
	TP1271-TR	5-Pin SOT23	Tape and Reel, 3,000	D41S
TP1272	TP1272-SR	8-Pin SOIC	Tape and Reel, 4,000	D42S
	TP1272-VR	8-Pin MSOP	Tape and Reel, 3,000	D42V
TP1274	TP1274-SR	14-Pin SOIC	Tape and Reel, 2,500	D44S
	TP1274-TR	14-Pin TSSOP	Tape and Reel, 3,000	D44T

Absolute Maximum Ratings Note 1

Supply Voltage: $V^+ - V^-$ Note 2.....40.0V
Input Voltage..... V^- – 0.3 to V^+ + 0.3
Input Current: +IN, –IN Note 3..... ±20mA
Output Short-Circuit Duration Note 4..... Indefinite
Current at Supply Pins……..... ±60mA

Operating Temperature Range.....–40°C to 125°C
Maximum Junction Temperature..... 150°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The op amp supplies must be established simultaneously, with, or before, the application of any input signals.

Note 3: The inputs are protected by ESD protection diodes to each power supply. If the input extends more than 500mV beyond the power supply, the input current should be limited to less than 10mA.

Note 4: A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8	3	kV
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Thermal Risistance

Package Type	θ_{JA}	θ_{JC}	Unit
5-Pin SOT23	250	81	℃/W
8-Pin SOIC	158	43	℃/W
8-Pin MSOP	210	45	℃/W
14-Pin SOIC	120	36	℃/W
14-Pin TSSOP	180	35	℃/W

Electrical Characteristics

The specifications are at T_A = 27°C. V_{SUPPLY} = ±15V, V_{CM} = V_{OUT} =0V, R_L = 2kΩ, C_L =100pF.Unless otherwise noted.

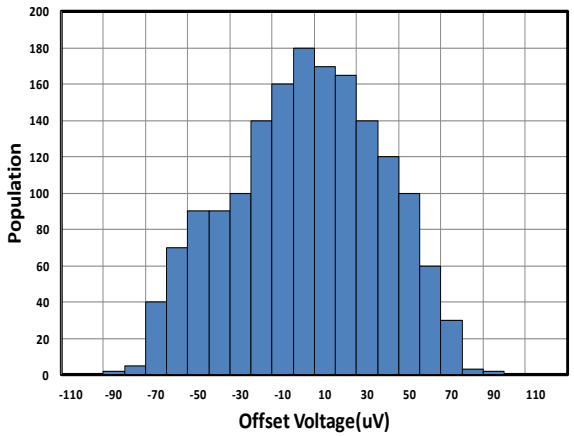
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{CM} = V_{DD}/2	-150	±50	+150	μV
V_{OS} TC	Input Offset Voltage Drift	-40°C to 125°C		0.9		μV/°C
I_B	Input Bias Current	T_A = 27 °C		3		pA
		T_A = 85 °C		250		pA
		T_A = 125 °C		7.7		nA
I_{OS}	Input Offset Current			0.001		pA
V_n	Input Voltage Noise	f = 0.1Hz to 10Hz		2.35		$μV_{RMS}$
e_n	Input Voltage Noise Density	f = 1kHz		19		nV/√Hz
C_{IN}	Input Capacitance	Differential Common Mode		4 2.5		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = -14.6V to 13V		126		dB
V_{CM}	Common-mode Input Voltage Range		V^- -0.3		V^+-2.0	V
PSRR	Power Supply Rejection Ratio			130		dB
A_{VOL}	Open-Loop Large Signal Gain	R_{LOAD} = 2kΩ	100	118		dB
V_{OL}, V_{OH}	Output Swing from Supply Rail	R_{LOAD} = 100kΩ		50		mV
R_{OUT}	Closed-Loop Output Impedance	G = 1, f =1kHz, I_{OUT} = 0		0.01		Ω
R_O	Open-Loop Output Impedance	f = 1kHz, I_{OUT} = 0		125		Ω
I_{SC}	Output Short-Circuit Current	Sink or source current		80		mA
V_{DD}	Supply Voltage		2.7		36	V
I_Q	Quiescent Current per Amplifier			900		μA
PM	Phase Margin	R_{LOAD} = 2kΩ, C_{LOAD} = 100pF		60		°
GM	Gain Margin	R_{LOAD} = 2kΩ, C_{LOAD} = 100pF		8		dB
GBWP	Gain-Bandwidth Product	f = 1kHz		7		MHz
SR	Slew Rate	A_V = 1, V_{OUT} = 0V to 10V, C_{LOAD} = 100pF, R_{LOAD} = 2kΩ		20		V/μs
FPBW	Full Power Bandwidth Note 1			210		kHz
t_S	Settling Time, 0.1% Settling Time, 0.01%	A_V = –1, 10V Step		1 1		μs
THD+N	Total Harmonic Distortion and Noise	f = 1kHz, A_V =1, R_L = 2kΩ, V_{OUT} = $3.5V_{RMS}$		0.0001		%
X_{talk}	Channel Separation	f = 1kHz, R_L = 2kΩ		110		dB

Note 1: Full power bandwidth is calculated from the slew rate FPBW = SR/π • V_{P-P}

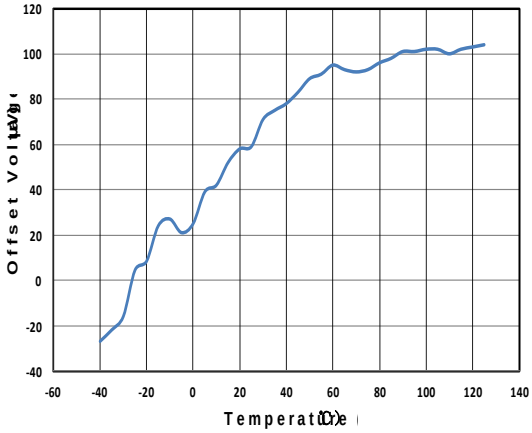
Typical Performance Characteristics

VS = ±15V, VCM = 0V, RL = Open, unless otherwise specified.

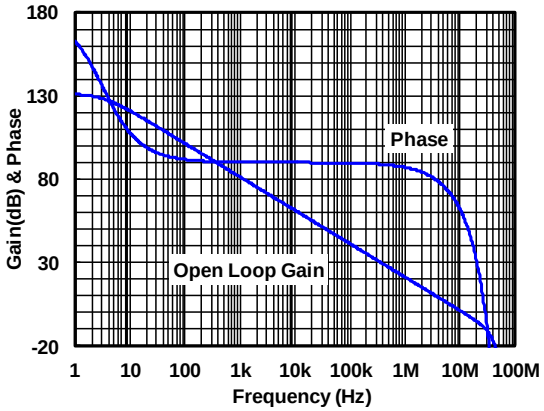
Offset Voltage Production Distribution



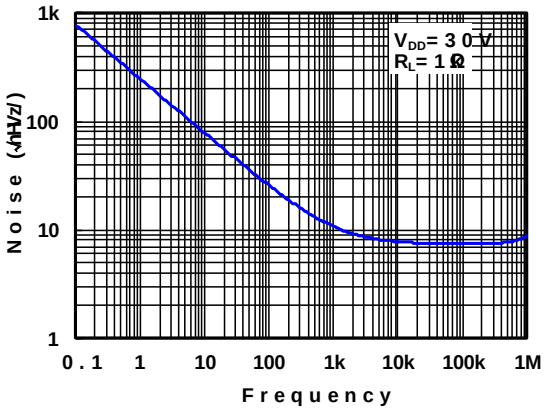
Offset Voltage vs. Temperature



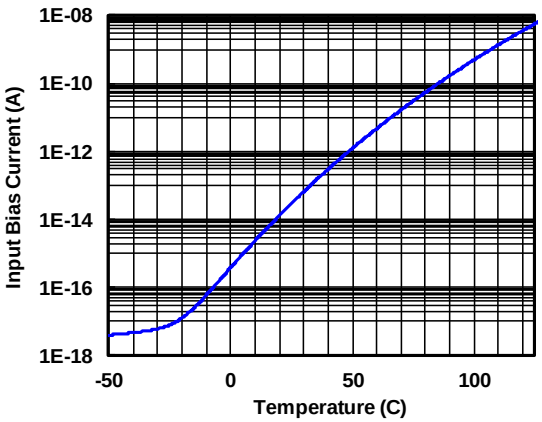
Open-Loop Gain and Phase



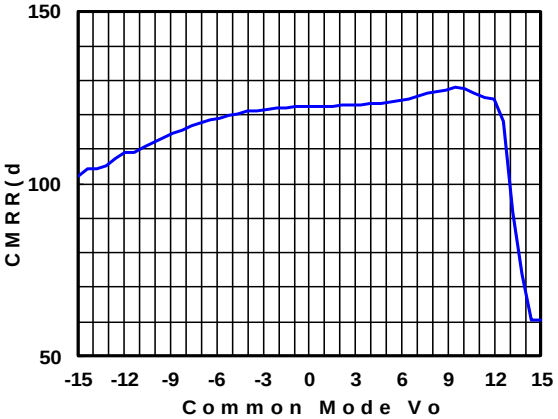
Input Voltage Noise Spectral Density



Input Bias Current vs. Temperature



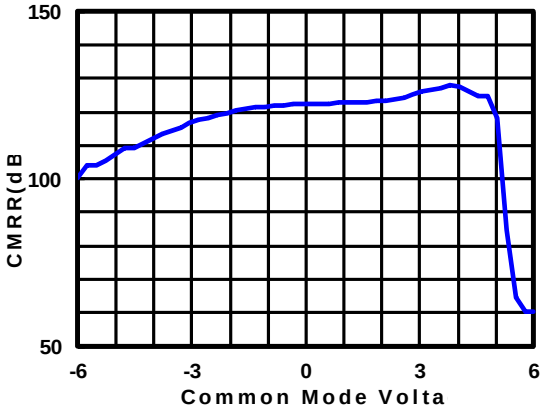
Input Bias Current vs. Input Common Mode Voltage



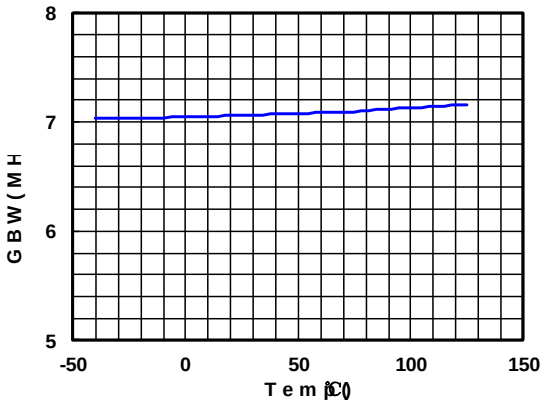
Typical Performance Characteristics

VS = ±15V, VCM = 0V, RL = Open, unless otherwise specified.(Continue)

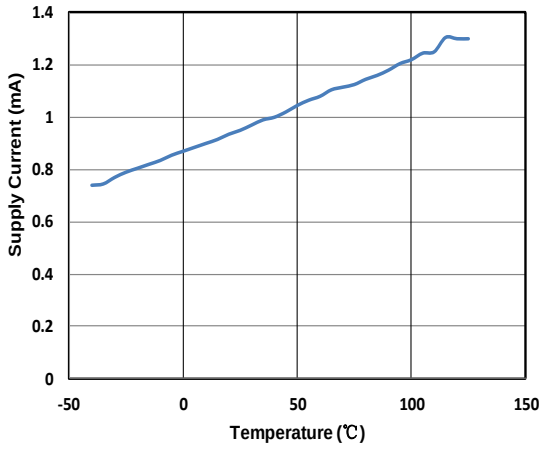
Common Mode Rejection Ratio



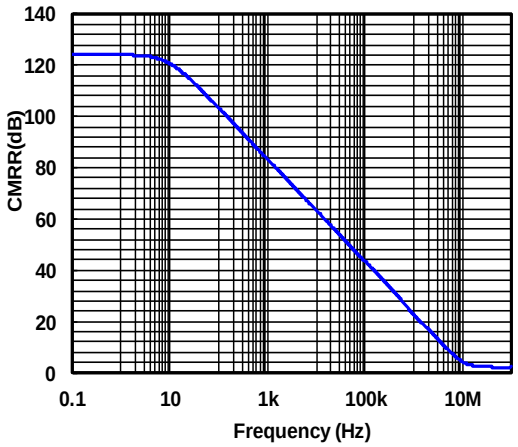
Unity Gain Bandwidth vs. Temperature



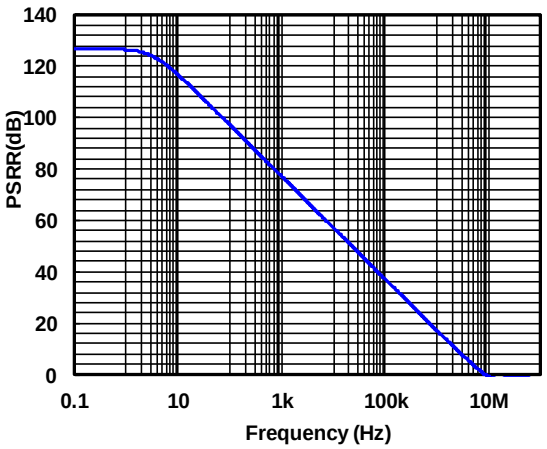
Quiescent Current vs. Temperature



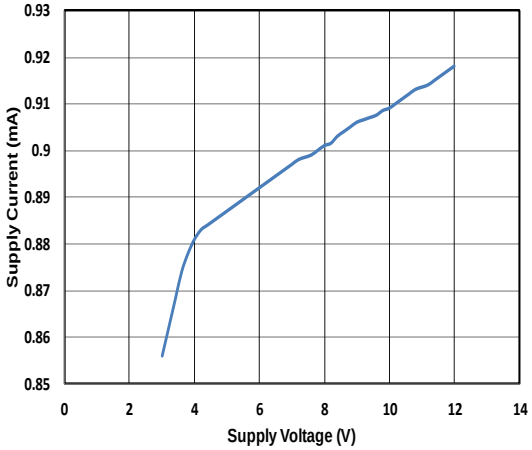
CMRR vs. Frequency



Power-Supply Rejection Ratio



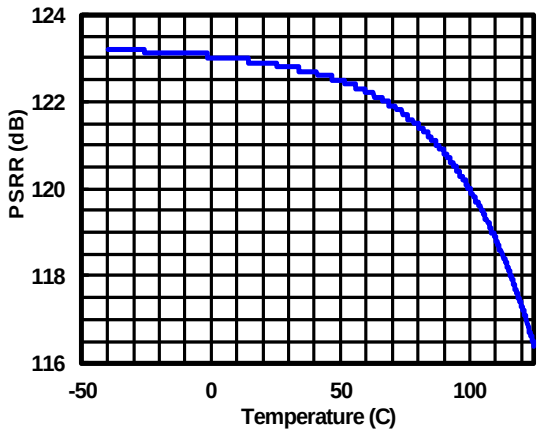
Quiescent Current vs. Supply Voltage



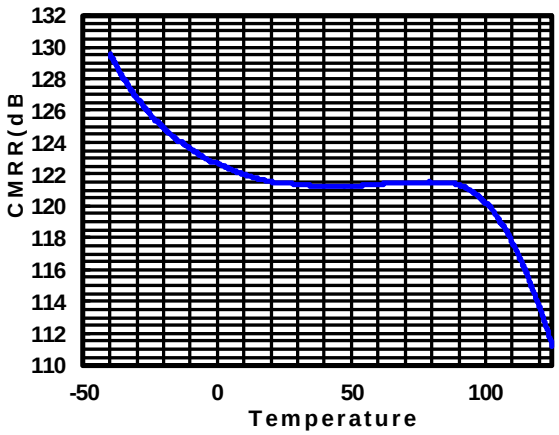
Typical Performance Characteristics

VS = ±15V, VCM = 0V, RL = Open, unless otherwise specified.(Continue)

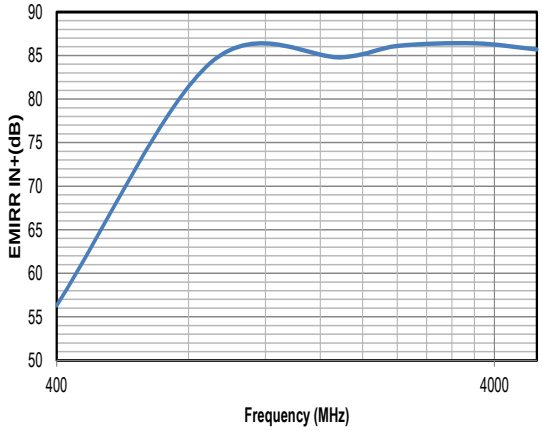
Power-Supply Rejection Ratio vs. Temperature



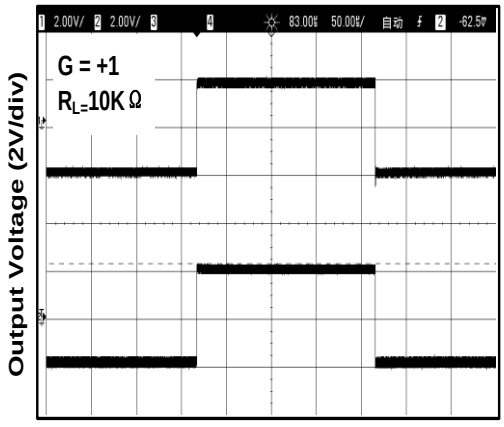
CMRR vs. Temperature



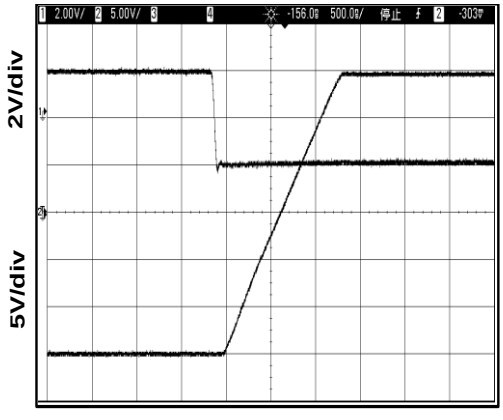
EMIRR IN+ vs. Frequency



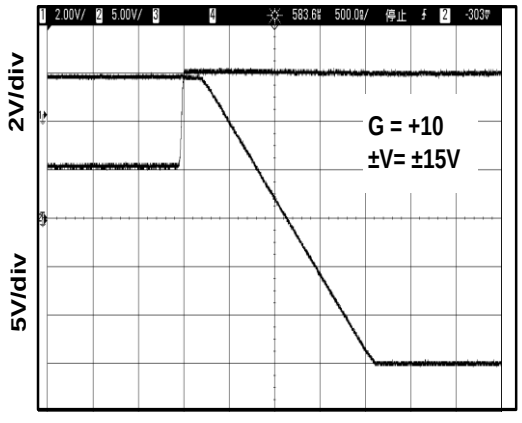
Large-Scale Step Response



Negative Over-Voltage Recovery



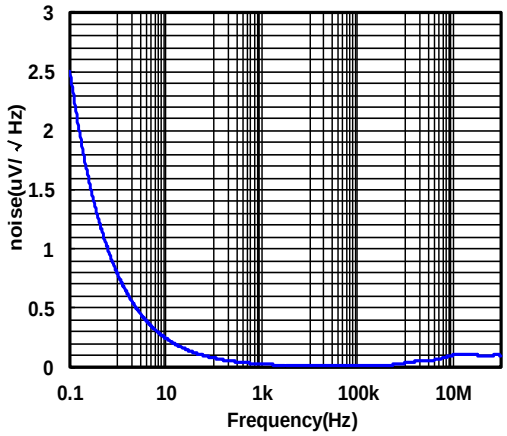
Positive Over-Voltage Recovery



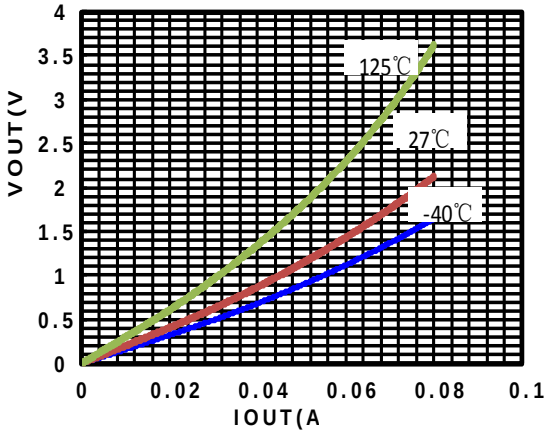
Typical Performance Characteristics

VS = ±15V, VCM = 0V, RL = Open, unless otherwise specified.(Continue)

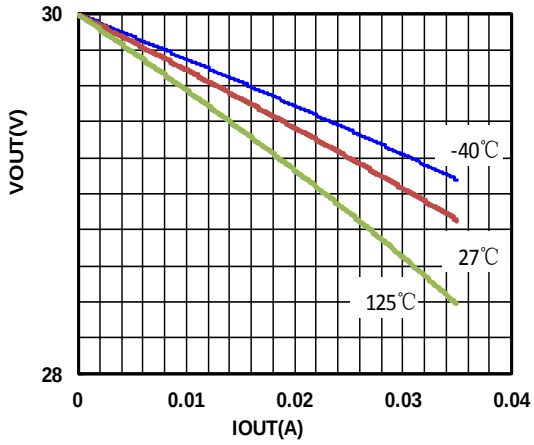
Voltage Noise Spectral Density vs. Frequency



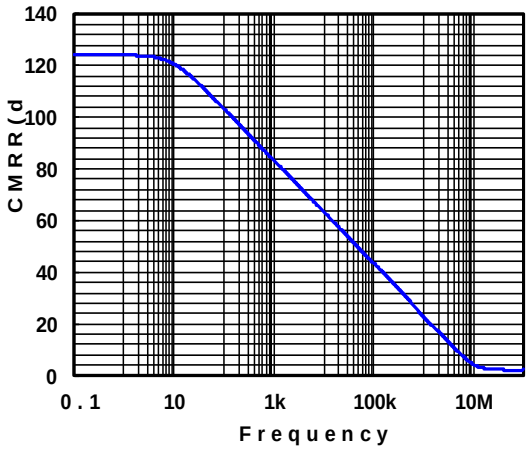
Negative Output Swing vs. Load Current



Positive Output Swing vs. Load Current



CMRR vs. Frequency



Pin Functions

-IN: Inverting Input of the Amplifier. Voltage range of this pin can go from V^- to (V^+ - 2.0V).

+IN: Non-Inverting Input of Amplifier. This pin has the same voltage range as –IN.

V+ or +V_S: Positive Power Supply. Typically the voltage is from 2.7V to 36V. Split supplies are possible as long as the voltage between V+ and V– is between 2.7V and 36V. A bypass capacitor of 0.1µF as close to the part as possible should be used between power supply pins or between supply pins and ground.

V^- or ^-V_S: Negative Power Supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V^+ and V^- is from 2.7V to 36V. If it is not connected to ground, bypass it with a capacitor of 0.1µF as close to the part as possible.

OUT: Amplifier Output. The voltage range extends to within milli-volts of each supply rail.

Operation

The TP127X have input signal range from V^- to (V^+ – 2.0V). The output can extend all the way to the supply rails. The input stage is comprised of a PMOS differential amplifier. The Class-AB control buffer and output bias stage uses a proprietary compensation technique to take full advantage of the process technology to drive very high capacitive loads. This is evident from the transient over shoot measurement plots in the Typical Performance Characteristics.

Applications Information

EMI Harden

The EMI hardening makes the TP1271/1272/1274 a must for almost all op amp applications. Most applications are exposed to Radio Frequency (RF) signals such as the signals transmitted by mobile phones or wireless computer peripherals. The TP1271/1272/1274 will effectively reduce disturbances caused by RF signals to a level that will be hardly noticeable. This again reduces the need for additional filtering and shielding Using this EMI resistant series of op amps will thus reduce the number of components and space needed for applications that are affected by EMI, and will help applications, not yet identified as possible EMI sensitive, to be more robust for EMI.

Wide Supply Voltage

The TP1271/1272/1274 operational amplifiers can operate with power supply voltages from 2.7V to 36V. Each amplifier draws 0.9mA quiescent current at 36V supply voltage. The TP1271/1272/1274 is optimized for wide bandwidth low power applications. They have an industry leading high GBW to power ratio and the GBW remains nearly constant over specified temperature range.

Low Input Bias Current

The TP1271/1272/1274 is a CMOS OPA family and features very low input bias current in 3pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on “PCB Surface Leakage” for more details.

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5pA of current to flow, which is greater than the TP1271/1272/1274 OPA’s input bias current at +27°C (±3pA, typical). It is recommended to use multi-layer PCB layout and route the OPA’s -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 2 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:

   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.

   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the Common Mode input voltage.

2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):

   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op-amp (e.g., V_{DD}/2 or ground).

   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

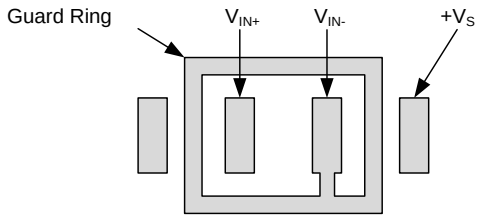


Figure 2 The Layout of Guard Ring

Ground Sensing and Rail to Rail Output

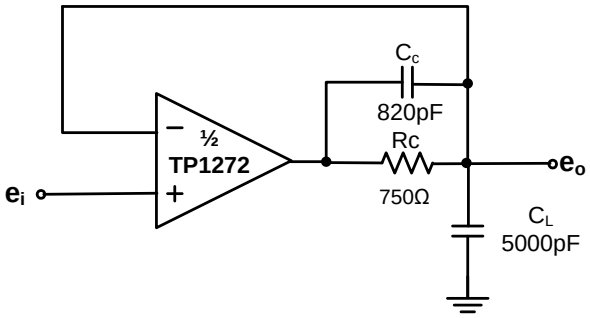
The TP1271/1272/1274 family has excellent output drive capability. It drives 2kΩ load directly with good THD performance. The output stage is a rail-to-rail topology that is capable of swinging to within 50mV of either rail.

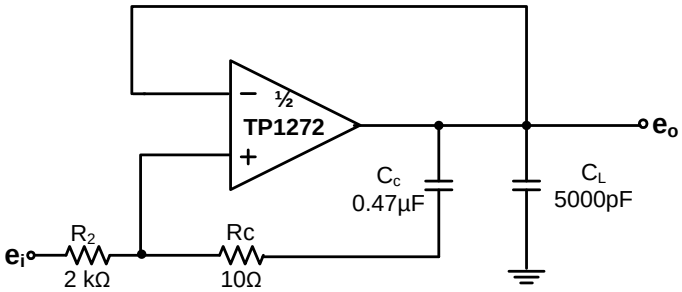
The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.3V beyond either supply, otherwise current will flow through these diodes.

Driving Large Capacitive Load

The TP1271/1272/1274 op-amp family is designed to drive large capacitive loads. As always, larger load capacitance decreases overall phase margin in a feedback system where internal frequency compensation is utilized. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in output step response. The unity-gain buffer (G = +1V/V) is the most sensitive to large capacitive loads.

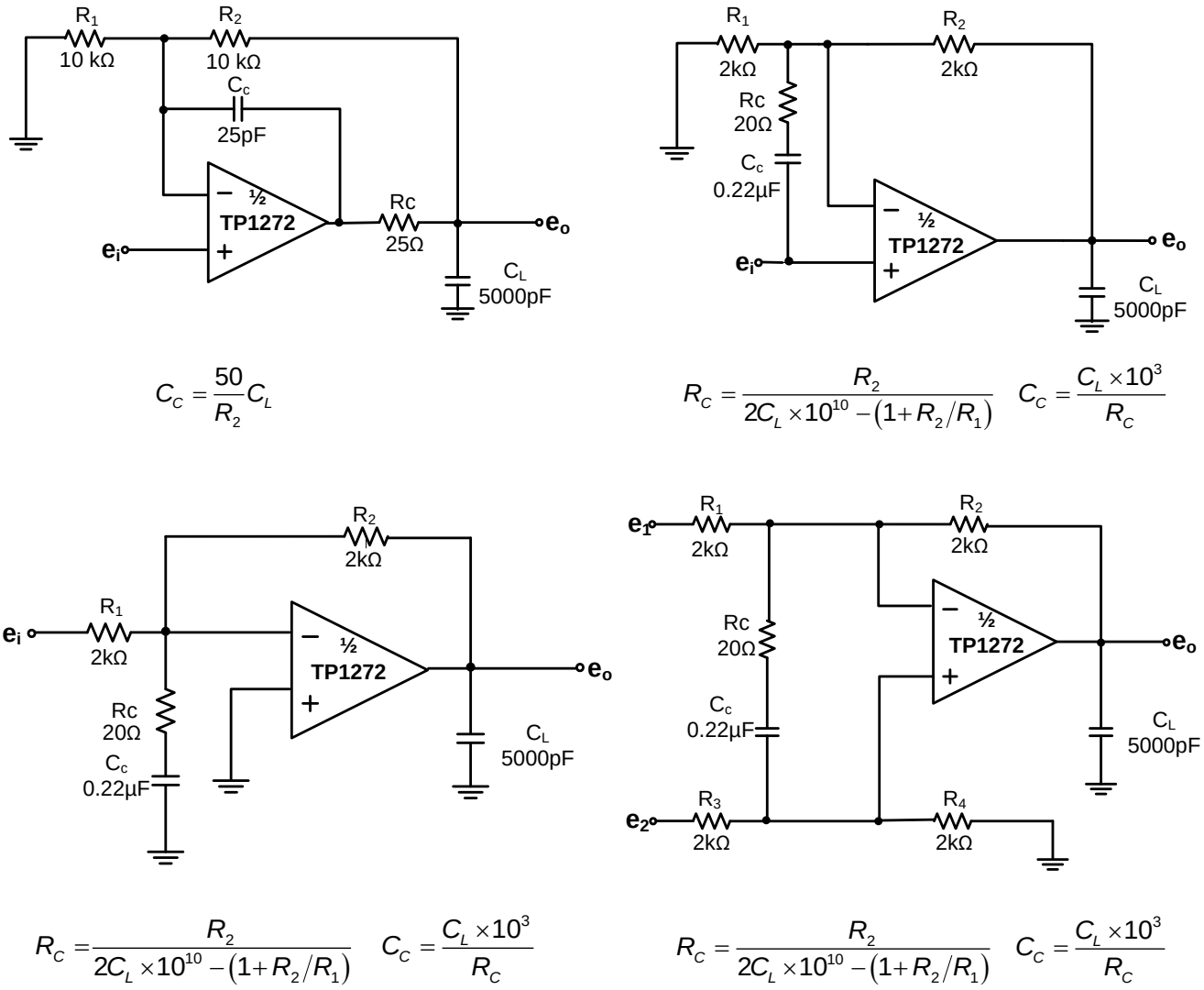
When driving large capacitive loads with the TP1271/1272/1274 op-amp family (e.g., > 1,000 pF), different compensation schemes (Figure 3) improve the feedback loop's phase margin and stability.





$$C_C = \sqrt{120\times10^{-12}C_L}$$

$$R_C = \frac{R_2}{4C_L\times10^{-10}-1} \qquad C_C = \frac{C_L\times10^3}{R_C}$$



NOTE: Design equations and component values are approximate, User adjustment is required for optimum performance.

Figure 3 Driving Large Capacitive Loads

Power Supply Layout and Bypass

The TP1271/1272/1274 OPA's power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA's inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place external components as close to the op amps' pins as possible.

Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

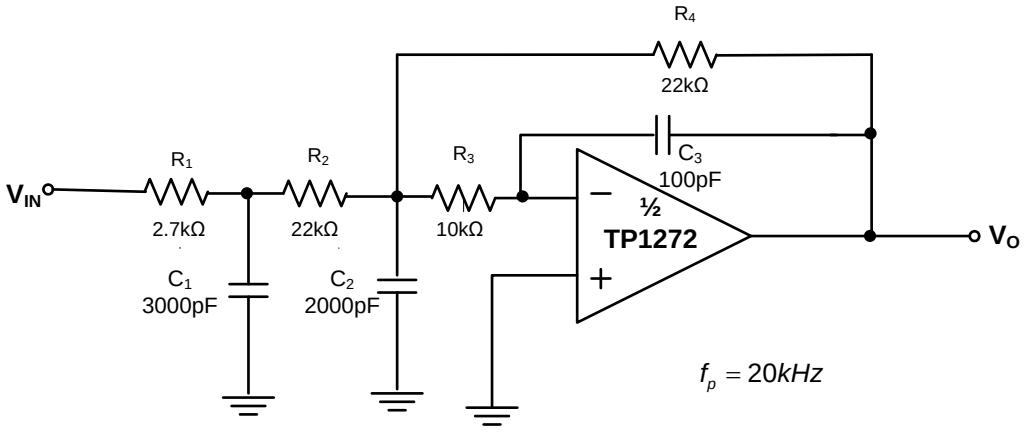
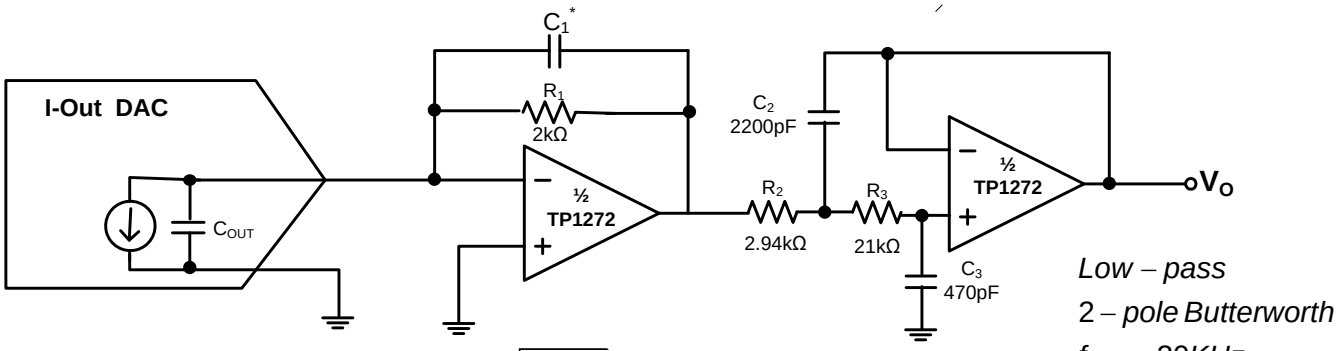


Figure 4 Three-Pole Low-Pass Filter

DAC I/V Amplifier and Low-Pass Filter



$$C_1^* = \sqrt{\frac{C_{OUT}}{2\pi R_1 f_c}}$$

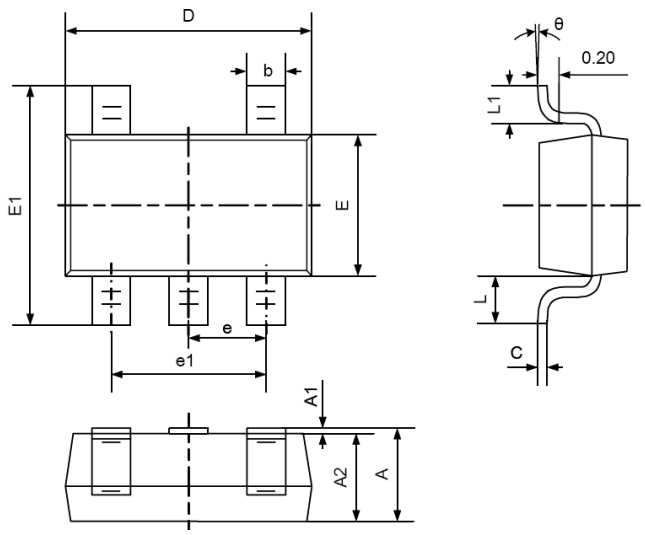
$R_1 = Feedback\ \ resistance = 2k\Omega$

$f_c = Crossover\ \ frequency = 8MHz$

Figure 5 DAC I/V Amplifier and Low-Pass Filter

Package Outline Dimensions

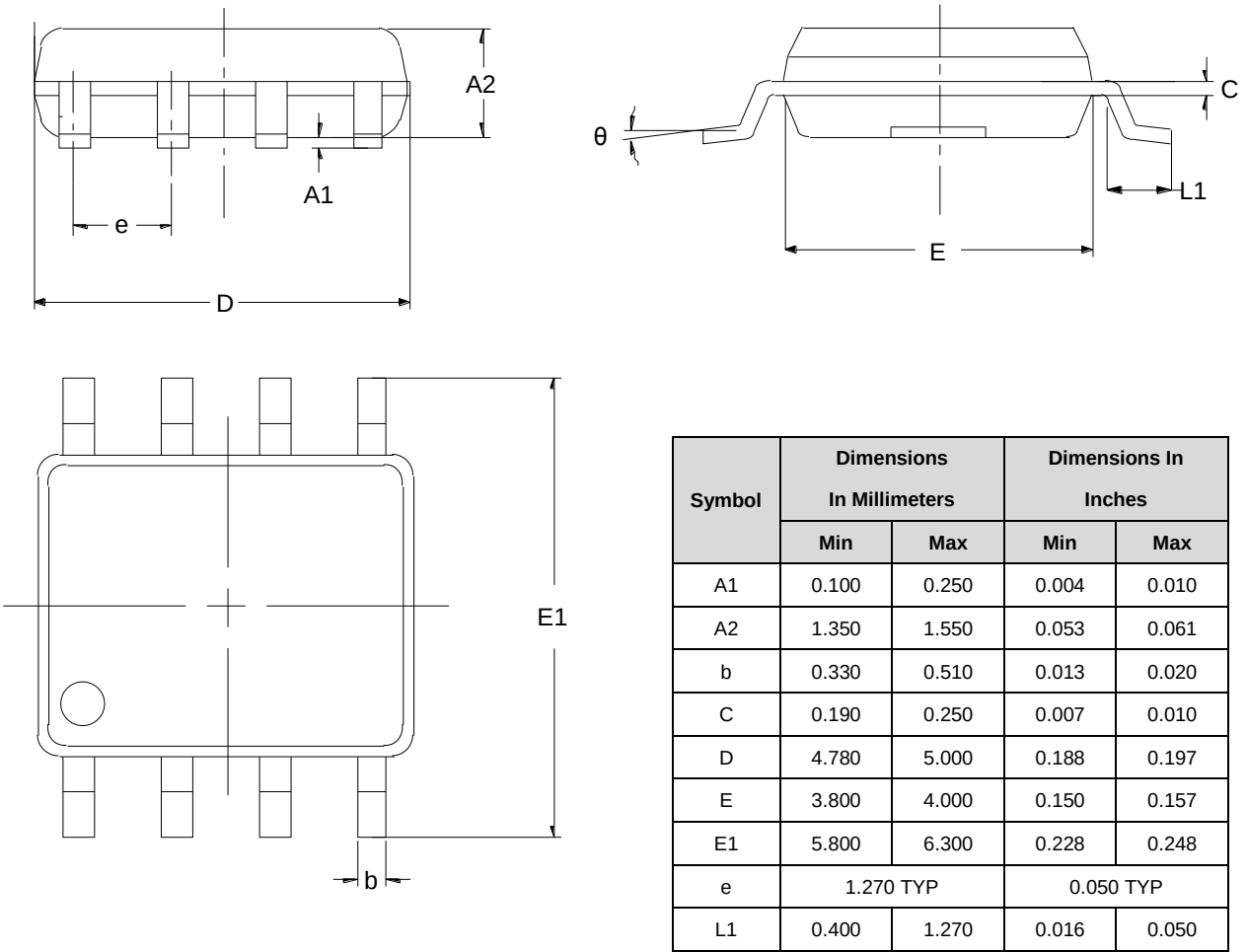
SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.460	0.012	0.024
θ	0°	8°	0°	8°

Package Outline Dimensions

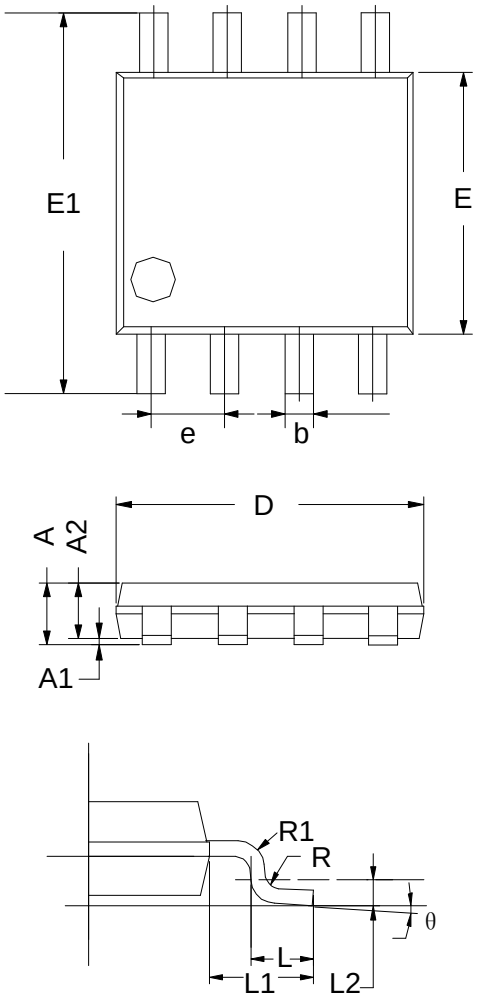
SO-8 (SOIC-8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270 TYP		0.050 TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Outline Dimensions

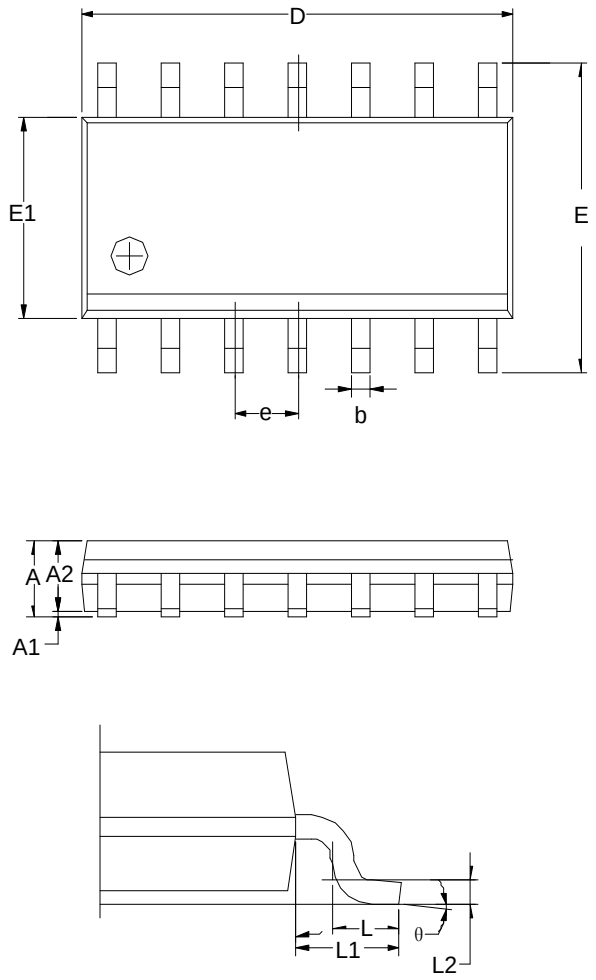
MSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
C	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L1	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

Package Outline Dimensions

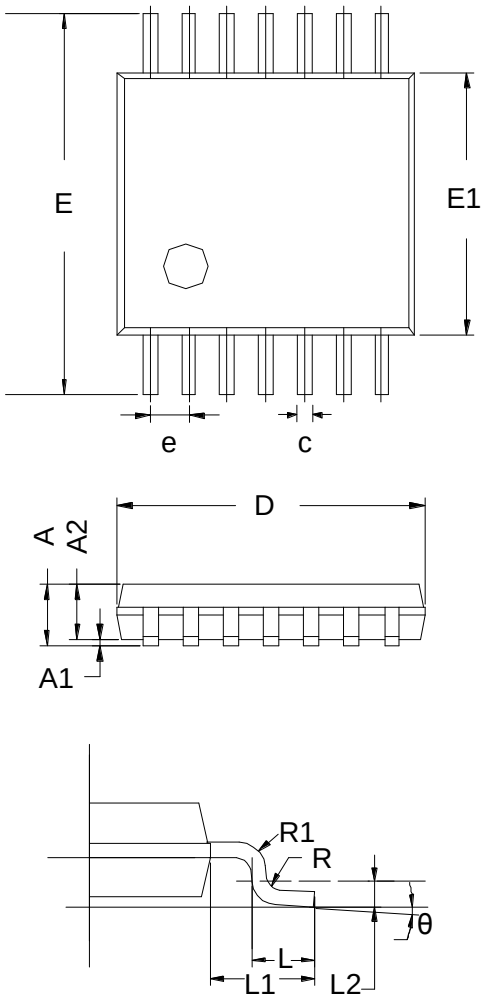
SO-14 (SOIC-14)



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.36		0.49
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
θ	0°		8°

Package Outline Dimensions

TSSOP-14



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
b	0.20	-	0.28
c	0.10	-	0.19
D	4.86	4.96	5.06
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25 BSC		
R	0.09	-	-
θ	0°	-	8°