TEXAS INSTRUMENTS

SN74LVC2G06

SCES307J – AUGUST 2001 – REVISED JULY 2015

SN74LVC2G06 Dual Inverter Buffer and Driver With Open-Drain Outputs

1 Features

- Available in the Texas Instruments Package
- Supports 5-V V_{CC} Operation
- Max t_{pd} of 3.4 ns at 3.3 V
- Low Power Consumption, 10-µA Max I_{CC}
- ±24-mA Output Drive at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Inputs and Open-Drain Outputs Accept Voltages up to 5.5 V
- I_{off} Supports Live Insertion, Partial-Power-Down Mode and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Supports Down-Translation (5 V to 3.3 V and 3.3 V to 1.8 V)
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- AV Receivers
- Blu-ray Players and Home Theaters
- DVD Recorders and Players
- Desktop or Notebook PCs
- Digital Radio or Internet Radio Players
- Digital Video Cameras (DVC)
- Embedded PC
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Projector Front-End
- Portable Media Players
- Pro Audio Mixers
- Smoke Detectors
- Solid-State Drive (SSD): Enterprise
- High-Definition (HDTV)

3 Description

This dual inverter buffer and driver is designed for 1.65-V to 5.5-V V_{CC} operation.

The output of the SN74LVC2G06 device is an open-drain which can be connected to other open-drain outputs to implement active-low, wired-OR, or active-high wired-AND functions. The maximum sink current is 32 mA.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Device Information[1]

ORDER NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC2G06DBV	SOT-23 (6)	2.90 mm × 1.60 mm
SN74LVC2G06DCK	SC70 (6)	2.00 mm × 1.25 mm
SN74LVC2G06DRY	SON (6)	1.45 mm × 1.00 mm
SN74LVC2G06DSF	SON (6)	1.00 mm × 1.00 mm
SN74LVC2G06YZP	DSBGA (6)	1.41 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
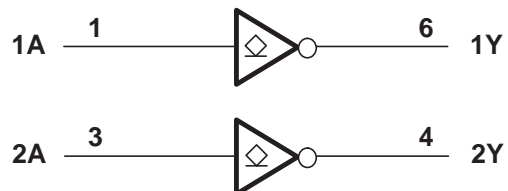
Logic Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (December 2013) to Revision J   **Page**

- Added *Device Information table*, *Pin Configuration and Functions* section, *ESD Ratings* table, *Typical Characteristics* section, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision H (August 2012) to Revision I   **Page**

- Updated document to new TI data sheet format. 1
- Removed Ordering Information table. 1
- Added ESD warning 1
- Updated operating temperature range. 5

Changes from Revision G (January 2007) to Revision H   **Page**

- Updated package views and ordering information. Added DRY & DSF packages 1

Product Folder Links: *SN74LVC2G06*

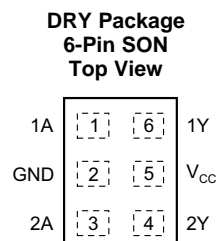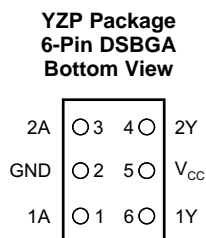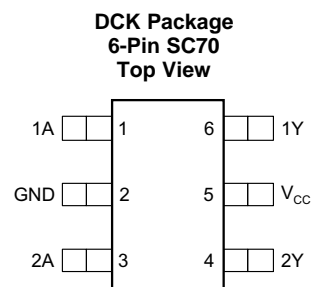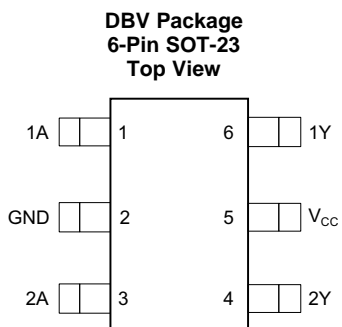# 5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View

1A — 1	6 — 1Y
GND — 2	5 — V$_{CC}$
2A — 3	4 — 2Y

DCK Package
6-Pin SC70
Top View

1A — 1	6 — 1Y
GND — 2	5 — V$_{CC}$
2A — 3	4 — 2Y

YZP Package
6-Pin DSBGA
Bottom View

2A ○3	4○ 2Y
GND ○2	5○ V$_{CC}$
1A ○1	6○ 1Y

DRY Package
6-Pin SON
Top View

1A 1	6 1Y
GND 2	5 V$_{CC}$
2A 3	4 2Y

DSF Package
6-Pin SON
Top View

1A 1	6 1Y
GND 2	5 V$_{CC}$
2A 3	4 2Y
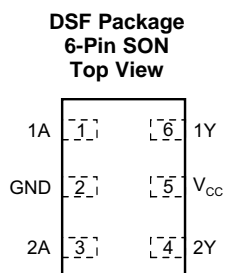
Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO		
GND	2	—	Ground
1A	1	I	Input 1
2A	3	I	Input 2
1Y	6	I	Open-drain output 1
2Y	4	O	Open-drain output 2
V$_{CC}$	5	—	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		−0.5	6.5	V
V_I	Input voltage[2]		−0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state[2]		−0.5	6.5	V
V_O	Voltage applied to any output in the high or low state[2][3]		−0.5	6.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage Temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	+2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	+1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Product Folder Links: *SN74LVC2G06*

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65		5.5	V
		Data retention only	1.5			
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$			V
		V_{CC} = 2.3 V to 2.7 V	1.7			
		V_{CC} = 3 V to 3.6 V	2			
		V_{CC} = 4.5 V to 5.5 V	$0.7 \times V_{CC}$			
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V			$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V			0.7	
		V_{CC} = 3 V to 3.6 V			0.8	
		V_{CC} = 4.5 V to 5.5 V			$0.3 \times V_{CC}$	
V_I	Input voltage		0		5.5	V
V_O	Output voltage		0		5.5	V
I_{OL}	Low-level output current	V_{CC} = 1.65 V			4	mA
		V_{CC} = 2.3 V			8	
		V_{CC} = 3 V			16	
					24	
		V_{CC} = 4.5 V			32	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V			20	ns/V
		V_{CC} = 3.3 V ± 0.3 V			10	
		V_{CC} = 5 V ± 0.5 V			5	
T_A	Operating free-air temperature		−40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]	SN74LVC2G06					UNIT
	DBV (SOT-23)	DCK (SC70)	DRY (SON)	YPZ (DSBGA)	DSF (SON)	
	6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	165	259	234	123	300	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	–40°C to 85°C			–40°C to 125°C			UNIT
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
V_{OL}		I_{OL} = 100 µA	1.65 V to 5.5 V			0.1			0.1	V
		I_{OL} = 4 mA	1.65 V			0.45			0.45	
		I_{OL} = 8 mA	2.3 V			0.3			0.3	
		I_{OL} = 16 mA	3 V			0.4			0.4	
		I_{OL} = 24 mA				0.55			0.55	
		I_{OL} = 32 mA	4.5 V			0.55			0.55	
I_I	A inputs	V_I = 5.5 V or GND	0 to 5.5 V			±5			±5	µA
I_{off}		V_I or V_O = 5.5 V	0			±10			±10	µA
I_{CC}		V_I = 5.5 V or GND, I_O = 0	1.65 V to 5.5 V			10			10	µA
ΔI_{CC}		One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	3 V to 5.5 V			500			500	µA
C_i		V_I = V_{CC} or GND	3.3 V		3.5			3.5		pF

(1)   All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics for –40°C to 85°C

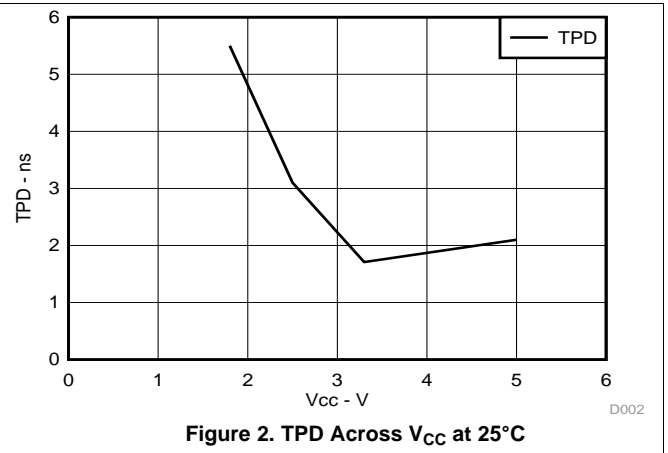over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.8	7.2	1	3.9	1	3.4	1	2.9	ns

6.7 Switching Characteristics for –40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.8	8.2	1	4.4	1	3.9	1	3.4	ns

6.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	2	2	3	4	pF

Product Folder Links: *SN74LVC2G06*

6.9 Typical Characteristics

Figure 1. TPD Across Temperature at 3.3-V V$_{CC}$

Figure 2. TPD Across V$_{CC}$ at 25°C

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7 Parameter Measurement Information
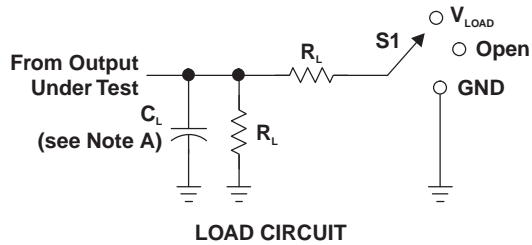
TEST	S1
t_{PZL} (see Notes E and F)	V_{LOAD}
t_{PLZ} (see Notes E and G)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

LOAD CIRCUIT

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
$1.8\ V \pm 0.15\ V$	V_{CC}	$\leq 2\ ns$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
$2.5\ V \pm 0.2\ V$	V_{CC}	$\leq 2\ ns$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\ V \pm 0.3\ V$	3 V	$\leq 2.5\ ns$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\ V \pm 0.5\ V$	V_{CC}	$\leq 2.5\ ns$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING
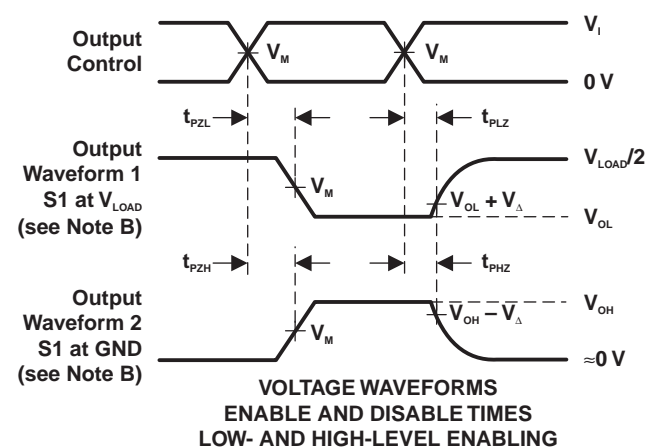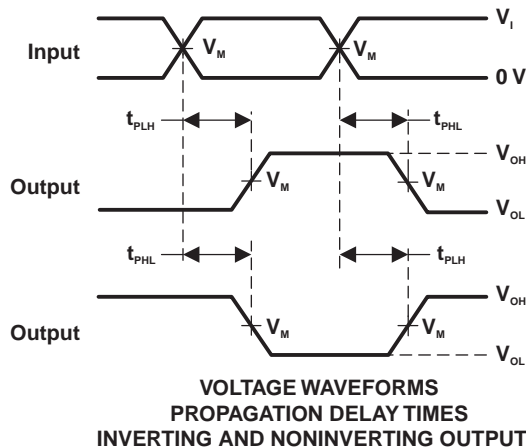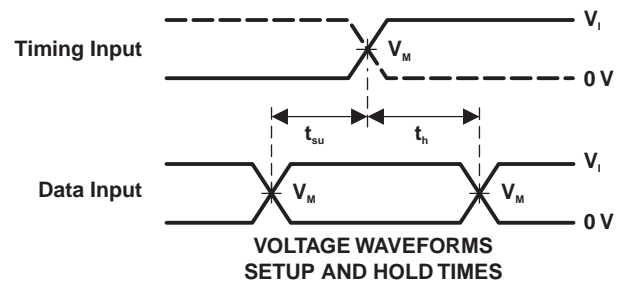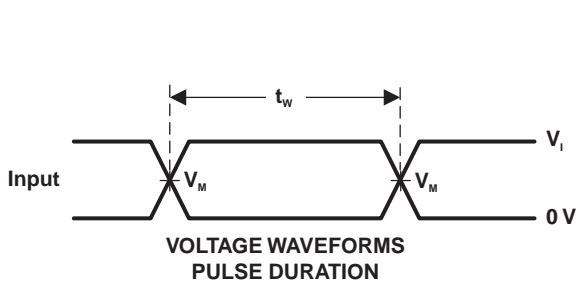
NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
   C. All input pulses are supplied by generators have the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
   D. The outputs are measured one at a time, with one transition per measurement.
   E. Because this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{PD}.
   F. t_{PZL} is measured at V_M.
   G. t_{PLZ} is measured at $V_{OL} + V_\Delta$.
   H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms (Open Drain)

Product Folder Links: *SN74LVC2G06*

8 Detailed Description

8.1 Overview

The SN74LVC2G06 dual open-drain inverter device contains one open-drain inverter with a maximum sink current of 32 mA. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram
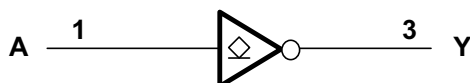
8.3 Feature Description

The wide operating voltage range of 1.65 V to 5.5 V allows the SN74LVC2G06 to be used in systems with many different voltage rails. In addition, the voltage tolerance on the output allows the device to be used for inverting up-translation or down-translation. The I_{OFF} feature safely allows voltage on the inputs and outputs when there's no V_{CC} is present.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC2G06.

Table 1. Function Table

INPUT A	OUTPUT Y
L	Hi-Z
H	L

9 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC2G06 is a dual high-drive CMOS device that implements a high-output drive buffer, such as an LED application. This device can sink 32 mA of current at 4.5 V making it ideal for high-drive applications and high-speed applications up to 100 MHz. The inputs are 5.5-V tolerant and let it to translate up or down to V_{CC}. The following *Typical Application* shows a simple LED driver application for a single channel of the device.

9.2 Typical Application
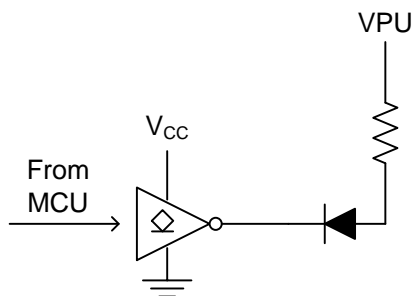
Figure 4. Typical Application Diagram

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Avoid bus contention because it can drive currents that exceed maximum limits. The high drive also creates fast edges into light loads. Consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs. See ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the *Recommended Operating Conditions* table at any valid V_{CC}.
2. Recommend Output Conditions
   - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in *Absolute Maximum Ratings* table.
   - Do not pull outputs above 5.5 V.

Product Folder Links: *SN74LVC2G06*

Typical Application (continued)
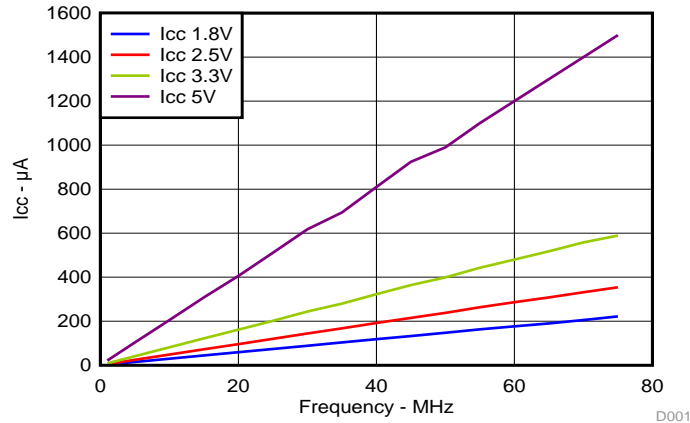
9.2.3 Application Curve

Figure 5. I_CC vs Frequency

10   Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin must have a good bypass capacitor in order to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and if there are multiple V_{CC} pins then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11   Layout

11.1   Layout Guidelines

When using multiple bit logic devices, inputs must never float. In many cases, functions or parts of functions of digital logic devices are unused. Examples include when only two inputs of a triple input and gate are used or when only three of the four buffer gates are used. Avoid leaving input pins unconnected because the undefined voltages at the outside connections result in undefined operational states. Observe the following rules under all circumstances. Connect all unused inputs of digital logic devices to a high or low bias to prevent them from floating. Based on the function of the device, apply the logic level to any unused input. Based on convenience, tie unused inputs to the GND or the V_{CC}.
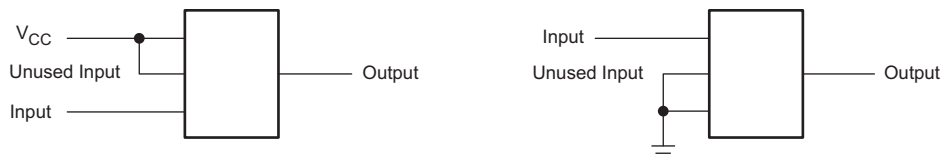
11.2   Layout Example

Figure 6. Layout Recommendation

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC2G06DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C065 ~ C06R)	Samples
SN74LVC2G06DBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C065 ~ C06R)	Samples
SN74LVC2G06DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C065 ~ C06R)	Samples
SN74LVC2G06DCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5 ~ CTR)	Samples
SN74LVC2G06DCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5 ~ CTR)	Samples
SN74LVC2G06DCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CT5 ~ CTR)	Samples
SN74LVC2G06DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT	Samples
SN74LVC2G06DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CT	Samples
SN74LVC2G06YZPR	ACTIVE	DSBGA	YZP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CT7 ~ CTN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC2G06 :

- Automotive: SN74LVC2G06-Q1

- Enhanced Product: SN74LVC2G06-EP

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G06DCKR	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC2G06DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC2G06DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC2G06YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G06DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC2G06DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC2G06DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC2G06YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

DBV (R−PDSO−G6)   PLASTIC SMALL−OUTLINE PACKAGE

DETAIL:
OPTIONAL ORIENTATION
MARKING

4073253−5/N 12/14

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
        D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
        E. Falls within JEDEC MO−178 Variation AB, except minimum lead width.

TEXAS INSTRUMENTS
www.ti.com

DBV (R−PDSO−G6)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

1,00

0,55

2,7

2,7

0,95

0,95

0,6

Solder Mask Opening

1,05

Pad Geometry

0,07
All Around

4209593−4/C 08/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D. Publication IPC−7351 is recommended for alternate designs.
         E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
             metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

TEXAS INSTRUMENTS
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DCK (R−PDSO−G6)   PLASTIC SMALL−OUTLINE PACKAGE

2,15
1,85

6   4

2,40
1,80

1,40
1,10

Pin 1
Index Area   1   3

0,65   6X   0,30
0,15

⊕ 0,10 ⓜ

1,30

0,22
0,08

Gauge Plane
Seating Plane

0,15   0°−8°

0,46
0,26

1,10
0,80

0,10   0,10

Seating Plane

0,10
0,00

4093553−4/G 01/2007

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
          D.   Falls within JEDEC MO−203 variation AB.

DCK (R−PDSO−G6)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

2,2

4x0,65

2x1,30

6x0,35

0,85

2,2

4x0,65

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356−3/C 07/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D. Publication IPC−7351 is recommended for alternate designs.
         E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
             metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

1,50 / 1,40 A

B

6 5 4

1,05 / 0,95

Pin 1 Index Area

1 2 3

0,60 / 0,51

// 0,05 C

0,15 Nominal
Lead Frame D

Seating Plane

0,05 C

0,05 / 0,00
Seating Height

C

1,00

0,50

1 2 3

6X 0,10 / 0,00

F Pin 1 Identifier
Pin shape will be
modified per device.

5X 0,45 / 0,25

6 5 4

5X 0,35 / 0,25

6X 0,25 / 0,15

⊕ 0,10 Ⓜ C A B
0,05 Ⓜ C

Bottom View

4207181/F 12/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
        B. This drawing is subject to change without notice.
        C. SON (Small Outline No–Lead) package configuration.
        D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
        E. This package complies to JEDEC MO–287 variation UFAD.
        F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

TEXAS
INSTRUMENTS
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DRY (R–PUSON–N6)   PLASTIC SMALL OUTLINE NO–LEAD

Example Board Layout

Example Stencil Design
(Note E, F, G)

Example Solder Mask Clearance
(Note D)

Example Pad Geometry
(Note C)

4208310/E   02/13

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC–7351 is recommended for alternate designs.
         D.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
         E.   Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
         F.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         G.   Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions
              if stencil manufacturing process allows for sufficient release at smaller opening.

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PIN 1 INDEX AREA

$\dfrac{1.05}{0.95}$

$\dfrac{1.05}{0.95}$

A   B

0.4 MAX

C

SEATING PLANE

⬧ 0.05 Ⓜ C

SYMM
₵

3   4

2X
0.7

4X
0.35

SYMM
₵

1   6

(0.1)
PIN 1 ID

6X $\dfrac{0.22}{0.12}$

6X $\dfrac{0.45}{0.35}$

⊕ | 0.07 Ⓜ | C | AⓈ | BⓈ |
  | 0.05 Ⓜ | C |

(0.11) TYP

$\dfrac{0.05}{0.00}$

4208186/F   10/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

DSF (S-PX2SON-N6)   PLASTIC SMALL OUTLINE NO-LEAD

Land Pattern   Stencil Pattern

Contact your PCB vendor for
allowable Solder Mask clearance (Notes C, D.)

0.20

0.35

0.53

0.15 1.20

0.70

0.53

0.20

0.165

0.35

0.53

0.15 1.20

0.70

4210277/D 05/12

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC-7351 is recommended for alternate designs.
         D.   Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
              If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
         E.   Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
         F.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         G.   Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
         H.   Component placement force should be minimized to prevent excessive paste block deformation.

B ◄─ E ─► A

BALL A1
CORNER

D

0.5 MAX

C

SEATING PLANE

0.19
0.15

BALL TYP

⌓ 0.05 C

0.5 TYP

C

SYMM
₵
B

1
TYP

0.5
TYP

A

D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

1   2

SYMM
₵

6X ⌀ 0.25
0.21

⊕ 0.015Ⓢ C AⓈ BⓈ

4219524/A   06/2014

NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

6X ($\varnothing$ 0.225)

(0.5) TYP

1   2

A

(0.5) TYP

B   SYMM
$\updownarrow$

C

SYMM
$\updownarrow$

LAND PATTERN EXAMPLE
SCALE:40X

($\varnothing$ 0.225)
METAL

0.05 MAX

SOLDER MASK
OPENING

NON-SOLDER MASK
DEFINED
(PREFERRED)

0.05 MIN

METAL
UNDER
MASK

($\varnothing$ 0.225)
SOLDER MASK
OPENING

SOLDER MASK
DEFINED
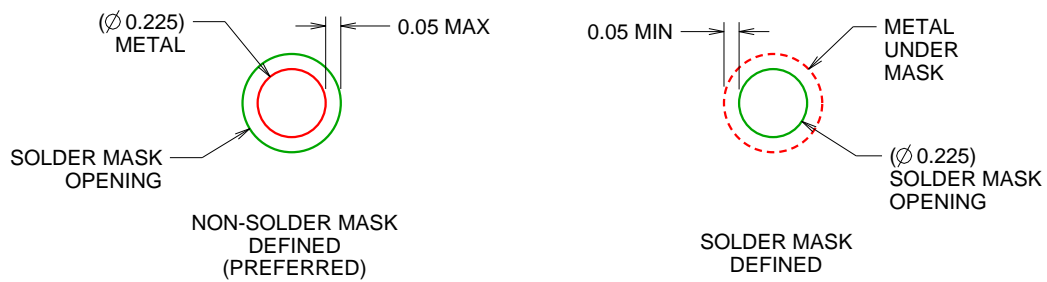
SOLDER MASK DETAILS
NOT TO SCALE

4219524/A   06/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A   06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.