TPS54140 1.5-A, 42-V Step-Down DC-DC Converter With Eco-mode™

1 Features

- 3.5- to 42-V Input Voltage Range
- 200-mΩ High-Side MOSFET
- High Efficiency at Light Loads with a Pulse Skipping Eco-mode™
- 116-µA Operating Quiescent Current
- 1.3-µA Shutdown Current
- 100-kHz to 2.5-MHz Switching Frequency
- Synchronizes to External Clock
- Adjustable Slow Start and Sequencing
- UV and OV Power-Good Output
- Adjustable UVLO Voltage and Hysteresis
- 0.8-V Internal Voltage Reference
- MSOP10 Package With PowerPAD™
- Supported by WEBENCH® Software Tool (www.TI.com/WEBENCH)

2 Applications

- 12-V and 24-V Industrial and Commercial Low Power Systems
- Aftermarket Auto Accessories: Video, GPS, Entertainment

3 Description

The TPS54140 device is a 42-V, 1.5-A, step-down regulator with an integrated high-side MOSFET. Current mode control provides simple external compensation and flexible component selection. A low-ripple pulse-skip mode reduces the no load, regulated output-supply current to 116 µA. Using the enable pin, the shutdown supply current is reduced to 1.3 µA.

Undervoltage lockout is internally set at 2.5 V, but can be increased using the enable pin. The output-voltage startup ramp is controlled by the slow-start pin that can also be configured for sequencing and tracking. An open-drain power-good signal indicates the output is within 94% to 107% of the nominal voltage.

A wide switching frequency range allows efficiency and external component size to be optimized. Frequency foldback and thermal shutdown protects the device during an overload condition.

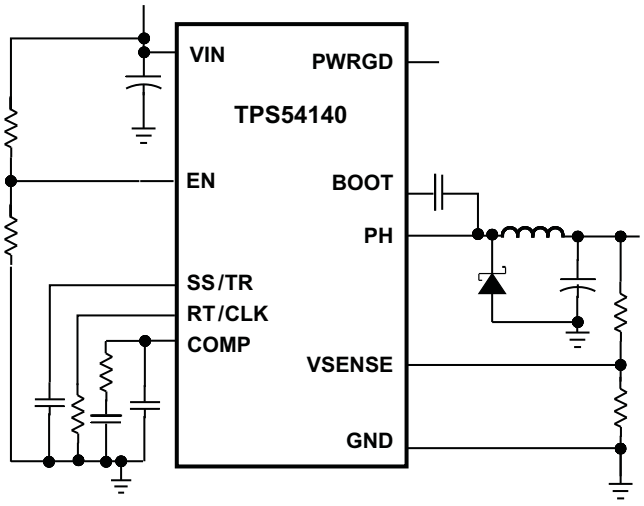
The TPS54140 device is available in a 10-pin thermally enhanced MSOP PowerPAD package.

Device Information(1)

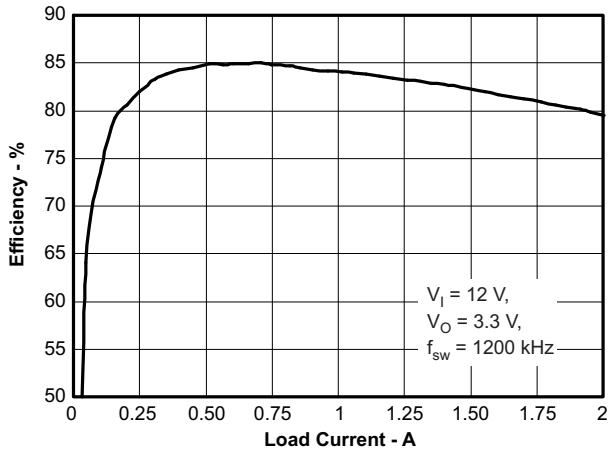
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54140	MSOP (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Efficiency vs Load Current



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5 Revision History

Changes from Revision B (September 2013) to Revision C — **Page**

- Added the *Handling Ratings* table and the following sections:*Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* ... 1

Changes from Revision A (August 2012) to Revision B — **Page**

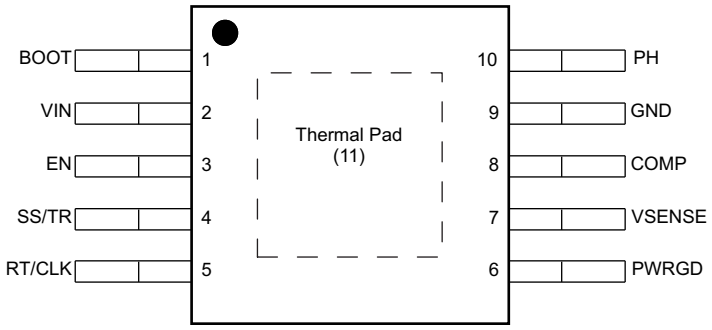
- Deleted SWIFT from the data sheet Title and Features ... 1

Changes from Original (October 2008) to Revision A — **Page**

- Changed Features Item From: 300kHz to 2.5MHz Switching Frequency To: 100kHz to 2.5MHz Switching Frequency ... 1
- Changed Description text From: "within 93% to 107% of its nom voltage." To: "within 94% to 107% of its nom voltage." ... 1
- Changed Enable threshold +50 mV TYP value From: ±3.8 To: –3.8 ... 5
- Changed Enable threshold ±50 mV TYP value From: ±0.9 To: –0.98 ... 5
- Changed Hysteresis current TYP value From: ±2.9 To: –2.9 ... 5
- Changed Error amplifier transconductance (g_M) Test Condition From: ±2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V To: –2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V ... 5
- Changed Error amplifier transconductance (g_M) during slow start From: ±2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V To: –2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V ... 5
- Changed text in the Error Amplifier section From: "the gm is 25 µA/V" To: "the gm is 26 µA/V" ... 14
- Changed text in the Slow Start and Tracking Pin (SS/TR) section From: "VIN UVLO is exceeded, EN pin pulled below 1.25V" To: "VIN pin is below the VIN UVLO, EN pin pulled below 1.25V" ... 15
- Changed Start Input Voltage (rising VIN) voltage From: 7.25 V To: 7.7 V ... 29
- Changed Start Input Voltage (falling VIN) voltage From: 6.25 V To: 6.7 V ... 29
- Changed Equation 29 ... 30
- Changed 7.25V to 7.7V and 6.25V to 6.7V in the Under Voltage Lock Out Set Point section. ... 34
- Changed Equation 47 ... 36
- Changed Equation 49 ... 36

6 Pin Configuration and Functions

DGQ Package
10-Pin MSOP With PowerPAD™
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	BOOT	O	A bootstrap capacitor is required between the BOOT and PH pins. If the voltage on this capacitor is below the minimum required by the device, the output is forced to switch off until the capacitor is refreshed.
2	VIN	I	This pin is the 3.5- to 42-V input supply voltage.
3	EN	I	This pin is the enable pin and internal pullup current source. To disable, pull below 1.2 V. Float this pin to enable. Adjust the input undervoltage lockout with two resistors.
4	SS/TR	I	This pin is the slow-start and tracking pin. An external capacitor connected to this pin sets the output rise time. Because the voltage on this pin overrides the internal reference, it can be used for tracking and sequencing.
5	RT/CLK	I	This pin is the resistor timing and external clock pin. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to a resistor set function.
6	PWRGD	O	This pin is an open drain output. This pin is asserted low if the output voltage is low because of thermal shutdown, dropout, overvoltage, or EN shut down.
7	VSENSE	I	This pin is the inverting node of the transconductance (gm) error amplifier.
8	COMP	O	This pin is the error amplifier output and input to the output-switch current comparator. Connect frequency compensation components to this pin.
9	GND	—	Ground pin
10	PH	O	This pin is the source of the internal high-side power MOSFET.
11	Thermal Pad	—	The GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.

7 Specifications

7.1 Absolute Maximum Ratings(1)

Over operating temperature range (unless otherwise noted).

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	47	V
	EN	–0.3	5	
	BOOT		55	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	PWRGD	–0.3	6	
	SS/TR	–0.3	3	
	RT/CLK	–0.3	3.6	
Output voltage	PH–BOOT		8	V
	PH	–0.6	47	
	PH, 10-ns Transient	–2	47	
Voltage Difference	PAD to GND		±200	mV
Source current	EN		100	µA
	BOOT		100	mA
	VSENSE		10	µA
	PH	Current Limit		A
	RT/CLK		100	µA
Sink current	VIN	Current Limit		A
	COMP		100	µA
	PWRGD		10	mA
	SS/TR		200	µA
Operating junction temperature		–40	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–1	1	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Operating input voltage on the VIN pin	3.5		42	V
	Output voltage	0.8		39	V
	Output current	0		1.5	A
T_J	Operating junction temperature	–40		150	°C

7.4 Thermal Information

THERMAL METRIC[1]		DGQ 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	38.4	
ψ_{JT}	Junction-to-top characterization parameter	1.9	
ψ_{JB}	Junction-to-board characterization parameter	38.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	46.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN = 3.5 to 42V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
	Operating input voltage		3.5		42	V
	Internal undervoltage lockout threshold	No voltage hysteresis, rising and falling		2.5		V
	Shutdown supply current	EN = 0 V, 25°C, 3.5 V ≤ VIN ≤ 42 V		1.3	4	µA
	Operating : nonswitching supply current	VSENSE = 0.83 V, VIN = 12 V, 25°C		116	136	µA
ENABLE AND UVLO (EN PIN)						
	Enable threshold voltage	No voltage hysteresis, rising and falling, 25°C	0.9	1.25	1.55	V
	Input current	Enable threshold 50 mV		–3.8		µA
		Enable threshold ±50 mV		–0.9		µA
	Hysteresis current			–2.9		µA
VOLTAGE REFERENCE						
	Voltage reference	T_J = 25°C	0.792	0.8	0.808	V
			0.784	0.8	0.816	V
HIGH-SIDE MOSFET						
	On-resistance	VIN = 3.5 V, BOOT-PH = 3 V		300		mΩ
		VIN = 12 V, BOOT-PH = 6 V		200	410	mΩ
ERROR AMPLIFIER						
	Input current			50		nA
	Error amplifier transconductance (g_M)	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		97		µMhos
	Error amplifier transconductance (g_M) during slow start	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V, V_{VSENSE} = 0.4 V		26		µMhos
	Error amplifier dc gain	V_{VSENSE} = 0.8 V		10 000		V/V
	Error amplifier bandwidth			2700		kHz
	Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100 mV overdrive		±7		µA
	COMP to switch current transconductance			6		A/V
CURRENT LIMIT						
	Current limit threshold	VIN = 12 V, T_J = 25°C	1.8	2.7		A
THERMAL SHUTDOWN						
	Thermal shutdown			182		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
	Switching Frequency Range using RT mode		100		2500	kHz
f_{SW}	Switching frequency	R_T = 200 kΩ	450	581	720	kHz
	Switching Frequency Range using CLK mode		300		2200	kHz

Electrical Characteristics (continued)

T_J = –40°C to 150°C, VIN = 3.5 to 42V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Minimum CLK pulse width			40		ns
	RT/CLK high threshold			1.9	2.2	V
	RT/CLK low threshold		0.5	0.7		V
	RT/CLK falling edge to PH rising edge delay	Measured at 500 kHz with RT resistor in series		60		ns
	PLL lock in time	Measured at 500 kHz		100		µs
SLOW START AND TRACKING (SS/TR)						
	Charge current	$V_{SS/TR}$ = 0.4 V		2		µA
	SS/TR-to-VSENSE matching	$V_{SS/TR}$ = 0.4 V		45		mV
	SS/TR-to-reference crossover	98% nominal		1.0		V
	SS/TR discharge current (overload)	VSENSE = 0 V, V(SS/TR) = 0.4 V		112		µA
	SS/TR discharge voltage	VSENSE = 0 V		54		mV
POWER GOOD (PWRGD PIN)						
V_{VSENSE}	VSENSE threshold	VSENSE falling		92%		
		VSENSE rising		94%		
		VSENSE rising		109%		
		VSENSE falling		107%		
	Hysteresis	VSENSE falling		2%		
	Output high leakage	VSENSE = VREF, V(PWRGD) = 5.5 V, 25°C		10		nA
	On resistance	I(PWRGD) = 3 mA, VSENSE < 0.79 V		50		Ω
	Minimum VIN for defined output	V(PWRGD) < 0.5 V, II(PWRGD) = 100 µA		0.95	1.5	V

7.6 Typical Characteristics

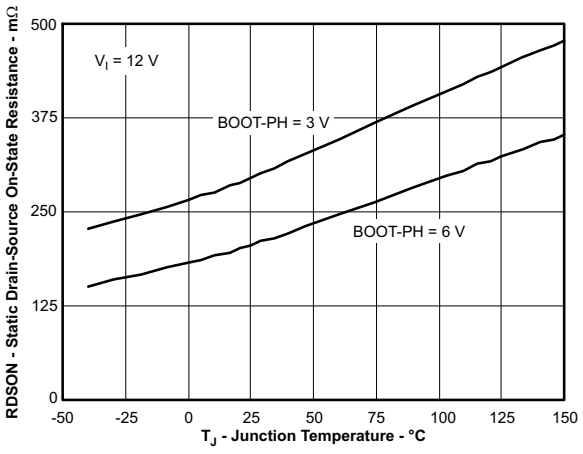


Figure 1. On Resistance vs Junction Temperature

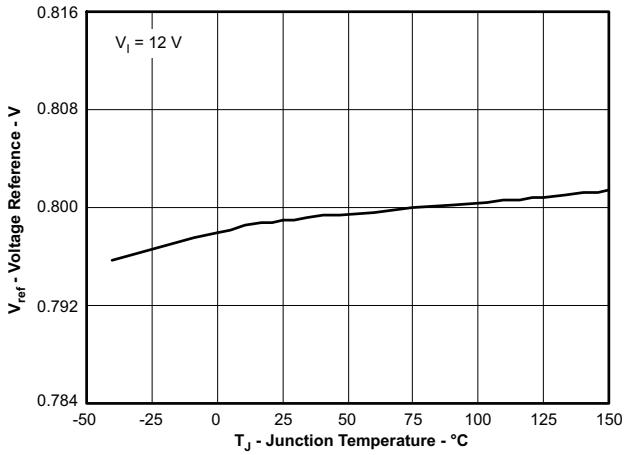


Figure 2. Voltage Reference vs Junction Temperature

Typical Characteristics (continued)

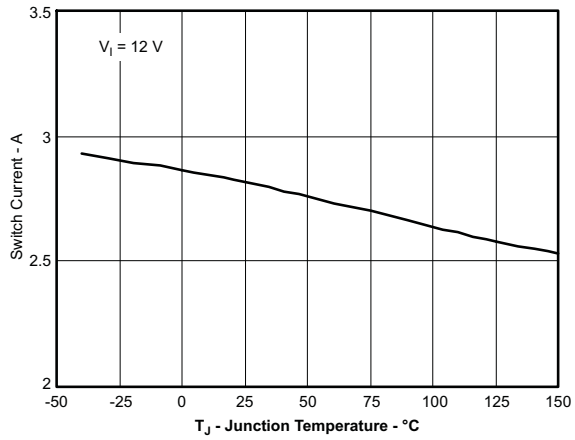


Figure 3. Switch Current Limit vs Junction Temperature

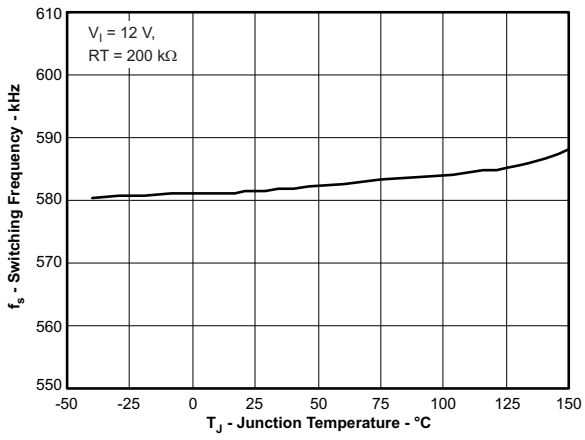


Figure 4. Switching Frequency vs Junction Temperature

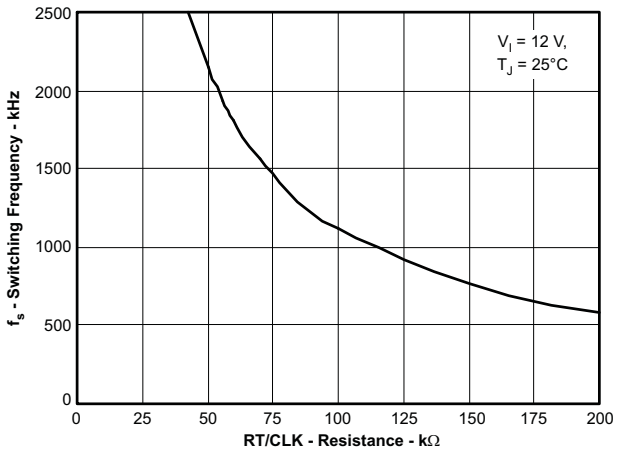


Figure 5. Switching Frequency vs RT/CLK Resistance, High Frequency Range

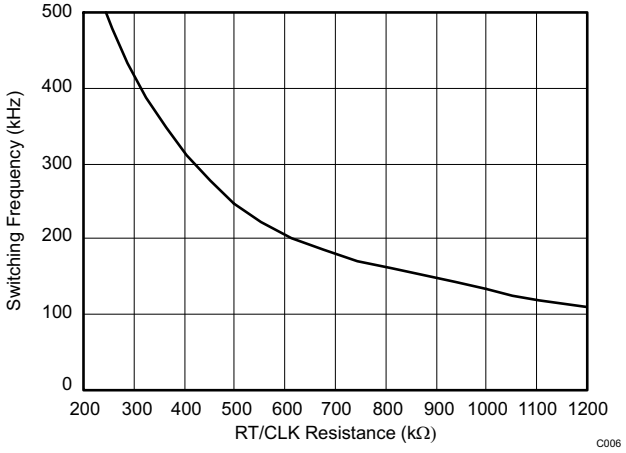


Figure 6. Switching Frequency vs RT/CLK Resistance, Low Frequency Range

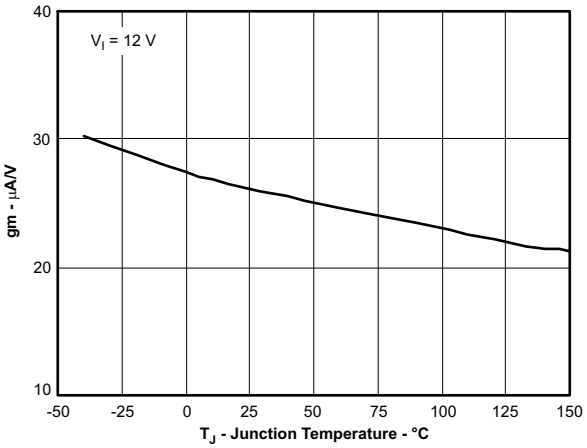


Figure 7. EA Transconductance During Slow Start vs Junction Temperature

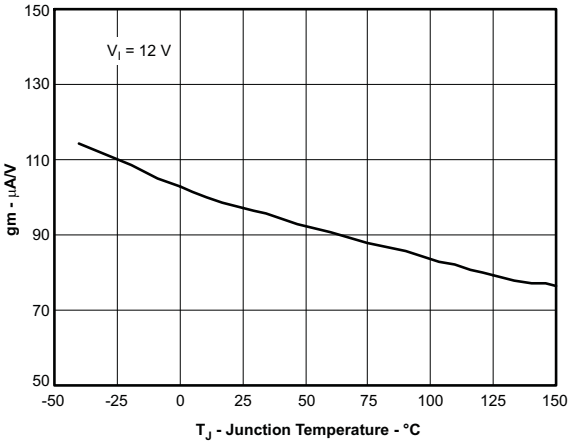


Figure 8. EA Transconductance vs Junction Temperature

Typical Characteristics (continued)

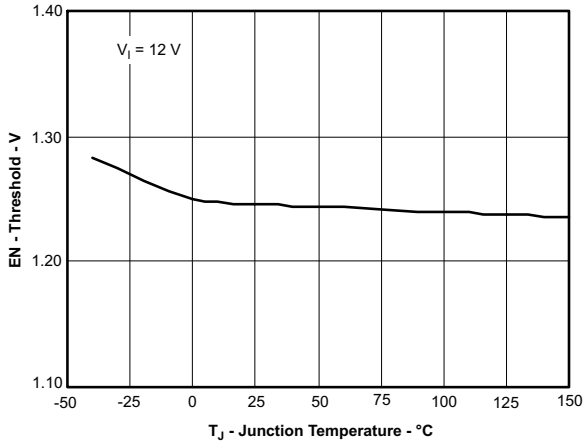


Figure 9. EN Pin Voltage vs Junction Temperature

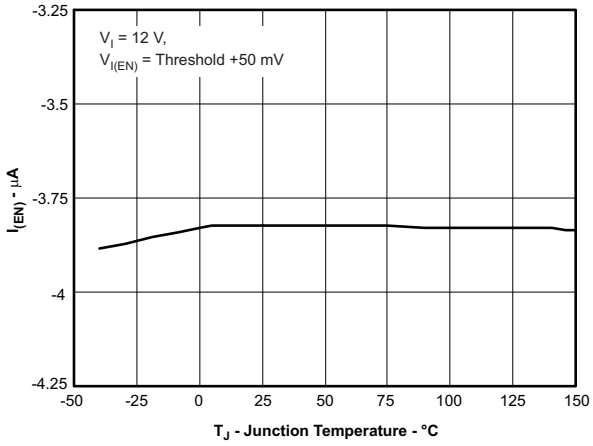


Figure 10. EN Pin Current vs Junction Temperature

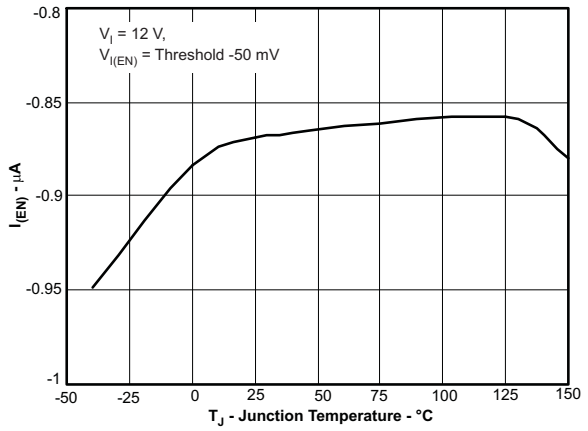


Figure 11. EN Pin Current vs Junction Temperature

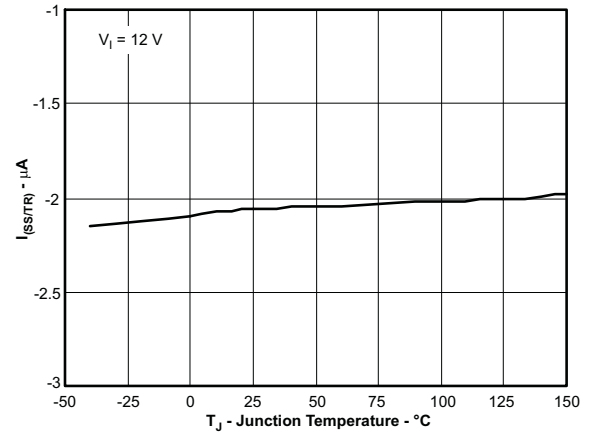


Figure 12. SS/TR Charge Current vs Junction Temperature

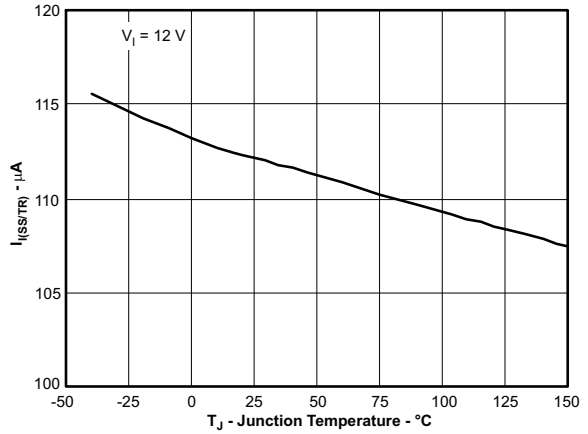


Figure 13. SS/TR Discharge Current vs Junction Temperature

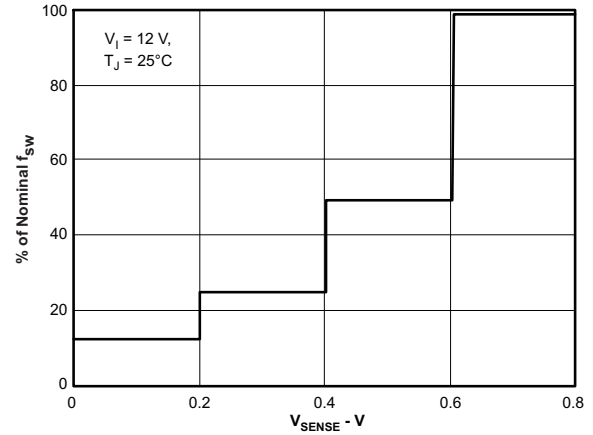


Figure 14. Switching Frequency vs VSENSE

Typical Characteristics (continued)

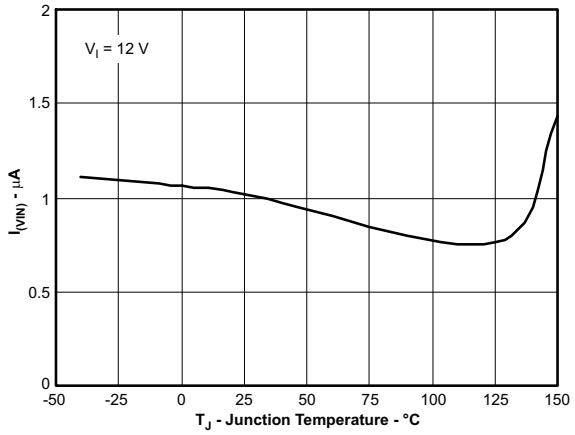


Figure 15. Shutdown Supply Current vs Junction Temperature

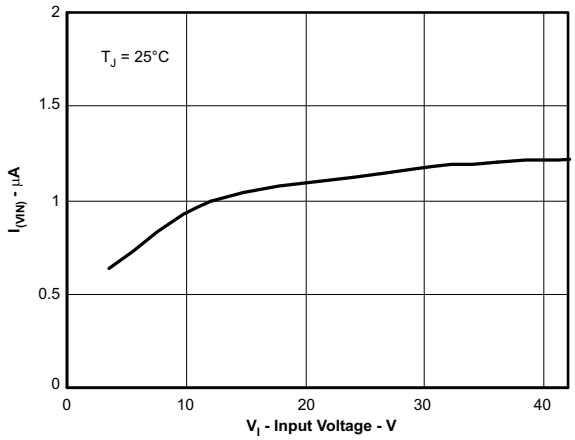


Figure 16. Shutdown Supply Current vs Input Voltage (V_{IN})

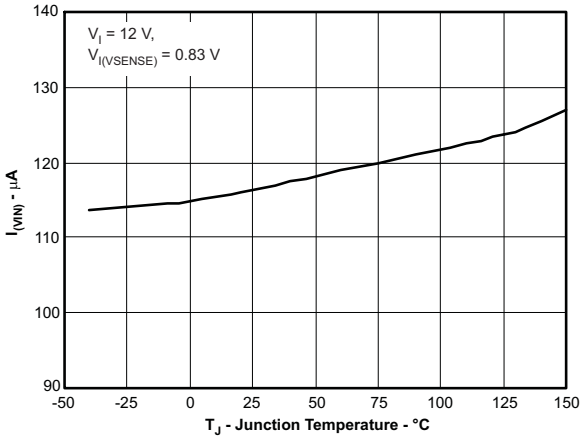


Figure 17. VIN Supply Current vs Junction Temperature

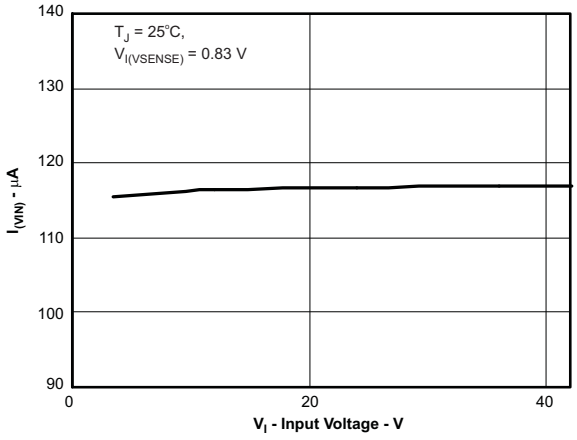


Figure 18. VIN Supply Current vs Input Voltage

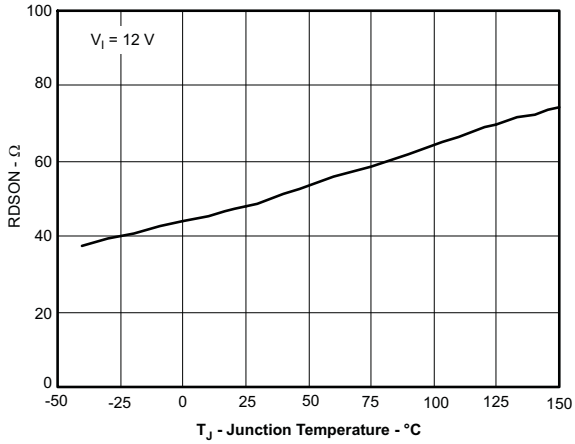


Figure 19. PWRGD On Resistance vs Junction Temperature

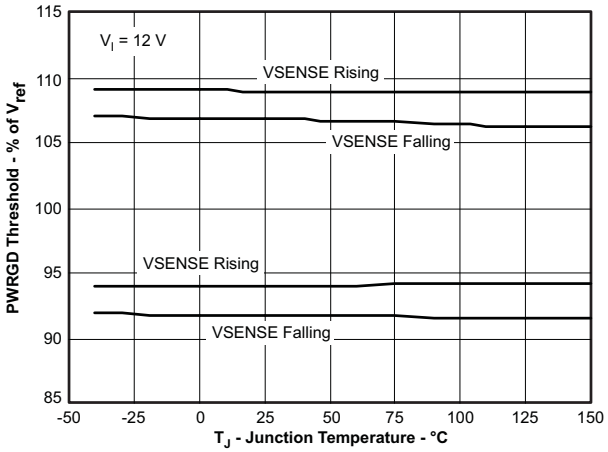


Figure 20. PWRGD Threshold vs Junction Temperature

Typical Characteristics (continued)

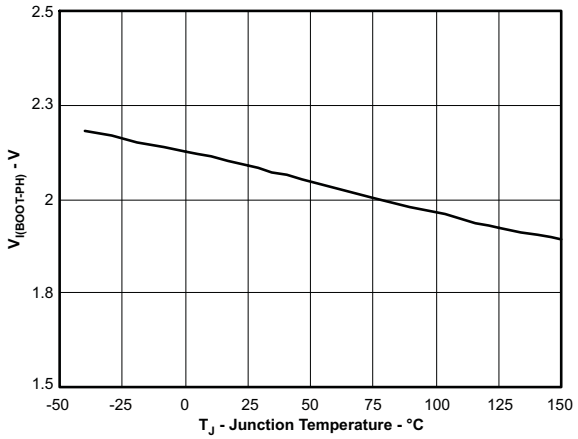


Figure 21. BOOT-PH UVLO vs Junction temperature

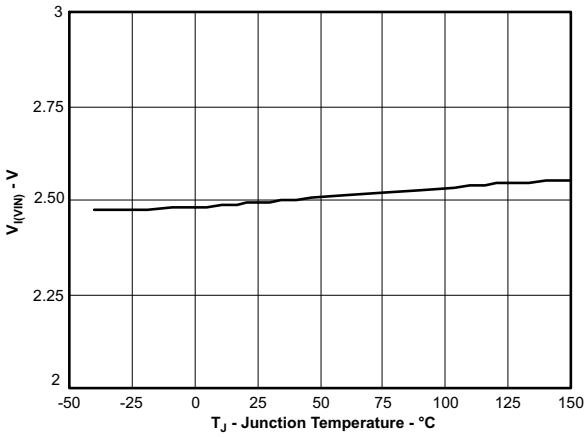


Figure 22. Input Voltage (UVLO) vs Junction Temperature

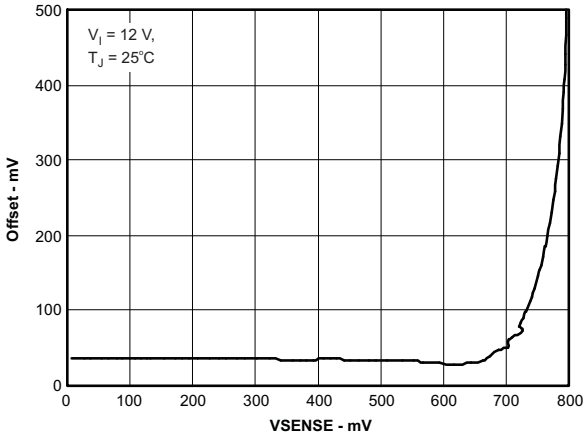


Figure 23. SS/TR to VSENSE Offset vs VSENSE

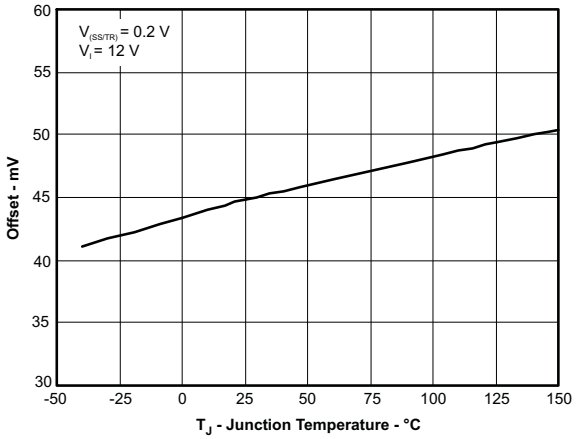


Figure 24. SS/TR to VSENSE Offset vs Temperature

8 Detailed Description

8.1 Overview

The TPS54140 device is a 42-V, 1.5-A, step-down (buck) regulator with an integrated high-side n-channel MOSFET. To improve performance during line and load transients, the device implements a constant-frequency, current mode control which reduces output capacitance and simplifies external frequency compensation design. The wide switching frequency of 100 kHz to 2500 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase-lock loop (PLL) on the RT/CLK pin that is used to synchronize the power-switch turn on to a falling edge of an external system clock.

The TPS54140 device has a default startup voltage of approximately 2.5 V. The EN pin has an internal pullup current-source that can be used to adjust the input-voltage undervoltage-lockout (UVLO) threshold with two external resistors. In addition, the pullup current provides a default condition. The device operates when the EN pin is floating. The operating current is 116 µA when not switching and under no load. When the device is disabled, the supply current is 1.3 µA.

The integrated 200-mΩ high-side MOSFET allows for high-efficiency power-supply designs capable of delivering 1.5 A of continuous current to a load. The TPS54140 device reduces the external component count by integrating the boot-recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor on the BOOT to PH pin. The boot-capacitor voltage is monitored by an UVLO circuit and turns the high-side MOSFET off when the boot voltage falls below a preset threshold. The TPS54140 device can operate at high duty cycles because of the boot UVLO. The output voltage can be stepped down to as low as the 0.8-V reference.

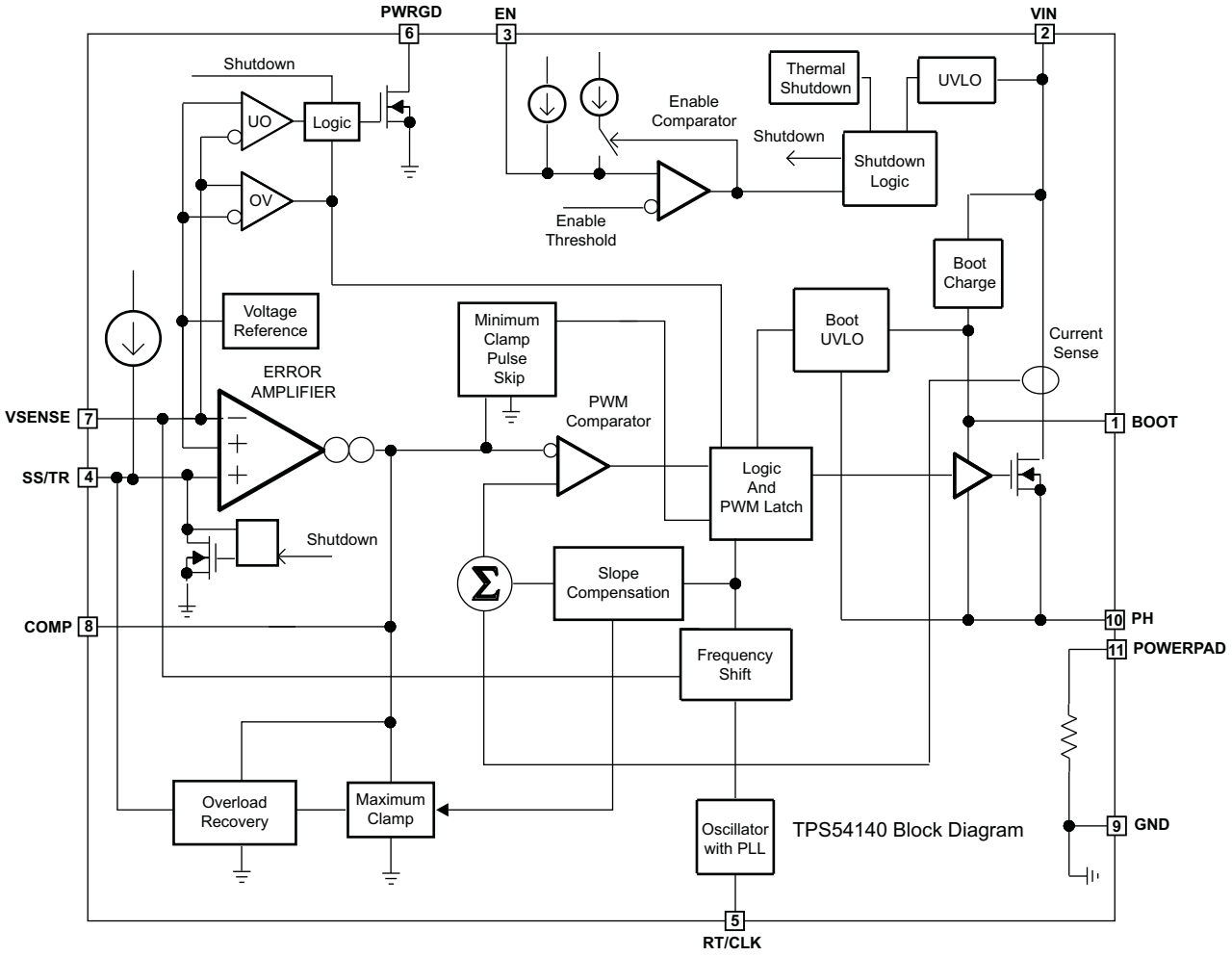
The TPS54140 device has a power good comparator (PWRGD) which asserts when the regulated output voltage is less than 92% or greater than 109% of the nominal output voltage. The PWRGD pin is an open drain output which deasserts when the VSENSE pin voltage is between 94% and 107% of the nominal output voltage allowing the pin to transition high when a pullup resistor is used.

The TPS54140 device minimizes excessive-output overvoltage (OV) transients by taking advantage of the OV power-good comparator. When the OV comparator is activated, the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 107%.

The SS/TR (slow start/tracking) pin is used to minimize inrush currents or provide power-supply sequencing during power up. A small value capacitor should be coupled to the pin to adjust the slow-start time. A resistor divider can be coupled to the pin for critical power-supply sequencing requirements. The SS/TR pin is discharged before the output powers up. This discharging ensures a repeatable restart after an over-temperature fault, UVLO fault, or a disabled condition.

The TPS54140 device also discharges the slow-start capacitor during overload conditions with an overload recovery circuit. The overload recovery circuit slow starts the output from the fault voltage to the nominal regulation voltage when a fault condition is removed. A frequency -foldback circuit reduces the switching frequency during startup and overcurrent fault conditions to help control the inductor current.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed Frequency PWM Control

The TPS54140 device uses an adjustable fixed-frequency, peak-current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side MOSFET power switch. The error amplifier output is compared to the high-side MOSFET power-switch current. When the power-switch current reaches the COMP voltage level the power switch is turned off. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level. The Eco-mode is implemented with a minimum clamp on the COMP pin.

8.3.2 Slope Compensation Output Current

The TPS54140 device adds a compensating ramp to the switch-current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current remains constant over the full duty-cycle range.

Feature Description (continued)

8.3.3 Bootstrap Voltage (BOOT)

The TPS54140 device has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate-drive voltage for the high-side MOSFET. The value of the ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R- or X5R-grade dielectric is recommended because of the stable characteristics over temperature and voltage. To improve drop out, the TPS54140 device is designed to operate at 100% duty cycle as long as the BOO-to-PH pin voltage is greater than 2.1 V. When the voltage from the BOOT to PH pins drops below 2.1 V, the high-side MOSFET is turned off using an UVLO circuit allowing for the low-side diode to conduct which allows refreshing of the BOOT capacitor. Because the supply current sourced from the BOOT capacitor is low, the high-side MOSFET can remain on for more switching cycles than it refreshes, thus, the effective duty-cycle limitation that is attributed to the boot regulator system is high.

8.3.4 Low Dropout Operation

The duty cycle during dropout of the regulator is mainly determined by the voltage drops across the power MOSFET, inductor, low-side diode, and printed circuit-board resistance. During operating conditions in which the input voltage drops, the high-side MOSFET can remain on for 100% of the duty cycle to maintain output regulation or until the BOOT-to-PH voltage falls below 2.1 V.

When the high-side MOSFET is off, the low-side diode conducts and the BOOT capacitor recharges. During this boot-capacitor recharge time, the inductor current ramps down until the high-side MOSFET turns on. The recharge time is longer than the typical high-side MOSFET off time of previous switching cycles, and thus, the inductor current ripple is larger. The larger ripple current results in more ripple voltage on the output. The recharge time is a function of the input voltage, boot capacitor value, and the impedance of the internal boot-recharge diode.

Attention must be given to maximum duty-cycle applications that experience extended time periods without a load current. The high-side MOSFET turns off when the voltage across the BOOT capacitors falls below the 2.1-V threshold in applications that have a difference in the input voltage and output voltage that is less than 3 V. However, the inductor does not have enough current to pull the PH pin down to recharge the boot capacitor. The regulator does not switch because the boot capacitor is less than 2.1 V and the output capacitor decays until the difference in the input voltage and output voltage is 2.1 V. At this time the boot undervoltage lockout is exceeded and the device switches until the desired output voltage is reached.

Figure 25 and Figure 26 show the start and stop voltages for 3.3-V and 5-V applications. The voltages are plotted versus the load current. The start voltage is defined as the input voltage required to regulate the output voltage with 1%. The stop voltage is defined as the input voltage at which the output drops by 5% or stops switching.

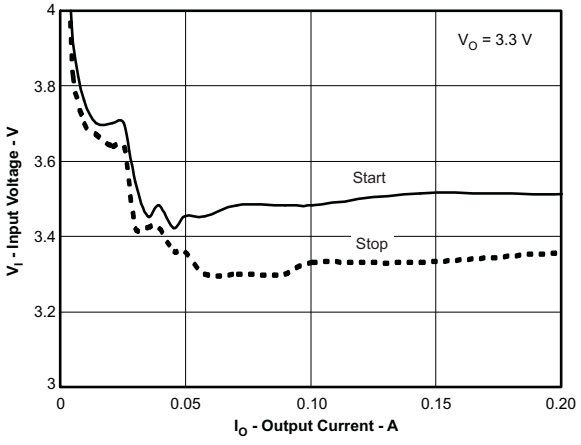


Figure 25. 3.3-V Start and Stop Voltage

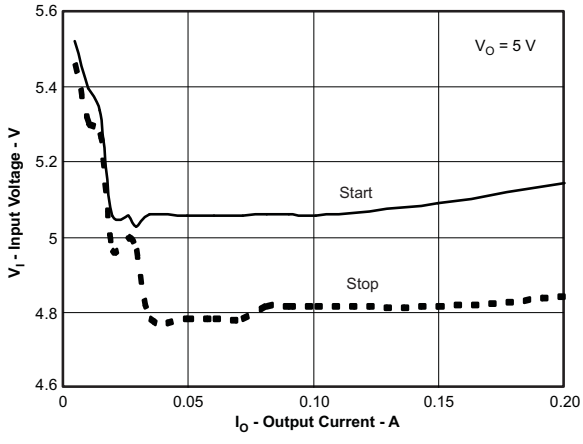


Figure 26. 5-V Start and Stop Voltage

Feature Description (continued)

8.3.5 Error Amplifier

The TPS54140 device has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the lower voltage of either the SS/TR pin voltage or the internal 0.8-V voltage reference. The transconductance (gm) of the error amplifier is 97 µA/V during normal operation. During the slow-start operation, the transconductance is a fraction of the normal operating gm. When the voltage of the VSENSE pin is below 0.8 V and the device is regulating using the SS/TR voltage, the gm is 26 µA/V.

The frequency compensation components (capacitor, series resistor, and capacitor) are added to the COMP pin to ground.

8.3.6 Voltage Reference

The voltage reference system produces a precise ±2% voltage reference over temperature by scaling the output of a temperature-stable bandgap circuit.

8.3.7 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. Using divider resistors with a tolerance of 1% or better is recommended. Begin with a value of 10 kΩ for the R2 resistor and use Equation 1 to calculate the value of R1. To improve efficiency at very light loads, consider using larger value resistors. If the values are too high the regulator will be more susceptible to noise and voltage errors from the VSENSE input current will be noticeable

$$R1 = R2 \times \left(\frac{(V_{OUT} - 0.8\,V)}{0.8\,V} \right) \quad (1)$$

8.3.8 Enable and Adjusting Undervoltage Lockout

The TPS54140 device is disabled when the VIN pin voltage falls below 2.5 V. If an application requires a higher undervoltage lockout (UVLO), use the EN pin as shown in Figure 27 to adjust the input voltage UVLO by using the two external resistors. Using the UVLO to adjust registers is not required but is highly recommended for operation to provide consistent power-up behavior. The EN pin has an internal pullup-current source, I1, of 0.9 µA that provides the default condition of the TPS54140 device while operating when the EN pin is floating. When the EN pin voltage exceeds 1.25 V, an additional 2.9 µA of hysteresis, Ihys, is added. This additional current facilitates input voltage hysteresis. Use Equation 2 to calculate R1 which sets the external hysteresis for the input voltage. Use Equation 3 to calculate R2 which sets the input start voltage.

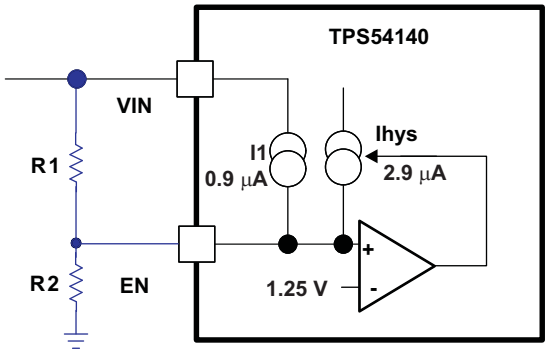


Figure 27. Adjustable Undervoltage Lockout (UVLO)

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS}} \quad (2)$$

$$R2 = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R1} + I_1} \quad (3)$$

Feature Description (continued)

Figure 28 shows another technique for adding input voltage hysteresis. This method can be used if the resistance values are high from the previous method and a wider voltage hysteresis is needed. The resistor, R3, sources additional hysteresis current into the EN pin.

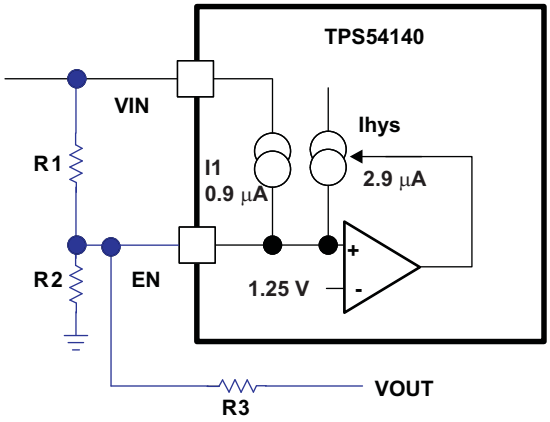


Figure 28. Adding Additional Hysteresis

$$R1 = \frac{V_{START} - V_{STOP}}{I_{HYS} + \frac{V_{OUT}}{R3}} \quad (4)$$

$$R2 = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R1} + I_1 - \frac{V_{ENA}}{R3}} \quad (5)$$

8.3.9 Slow Start and Tracking Pin (SS/TR)

The TPS54140 device effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage of the power supply and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow-start time. The TPS54140 device has an internal pullup-current source of 2 µA that charges the external slow-start capacitor. Use Equation 6 to calculate the value of the slow-start capacitor, C_{SS}, which sets the slow-start time, t_{SS} (10% to 90%). The slow-start capacitor should remain lower than 0.47µF and greater than 0.47nF.

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V) \times 0.8} \quad (6)$$

where

- The voltage reference (V_{REF}) is 0.8 V
- The slow start current (I_{SS}) is 2 µA

At power up, the TPS54140 device does not begin switching until the slow-start pin is discharged to less than 40 mV to ensure a proper power up (see Figure 29).

Also, during normal operation, the TPS54140 device stops switching and the SS/TR must be discharged to 40 mV when the voltage at the VIN pin is below the VIN UVLO, EN pin pulled below 1.25 V, or a thermal shutdown event occurs.

The VSENSE voltage follows the SS/TR pin voltage with a 45-mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% on the internal reference voltage the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference (see Figure 23). The SS/TR voltage ramps linearly until clamped at 1.7 V.

Feature Description (continued)

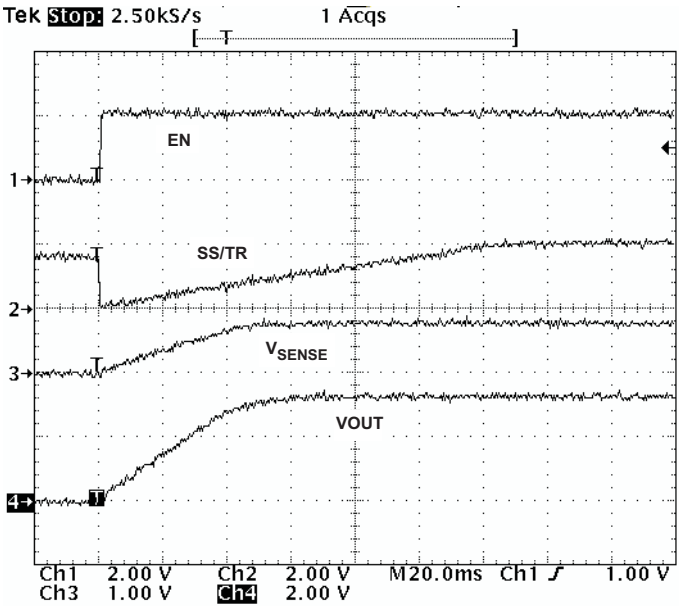


Figure 29. Operation of SS/TR Pin When Starting

8.3.10 Overload-Recovery Circuit

The TPS54140 device has an overload-recovery (OLR) circuit. The OLR circuit slow starts the output from the overload voltage to the nominal regulation voltage when the fault condition is removed. The OLR circuit discharges the SS/TR pin to a voltage slightly greater than the VSENSE pin voltage using an internal pulldown of 100 µA when the error amplifier is changed to a high voltage from a fault condition. When the fault condition is removed, the output slow starts from the fault voltage to nominal output voltage.

8.3.11 Sequencing

Many of the common power-supply sequencing methods can be implemented using the SS/TR, EN, and PWRGD pins. The sequential method can be implemented using an open-drain output of the power-on reset pin of another device. Figure 30 shows the sequential method using two TPS54140 devices. The power good is coupled to the EN pin on the TPS54140 device which enables the second power supply when the primary supply reaches regulation. If needed, a 1-nF ceramic capacitor on the EN pin of the second power supply provides a 1-ms startup delay. Figure 31 shows the results of Figure 30.

Feature Description (continued)

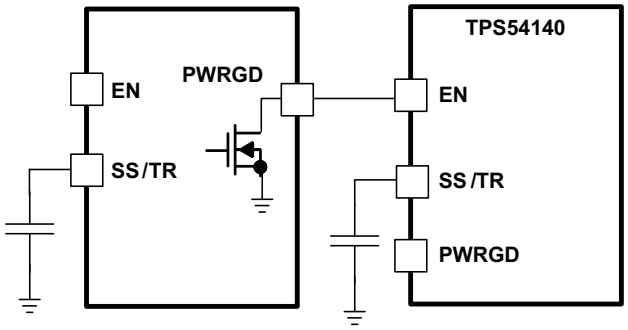


Figure 30. Schematic for Sequential Startup Sequence

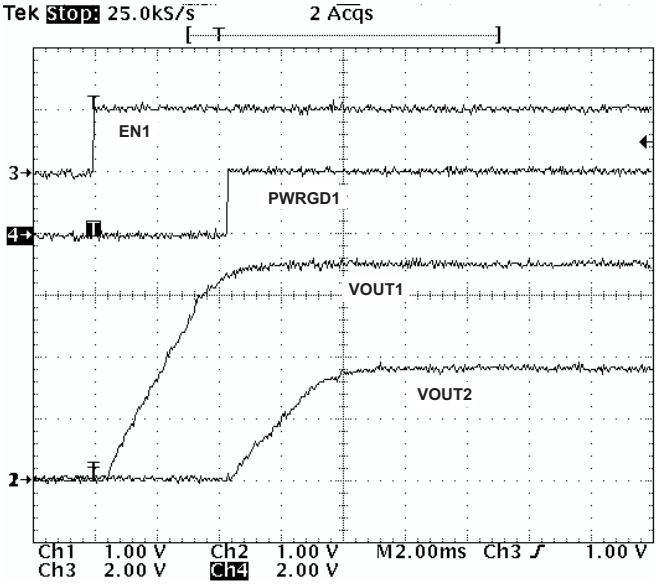


Figure 31. Sequential Startup using EN and PWRGD

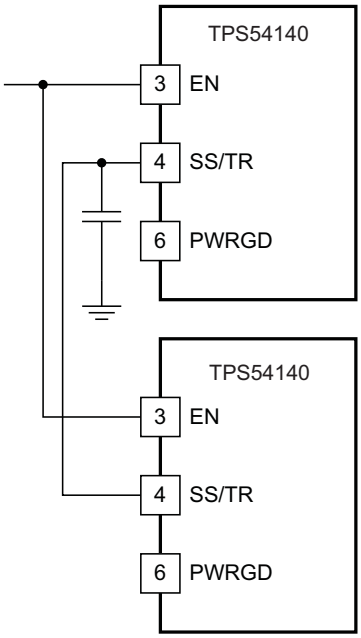


Figure 32. Schematic for Ratiometric Startup Sequence

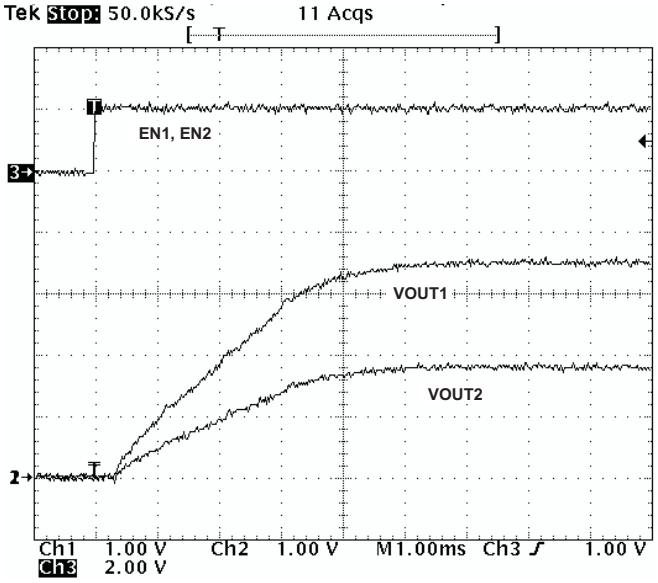


Figure 33. Ratio-Metric Startup using Coupled SS/TR pins

Figure 32 shows a method for ratiometric start up sequence by connecting the SS/TR pins together. The regulator outputs will ramp up and reach regulation at the same time. When calculating the slow-start time the pullup current source must be doubled in Equation 6. Figure 33 shows the results of Figure 32.

Feature Description (continued)

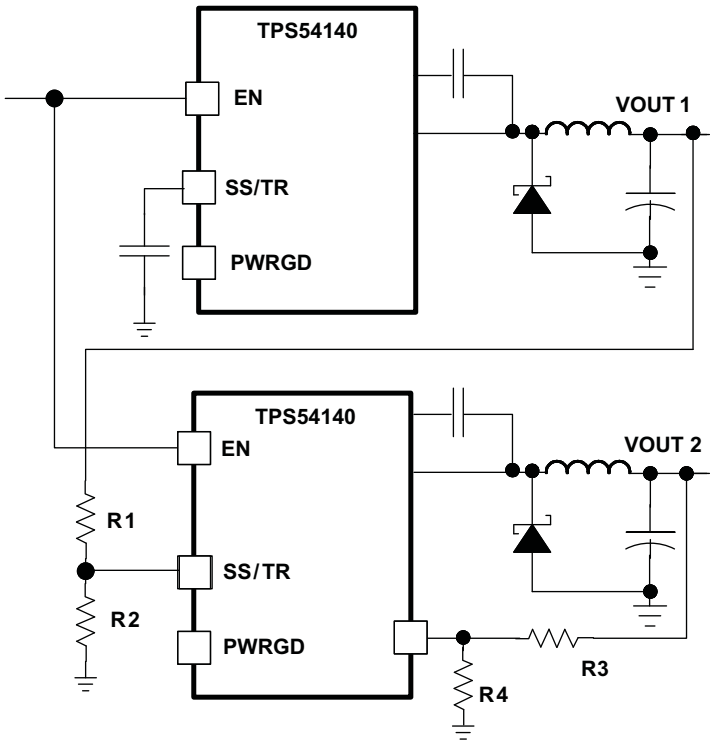


Figure 34. Schematic for Ratiometric and Simultaneous Startup Sequence

Ratiometric and simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in Figure 34 to the output of the power supply that needs to be tracked or another voltage reference source. Using Equation 7 and Equation 8, the tracking resistors can be calculated to initiate V_{OUT2} slightly before, after, or at the same time as V_{OUT1}. Equation 9 is the voltage difference between V_{OUT1} and V_{OUT2} at the 95% of nominal output regulation.

The ΔV variable is 0 V for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset ($V_{SS(offset)}$) in the slow-start circuit and the offset created by the pullup current source (I_{SS}) and tracking resistors. $V_{SS(offset)}$ and I_{SS} are included as variables in the equations.

To design a ratiometric startup in which the V_{OUT2} voltage is slightly greater than the V_{OUT1} voltage when V_{OUT2} reaches regulation, use a negative number in Equation 7 through Equation 9 for ΔV. Equation 9 results in a positive number for applications which the V_{OUT2} is slightly lower than V_{OUT1} when V_{OUT2} regulation is achieved.

Because the SS/TR pin must be pulled below 40 mV before starting after an EN, UVLO, or thermal shutdown fault, careful selection of the tracking resistors is needed to ensure the device restarts after a fault. To ensure the device can recover from a fault, the calculated value of R1 from Equation 7 must be greater than the value calculated in Equation 10.

As the SS/TR voltage becomes more than 85% of the nominal reference voltage, $V_{SS(offset)}$ becomes larger as the slow-start circuits gradually handoff the regulation reference to the internal voltage reference. The SS/TR pin voltage must be greater than 1.3 V for a complete handoff to the internal voltage reference as shown in Figure 23.

$$R1 = \frac{V_{OUT2} + \Delta V}{V_{REF}} + \frac{V_{SS(offset)}}{I_{SS}} \quad (7)$$

$$R2 = \frac{V_{REF} \times R1}{V_{OUT2} + \Delta V - V_{REF}} \quad (8)$$

$$\Delta V = V_{OUT1} - V_{OUT2} \quad (9)$$

Feature Description (continued)

$$R1 > 2800 \times V_{OUT1} - 180 \times \Delta V \quad (10)$$

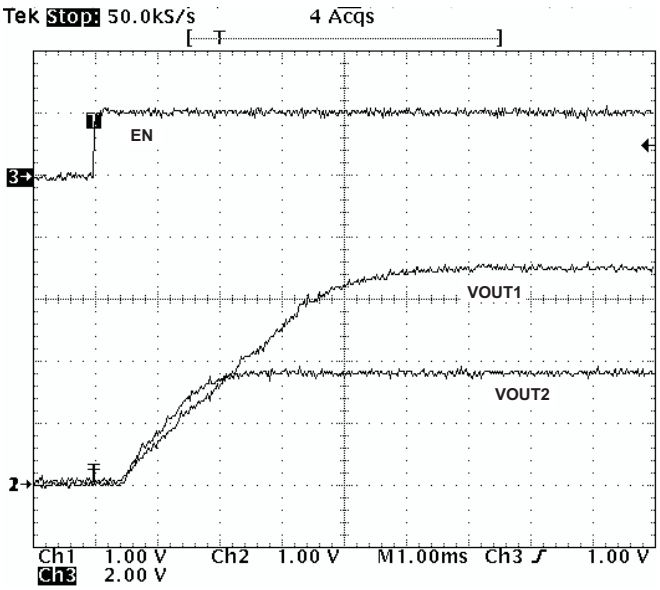


Figure 35. Ratiometric Startup with Tracking Resistors

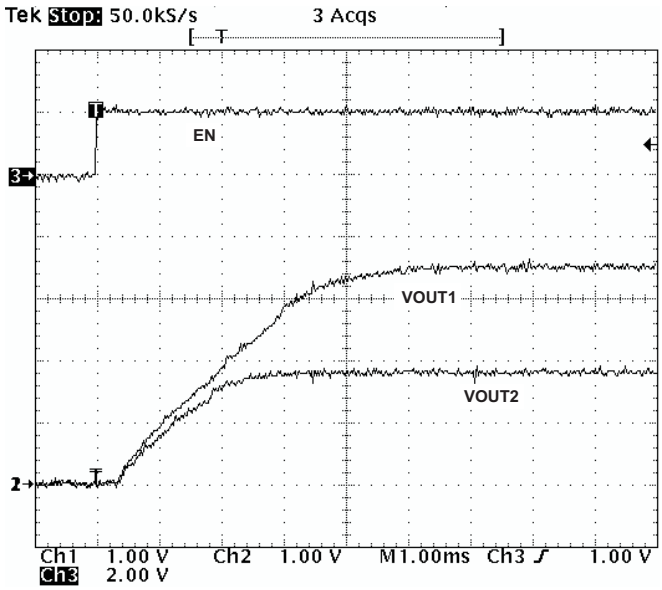


Figure 36. Ratiometric Startup with Tracking Resistors

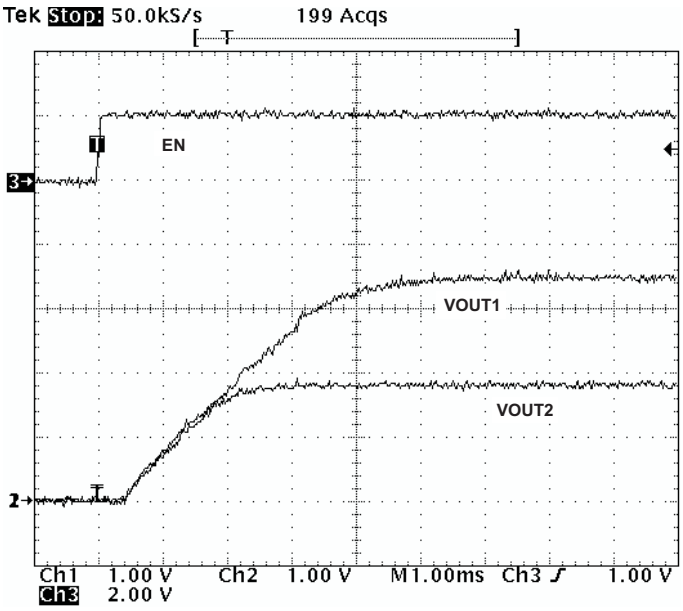


Figure 37. Simultaneous Startup With Tracking Resistor

Feature Description (continued)

8.3.12 Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS54140 device is adjustable over a wide range from approximately 100 kHz to 2500 kHz by placing a resistor on the RT/CLK pin. The RT/CLK pin voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 11 or the curves in Figure 38 or Figure 39. To reduce the solution size, a user typically sets the switching frequency as high as possible, but tradeoffs of the supply efficiency, maximum input voltage and minimum controllable on time should be considered.

The minimum controllable on time is 130 ns (typical) and limits the maximum operating input voltage.

The maximum switching frequency is also limited by the frequency shift circuit. The following sections describe the maximum switching frequency in detail.

$$R_{RT}\left(k\Omega\right) = \frac{206033}{f_{SW}\left(kHz\right)^{1.0888}} \tag{11}$$

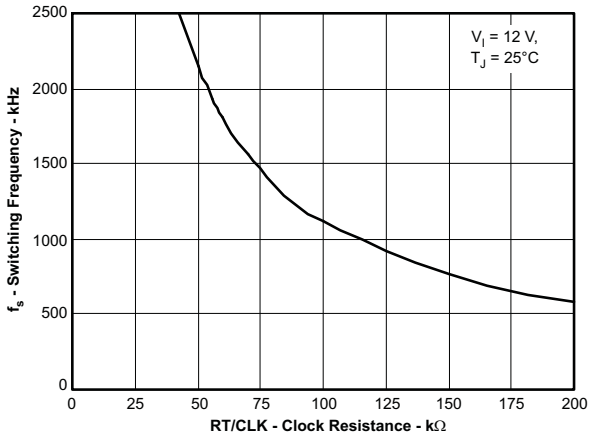


Figure 38. High Range RT

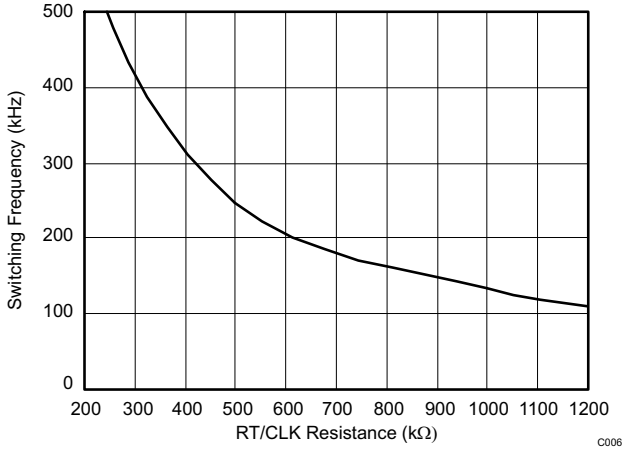


Figure 39. Low Range RT

8.3.13 Overcurrent Protection and Frequency Shift

The TPS54140 device implements current mode control which uses the COMP pin voltage to turn off the high-side MOSFET on a cycle-by-cycle basis. During each cycle the switch current and COMP pin voltage are compared. When the peak inductor current intersects the COMP pin voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, causing the switch current to increase. The COMP pin has a maximum clamp internally, which limits the output current.

To increase the maximum operating switching frequency at high input voltages the TPS54140 device implements a frequency shift. The switching frequency is divided by 8, 4, 2, and 0 as the voltage ramps from 0 to 0.8 V on VSENSE pin.

The device implements a digital frequency shift to enable synchronizing to an external clock during normal startup and fault conditions. Because the device can only divide the switching frequency by 8 at the most, a maximum input voltage limit exists in which the device can operate and still have frequency shift protection.

During short-circuit events (particularly with high input-voltage applications), the control loop has a finite, minimum controllable on time and the output has a very low voltage. During the switch on time, the inductor current ramps to the peak current limit because of the high input voltage and minimum on time. During the switch off time, the inductor would normally not have enough off time and output voltage for the inductor to ramp down by the ramp up amount. The frequency shift effectively increases the off time allowing the current to ramp down.

Feature Description (continued)

8.3.14 Selecting the Switching Frequency

The switching frequency that is selected should be the lower value of the Equation 12 and Equation 13. Use Equation 12 to calculate the maximum switching frequency limitation set by the minimum controllable on time. Setting the switching frequency above this value causes the regulator to skip switching pulses.

Use Equation 13 to calculate the maximum switching-frequency limit set by the frequency shift protection. For adequate output short-circuit protection at high input voltages, the switching frequency should be set to a value less than the $f_{sw(maxshift)}$ frequency. In Equation 13, to calculate the maximum switching frequency, consider that the output voltage decreases from the nominal voltage to 0 V and that the f_{div} integer increases from 1 to 8 corresponding to the frequency shift.

In Figure 40, the solid line indicates a typical, safe operating area in regard to frequency shift. The following assumptions can be made: the output voltage is 0 V, the resistance of the inductor is 0.1 Ω, the FET on-resistance is 0.2 Ω, and the diode voltage drop is 0.5 V. The dashed line indicates the maximum switching frequency to avoid pulse skipping. Enter these equations in a spreadsheet or software to determine the switching frequency. Texas Instrument's WEBENCH software tool can also be used to determine the switching frequency.

$$f_{SW(max\,skip)} = \frac{1}{t_{on(min)}} \times \left(\frac{I_L \times R_{dc} + V_{OUT} + V_d}{V_{IN} - I_L \times R_{DS(on)} + V_d} \right) \quad (12)$$

where

- $t_{on(min)}$ is the minimum controllable on time
- I_L is the inductor current
- R_{dc} is the inductor resistance
- V_{OUT} is the output voltage
- V_d is the diode voltage drop
- $R_{DS(on)}$ is the switch on resistance

$$f_{SW(shift)} = \frac{f_{SW(DIV)}}{t_{on(min)}} \times \left(\frac{I_L \times R_{dc} + V_{OUT(SC)} + V_d}{V_{IN} - I_L \times R_{DS(on)} + V_d} \right) \quad (13)$$

where

- f_{DIV} is the frequency divide (equal to 1, 2, 4, or 8)
- $V_{OUT(sc)}$ is the output voltage during a short

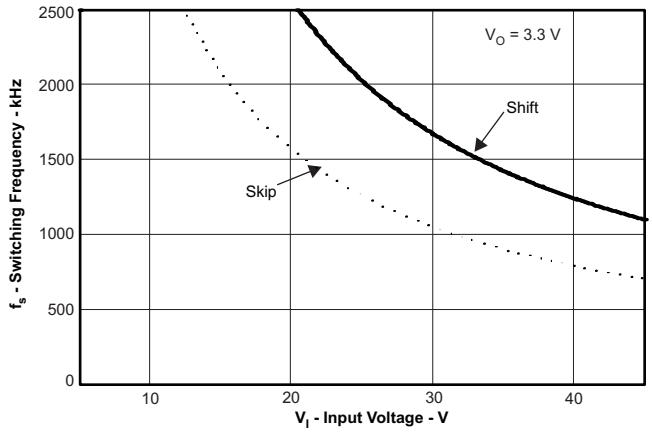


Figure 40. Maximum Switching Frequency vs. Input Voltage

Feature Description (continued)

8.3.15 How to Interface to RT/CLK Pin

The RT/CLK pin can be used to synchronize the regulator to an external system clock. To implement the synchronization feature connect a square wave to the RT/CLK pin through the circuit network shown in Figure 41. The square wave amplitude must transition lower than 0.5 V and higher than 2.2 V on the RT/CLK pin and have an on time greater than 40 ns and an off time greater than 40 ns. The synchronization frequency range is 300 kHz to 2200 kHz. The rising edge of the PH pin synchronizes to the falling edge of RT/CLK signal. The external synchronization circuit should be designed in such a way that the device has the default-frequency set resistor connected from the RT/CLK pin to ground if the synchronization signal turns off. Using a frequency set resistor connected through a 50-Ω resistor to ground is recommended as shown in Figure 41. The resistor should set the switching frequency close to the external CLK frequency. TI recommends to AC couple the synchronization signal through a 10-pF ceramic capacitor to the RT/CLK pin and a 4-kΩ series resistor. The series resistor reduces PH jitter in heavy load applications when synchronizing to an external clock and in applications which transition from synchronizing to RT mode. The first time the CLK is pulled above the CLK threshold the device switches from the RT resistor frequency to PLL mode. The internal 0.5-V voltage source is removed and the CLK pin becomes high impedance as the PLL begins to lock onto the external signal. Because the regulator has a PLL, the switching frequency can be higher or lower than the frequency set with the external resistor. The device transitions from the resistor mode to the PLL mode and then increases or decreases the switching frequency until the PLL locks onto the CLK frequency within 100 ms.

When the device transitions from the PLL to resistor mode, the switching frequency slows down from the CLK frequency to 150 kHz and then reapplies the 0.5-V voltage. The resistor then sets the switching frequency. The switching frequency is divided by 1, 2, 4, and 8 as the voltage ramps from 0 to 0.8 V on VSENSE pin. The device implements a digital frequency shift to enable synchronizing to an external clock during normal startup and fault conditions. Figure 42, Figure 43 and Figure 44 show the device synchronized to an external system clock in continuous conduction mode (CCM) discontinuous conduction (DCM) and pulse-skip mode (PSM).

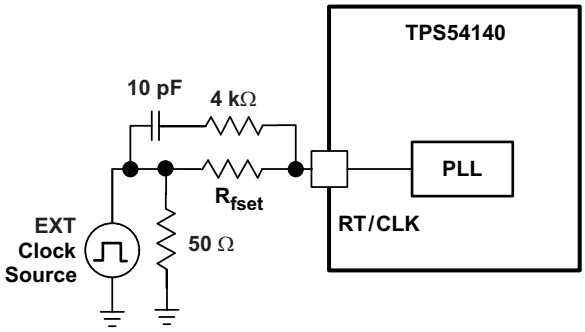


Figure 41. Synchronizing to a System Clock

Feature Description (continued)

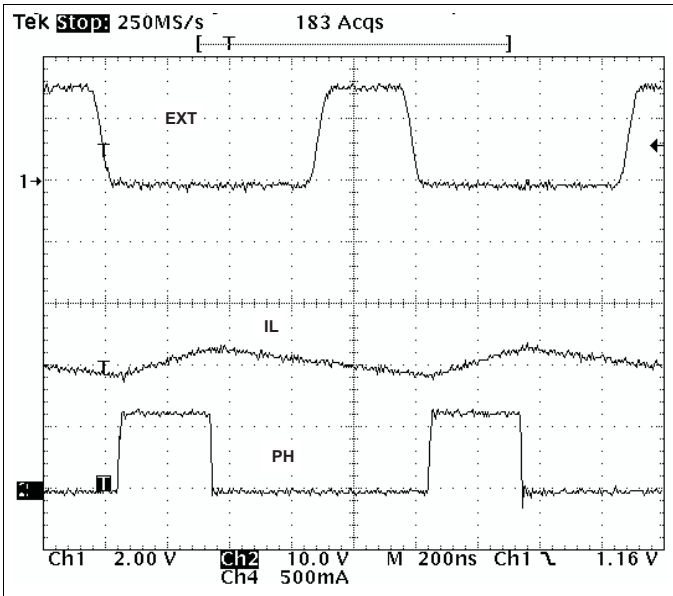


Figure 42. Plot of Synchronizing in CCM

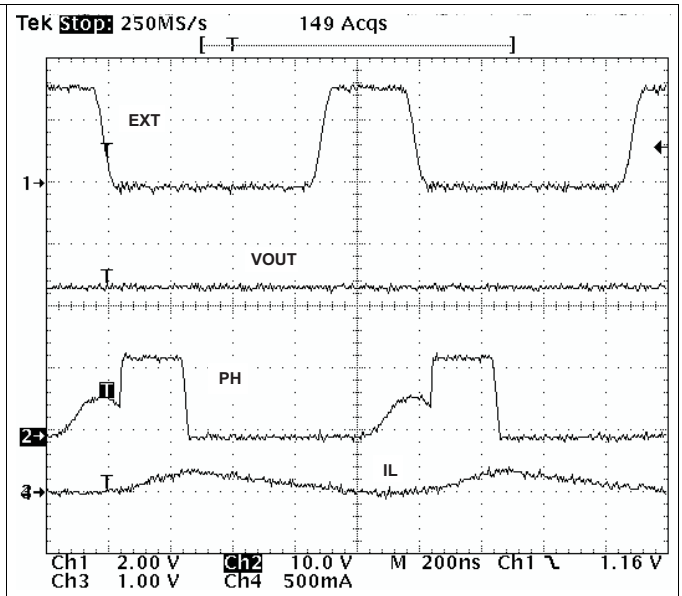


Figure 43. Plot of Synchronizing in DCM

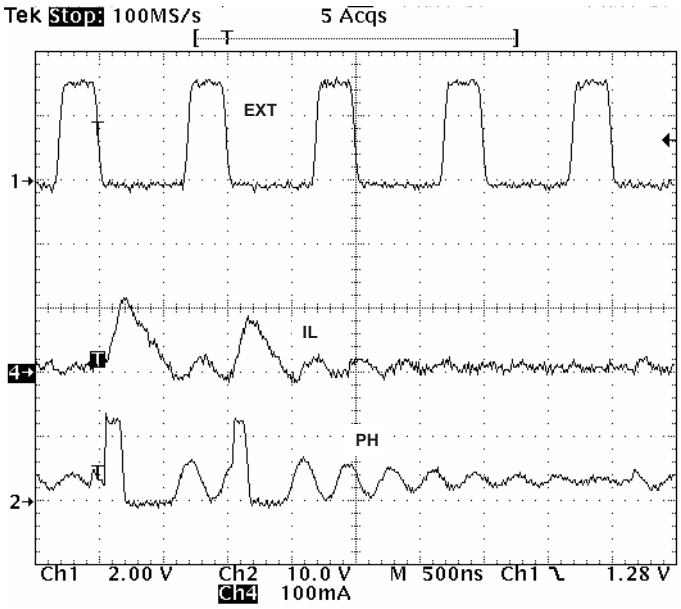


Figure 44. Plot of Synchronizing in PSM

8.3.16 Power Good (PWRGD Pin)

The PWRGD pin is an open drain output. When the VSENSE pin is between 94% and 107% of the internal voltage reference, the PWRGD pin is deasserted and the pin floats. Using a pullup resistor with a value between 10 and 100 kΩ connected to a voltage source that is 5.5 V or less is recommended. The PWRGD pin is in a defined state when the VIN input voltage is greater than 1.5 V but has reduced current sinking capability. The PWRGD achieves full current-sinking capability as the VIN input voltage approaches 3 V.

The PWRGD pin is pulled low when the VSENSE pin is lower than 92% or greater than 109% of the nominal internal reference voltage. Also, the PWRGD pin is pulled low if the UVLO or thermal shutdown are asserted or the EN pin is pulled low.

Feature Description (continued)

8.3.17 Overvoltage Transient Protection

The TPS54140 device incorporates an overvoltage transient-protection (OVTP) circuit to minimize voltage overshoot when recovering from output-fault conditions or strong unload transients on power-supply designs with low-value output capacitance. For example, when the power-supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier responds by clamping the error amplifier output to a high voltage. Thus, requesting the maximum output current. When the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state duty cycle. In some applications, the power-supply output voltage can respond faster than the error-amplifier output can respond which leads to the possibility of an output overshoot. The OVTP feature minimizes the output overshoot when using a low-value output capacitor by implementing a circuit to compare the VSENSE pin voltage to OVTP threshold which is 109% of the internal voltage reference. If the VSENSE pin voltage is greater than the OVTP threshold, the high-side MOSFET is disabled which prevents current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVTP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

8.3.18 Thermal Shutdown

The device implements an internal thermal shutdown to protect the device if the junction temperature exceeds 182°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. When the die temperature decreases below 182°C, the device reinitiates the power-up sequence by discharging the SS/TR pin.

8.3.19 Small-Signal Model for Loop Response

Figure 45 shows an equivalent model for the TPS54140 control loop which can be modeled in a circuit simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm_{EA} of 97 µA/V. The error amplifier can be modeled using an ideal voltage-controlled current source. The resistor, R_O, and capacitor, C_O, model the open loop gain and frequency response of the amplifier. The 1-mV AC voltage source between the nodes *a* and *b* effectively breaks the control loop for the frequency response measurements. Plotting *c-a* shows the small-signal response of the frequency compensation. Plotting *a-b* shows the small-signal response of the overall loop. The dynamic loop response can be checked by replacing R_L with a current source that has the appropriate load-step amplitude and step rate in a time domain analysis. This equivalent model is only valid for continuous-conduction mode designs.

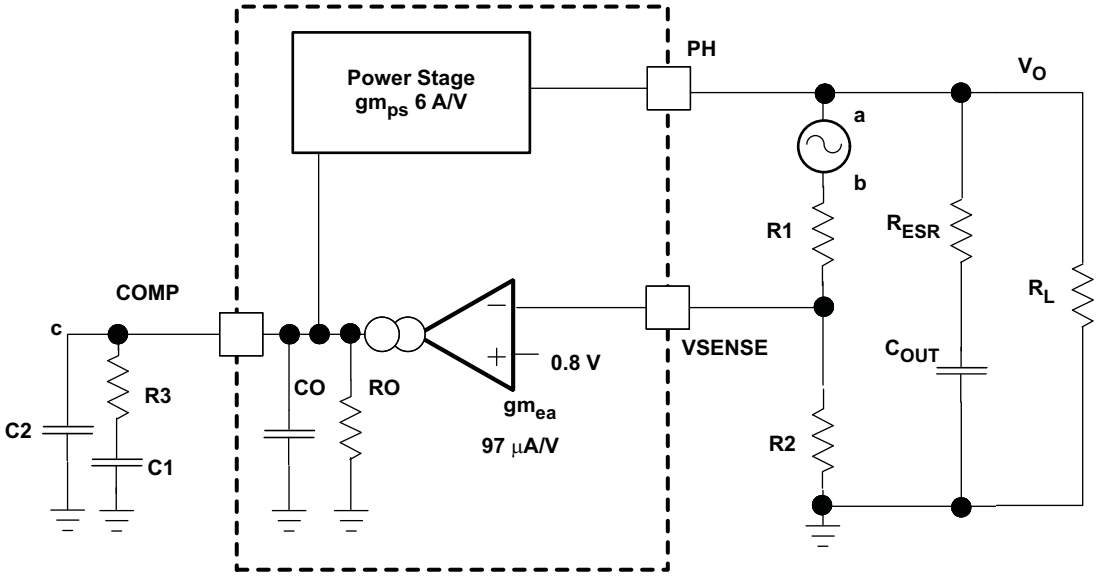


Figure 45. Small-Signal Model for Loop Response

Feature Description (continued)

8.3.20 Simple Small-Signal Model for Peak-Current Mode Control

Figure 46 describes a simple small-signal model that can be used to understand how to design the frequency compensation. The TPS54140 power stage can be approximated to a voltage-controlled current source (duty-cycle modulator) that supplies current to the output capacitor and load resistor. Equation 14 shows the control to the output transfer function and consists of a DC gain, one dominant pole, and one ESR zero. The quotient of the change in the switch current and the change in the COMP pin voltage (node *c* in Figure 45) is the power stage transconductance. The gm_{PS} for the TPS54140 device is 6 A/V. The low-frequency gain of the power-stage frequency response is the product of the transconductance and the load resistance as shown in Equation 15.

As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load may seem problematic at first glance, but fortunately the dominant pole moves with the load current (see Equation 16). The combined effect is highlighted by the dashed line in the right half of Figure 46. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes designing the frequency compensation easier. The type of selected output capacitor determines whether the ESR zero has a profound effect on the frequency compensation design. Using high ESR aluminum electrolytic capacitors may reduce the number frequency compensation components needed to stabilize the overall loop because the phase margin increases from the ESR zero at the lower frequencies (see Equation 17).

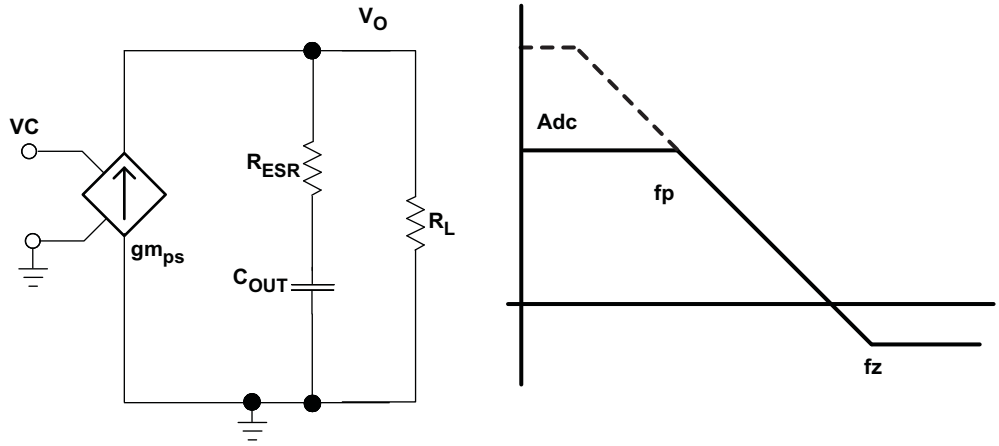


Figure 46. Simple Small-Signal Model and Frequency Response for Peak-Current Mode Control

$$\frac{V_{OUT}}{V_C} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \quad (14)$$

$$Adc = gm_{ps} \times R_L \quad (15)$$

$$f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (16)$$

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (17)$$

Feature Description (continued)

8.3.21 Small-Signal Model for Frequency Compensation

The TPS54140 device uses a transconductance amplifier for the error amplifier and readily supports three of the commonly-used frequency compensation circuits. Compensation circuits Type 2A, Type 2B, and Type 1 are shown in Figure 47. Type 2 circuits most likely implemented in high bandwidth power-supply designs using low ESR output capacitors. The Type 1 circuit is used with power-supply designs with high-ESR aluminum electrolytic or tantalum capacitors. Equation 18 and Equation 19 show how to relate the frequency response of the amplifier to the small-signal model in Figure 47. Figure 47 shows the open-loop gain and bandwidth are modeled using R_O and C_O. See the *Typical Application* section for a design example using a Type 2A network with a low-ESR output capacitor.

Equation 18 through Equation 27 are provided as a reference for those who prefer to compensate using their preferred methods. Those who prefer to use prescribed method can use the method outlined in the *Typical Application* section or use switched information.

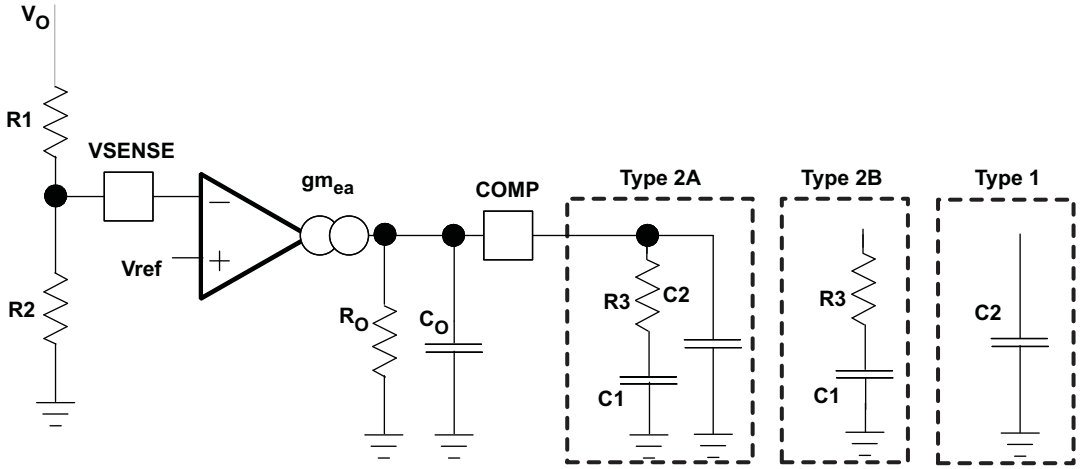


Figure 47. Types of Frequency Compensation

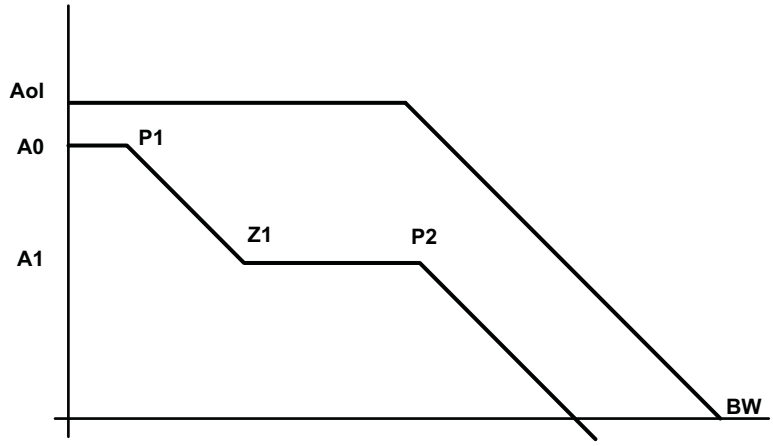


Figure 48. Frequency Response of the Type 2A and Type 2B Frequency Compensation

$$Ro = \frac{AoI(V/V)}{gm_{ea}} \quad (18)$$

$$C_{OUT} = \frac{gm_{ea}}{2\pi \times BW\ (Hz)} \quad (19)$$

Feature Description (continued)

$$EA = A0 \times \frac{\left(1 + \frac{s}{2\pi \times f_{Z1}}\right)}{\left(1 + \frac{s}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{P2}}\right)} \quad (20)$$

$$A0 = gm_{ea} \times Ro \times \frac{R2}{R1 + R2} \quad (21)$$

$$A1 = gm_{ea} \times Ro \| R3 \times \frac{R2}{R1 + R2} \quad (22)$$

$$P1 = \frac{1}{2\pi \times Ro \times C1} \quad (23)$$

$$Z1 = \frac{1}{2\pi \times R3 \times C1} \quad (24)$$

$$P2 = \frac{1}{2\pi \times R3 \| R \times (C2 + C_{OUT})} \text{ type 2a} \quad (25)$$

$$P2 = \frac{1}{2\pi \times R3 \| R \times C_{OUT}} \text{ type 2b} \quad (26)$$

$$P2 = \frac{1}{2\pi \times R \times (C2 + C_{OUT})} \text{ type 1} \quad (27)$$

8.4 Device Functional Modes

8.4.1 Pulse Skip Eco-mode

The TPS54140 device enters the pulse-skip mode when the voltage on the COMP pin is the minimum clamp value. The TPS54140 device operates in a pulse-skip mode at light-load currents to improve efficiency. The peak switch current during the pulse-skip mode is the greater value of either 50 mA or the peak inductor current that is a function of the minimum on time, input voltage, output voltage, and inductance value. When the load current is low and the output voltage is within regulation the device enters a sleep mode and draws only 116-µA input quiescent current. While the device is in sleep mode the output power is delivered by the output capacitor. As the load current decreases, the time the output capacitor supplies the load current increases and the switching frequency decreases reducing gate drive and switching losses. As the output voltage drops, the TPS54140 device wakes up from the sleep mode and the power switch turns on to recharge the output capacitor (see Figure 49). The internal PLL remains operating when in sleep mode. When operating at light-load currents in the pulse-skip mode the switching transitions occur synchronously with the external clock signal.

Device Functional Modes (continued)

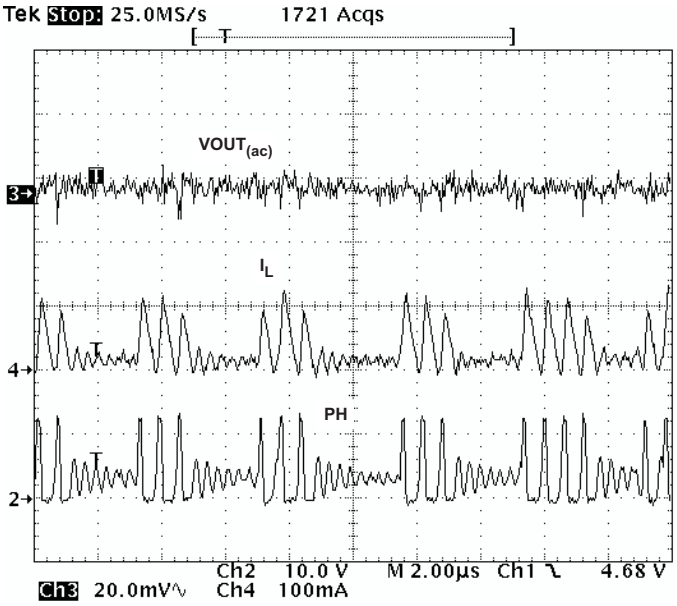


Figure 49. Pulse-Skip Mode Operation

8.4.2 Operation With V_{IN} < 3.5 V

The device is recommended to operate with input voltages above 3.5 V. The typical VIN UVLO threshold is not specified and the device can operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage, the device does not switch. If the EN pin is externally pulled up or left floating, the device becomes active when the VIN pin passes the UVLO threshold. Switching begins when the slow-start sequence is initiated.

8.4.3 Operation With EN Control

The enable threshold voltage is 1.25 V (typical). With the EN pin is held below that voltage the device is disabled and switching is inhibited even if the VIN pin is above the UVLO threshold. The IC quiescent current is reduced in this state. If the EN voltage increases above the threshold while the VIN pin is above the UVLO threshold, the device becomes active. Switching is enabled, and the slow-start sequence is initiated.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS54140 device is typically used as a step-down converter, which converts a voltage from 3.5 V to 42 V to a lower voltage. WEBENCH software is available to aid in the design and analysis of circuits.

9.2 Typical Application

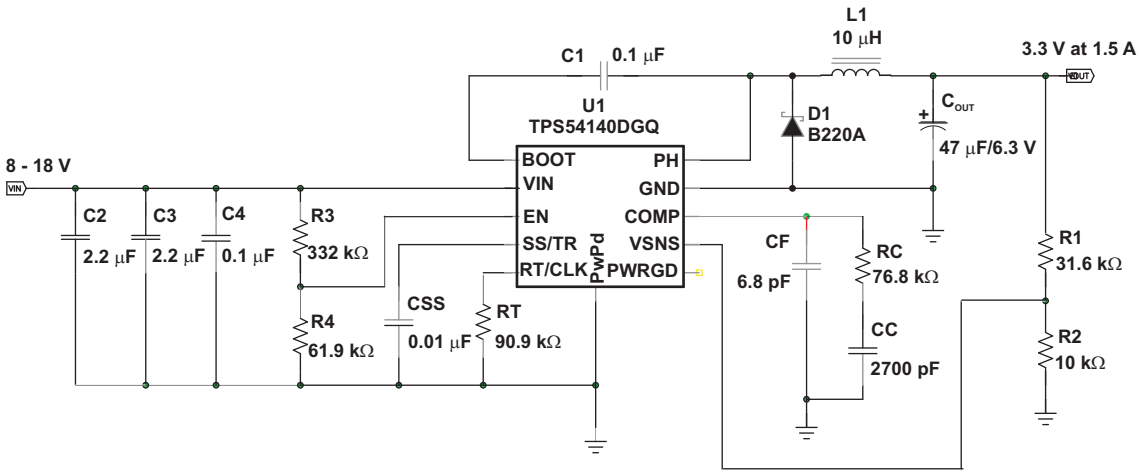


Figure 50. High Frequency, 3.3-V Output Power Supply Design With Adjusted UVLO

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Output voltage	3.3 V
Transient response 0 to 1.5-A load step	ΔV_{OUT} = 4%
Maximum output current	1.5 A
Input voltage	12 V nominal, 8 to 18 V
Output voltage ripple	< 33 mV_{pp}
Start input voltage (rising VIN)	7.7 V
Stop input voltage (falling VIN)	6.7 V

9.2.2 Detailed Design Procedure

This example details the design of a high-frequency switching-regulator design using ceramic output capacitors. A few parameters must be known to start the design process. These parameters are typically determined at the system level.

9.2.2.1 Selecting the Switching Frequency

The first step of the design process is to decide on a switching frequency for the regulator. Typically, the user selects the highest switching frequency possible because it produces the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage, and the output voltage and the frequency shift limitation.

Equation 12 and Equation 13 must be used to find the maximum switching frequency for the regulator. Select the lower value of the two equations. Switching frequencies higher than these values result in pulse skipping or the lack of overcurrent protection during a short circuit.

The typical minimum on time, t_{onmin}, is 130 ns for the TPS54140 device. For this example, the output voltage is 3.3 V and the maximum input voltage is 18 V, which allows for a maximum switch frequency up to 1600 kHz when including the inductor resistance, on resistance, and diode voltage in Equation 12. To ensure that overcurrent runaway is not a concern during short circuits in the design use Equation 13 or the solid curve in Figure 40 to determine the maximum switching frequency. The maximum switching frequency is approximately 1600 kHz with a maximum input voltage of 20 V and assuming the following: a diode voltage of 0.5 V, inductor resistance of 100 mΩ, switch resistance of 200 mΩ, and an output current of 2.8 A.

Selecting the lower of the two values and adding some margin, a switching frequency of 1200 kHz is used. To determine the timing resistance for a given switching frequency, use Equation 11 or the curve in Figure 38.

The switching frequency is set by resistor R_t shown in Figure 50.

9.2.2.2 Output Inductor Selection (L_O)

Use Equation 28 to calculate the minimum value of the output inductor.

$$L_{O(min)} = \frac{V_{IN(max)} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} \quad (28)$$

where

- K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current

The inductor ripple current is filtered by the output capacitor. Therefore, selecting high inductor ripple currents impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, the following guidelines may be used.

For designs using low-ESR output capacitors such as ceramics, a value as high as K_{IND} = 0.3 can be used. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results. Because the inductor ripple current is part of the PWM control system, the inductor ripple current should always be greater than 100 mA for dependable operation. In a wide input voltage regulator, selecting an inductor ripple current on the larger side is best which allows the inductor to still have a measurable ripple current with the input voltage at the minimum.

For this design example, use K_{IND} = 0.2 and the minimum inductor value which is calculated as 7.6 µH. For this design, the nearest standard value of 10 µH was selected. For the output filter inductor, the RMS current and saturation current ratings must not be exceeded. Use Equation 30 to calculate the inductor ripple current, I_{RIPPLE}.

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_O \times f_{SW}} \quad (29)$$

Use Equation 30 to calculate the RMS inductor current, $I_{L(rms)}$.

$$I_{L(rms)} = \sqrt{(I_{OUT})^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_O \times f_{SW}} \right)^2} \quad (30)$$

Use Equation 31 to calculate the peak inductor current.

$$I_{L(peak)} = I_{OUT} + \frac{I_{RIPPLE}}{2} \quad (31)$$

For this design, the RMS inductor current is 1.506 A and the peak inductor current is 1.62 A. The selected inductor is a MSS6132-103 and has a saturation current rating of 1.64 A and an RMS current rating of 1.9 A.

As the equation set demonstrates, lower ripple currents reduce the output voltage ripple of the regulator but require a larger value of inductance. Selecting higher ripple currents increases the output voltage ripple of the regulator but allows for a lower inductance value.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the peak-inductor current level that was calculated using Equation 31. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation-current rating equal to or greater than the switch current limit rather than the peak inductor current.

9.2.2.3 Output Capacitor

Consider three primary factors when selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance must be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the regulator cannot. This situation occurs if the desired hold-up times are present for the regulator. In this case, the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily unable to supply sufficient output current if a large, fast increase occurs affecting the current requirements of the load, such as a transition from no load to full load. The regulator usually requires two or more clock cycles for the control loop to notice the change in load current and output voltage and to adjust the duty cycle to react to the change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Use Equation 32 to calculate the minimum output capacitance required to supply the difference in current.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}}$$

where

- ΔI_{OUT} is the change in output current
- f_{SW} is the regulators switching frequency
- ΔV_{OUT} is the allowable change in the output voltage (32)

For this example, the transient load response is specified as a 4% change in V_{OUT} for a load step from 0 A (no load) to 1.5 A (full load). For this example, ΔI_{OUT} = 1.5 – 0 = 1.5 A and ΔV_{OUT} = 0.04 × 3.3 = 0.132 V. Using these values results in a minimum capacitance of 18.9 µF. This value does not consider the ESR of the output capacitor in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR which should be taken into consideration.

The catch diode of the regulator cannot sink current and therefore any stored energy in the inductor produces an output-voltage overshoot when the load current rapidly decreases (see Figure 51). The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. The excess energy that is stored in the output capacitor increases the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Use Equation 33 to calculate the minimum capacitance to keep the output voltage overshoot to a desired value.

$$C_{OUT} > L_O \times \frac{\left((I_{OH})^2 - (I_{OL})^2\right)}{\left((V_f)^2 - (V_i)^2\right)}$$

where

- L is the value of the inductor
- I_{OH} is the output current under heavy load
- I_{OL} is the output under light load
- V_f is the final peak output voltage
- V_i is the initial capacitor voltage

(33)

For this example, the worst-case load step is be from 1.5 A to 0 A. The output voltage increases during this load transition and the stated maximum in the specification is 4% of the output voltage. Therefore V_f = 1.04 × 3.3 = 3.432. The initial capacitor voltage, V_i, is the nominal output voltage of 3.3 V. Using these values in Equation 33 yields a minimum capacitance of 25.3 µF.

Use Equation 34 to calculate the minimum output capacitance required to meet the output voltage ripple specification.

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\left(\frac{V_{OUT(ripple)}}{I_{RIPPLE}}\right)}$$

where

- f_{SW} is the switching frequency
- $V_{OUT(ripple)}$ is the maximum allowable output voltage ripple
- I_{RIPPLE} is the inductor ripple current

(34)

Equation 35 yields 0.7µF.

Use Equation 35 to calculate the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. Equation 35 indicates the ESR should be less than 144 mΩ.

$$R_{ESR} = \frac{V_{OUT(ripple)}}{I_{RIPPLE}}$$

(35)

The most stringent criterion for the output capacitor is 25.3 µF of capacitance to maintain the output voltage in regulation during an unload transient.

Additional capacitance deratings for aging, temperature, and DC bias should be considered which increases this minimum value. For this example, a 47-µF 6.3-V X7R ceramic capacitor with 5 mΩ of ESR is used.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the root-mean-square (RMS) value of the maximum ripple current. Use Equation 36 to calculate the RMS ripple current that the output capacitor must support. For this application, Equation 36 yields 66 mA.

$$I_{COUT(rms)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{\sqrt{12} \times V_{IN(max)} \times L_O \times f_{SW}}$$

(36)

9.2.2.4 Catch Diode

The TPS54140 device requires an external catch diode between the PH and GND pins. The selected diode must have a reverse voltage rating equal to or greater than $V_{IN(max)}$. The peak current rating of the diode must be greater than the maximum inductor current. The diode should also have a low forward voltage. Schottky diodes are typically a good choice for the catch diode because of the low forward voltage of these diodes. The lower the forward voltage of the diode, the higher the efficiency of the regulator will be.

Typically, the higher the voltage and current ratings of the diode, the higher the forward voltage will be. Because the design example has an input voltage up to 18 V, a diode with a minimum of 20-V reverse voltage is selected.

For the example design, the B220A Schottky diode is selected because of the lower forward voltage and because it comes in a larger package size which has good thermal characteristics over small devices. The typical forward voltage of the B220A is 0.5 V.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode which equals the conduction losses of the diode. At higher switch frequencies, the AC losses of the diode must be considered. The AC losses of the diode are because of the charging and discharging of the junction capacitance and reverse recovery. Use Equation 37 to calculate the total power dissipation, conduction losses, and AC losses of the diode.

The B220A diode has a junction capacitance of 120 pF. Using Equation 37, the selected diode dissipates 0.632 W. Depending on mounting techniques, this power dissipation should produce a 16°C temperature rise in the diode when the input voltage is 18 V and the load current is 1.5 A.

If the power supply spends a significant amount of time at light-load currents or in sleep mode, consider using a diode that has a low leakage current and slightly-higher forward-voltage drop.

$$P_D = \frac{\left(V_{IN(max)} - V_{OUT}\right) \times I_{OUT} \times Vfd}{V_{IN(max)}} + \frac{C_j \times f_{SW} \times \left(V_{IN} + Vfd\right)^2}{2} \quad (37)$$

9.2.2.5 Input Capacitor

The TPS54140 device requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor with an effective capacitance value of at least 3 µF and in some applications additional bulk capacitance. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple-current rating greater than the maximum input current ripple of the TPS54140 device. Use Equation 38 to calculate the input ripple current, $I_{CI(rms)}$.

$$I_{CI(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} \quad (38)$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations because temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power-regulator capacitors because these dielectrics have a high capacitance-to-volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 20-V voltage rating is required to support the maximum input voltage. Common standard ceramic-capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V, or 100 V. Therefore, a 25-V capacitor should be selected. For this example, two 2.2-µF, 25-V capacitors in parallel have been selected. Table 2 lists a selection of high-voltage capacitors. The input capacitance value determines the input ripple voltage of the regulator. Use Equation 39 to calculate the input voltage ripple.

$$\Delta V_{IN} = \frac{I_{OUT(max)} \times 0.25}{C_{IN} \times f_{SW}} \quad (39)$$

Using the design example values, $I_{OUT(max)}$ = 1.5 A, C_{IN} = 4.4 µF, f_{SW} = 1200 kHz, yields an input voltage ripple of 71 mV and an RMS input ripple current of 0.701 A.

Table 2. Capacitor Types

VENDOR	VALUE (µF)	EIA Size	VOLTAGE (V)	DIALECTRIC	COMMENTS
Murata	1 to 2.2	1210	100	X7R	GRM32 series
	1 to 4.7		50		
	1	1206	100		GRM31 series
	1 to 2.2		50		
Vishay	1 to 1.8	2220	50		VJ X7R series
	1 to 1.2		100		
	1 to 3.9	2225	50		
	1 to 1.8		100		
TDK	1 to 2.2	1812	100		C series C4532
	1.5 to 6.8		50		
	1 to 2.2	1210	100		C series C3225
	1 to 3.3		50		
AVX	1 to 4.7	1210	50		X7R dielectric series
	1		100		
	1 to 4.7	1812	50		
	1 to 2.2		100		

9.2.2.6 Slow-Start Capacitor

The slow-start capacitor determines the minimum amount of time required for the output voltage to reach the nominal programmed value during power up which is useful if a load requires a controlled-voltage slew rate. This feature is also used if the output capacitance is very large and requires large amounts of current to quickly charge the capacitor to the output voltage level. The large currents required to charge the capacitor may make the TPS54140 device reach the current limit, or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output-voltage slew rate solves both of these problems.

The slow-start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. Use Equation 40 to calculate the minimum slow-start time, t_{SS}, required to charge the output capacitor, COUT, from 10% to 90% of the output voltage, V_{OUT}, with an average slow start current of $I_{SS(avg)}$.

$$t_{SS} > \frac{C_{OUT} \times V_{OUT} \times 0.8}{I_{SS(avg)}} \quad (40)$$

In the example, to charge the 47-µF output capacitor up to 3.3 V while only allowing the average input current to be 0.125 A requires a 1-ms slow-start time.

When the slow-start time is known, the slow-start capacitor value can be calculated using Equation 6. For the example circuit, the slow-start time is not too critical because the output capacitor value is 47 µF which does not require much current to charge to 3.3 V. The example circuit has the slow-start time set to an arbitrary value of 1 ms which requires a 3.3-nF capacitor.

9.2.2.7 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT and PH pins for proper operation. Using a ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10-V or higher voltage rating.

9.2.2.8 Undervoltage-Lockout Set Point

The undervoltage lockout (UVLO) can be adjusted using an external voltage divider on the EN pin of the TPS54140 device. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and begin switching when the input voltage increases above 7.7 V (enabled). After the regulator begins switching, it should continue to do so until the input voltage falls below 6.7 V (UVLO stop).

The programmable UVLO and enable voltages are set using a resistor divider between VIN and ground to the EN pin. Equation 2 through Equation 3 can be used to calculate the resistance values necessary. For the example application, a 332 kΩ between VIN and EN and a 61.9 kΩ between EN and ground are required to produce the 7.7-V and 6.7-V start and stop voltages.

9.2.2.9 Output Voltage and Feedback Resistors Selection

For the example design, a value of 10 kΩ was selected for R2. Using Equation 1, the value of R1 is calculated as 31.25 kΩ. The nearest standard 1% resistor is 31.6 kΩ. Because of the current leakage of the VSENSE pin, the current flowing through the feedback network should be greater than 1 µA to maintain the output voltage accuracy. This requirement makes the maximum value of R2 equal to 800 kΩ. Selectinging higher resistor values decreases quiescent current and improves efficiency at low output currents but may introduce noise immunity problems.

9.2.2.10 Compensation

Several possible methods exist to design closed loop compensation for DC-DC converters. The method presented here yields high phase margins. For most conditions, the regulator has a phase margin between 60 and 90 degrees. The method presented here ignores the effects of the slope compensation that is internal to the TPS54140 device. Because the slope compensation is ignored, the actual crossover frequency is usually lower than the crossover frequency used in the calculations.

For a more accurate design use the WEBENCH software.

The uncompensated regulator has a dominant pole that is typically located between 300 Hz and 3 kHz because the output capacitor and load resistance and a pole from the error amplifier. One zero exists because of the output capacitor and the ESR. The zero frequency is higher than either of the two poles.

If left uncompensated, the double pole created by the error amplifier and the modulator can lead to an unstable regulator. To stabilize the regulator, one pole must be canceled out. One design approach is to locate a compensating zero at the modulator pole. Then select a crossover frequency that is higher than the modulator pole. The gain of the error amplifier can be calculated to achieve the desired crossover frequency. The capacitor used to create the compensation zero along with the output impedance of the error amplifier form a low frequency pole to provide a minus-one slope through the crossover frequency. Then a compensating pole is added to cancel the zero because of the ESR of the output capacitor. If the ESR zero resides at a frequency higher than the switching frequency then it can be ignored.

To compensate the TPS54140 device using this method, first calculate the modulator pole and zero using the following equations:

$$f_{P(mod)} = \frac{I_{OUT(max)}}{2 \times \pi \times V_{OUT} \times C_{OUT}}$$

where

- $I_{OUT(max)}$ is the maximum output current
- V_{OUT} is the nominal output voltage
- C_{OUT} is the output capacitance

(41)

$$f_{Z(mod)} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

(42)

For the example design, the modulator pole is located at 1.5 kHz and the ESR zero is located at 338 kHz.

Next, the designer must select a crossover frequency to determine the bandwidth of the control loop. The crossover frequency must be located at a frequency at least five times higher than the modulator pole. The crossover frequency must also be selected so that the available gain of the error amplifier at the crossover frequency is high enough to allow for proper compensation.

Use Equation 47 to calculate the maximum crossover frequency when the ESR zero is located at a frequency that is higher than the desired crossover frequency which is usually the case for ceramic or low-ESR tantalum capacitors. Aluminum Electrolytic and Tantalum capacitors will typically produce a modulator zero at a low frequency due to their high ESR.

The example application is using a low ESR ceramic capacitor with 10 mΩ of ESR making the zero at 338 kHz.

This value is much higher than typical crossover frequencies so the maximum crossover frequency is calculated using both Equation 43 and Equation 46.

Using Equation 46 results in a minimum crossover frequency of 7.6 kHz and Equation 43 results in a maximum crossover frequency of 45.3 kHz.

A crossover frequency of 45 kHz is arbitrarily selected from this range.

For ceramic capacitors use Equation 43:

$$f_{C(max)} \le 2100\sqrt{\frac{f_{P(mod)}}{V_{OUT}}} \tag{43}$$

For tantalum or aluminum capacitors use Equation 44:

$$f_{C(max)} \le \frac{51442}{\sqrt{V_{OUT}}} \tag{44}$$

For all cases use Equation 45 and Equation 46:

$$f_{C(max)} \le \frac{f_{SW}}{5} \tag{45}$$

$$f_{C(min)} \ge 5 \times f_{P(mod)} \tag{46}$$

When a crossover frequency, f_C, is selected, the gain of the modulator at the crossover frequency is calculated. Use Equation 47 to calculate the gain of the modulator at the crossover frequency.

$$G_{MOD(fc)} = \frac{gm_{(PS)} \times R_{LOAD} \times (2\pi \times f_C \times C_{OUT} \times R_{ESR} + 1)}{2\pi \times f_C \times C_{OUT} \times (R_{LOAD} + R_{ESR}) + 1} \tag{47}$$

For the example problem, the gain of the modulator at the crossover frequency is 0.542. Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole. However, calculating the values of these components varies depending on if the ESR zero is located above or below the crossover frequency. For ceramic or low-ESR tantalum output capacitors, the zero is usually be located above the crossover frequency. For aluminum electrolytic and tantalum capacitors, the modulator zero is usually located lower in frequency than the crossover frequency. For cases where the modulator zero frequency is higher than the crossover frequency (for example using ceramic capacitors) use Equation 48, Equation 49, and Equation 50 to calculate the R_C, C_C, and C_f values.

$$R_C = \frac{V_{OUT}}{G_{MOD(fc)} \times gm_{(EA)} \times V_{REF}} \tag{48}$$

$$C_C = \frac{1}{2\pi \times R_C \times f_{P(mod)}} \tag{49}$$

$$C_f = \frac{C_{OUT} \times R_{ESR}}{R_C} \tag{50}$$

For cases where the modulator zero is less than the crossover frequency (Aluminum or Tantalum capacitors), the equations are as follows:

$$R_C = \frac{V_{OUT}}{G_{MOD(fc)} \times f_{Z(mod)} \times gm_{(EA)} \times V_{REF}} \tag{51}$$

$$C_C = \frac{1}{2\pi \times R_C \times f_{P(mod)}} \tag{52}$$

$$C_f = \frac{1}{2\pi \times R_C \times f_{Z(mod)}} \tag{53}$$

For the example problem, the ESR zero is located at a higher frequency compared to the crossover frequency so Equation 48 through Equation 50 are used to calculate the compensation components. For the example problem, the components are calculated to be: R_C = 76.2kΩ, C_C = 2710pF, and Cf = 6.17pF.

The calculated value of the C_f capacitor is not a standard value, so a value of 2700pF is used. A value of 6.8 pF is used for C_C. The R_C resistor sets the gain of the error amplifier which determines the crossover frequency. The calculated value of the R_C resistor is not a standard value, so a value of 76.8 kΩ is used.

9.2.2.11 Power Dissipation Estimate

The following formulas show how to estimate the device power dissipation under continuous-conduction mode (CCM) operation. These equations should not be used if the device is working in discontinuous conduction mode (DCM).

The power dissipation of the device includes conduction loss (P_{COND}), switching loss (P_{SW}), gate drive loss (P_{GD}) and supply current (P_Q).

$$P_{COND} = (I_{OUT})^2 \times R_{DS(on)} \times \left(\frac{V_{OUT}}{V_{IN}} \right)$$

where

- $R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω)
- V_{OUT} is the output voltage (V)
- V_{IN} is the input voltage (V)

(54)

$$P_{SW} = (V_{IN})^2 \times f_{SW} \times I_{OUT} \times 0.25 \times 10^{-9}$$

where

- I_{OUT} is the output current (A)
- f_{SW} is the switching frequency (Hz)

(55)

$$P_{GD} = V_{IN} \times 3 \times 10^{-9} \times f_{SW} \quad (56)$$

$$P_Q = 116 \times 10^{-6} \times V_{IN} \quad (57)$$

$$P_{TOT} = P_{COND} \times P_{SW} \times P_{GD} \times P_Q$$

where

- P_{TOT} s the total device power dissipation (W)

(58)

For given T_A:

$$T_J = T_A + R_{TH} \times P_{TOT}$$

where

- T_J is the junction temperature (°C)
- T_A is the ambient temperature (°C)
- R_{TH} is the thermal resistance of the package (°C/W)

(59)

For given T_{JMAX} = 150°C:

$$T_{A(max)} = T_{J(max)} - R_{TH} \times P_{TOT}$$

where

- $T_{A(max)}$ is maximum ambient temperature (°C).
- $T_{J(max)}$ is maximum junction temperature (°C)

(60)

Additional power losses occur in the regulator circuit because of the inductor AC and DC losses, the catch diode, and trace resistance that impact the overall efficiency of the regulator.

9.2.3 Application Curves

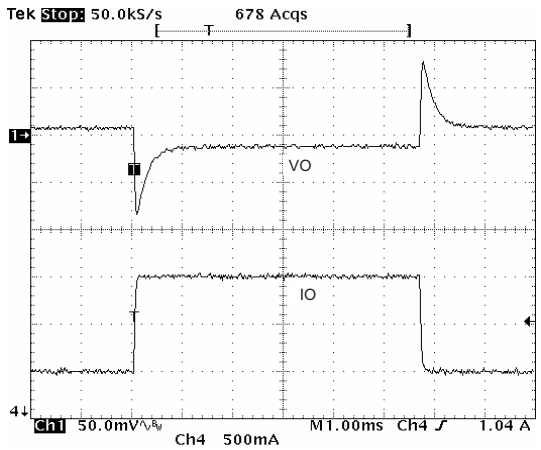


Figure 51. Load Transmit

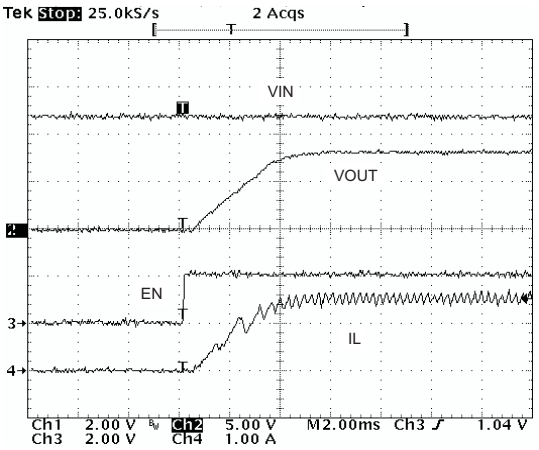


Figure 52. Startup With EN

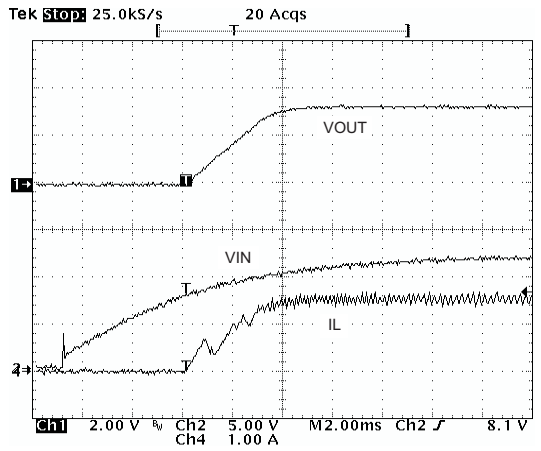


Figure 53. VIN Power Up

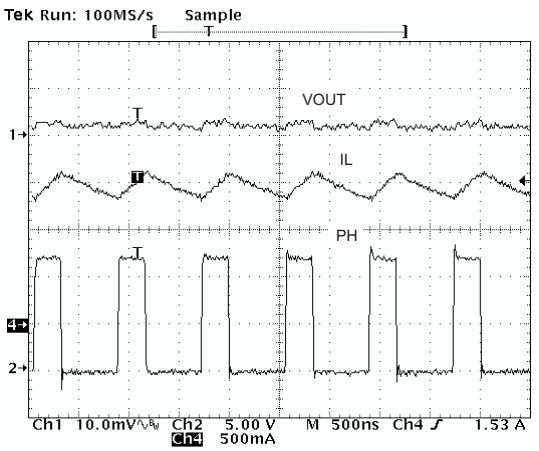


Figure 54. Output Ripple CCM

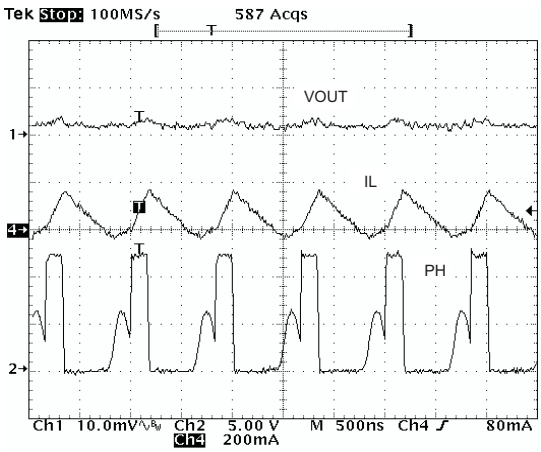


Figure 55. Output Ripple, DCM

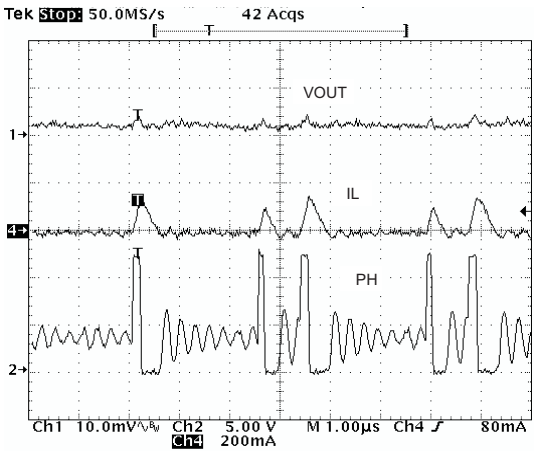


Figure 56. Output Ripple, PSM

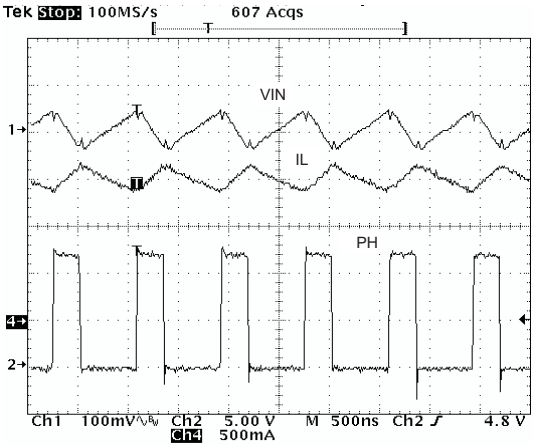


Figure 57. Input Ripple CCM

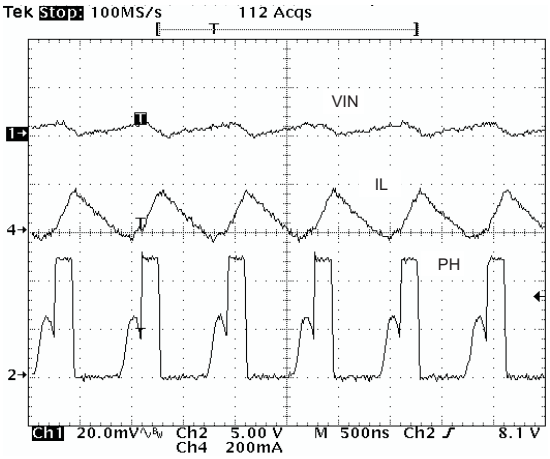


Figure 58. Input Ripple DCM

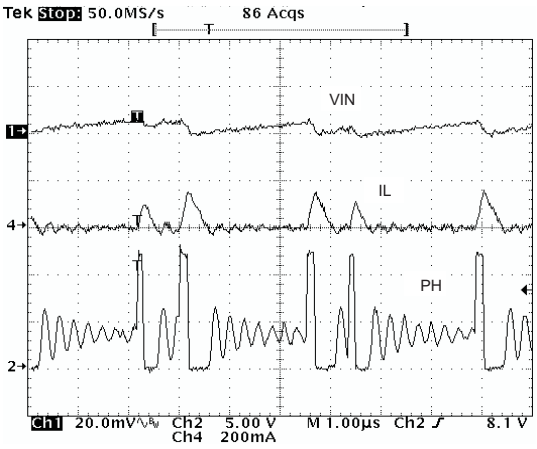


Figure 59. Input Ripple PSM

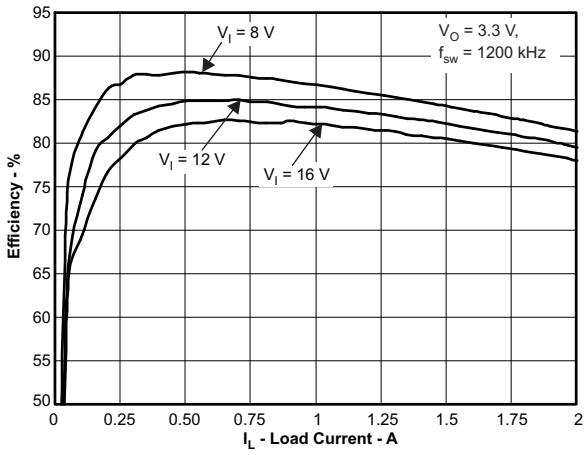


Figure 60. Efficiency vs Load Current

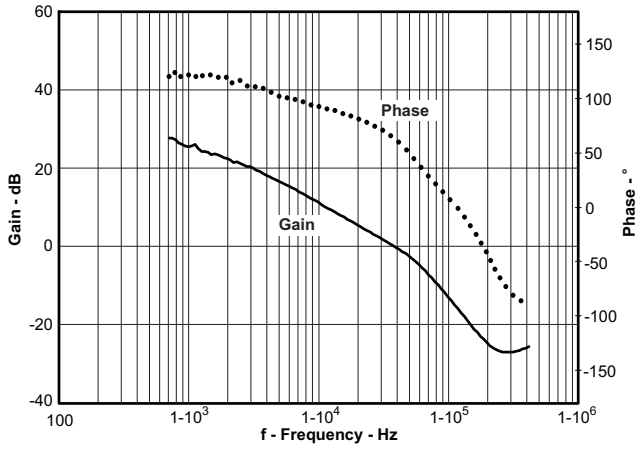


Figure 61. Overall Loop Frequency Response

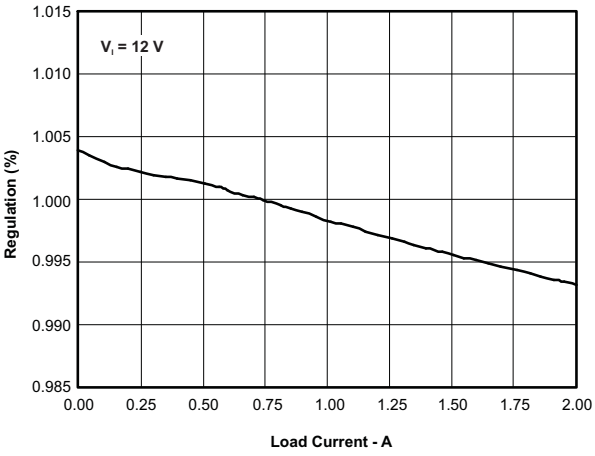


Figure 62. Regulation vs Load Current

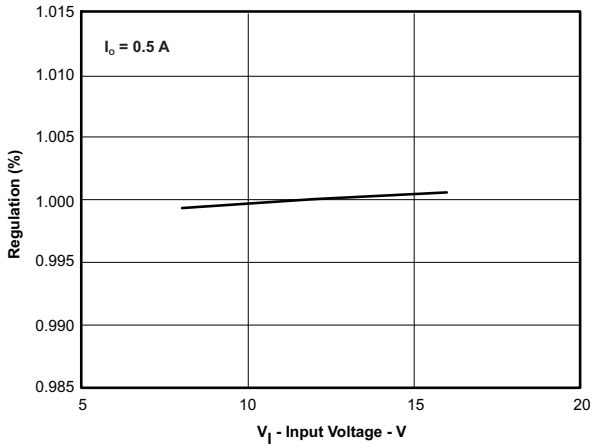


Figure 63. Regulation vs Input Voltage

10 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 3.5 V and 42 V. This input supply should be well regulated. If the input supply is located more than a few inches from the converter additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power-supply design. Several signals paths that conduct fast changing currents or voltages can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low-ESR ceramic bypass capacitor with a X5R- or X7R- dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the anode of the catch diode. See Figure 64 for a PCB layout example. The GND pin should be tied directly to the thermal pad under the IC and the thermal pad.

The thermal pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. The PH pin should be routed to the cathode of the catch diode and to the output inductor. Because the PH connection is the switching node, the catch diode and output inductor should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, the top-side ground area must provide adequate heat dissipating area. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. Obtaining acceptable performance with alternate PCB layouts may be possible, however this layout has been shown to produce good results and is meant as a guideline.

11.2 Layout Example

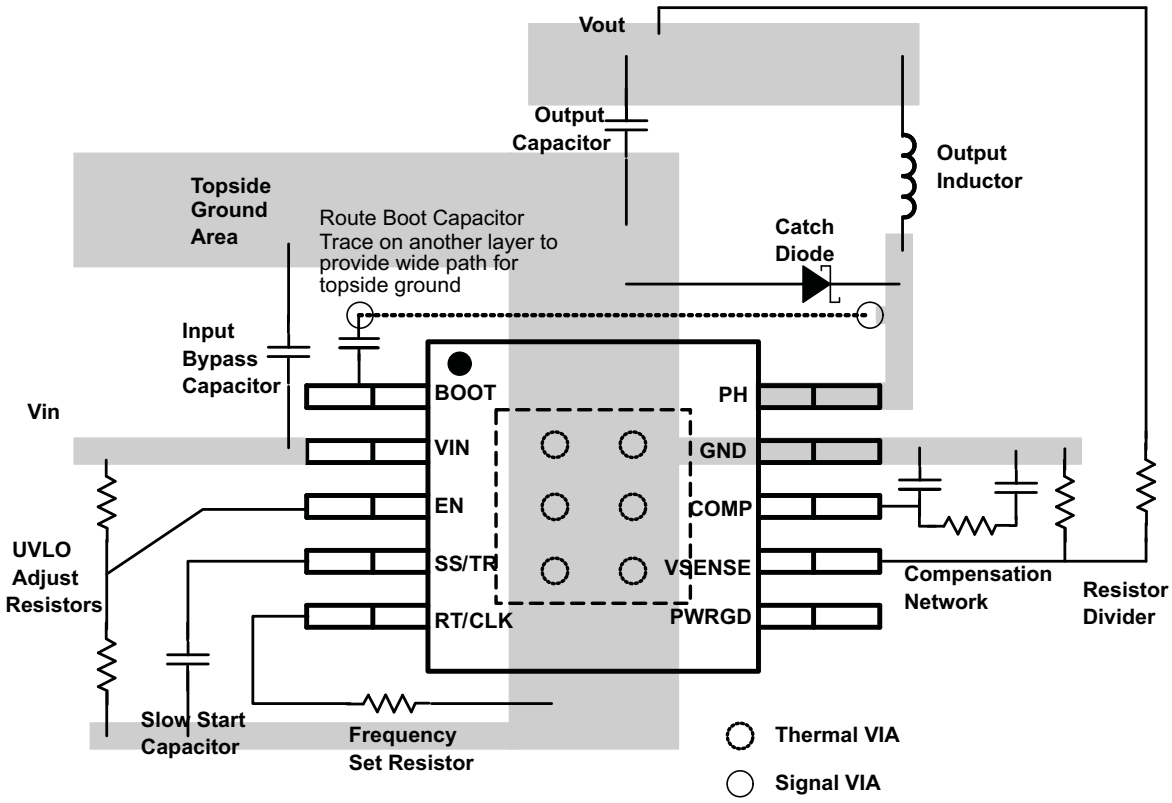


Figure 64. PCB Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.1.2 Development Support

For the WEBENCH Software Tool, go to www.TI.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *Designing Type III Compensation for Current Mode Step-Down Converters*, SLVA352
- *TPS54140EVM-429 1.5-A, SWIFT™ Regulator Evaluation Module*, SLVU285

12.3 Trademarks

Eco-mode, PowerPAD are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54140DGQ	ACTIVE	MSOP-PowerPAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	54140	Samples
TPS54140DGQR	ACTIVE	MSOP-PowerPAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	54140	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS54140 :

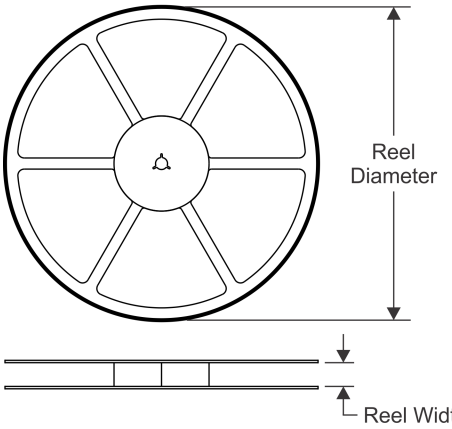
- Automotive: TPS54140-Q1

NOTE: Qualified Version Definitions:

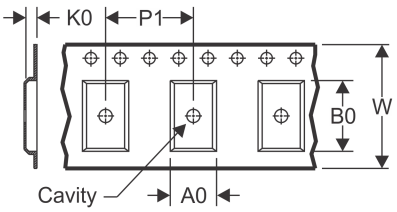
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

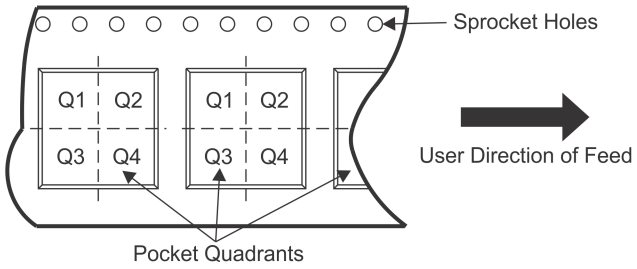


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

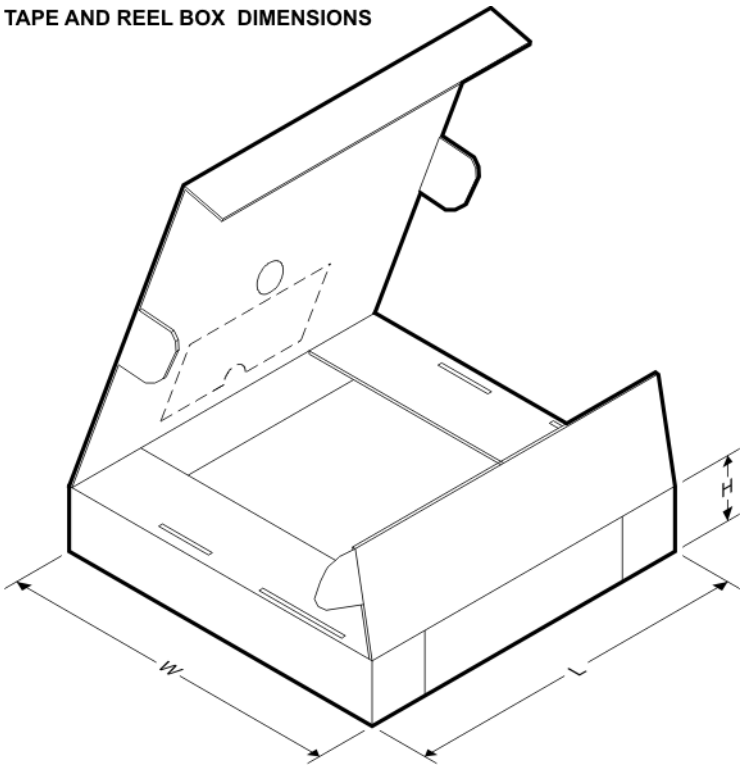
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54140DGQR	MSOP-Power PAD	DGQ	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS54140DGQR	MSOP-Power PAD	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

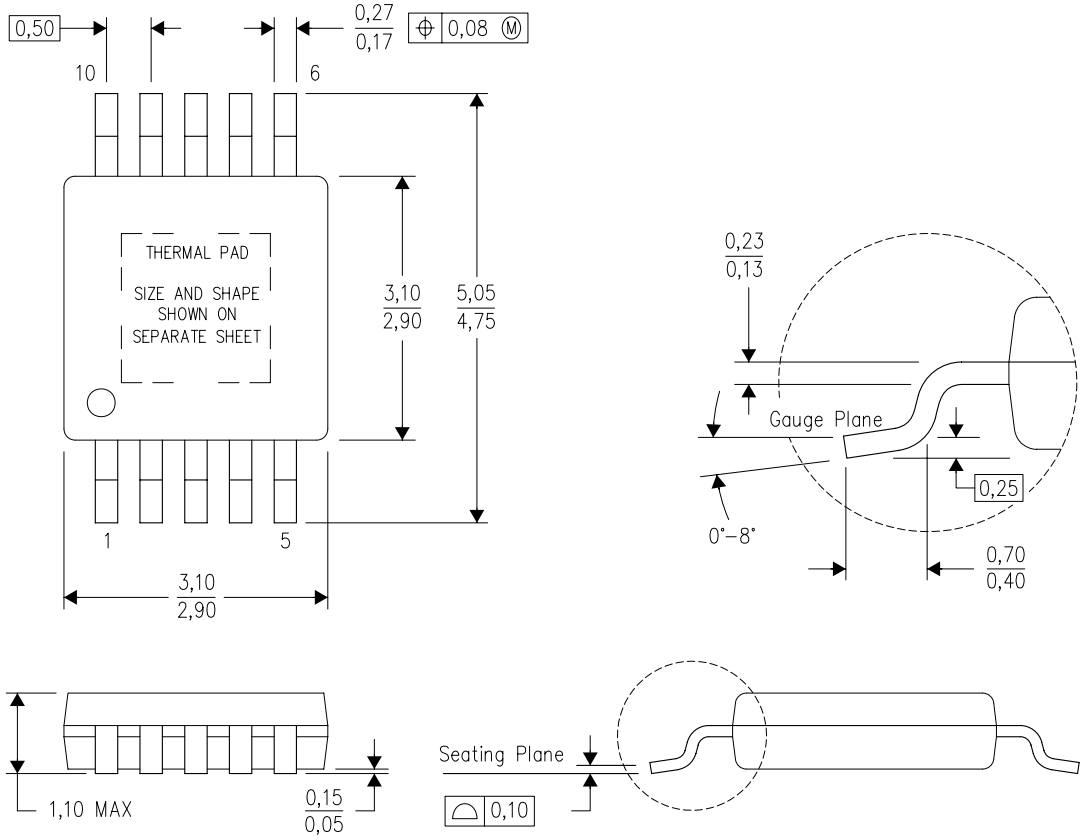
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54140DGQR	MSOP-PowerPAD	DGQ	10	2500	346.0	346.0	35.0
TPS54140DGQR	MSOP-PowerPAD	DGQ	10	2500	364.0	364.0	27.0

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE



4073273/F 11/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation BA–T.

PowerPAD is a trademark of Texas Instruments.

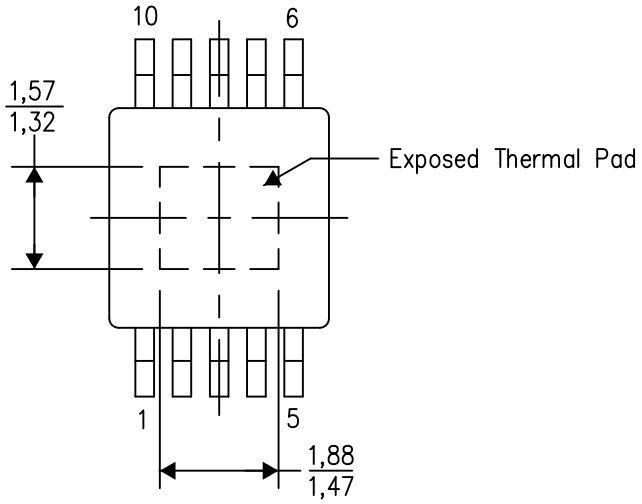
DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

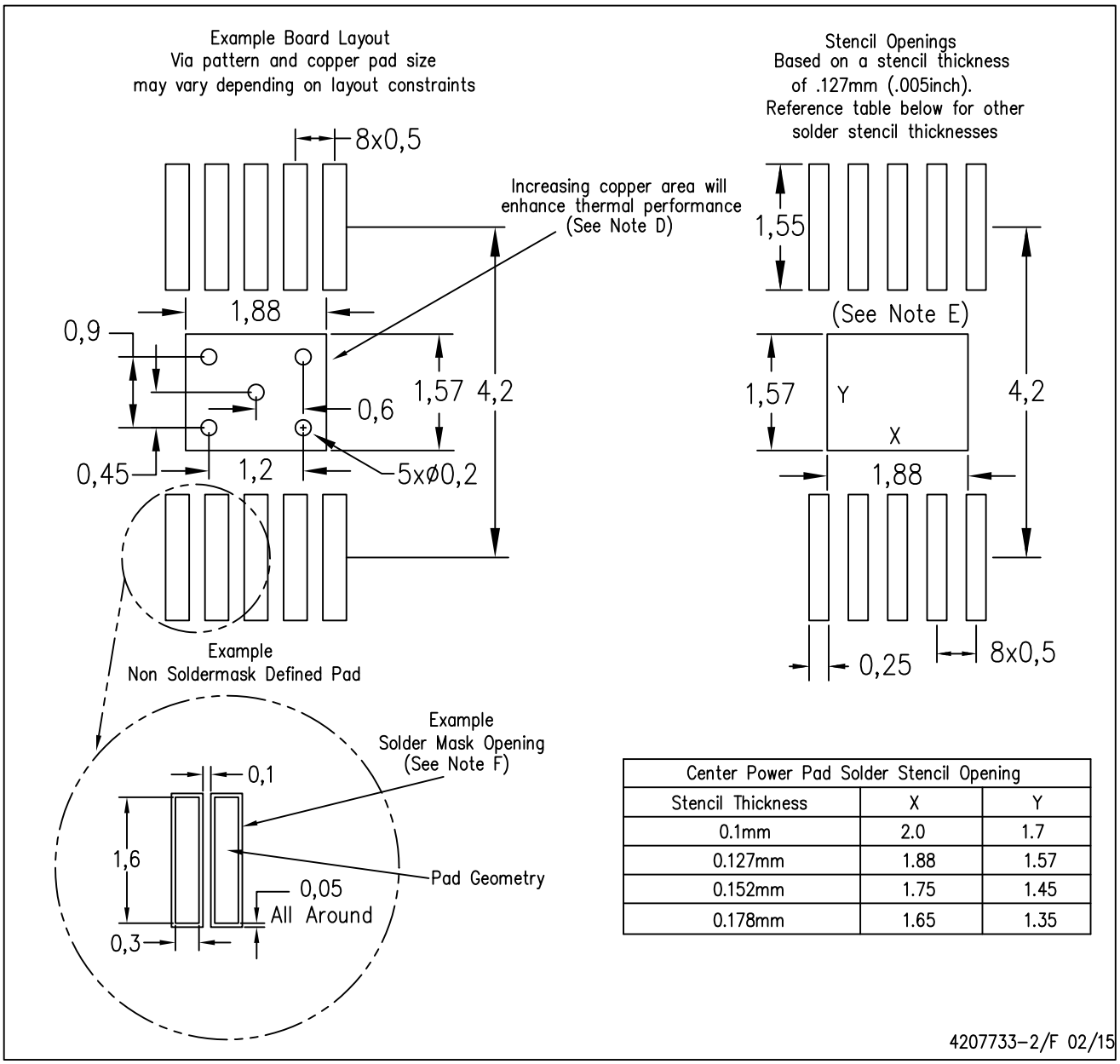
Exposed Thermal Pad Dimensions

4206324–2/H 12/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.88	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE

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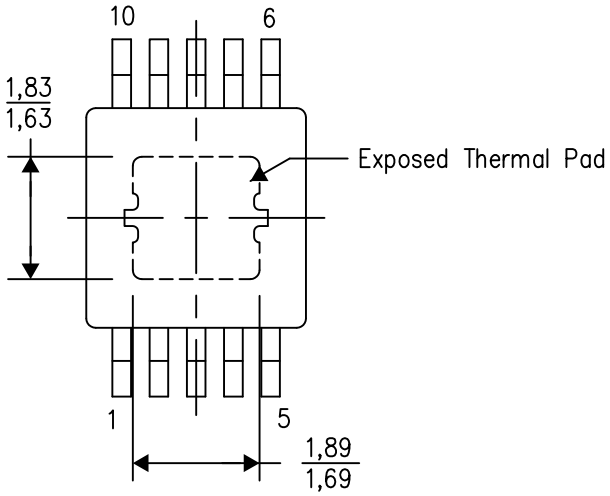
The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206324–7/H 12/14

NOTE: A. All linear dimensions are in millimeters

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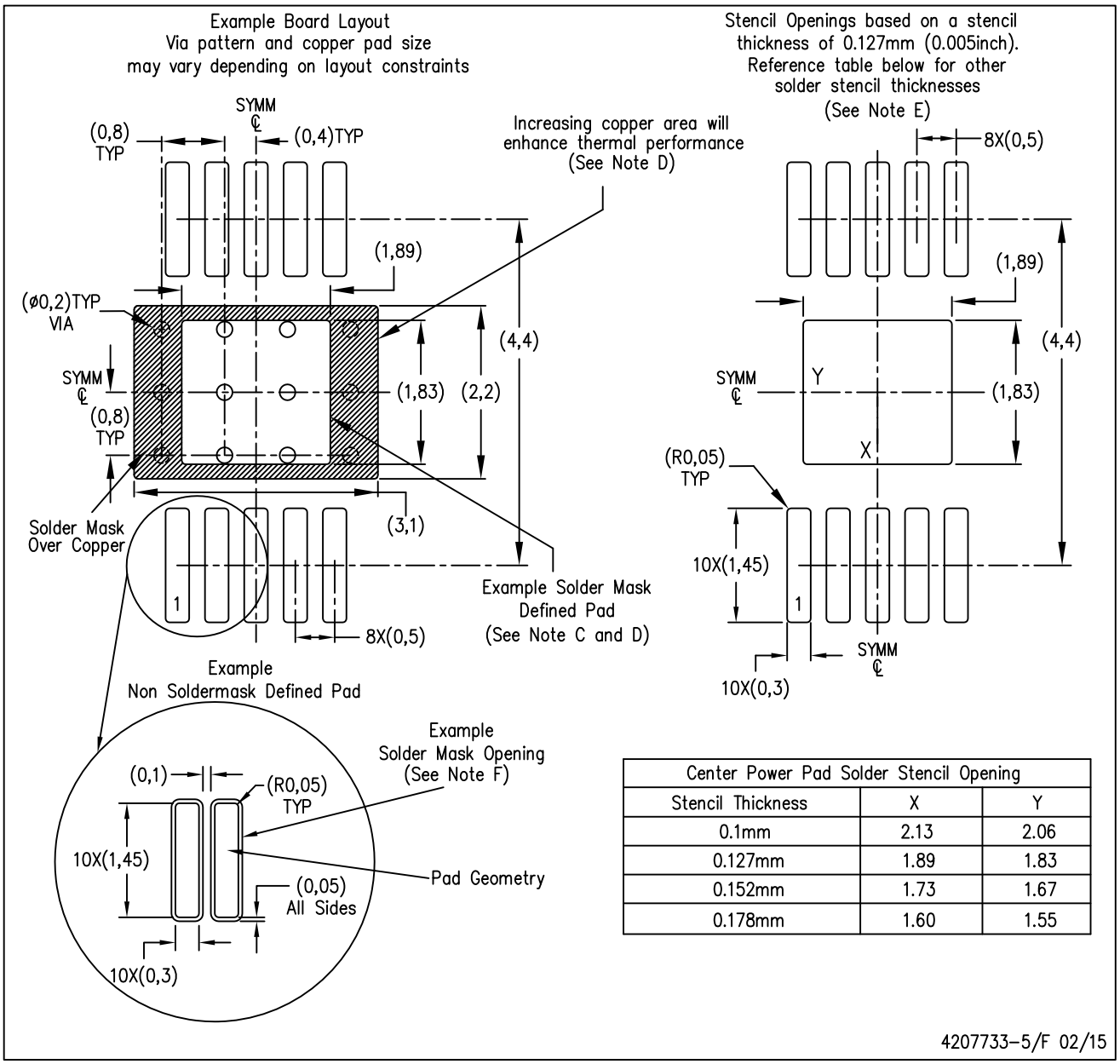
DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.13	2.06
0.127mm	1.89	1.83
0.152mm	1.73	1.67
0.178mm	1.60	1.55

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
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