1. General Description

This EPROM-Based 8-bit micro-controller uses a fully static CMOS technology process to achieve higher speed and smaller size with the low power consumption and high noise immunity. On chip memory includes 1K words of ROM, and 128 bytes of static RAM.

2. Features

The followings are some of the features on the hardware and software:

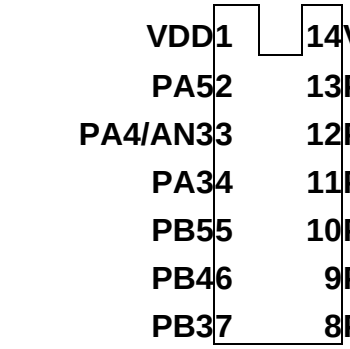
- ◆ Fully CMOS static design
- ◆ 8-bit data bus
- ◆ On chip EPROM size: 1K words
- ◆ Internal RAM size: 128 bytes
- ◆ 35 single word instructions
- ◆ 14-bit instructions
- ◆ 8-level stacks
- ◆ Operating voltage: 2.5 V ~ 5.5 V
- ◆ Operating frequency: 0 ~ 20 MHz
- ◆ The most fast execution time is 200 ns under 20 MHz in all single cycle instructions except the branch instruction
- ◆ Addressing modes include direct, indirect and relative addressing modes
- ◆ Power-on Reset
- ◆ Power edge-detector Reset
- ◆ Sleep Mode for power saving
- ◆ 5 types of oscillator can be selected by programming option:
  - INRC—Internal 4MHz RC oscillator
  - RC—Low cost RC oscillator
  - LFXT—Low frequency crystal oscillator
  - XTAL—Standard crystal oscillator
  - HFXT—High frequency crystal oscillator
- ◆ 8-bit real time clock/counter (RTCC) with 8-bit programmable prescaler
- ◆ On-chip RC oscillator based Watchdog Timer (WDT)
- ◆ 4-channel, 8-bit AD
- ◆ Interrupt source:
  - Timer0, INT, Pin change, AD

3. Applications

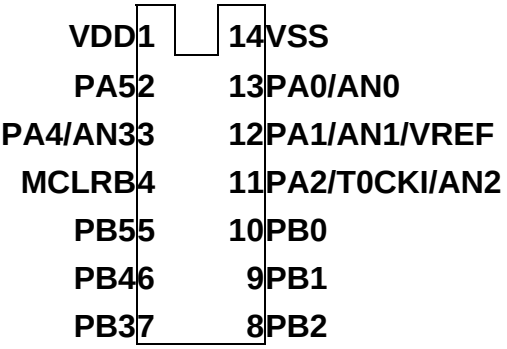
The application areas range from appliance motor control and high speed automotive to low power remote transmitters/receivers, small instruments, chargers, toy, automobile and PC pe-ripheral … etc.

4. Pin Assignment

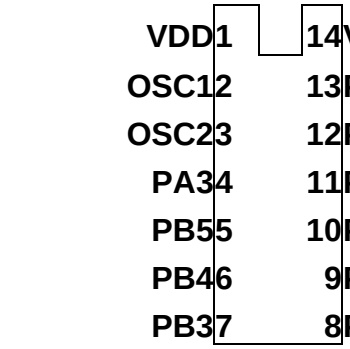
MDT10P57A1P / MDT10P57A1S



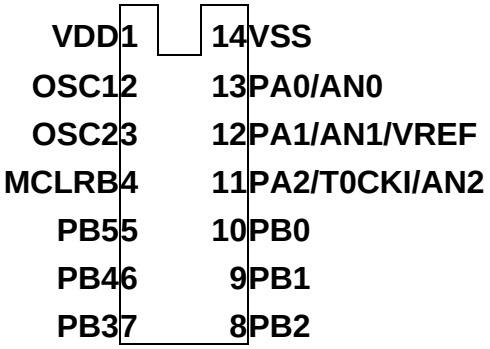
MDT10P57A3P / MDT10P57A3S



MDT10P57A2P / MDT10P57A2S



MDT10P57A4P / MDT10P57A4S



5. Pin Function Description

Pin Name	I/O	Function Description
PA5	I/O	Port A, TTL input level / Schmitt Trigger input levels.
PA4/AN3	I/O	Port A, TTL input level.
PA3	I	Port A, TTL input level / Schmitt Trigger input levels. Input only.
PA2/T0CKI/AN2/INT	I/O	Port A, Schmitt Trigger input levels.
PA1/AN1/VREF	I/O	Port A, TTL input level / Schmitt Trigger input levels.
PA0/AN0	I/O	Port A, TTL input level / Schmitt Trigger input levels.
PB5~PB0	I/O	Port B, TTL input level.
OSC1	I	Oscillator Input.
OSC2	O	Oscillator Output.
MCLRB	I	Master Clear.
VDD		Power supply
VSS		Ground

6. Memory Map

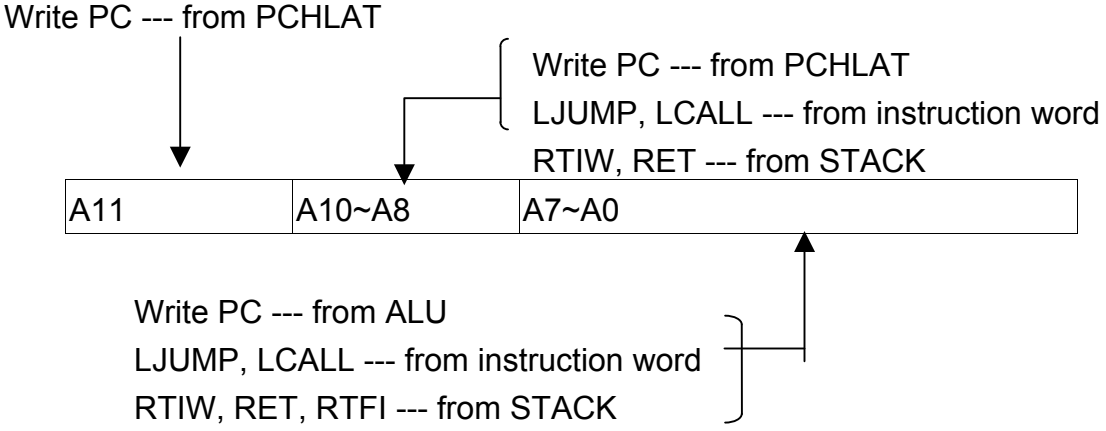
(A) Register Map

Address	Description
BANK0	
00	Indirect Addressing Register
01	RTCC
02	PCL
03	STATUS
04	MSR
05	Port A
06	Port B
0A	PCHLAT
0B	INTS
0C	PIFB1
1E	ADRES
1F	ADS0
20~7F	General purpose register
BANK1	
01	TMR
05	CPIO A
06	CPIO B
0C	PIEB1
0E	PSTA
1F	ADS1
A0~BF	General purpose register

(1) IAR (Indirect Address Register): R00

(2) RTCC (Real Time Counter/Counter Register): R01

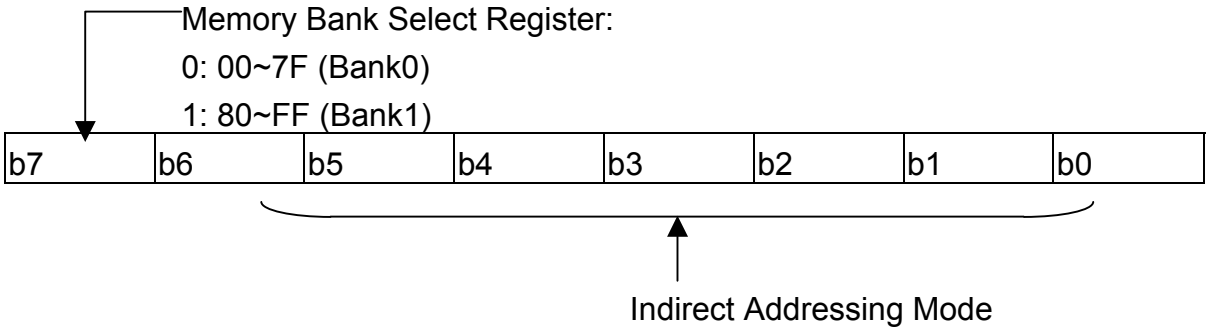
(3) PC (Program Counter): R02, R0A



(4) STATUS (Status register): R03

Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	PF	Power loss Flag bit
4	TF	WDT Timer overflow Flag bit
5	RBS0	Register Bank Select bit: 0: 00H~7FH (Bank0) 1: 80H~FFH (Bank1)
7~6	--	General purpose bit

(5) MSR (Memory Bank Select Register): R04



(6) PORT A: R05 (PA5~PA0, I/O Register)

(7) PORT B: R06 (PB5~PB0, I/O Register)

(8) PCHLAT: R0A (High byte of PC)

Bit	Function
4~0	High byte of PC.
7~5	Unimplemented, reads as '0'.

(9) INTS (Interrupt Status Register): R0B

Bit	Symbol	Function
0	RAIF	PORT A change interrupt flag. Set when PA0, PA1, PA3 inputs change.
1	INTF	Set when INT interrupt occurs. INT interrupt flag.
2	TIF	Set when TMR0 overflows.
3	RAIE	0: disable PA change interrupt. 1: enable PA change interrupt.
4	INTS	0: disable INT interrupt. 1: enable INT interrupt.
5	TIS	0: disable TMR0 interrupt. 1: enable TMR0 interrupt.

Bit	Symbol	Function
6	PEIE	0: disable all peripheral interrupt. 1: enable all peripheral interrupt.
7	GIS	0: disable global interrupt. 1: enable global interrupt.

(10) PIFB1 (Peripheral Interrupt Flag Bit): R0C

Bit	Symbol	Function
0~5	--	Unimplemented
6	ADIF	A/D interrupt flag 0: A/D conversion is not complete 1: A/D conversion completed
7	--	Unimplemented

(11) ADRES (A/D result register): R1E

(12) ADS0 (A/D Status Register): R1F

Bit	Symbol	Function
0	ADRUN	0: A/D converter module is shut off and consumes no operating current 1: A/D converter module is operating
1	--	Unimplemented
2	GO/DONEB	0: A/D conversion not in progress 1: A/D conversion in progress
4~3	CHS1~0	00: AIC0, 01: AIC1, 10: AIC2, 11: AIC3
5	--	Unimplemented
7~6	ASCS1-0	00: fosc/2, 01: fosc/8, 10: fosc/32, 11: f RC (*Note)

*Note: determined by OSC mode, HF: fosc/32, XT: fosc/8, LF: fosc/2, RC: fosc/2

(13) TMR (Time Mode Register): R81

Bit	Symbol	Function		
		Prescaler Value	RTCC rate	WDT rate
2~0	PS2~0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128 1 : 256	1 : 1 1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128
3	PSC	0: RTCC 1: Watchdog Timer		

Bit	Symbol	Function
4	TCE	0: Increment on low-to-high transition on RTCC pin 1: Increment on high-to-low transition on RTCC pin
5	TCS	0: Internal instruction cycle clock 1: Transition on RTCC pin
6	IES	0: Interrupt on falling dege on PA2 1: Interrupt on rising edge on PA2
7	PABPH	0: PORTA, PORTB pull-hi are enable 1: PORTA, PORTB pull-hi are disable

(14) CPIO A (Control Port I/O Mode Register): R85

＝“0”, I/O pin in output mode.

＝“1”, I/O pin in input mode.

(15) CPIO B (Control Port I/O Mode Register): R86

＝“0”, I/O pin in output mode.

＝“1”, I/O pin in input mode.

(16) PIEB1: R8C

Bit	Symbol	Function
5~0	--	Unimplemented
6	ADIE	0: disable A/D interrupt 1: enable A/D interrupt
7	--	Unimplemented

(17) PSTA: R8E

Bit	Symbol	Function
1	PORB	0:Power on Reset occurred 1:No Power on Reset occurred

(18) ADS1 (A/D Status Register): R9F

Bit	Symbol	Function
2~0	PAVM2~0	0 0 0: PA0~2,PA4= analog input. VREF= VDD. 0 0 1: PA0~2,PA4= analog input. PA1= ref input, VREF= PA1. 0 1 0: PA0~2= analog input. VREF= VDD. 0 1 1: PA0~2= analog input. PA1= ref input, VREF= PA1. 1 0 0: PA0, 1= analog input. PA2, 4= digital I/O, VREF= VDD. 1 0 1: PA0, 1= analog input. PA2, 4= digital I/O, VREF=PA1. 1 1 0: PA0= analog input. PA1, 2, 4= digital I/O, VREF=VDD. 1 1 1: PA0~2, 4= digital I/O.

(19) Configurable options for EPROM (Set by writer):

Type	Option
Oscillator Type	INRC Oscillator
	RC Oscillator
	HFXT Oscillator
	XTAL Oscillator
	LFXT Oscillator
Watchdog Timer control	Watchdog timer disable all the time
	Watchdog timer enable all the time
Oscillator-start Timer control	0ms
	80ms
Power-edge Detect	PED Disable
	PED Enable
Security state	Security Disable
	Security Enable

The default security state of EPROM is weak disable. Once the IC was set to enable or disable, it's forbidden to change.

(B) Program Memory

Address	Description
000-3FF	Program memory
000	The starting address of power on, external reset or WDT time-out reset.
004	Interrupt vector

7. Reset Condition for all Registers

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
IAR	00h	N/A	N/A	N/A
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PC	0Ah,02h	0000 0000 0000	0000 0000 0000	PC + 1
STATUS	03h	0001 1xxx	000# #uuu	000# #uuu
MSR	04h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT A	05h	--xx xxxx	--uu uuuu	--uu uuuu
PORT B	06h	--xx xxxx	--uu uuuu	--uu uuuu
PCHLAT	0Ah	---0 0000	---0 0000	---u uuuu
INTS	0Bh	0000 000x	0000 000u	uuuu uuuu
PIFB1	0Ch	-0-- ----	-0-- ----	-u-- ----
ADRES	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADS0	1Fh	00-0 00-0	00-0 00-0	uu-u uu-u
TMR	81h	1111 1111	1111 1111	uuuu uuuu
CPIOA	85h	--11 1111	--11 1111	--uu uuuu
CPIOB	86h	--11 1111	--11 1111	--uu uuuu
PIEB1	8Ch	-0-- ----	-0-- -----	-u-- ----
PSTA	8Eh	---- --0-	---- --u-	---- --u-
ADS1	9Fh	---- -000	---- -000	---- -uuu

Note : u＝unchanged, x＝unknown, - ＝unimplemented, read as “0”

#＝value depends on the condition of the following table

Condition	Status: bit 4	Status: bit 3	PSTA: bit 1
/MCLR reset (not during SLEEP)	u	u	1
/MCLR reset during SLEEP	1	0	1
WDT reset (not during SLEEP)	0	1	1
WDT reset during SLEEP	0	0	1
Power-on reset	1	1	0
Power-range reset	1	1	1

8. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operating	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	TF, PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	TF, PF
010000 00000100	RET	Return from subroutine	Stack→PC	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiiiii	LDWI I	Load immediate to W	I→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔R(4~7)]→t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R – W→t or (R+/W+1→t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R – 1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R – 1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI i	AND W and immediate	i ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiiiii	IORWI i	Inclu. OR W and immediate	i ∪ W→W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI i	Exclu. OR W and immediate	i ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) →R(n-1), C→R(7), R(0)→C	C
010101 trrrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0→R(b)	None
0010bb brrrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None

Instruction Code	Mnemonic Operands	Function	Operating	Status
100nnn nnnnnnnn	LCALL n	Long CALL subroutine	n→PC, PC+1→Stack	None
101nnn nnnnnnnn	LJUMP n	Long JUMP to address	n→PC	None
110111 iiiiiiii	ADDWI i	Add immediate to W	W+i→W	C, HC, Z
110001 iiiiiiii	RTIW i	Return, place immediate to W	Stack→PC,i→W	None
111000 iiiiiiii	SUBWI i	Subtract W from immediate	i-W→W	C, HC, Z
010000 00001001	RTFI	Reture from interrupt	Stack→PC,1→GIS	None

Note:

W	Working register	b	Bit position
WT	Watchdog timer	T	Target
TMODE	TMODE mode register	0	Working register
CPIO	Control I/O port register	1	General register
TF	Timer overflow flag	R	General register address
PF	Power loss flag	C	Carry flag
PC	Program Counter HC	HC	Half carry
OSC	Oscillator	Z	Zero flag
Inclu.	Inclusive ‘∪’	/	Complement
Exclu.	Exclusive ‘⊕’	x	Don’t care
AND	Logic AND ‘∩’	i	Immediate data (8 bits)
		n	Immediate address

9. Electrical Characteristics

*Note: Temperature=25°C

1.Operation Current :

(1) HF (C=10p) , WDT - enable

	4M	10M	20M	Sleep
2.5V	350uA	800uA	1.4mA	3uA
3.0V	530uA	1.1mA	1.8mA	8uA
4.0V	940uA	1.7mA	2.9mA	16uA
5.0V	1.5mA	2.5mA	4.4mA	30uA
5.5V	2.2mA	3.5mA	6mA	50uA

These parameters are for reference only.

(2) XT (C=10p) , WDT - enable

	1M	4M	10M	Sleep
2.5V	120uA	300uA	800uA	3uA
3.0V	170uA	390uA	910uA	8uA
4.0V	310uA	720uA	1.5mA	16uA
5.0V	610uA	1.1mA	2.1mA	30uA
5.5V	990uA	1.6mA	2.8mA	50uA

These parameters are for reference only.

(3) LF (C=10p) , WDT - enable

	32K(50p)	455K	1M	Sleep
2.5V	20uA	X	90uA	3uA
3.0V	30uA	80uA	120uA	8uA
4.0V	70uA	160uA	220uA	16uA
5.0V	140uA	260uA	340uA	30uA
5.5V	250uA	360uA	520uA	50uA

These parameters are for reference only.

(4) RC , WDT - Enable , @Vdd = 5.0V

C	R	Freq.	Current
3p	4.7k	6.5M	1.3mA
	10k	3.2M	790uA
	47k	700K	350uA
	100k	320K	280uA
	300k	110K	250uA
	470k	66K	240uA
20p	4.7k	4.2M	900uA
	10k	2.1M	600uA
	47k	460K	310uA
	100k	214K	270uA
	300k	72K	250uA
	470k	43K	240uA
100p	4.7k	1.8M	530uA
	10k	904K	370uA
	47k	196K	260uA
	100k	93K	250uA
	300k	31K	240uA
	470k	19K	240uA

C	R	Freq.	Current
300p	4.7k	820K	350uA
	10k	404K	280uA
	47k	88K	240uA
	100k	42K	230uA
	300k	14K	230uA
	470k	9K	230uA

These parameters are for reference only.

(5) INT_RC , WDT - enable

	4MHz	Sleep
3.0V	600uA	8uA
4.0V	900uA	16uA
5.0V	1.2mA	30uA

These parameters are for reference only.

2. Input Voltage (Vdd = 5V) :

	Port	Min	Max
Vil	TTL	Vss	1.0V
	Schmitt trigger	Vss	1.0V
Vih	TTL	2V	Vdd
	Schmitt trigger	3.5V	Vdd

These parameters are for reference only.

3. Output Voltage (Vdd = 5V) :

	PA,PB	Condition
Voh	3.5V	Ioh =-20mA
Vol	0.8V	Iol =+20mA
Voh	4.3V	Ioh = -5mA
Vol	0.6V	Iol = +5mA

These parameters are for reference only.

4. Output Current (Max.) (Vdd = 5V) :

Port A:

	Current
Source current	25mA
Sink current	25mA

These parameters are for reference only.

Port B:

	Current
Source current	25mA
Sink current	25mA

These parameters are for reference only.

5. The basic WDT time-out cycle time :

	Time
2.5V	24ms
3.0V	22ms
4.0V	19ms
5.0V	18ms
5.5V	17ms

These parameters are for reference only.

6. PORTA,PORTB pull high resisto :

	Pull high resistor
PA0,1,2,4,5	50KΩ
PA3	340KΩ
PB0,1,2,3,4,5	50KΩ

These parameters are for reference only.

7. INRC Frequency :

	Frequency(error%)
@VDD=5V,25℃	4M
@VDD=6V,25℃	4.1M(2.5%)
@VDD=2.5V,25℃	3.9M(2.5%)
@VDD=5V,0℃	4.1M(2.5%)
@VDD=5V,40℃	3.9M(2.5%)
@VDD=5V,80℃	3.6M(10%)

These parameters are for reference only.