USB-Compliant Single-Cell Li-Ion Switching Charger with USB-OTG Boost Regulator

Description

The PSC5415 combines a highly integrated switch-mode charger, to minimize single-cell Lithium-ion (Li-ion) charging time from a USB power source, and a boost regulator to power a USB peripheral from the battery.

The charging parameters and operating modes are programmable through an I^2C interface that operates up to 3.4Mbps. The charger and boost regulator circuits switch at 1.5MHz to minimize the size of external passive components.

The PSC5415 provides battery charging in three phases: conditioning, constant current, and constant voltage.

To ensure USB compliance and minimize charging time, the input current is limited to the value set through the I^2C host. Charge termination is determined by 1/10 of the setting current.

The integrated circuit (IC) automatically restarts the charge cycle when the battery falls below an internal threshold. If the input source is removed, the IC enters a high-impedance mode with leakage from the battery to the input prevented. Charge status is reported back to the host through the I^2C port. Charge current is reduced when the die temperature reaches 120℃.

The PSC5415 can operate as a boost regulator on command from the system. The boost regulator includes a soft-start that limits inrush current from the battery.

The PSC5415 is available in a 2.0 x 1.7mm, 20-bump, 0.4mm pitch WLCSP package.

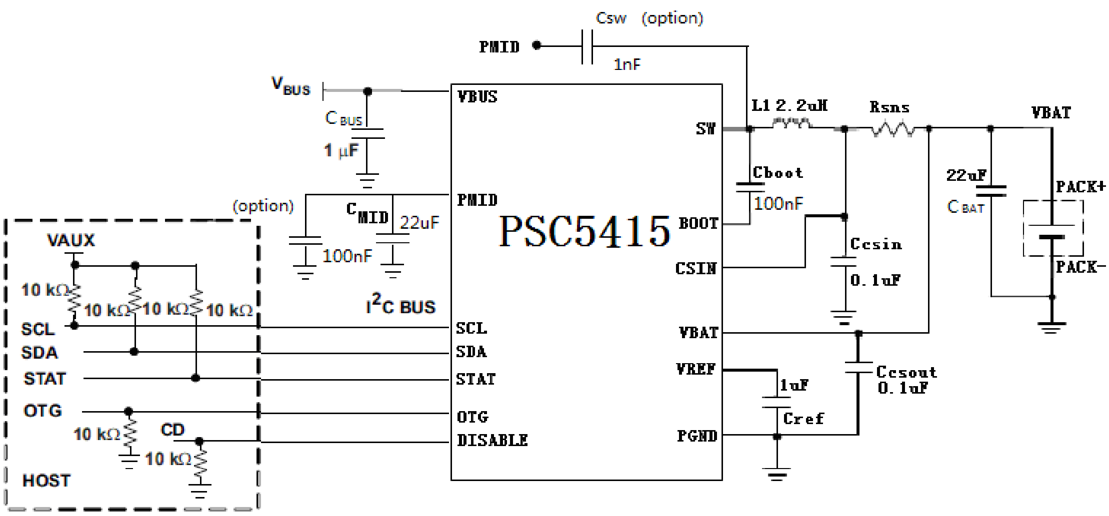


Figure 1: Typical Application

Feature

- Fully Integrated, High-Efficiency Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
- Faster Charging than Linear
- Charge Voltage Accuracy: ±1% 25℃
- ±7.5% Charge Current Regulation Accuracy
- 20V Absolute Maximum Input Voltage
- 6V Maximum Input Operating Voltage
- 1.5A Maximum Charge Rate

Application

- Cellular Phones, Smart Phones, PDAs
- Tablet, Portable Media Players
- Gaming Device, Digital Cameras

- Programmable through High-Speed I^2C Interface (3.4Mb/s) with Fast Mode Plus Compatibility
  - -Input Current
  - -Fast-Charge/Termination Current
  - -Charger Voltage
  - -Termination Enable
- 1.5MHz Synchronous Buck PWM Controller with Wide Duty Cycle Range
- Small Footprint 2.2μH External Inductor
- Weak Input Sources Accommodated by Reducing Charging Current to Maintain Minimum VBUS Voltage
- Low Reverse Leakage to Prevent Battery Drain to VBUS
- 5V, 500mA Boost Mode for USB OTG for 2.7 to 4.5V Battery Input

Recommended External Components

Component	Description	Vendor	Parameter	Typ.	Units
L1 (Ich<=1.5A)	2.2uH, 20%, 2.2A 4mm*4mm*1.8mm	SUNLORD:SPH4018H2R2MT	L	2.2	μH
			DCR(Series R)	42	mΩ
L1 (Ich>1.5A)	2.2uH, 20%, 4.9A 8mm*8mm*3mm	SUNLORD:SPH8030H2R2MT	L	2.2	μH
			DCR(Series R)	12	mΩ
C_{BAT}	22μF,10%,6.3V,X5R,0603	Murata: GRM188R60J226M	C	22	μF
C_{MID}	22μF,10%,6.3V,X5R,0603	Murata: GRM188R60J226M	C	22	μF
C_{BUS}	1.0μF,10%,25V,X5R,0603	Murata: GRM188R61E105M	C	1.0	μF

Block Diagram

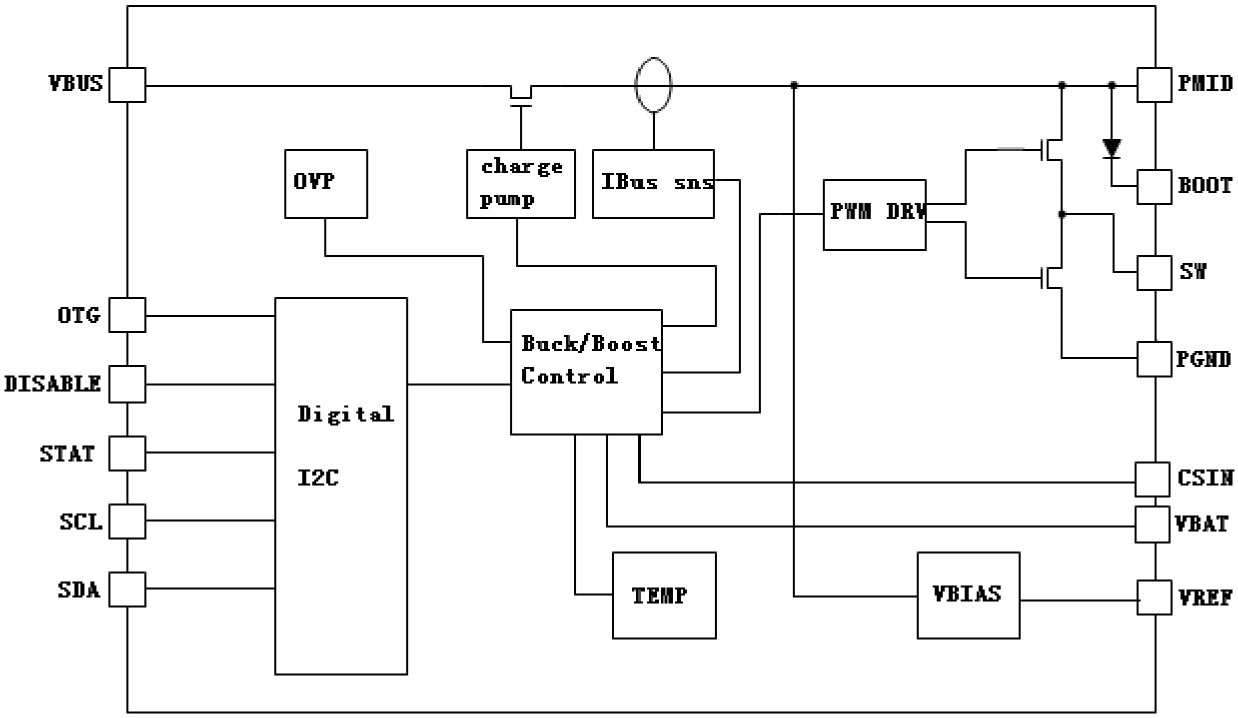


Figure 2: IC and System Block Diagram

Pin Configuration

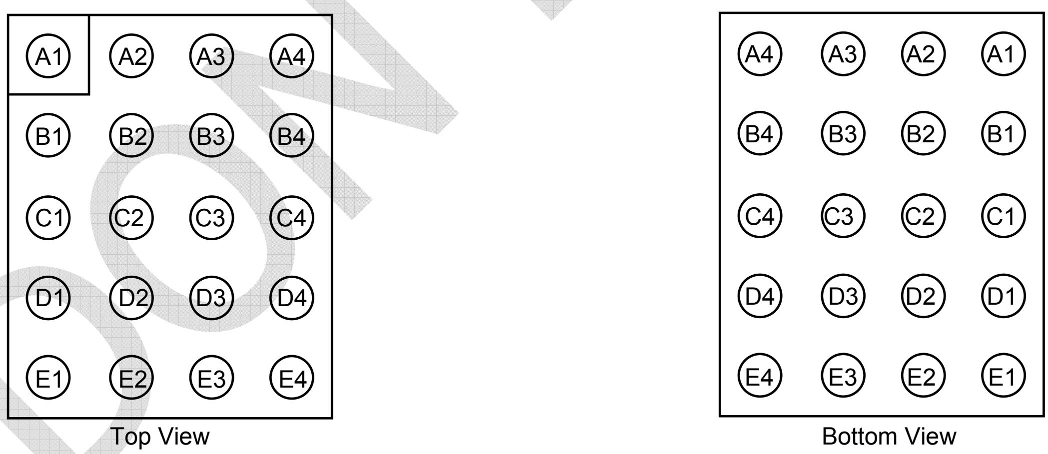


Figure 3: WLCSP-20 Pin Assignments

Pin Definitions

Pin#	Name	Description
A1,A2	VBUS	**Charger Input Voltage** and USB-OTG output voltage. Bypass with a 1μF capacitor to PGND
A3	BOOT	**Boost strap capacitor** connection for high side NMOS gate driver. Connect 33nF~100nF ceramic capacitor (voltage rating ≥ 10V) from BOOT to SW pin.
A4	SCL	**I^2C Interface Serial Clock.** This pin should not be left floating.
B1-B3	PMID	**Power Input Voltage.** Power input to the charger regulator, bypass point for the input current sense, and high-voltage input switch. Bypass with a minimum of 22μF, 6.3V capacitor to PGND.
B4	SDA	**I^2C Interface Serial Data.** This pin should not be left floating.
C1-C3	SW	**Switching Node.** Connect to output inductor.
C4	STAT	**Status.** Open-drain output indicating charge status. The IC pulls this pin LOW when charge is in process.
D1-D3	PGND	**Power Ground.** Power return for gate drive and power transistors. The connection from this pin to the bottom of C_{MID} should be as short as possible.
D4	OTG	**On-The-Go.** Enables boost regulator in conjunction with OTG_EN and OTG_PL bits *(see Table 16)*.
E1	CSIN	**Current-Sense Input.** Connect to the sense resistor in series with the battery. The IC uses this node to sense current into the battery. Bypass this pin with a 0.1μF capacitor to PGND.
E2	DISABLE	**Charge Disable.** If this pin is "1", charging is disabled. When LOW, charging is controlled by I2C registers.
E3	VREF	**Bias voltage.** Connect to a 1uF capacitor to PGND. The output voltage is PMID, which is limited to 6.5V. Any resistor loading to VREF is **NOT** recommended.
E4	VBAT	**Battery Voltage.** Connect to the positive (+) terminal of the battery pack. Bypass with a 0.1μF capacitor to PGND if the battery is connected through long leads.

Maximum Ratings and Thermal Characteristics(T_A=25℃ unless otherwise noted)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter		Symbol	Min.	Max.	Units
VBUS Voltage	Continuous	V_{BUS}	-1.4	20.0	V
	Pulsed,100ms Maximum Non-Repetitive		-2.0		
STAT Voltage		V_{STAT}	-0.3	20	V
PMID Voltage		V_I		7.0	V
SW,CSIN,VBAT,VREF, DISABLE Voltage			-0.3	7.0	
Voltage on Other Pins		V_O	-0.3	6.5(2)	V
Maximum VBUS Slope above 5.5V when Boost or Charger are Active		$\frac{dV_{BUS}}{dt}$		4	V/μs
Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	ESD	2000		V
	Charged Device Model per JESD22-C101		500		
Junction Temperature		T_J	-40	+150	℃
Storage Temperature		T_{STG}	-65	+150	℃
Lead Soldering Temperature, 10 Seconds		T_L		+260	℃

Note:

2: Lesser of 6.5V or V_I + 0.3V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Prisemi does not recommend exceeding them or designing to absolute maximum ratings.

Parameter		Symbol	Min.	Max.	Units
Supply Voltage		V_{BUS}	4.5	6	V
Maximum Battery Voltage when Boost enabled		$V_{BAT(MAX)}$		4.5	V
Negative VBUS Slew Rate during VBUS Short Circuit, C_{MID}≤ 22μF, see VBUS Short While Charging	T_A≤60℃	$-\frac{dV_{BUS}}{dt}$		4	V/μs
	T_A≥60℃			2	
Ambient Temperature		T_A	-30	+85	℃
Junction Temperature (see Thermal Protection section)		T_J	-30	+140	℃

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperature T_A. For measured data, see Table 11.

Parameter	Symbol	Typical	Units
Junction-to-Ambient Thermal Resistance	θ_{JA}	60	℃/W
Junction-to-PCB Thermal Resistance	θ_{JB}	20	℃/W

Electrical characteristics per line@25℃(unless otherwise specified)

Unless otherwise specified: according to the circuit of Figure 1; recommended operating temperature range for T_J and T_A; V_{BUS}=5.0V; HZ_MODE; OPA_MODE=0; (Charge Mode); SCL, SDA, OTG=0 or 1.8V; and typical values are for T_J=25℃.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Power Supplies						
VBUS Current	I_{VBUS}	$V_{BUS}>V_{BUS(MIN)}$, PWM Switching		10		mA
		$V_{BUS}>V_{BUS(MIN)}$; PWM Enabled, Not Switching (Battery OVP Condition); I_IN Setting=100mA		2.5		mA
VBAT to VBUS Leakage Current	I_{LKG}	0℃<T_J<85℃, HZ_MODE=1 V_{BAT}=4.2V,V_{BUS}=0V		0.2		μA
Battery Discharge Current in High-Impedance Mode	I_{BAT}	0℃<T_J<85℃, HZ_MODE=1 V_{BAT}=4.2V		0.2		μA
		0℃<T_J<85℃, HZ_MODE=0 V_{BAT}=4.2V		16		
Charger Voltage Regulation						
Charge Voltage Range	V_{OREG}		4.2		4.40	V
Charge Voltage Accuracy		TJ=25℃	-1%		+1%	
Charging Current Regulation						
Output Charge Current Range	I_{OCHRG}	V_{LOWV} < V_{BAT} < V_{OREG} V_{BUS} > V_{SLP}, R_{SENSE}=68mΩ	500		1544	mA
Charge Current Accuracy Across R_{SENSE}		T_J<85℃,VBAT=3.8V	92.5	100	107.5	%

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Weak Battery Detection						
Weak Battery Threshold Range	V_{LOWV}		3.45		3.65	V
Logic Levels: DISABLE, SDA, SCL, OTG						
High-Level Input Voltage	V_{IH}		1.2			V
Low-Level Input Voltage	V_{IL}				0.4	V
Input Bias Current	I_{IN}	Input Tied to GND or V_{IN}		0.01	1.00	μA
Charge Termination Detection						
Termination Current Range	$I_{(TERM)}$	$V_{BAT} > V_{OREG} - V_{RCH}$ $V_{BUS} > V_{SLP}$, R_{SENSE}=68mΩ	50		154	mA
Termination Current Accuracy			-25		+25	%
Input Power Source Detection						
VBUS Input Voltage Rising	$V_{IN(MIN)1}$	To Initiate and Pass VBUS		4.29	4.42	V
Minimum VBUS during Charge	$V_{IN(MIN)2}$	During Charging		4.1	4.15	V
VBUS Validation Time	t_{VBUS_VALID}			25		ms
Special Charger (V_{BUS})						
Special Charger Setpoint Accuracy	V_{SP}		-10		+10	%
Input Current Limit						
Input Current Limit Threshold	I_{INLIM}	I_{IN} Set to 500mA		500		mA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Battery Recharge Threshold						
Recharge Threshold	V_{RCH}	Below $V_{(OREG)}$		100		mV
STAT Output						
STAT Output Low	$V_{STAT(OL)}$	I_{STAT}=10mA			0.4	V
STAT High Leakage Current	$I_{STAT(OH)}$	V_{STAT}=5V			1	μA
Sleep Comparator						
Sleep-Mode Entry Threshold, $V_{BUS} – V_{BAT}$	V_{SLP}	2.3V ≤ V_{BAT} ≤V_{OREG}, V_{BUS} Falling	0	0.04	0.10	V
Power Switches (see Figure 3)						
Q3 On Resistance (VBUS to PMID)	$R_{DS(ON)}$	$I_{IN(LIMIT)}$=500mA		150	250	mΩ
Q1 On Resistance (PMID to SW)				120	225	
Q2 On Resistance (SW to GND)				120	225	
Charger PWM Modulator						
Oscillator Frequency	f_{SW}			1.5		MHz
Maximum Duty Cycle	D_{MAX}				100	%
Minimum Duty Cycle	D_{MIN}			0		%
Boost Mode Operation (OPA_MODE=1, HZ_MODE=0)						
Boost Output Voltage at VBUS	V_{BOOST}	2.7V<V_{BAT}<4.5V, I_{LOAD} from 0 to 500mA	4.8	5.15	5.3	V
Boost Mode Quiescent Current	$I_{BAT(BOOST}$	PFM Mode, V_{BAT}=3.6V, I_{OUT}=0		6	10	mA
Q2 Current Limit	$I_{LIM(BST)}$		3	4	5.5	A
Minimum Battery Voltage for Boost Operation	$UVLO_{BST}$			2.58	2.70	V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
VBUS Load Resistance						
VBUS to PGND Resistance	R_{VBUS}	Normal Operation		1500		KΩ
Protection and Timers						
VBUS Over-Voltage Shutdown	$VBUS_{OVP}$	V_{BUS} Rising		6.0		V
Hysteresis		V_{BUS} Falling		150		mV
Battery Short-Circuit Threshold	V_{SHORT}	V_{BAT} Rising	2.25	2.4	2.55	V
Hysteresis		V_{BAT} Falling		0.1		
Linear Charging Current	I_{SHORT}	$V_{BAT} < V_{SHORT}$	20	30	40	mA
Thermal Shutdown Threshold(4)	$T_{SHUTDWN}$	T_J Rising		145		℃
Hysteresis(4)		T_J Falling		10		
Thermal Regulation Threshold(4)	T_{CF}	Charge Current Reduction Begins		120		℃
12H timer	t_{12H}	Charger Enabled		12		hour
90-Minute Timer	T_{90MIN}	90-Minute Mode		90		min

Notes:

4: Guaranteed by design; not tested in production.

I²C Timing Specifications

Guaranteed by design.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
SCL Clock Frequency	f_{SCL}	Standard Mode			100	kHz
		Fast Mode			400	
		High-Speed Mode, $C_B \leq$ 100pF			3400	
		High-Speed Mode, $C_B \leq$ 400pF			1700	
Bus-Free Time between STOP and START Conditions	t_{BUF}	Standard Mode		4.7		μs
		Fast Mode		1.3		

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
START or Repeated START Hold Time	$t_{HD;STA}$	Standard Mode		4		μs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
SCL LOW Period	t_{LOW}	Standard Mode		4.7		μs
		Fast Mode		1.3		
		High-Speed Mode, $C_B \le 100pF$		160		ns
		High-Speed Mode, $C_B \le 400pF$		320		
SCL HIGH Period	t_{HIGH}	Standard Mode		4		μs
		Fast Mode		600		ns
		High-Speed Mode, $C_B \le 100pF$		60		ns
		High-Speed Mode, $C_B \le 400pF$		120		ns
Repeated START Setup Time	$t_{SU;STA}$	Standard Mode		4.7		μs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
Data Setup Time	$t_{SU;DAT}$	Standard Mode		250		ns
		Fast Mode		100		
		High-Speed Mode		10		
Data Hold Time	$t_{HD;DAT}$	Standard Mode	0		3.45	μs
		Fast Mode	0		900	ns
		High-Speed Mode, $C_B \le 100pF$	0		70	ns
		High-Speed Mode, $C_B \le 400pF$	0		150	ns
SCL Rise Time	t_{RCL}	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \le 100pF$		10	80	
		High-Speed Mode, $C_B \le 400pF$		20	160	
SCL Fall Time	t_{FCL}	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \le 100pF$		10	40	
		High-Speed Mode, $C_B \le 400pF$		20	80	
SDA Rise Time Rise Time of SCL after a Repeated START Condition and after ACK Bit	t_{RDA} t_{RCL1}	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \le 100pF$		10	80	
		High-Speed Mode, $C_B \le 400pF$		20	160	

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
SDA Fall Time	t_{FDA}	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	
		High-Speed Mode, $C_B \le 100pF$		10	80	
		High-Speed Mode, $C_B \le 400pF$		20	160	
Stop Condition Setup Time	$t_{SU;STO}$	Standard Mode		4		μs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
Capacitive Load for SDA, SCL	C_B				400	pF

Timing Diagrams

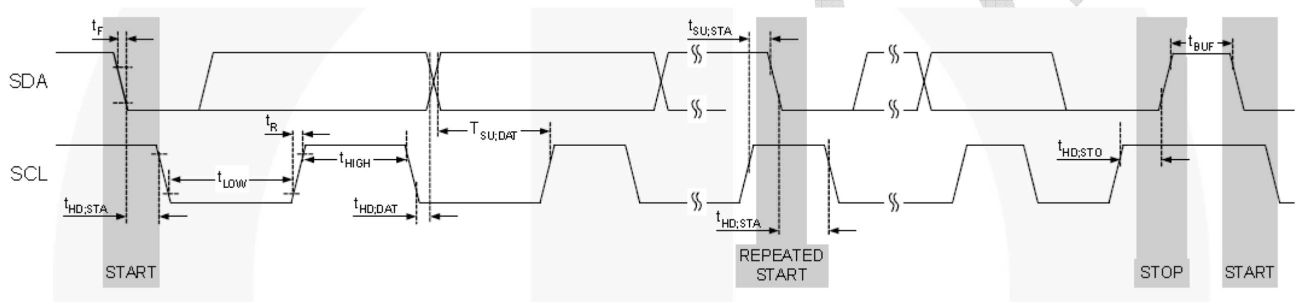
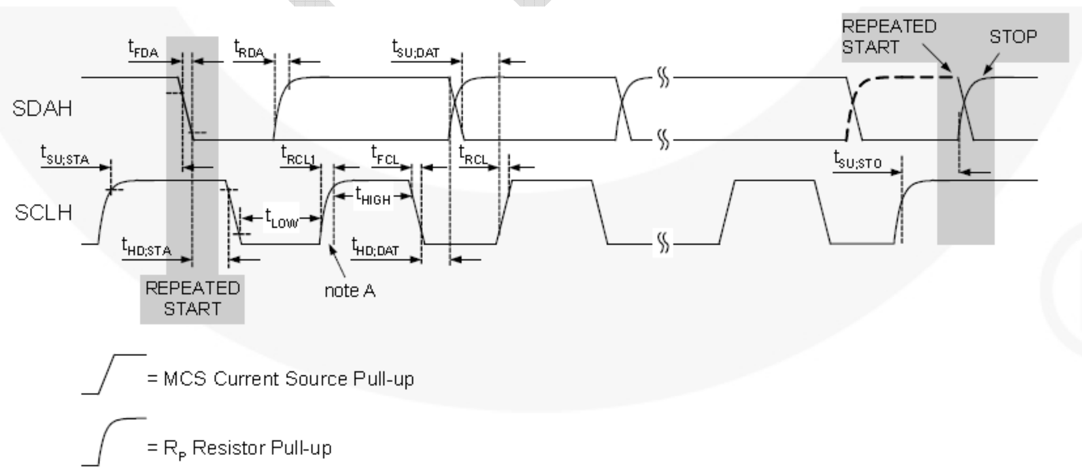


Figure 5. I^{2}C Interface Timing for Fast and Slow Modes



Note A: First rising edge of SCLH after Repeated Start each ACK bit.

Figure 6. I^{2}C Interface Timing for High-Speed Mode

Charge Mode Typical Characteristics

Unless otherwise specified, circuit of Figure 1, V_{OREG}=4.35V, V_{BUS}=5.0V, and T_A=25℃.

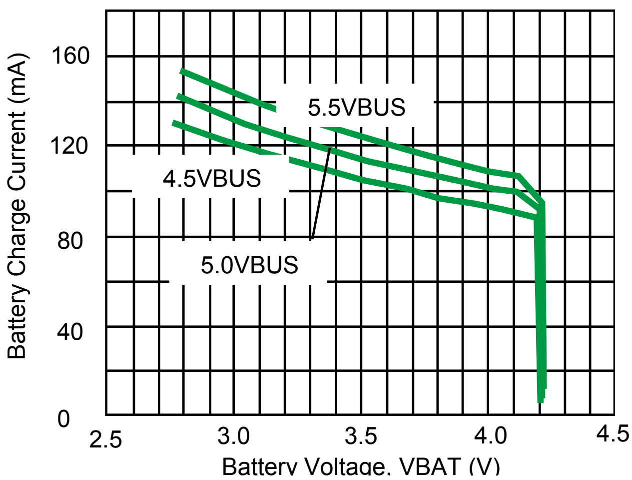


Fig 7. Battery Charge Current vs. V_{BUS} with I_{INLIM}=100mA

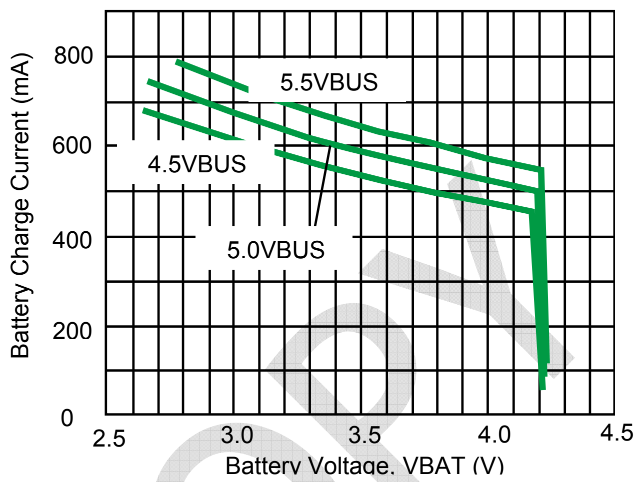


Figure 8. Battery Charge Current vs. V_{BUS} with I_{INLIM}=500mA

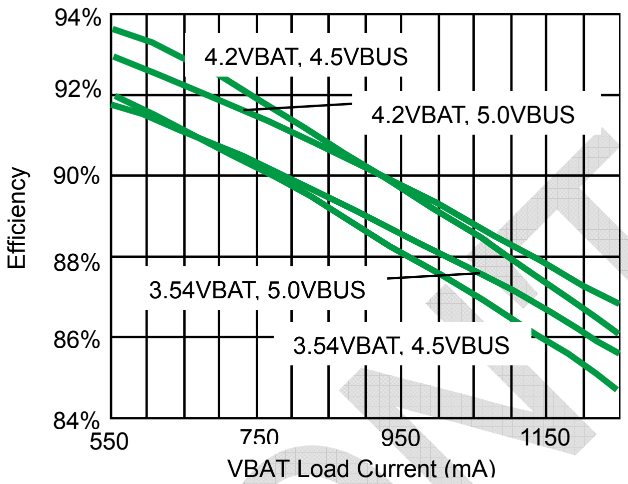


Fig 9. Charger Efficiency, No I_{INLIM}, $I_{OCHARGE}$=1250mA

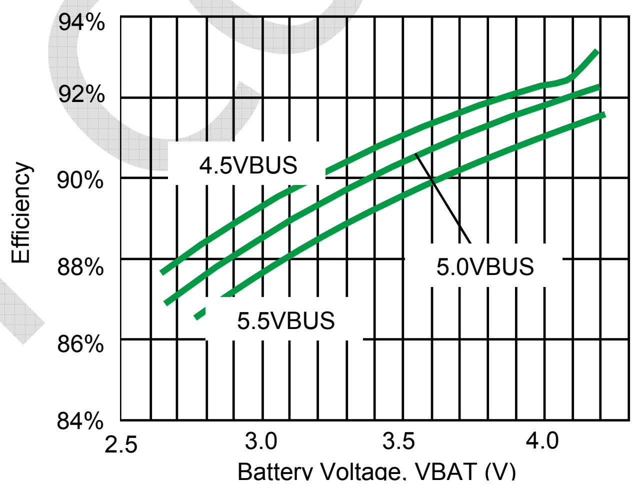


Figure 10. Charger Efficiency vs. V_{BUS}, I_{INLIM}=500mA

Figure 11. Auto-Charge Startup at V_{BUS} Plug-in, I_{INLIM}=100mA, V_{BAT}=3.9V

Figure 12. Auto-Charge Startup at V_{BUS} Plug-in, I_{INLIM}=500mA, V_{BAT}=3.9V

Figure 13. Auto-Charge Startup with 300mA Limited Charger/Adaptor, I_{INLIM}=500mA, V_{BAT}=3.9V

Figure 14. Charger Startup with HZ_MODE Bit Reset, I_{INLIM}=500mA, $I_{OCHARGE}$=956mA, OREG=4.2V, V_{BAT}=3.6V

Figure 15. Battery Removal / Insertion during Charging, V_{BAT}=3.9V, $I_{OCHARGE}$=956mA, No I_{INLIM}, TE=0

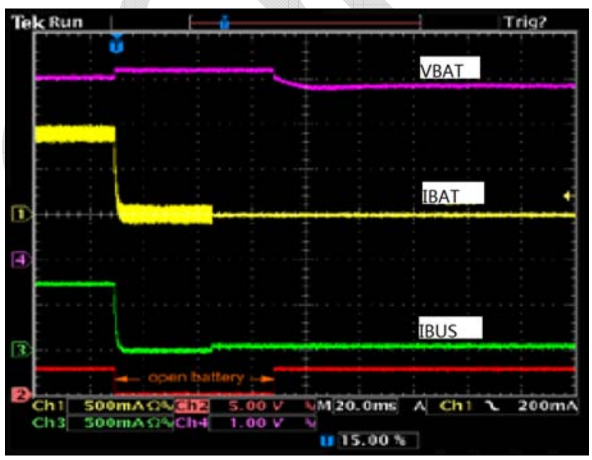


Figure 16. Battery Removal / Insertion during Charging, V_{BAT}=3.9V, $I_{OCHARGE}$=956mA, No I_{INLIM}, TE=1

Figure 17. No Battery at V_{BUS} Power-up

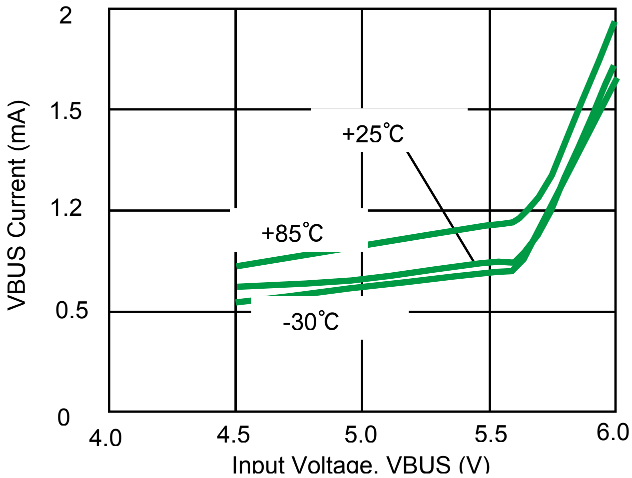


Fig 18. VBUS Current with Battery Open

Boost Mode Typical Characteristics

Unless otherwise specified, using circuit of Figure 1, V_{BAT}=3.6V, T_A=25℃.

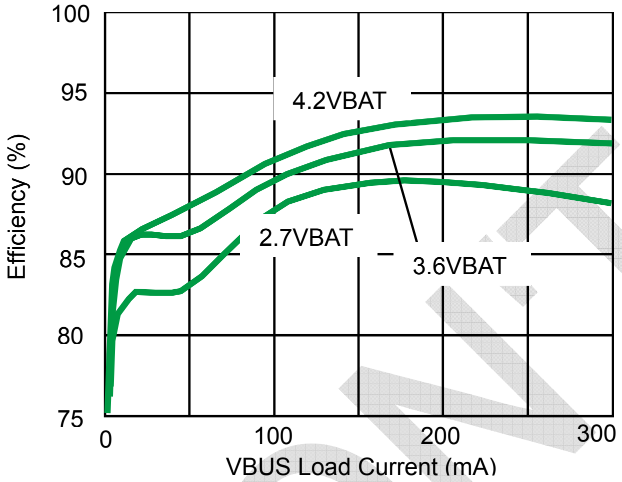


Fig 20. Efficiency vs. VBAT

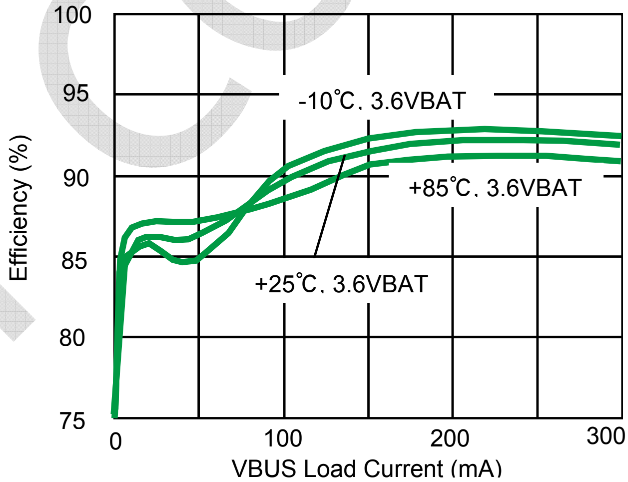


Figure 21. Efficiency Over Temperature

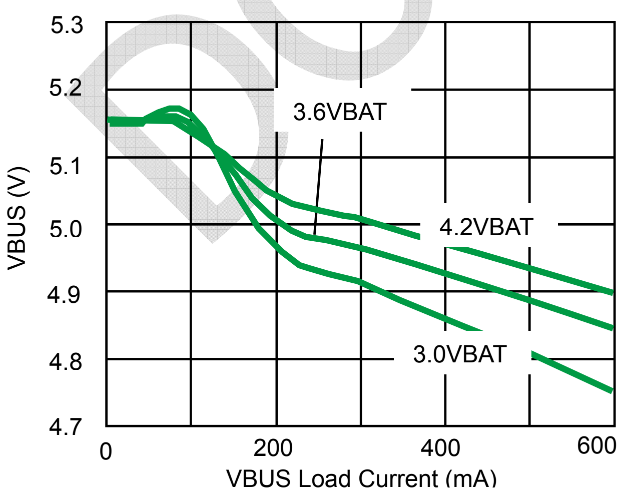


Fig 22. Output Regulation vs. VBAT

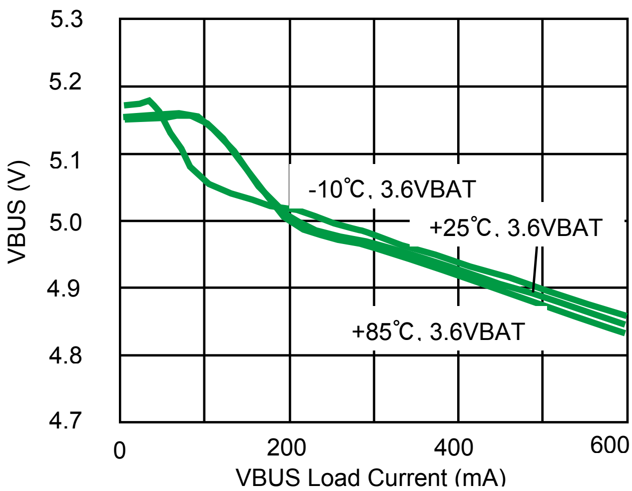


Figure 23. Output Regulation Over Temperature

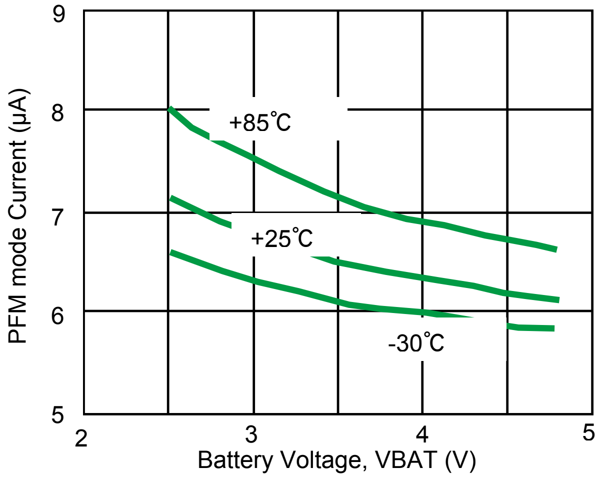


Fig 24. PFM mode Current

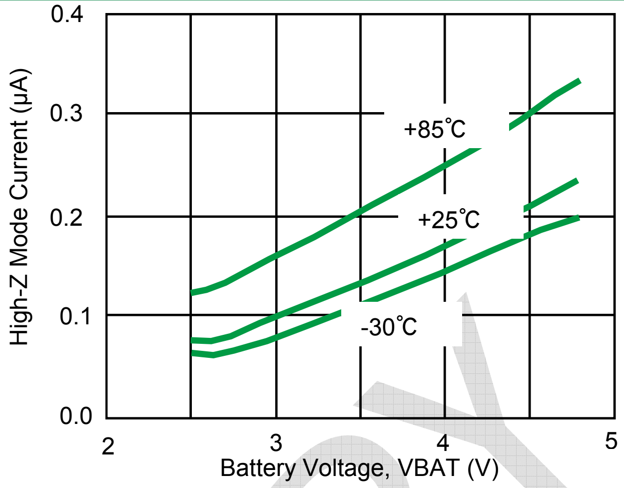


Figure 25. High-Impedance Mode Battery Current HZ_MODE=1

Figure 26. Boost PWM Waveform

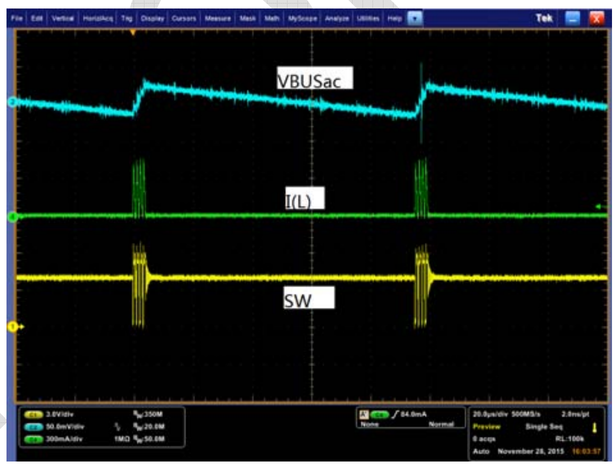


Figure 27. Boost PFM Waveform

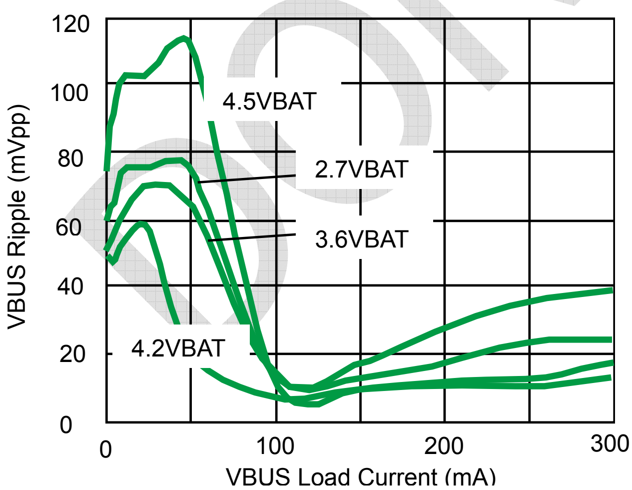


Fig 28. Output Ripple vs. VBAT

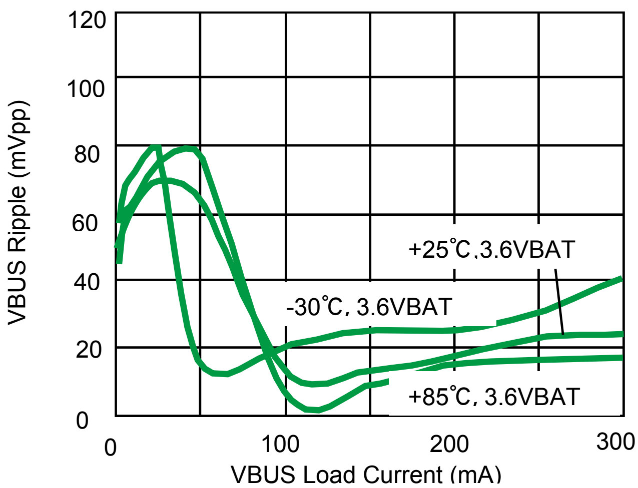


Figure 29. Output Ripple vs. Temperature

Figure 30.Startup, 3.6VBAT,44Ω Load, Additional 10μF, X5R Across VBUS

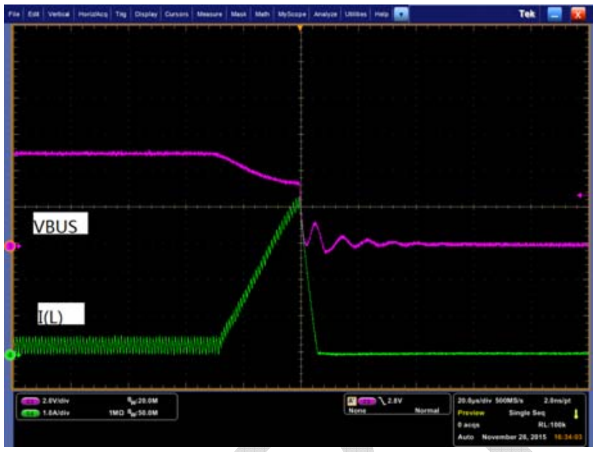


Figure 31. VBUS Fault Response, 3.6VBAT

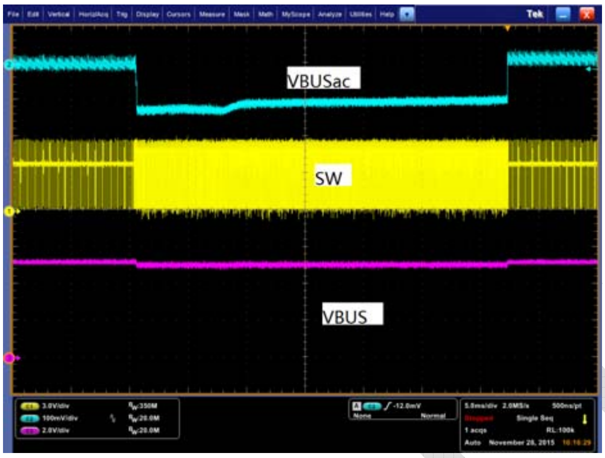


Figure 32. Load Transient, 1-150-1mA, t_R=t_F=100ns

Circuit Description/ Overview

When charging batteries with a current-limited input source, such as USB, a switching charger's high efficiency over a wide range of output voltages minimizes charging time.

PSC5415 combines a highly integrated synchronous buck regulator for charging with a synchronous boost regulator, which can supply 5V to USB On-The-Go (OTG) peripherals. The regulator employs synchronous rectification for both the charger and boost regulators to maintain high efficiency over a wide range of battery voltages and charge states.

The PSC5415 has three operating modes:

1. Charge Mode (VBUS is valid.):

Charge a single-cell Li-ion or Li-polymer battery.

2. Boost Mode:

Provide 5V power to USB-OTG with an integrated synchronous rectification boost regulator using the battery as input.

3. Standby mode (VBUS is not valid.)

Current flow from VBUS to the battery or from the battery to VBUS is blocked.

1) If HZ_MODE=0, boost can be turned on thru I2C,this mode consumes about 16uA current from battery.

2) If HZ_MODE=1, boost is always off. This mode consumes lower than 1uA current from the battery.

Note: Default settings are denoted by bold typeface.

Charge Mode

In Charge Mode, PSC5415 employs four regulation loops:

1. Input Current: Limits the amount of current drawn from VBUS. This current is sensed internally and can be programmed through the I^2C interface.
2. Charging Current: Limits the maximum charging current. This current is sensed using an external R_{SENSE} resistor.
3. Charge Voltage: The regulator is restricted from exceeding this voltage. As the internal battery voltage rises, the battery's internal impedance and R_{SENSE} work in conjunction with the charge voltage regulation to decrease the amount of current flowing to the battery. Battery charging is completed when the voltage across R_{SENSE} drops below the I_{TERM} threshold.
4. Input Voltage: PSC5415 employ an additional loop to limit the amount of drop on VBUS to a programmable voltage (V_{SP}) to accommodate "special chargers" that limit current to a lower current than might be available from a "normal" USB wall charger.

Battery Charging Curve

If the battery voltage is below V_{SHORT}, a linear current source pre-charges the battery until V_{BAT} reaches V_{SHORT}. The PWM charging circuit is then started and the battery is charged with a constant current if sufficient input power is available. The current slew rate is limited to prevent overshoot.

The PSC5415 is designed to work with a current-limited input source at VBUS. During the current regulation phase of charging, I_{INLIM} or the programmed charging current limits the amount of current available to charge the battery and power the system. The effect of I_{INLIM} on I_{CHARGE} can be seen in Figure 35.

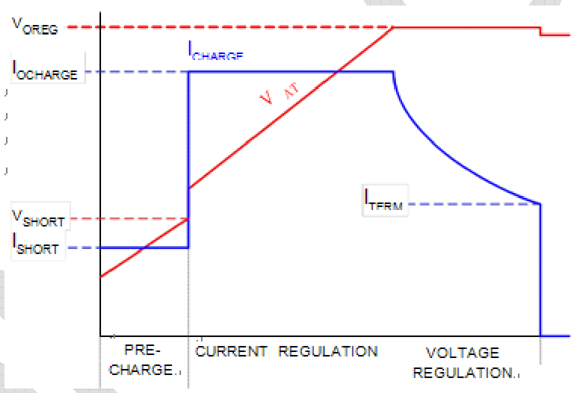


Figure 34. Charge Curve, I_{CHARGE} Not Limited by I_{INLIM}

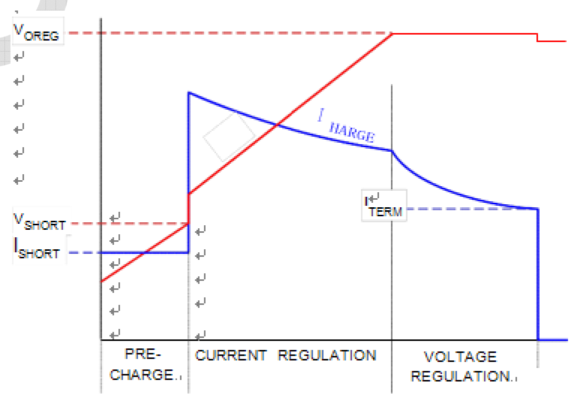


Figure 35. Charge Curve, I_{INLIM} Limits I_{CHARGE}

Assuming that V_{OREG} is programmed to the cell's fully charged "float" voltage, the current that the battery accepts with the PWM regulator limiting its output (sensed at VBAT) to V_{OREG} declines, and the charger enters the voltage regulation phase of charging. When the current declines to the programmed I_{TERM} value, the charge cycle is complete. Charge current termination can be disabled by resetting the TE bit (REG1[3]).

The charger output or "float" voltage can be programmed by the OREG bits from 4.2V to 4.4V as shown in Table 3.

Table 3. OREG Bits (OREG[7:2]) vs. Charger V_{OUT} (V_{OREG}) Float Voltage

Decimal	Hex	VOREG
0-35	00-23	4.20
36-44	24-2C	4.35
45-62	2D-3E	4.40

The following charging parameters can be programmed by the host through I^2C:

Table 4. Programmable Charging Parameters

Parameter	Name	Register
Output Voltage Regulation	V_{OREG}	REG2[7:2]
Battery Charging Current Limit	I_{OCHRG}	REG4[6:4]
Input Current Limit	I_{INLIM}	REG1[7:6]
Charge Termination Limit	I_{TERM}	Reserved.
Weak Battery Voltage	V_{LOWV}	Reserved.

A new charge cycle begins when one of the following occurs:

- The battery voltage falls below V_{OREG}-V_{RCH}

Charge Current Limit ($I_{OCHARGE}$)

Table 5. IOCHARGE (REG4 [6:4]) Current as Function of IOCHARGE Bits and RSENSE Resistor Values

DEC	BIN	HEX	V_{RSENSE}(mV)	$I_{OCHARGE}$(mA)	
				68mΩ	100mΩ
0	000	00	34	500	330
1	001	01	44	647	440
2	010	02	54	794	530
3	011	03	65	956	650
4	100	04	75	1103	750
5	101	05	82	1206	820
6	110	06	95	1397	950
7	111	07	105	1544	1050

Termination Current Limit

Current charge termination is enabled when TE (REG1[3])=1. Typical termination current values are 1/10 of charging current.

Function of I_{TERM} Bits (REG4[2:1]) are reserved.

When charge current falls below I_{TERM}, PWM charging stops. If the charging source is still connected, STAT changes to CHARGE DONE (10).

PWM Controller in Charge Mode

The IC uses a current-mode PWM controller to regulate the output voltage and battery charge currents.

Safety Timer

The charger has a time out function for wake-up charge and normal charge. For wake-up charge the internal timer is set to typically 90 minutes. After 90 minutes of charging, if IOLEVEL still keeps HIGH, the charger is turned OFF and will not resume operation.

For normal charging the timer is set to 12 hours.

If the charger is still operating after typical 12 hours it will be turned OFF and will resume operating only if the condition (VOREG-VBAT) >100mV is met.

The 90-min and 12-hour timer can be reset by plugging out/in the adapter

VBUS POR / Non-Compliant Charger Rejection

When VBUS is inserted, VBUS must remain above $V_{IN(MIN)1}$ and below $VBUS_{OVP}$ for t_{VBUS_VALID} (30ms) before the IC initiates charging. The VBUS validation sequence always occurs before charging is initiated or re-initiated (for example, after a VBUS OVP fault or a V_{RCH} recharge initiation).

t_{VBUS_VALID} ensures that unfiltered 50/60Hz chargers and other non-compliant chargers are rejected.

Input Current Limiting

To minimize charging time without overloading VBUS current limitations, the IC's input current limit can be programmed by the I_{INLIM} bits (REG1[7:6]).

Table 7. Input Current Limit

I_{INLIM} REG1[7:6]	Input Current Limit
00	100mA
01	500mA
10	800mA
11	No Limit

Special Charger

The PSC5415 have additional functionality to limit input current in case a current-limited "special charger" is supplying VBUS. The PSC5415 slowly increases the charging current until either:

I_{INLIM} or $I_{OCHARGE}$ is reached or V_{BUS}=V_{SP}

If V_{BUS} collapses to V_{SP} when the current is ramping up, the PSC5415 charge with an input current that keeps V_{BUS}=V_{SP}.

Table 8. VSP as Function of SP Bits (REG5[2:0])

SP (REG5[2])	V_{SP}
0	4.26
1	4.54 (default)

Safety Settings

The PSC5415 contain a SAFETY register (REG6) that prevents the values in OREG (REG2[7:2]) and $I_{OCHARGE}$ (REG4[6:4]) from exceeding the values of the V_{SAFE} and I_{SAFE} values.

The I_{SAFE} (REG6[6:4]) and V_{SAFE} (REG6[3:0]) registers establish values that limit the maximum values of $I_{OCHARGE}$ and V_{OREG} used by the control logic. If the host attempts to write a value higher than V_{SAFE} or I_{SAFE} to OREG or $I_{OCHARGE}$, respectively; the V_{SAFE}, I_{SAFE} value appears as the OREG, $I_{OCHARGE}$ register value, respectively.

Table 9. I_{SAFE} ($I_{OCHARGE}$ Limit) as Function of I_{SAFE} Bits (REG6[6:4])

I_{SAFE} (REG6[6:4])					
DEC	BIN	HEX	V_{RSENSE}(mV)	I_{SAFE}(mA) 68mΩ	I_{SAFE}(mA) 100mΩ
0	000	00	34	500	330
1	001	01	44	647	440
2	010	02	54	794	530
3	011	03	65	956	650
4	100	04	75	1103	750
5	101	05	82	1206	820
6	110	06	95	1397	950
7	111	07	105	1544	1050

Table 10. V_{SAFE} (V_{OREG} Limit) as Function of V_{SAFE} Bits (REG6[3:0])

V_{SAFE} (REG6[3:0])				
DEC	BIN	HEX	Max. OREG (REG2[7:2])	VOTEG Max.
0	0000	00	100011	4.20
1-9	0001-1001	01-09	100100-101100	4.35
10-15	1010-1111	0A-0F	101101-110010	4.4

Thermal Protection

If the temperature increases beyond $T_{SHUTDOWN}$; charging is suspended, the FAULT bits are set to 101. In Suspend Mode, all timers stop and the state of the IC’s logic is preserved. Charging resumes at programmed current after the die cools to about 120℃.

Additional $θ_{JA}$ data points, measured using the PSC5415 evaluation board, are given in Table 11 (measured with T_A=25℃). Note that as power dissipation increases, the effective $θ_{JA}$ decreases due to the larger difference between the die temperature and its ambient.

Charge Mode Input Supply Protection

Input Supply Low-Voltage Detection

The IC continuously monitors VBUS during charging. If V_{BUS} falls below $V_{IN(MIN)}$, the IC terminates charging.

Input Over-Voltage Detection

When the VBUS exceeds $VBUS_{OVP}$, the IC suspends charging

When VBUS falls about 150mV below $VBUS_{OVP}$, the fault is cleared and charging resumes after VBUS is revalidated *(see VBUS POR / Non-Compliant Charger Rejection)*.

Charge Mode Battery Detection & Protection

VBAT Over-Voltage Protection

The OREG voltage regulation loop prevents VBAT from overshooting the OREG voltage by more than 50mV when the battery is removed. When the PWM charger runs with no battery, the TE bit is not set and a battery is inserted that is charged to a voltage higher than V_{OREG}; PWM pulses stop.

System Operation with No Battery

The PSC5415 continue charging after V_{BUS} POR with the default parameters, regulating the V_{BAT} line to 4.2V until the host processor issues commands. In this way, the PSC5415 can start the system without a battery.

Using following sequence is suggested:

1. When VBUS is plugged in, I_{INLIM} is set to 500mA until the system processor powers up and can set parameters through I^2C.
2. Program the Safety Register.
3. Set I_{INLIM} to 11 (no limit).
4. Set OREG to the desired value (typically 4.2V).
5. Reset the IO_LEVEL bit, and then set $I_{OCHARGE}$.
6. Set I_{INLIM} to 500mA if a USB source is connected.

During the initial system startup, while the charger IC is being programmed, the system current is limited to 500mA before step 5. This is the value of the soft-start I_{CHARGE} current used when I_{INLIM} is set to No Limit.

Charger Status / Fault Status

The STAT pin is for test purpose, the IC provides the charging status in REG0[5:4].

The FAULT bits (R0[2:0]) indicate the type of fault in Charge Mode *(see Table 12)*.

Table 12. Fault Status Bits During Charge Mode

Fault Bit			Fault Description
B2	B1	B0	
0	0	0	Normal (No Fault)
0	0	1	VBUS OVP
0	1	0	RESERVED
0	1	1	Poor Input Source
1	0	0	Battery OVP
1	0	1	Thermal Shutdown
1	1	0	RESERVED
1	1	1	RESERVED

Operational Mode Control

OPA_MODE (REG1[0]) and the HZ_MODE (REG1[1]) bits in conjunction with the DISABLE pin define the operational mode of the charger.

Table 14. Operation Mode Control

HZ_ MODE	OPA_MODE	DISABLE	Operation Mode
X	0	0	Charge
X	X	1	Charger disabled
0	1	X	Boost
1	X	X	High Impedance

The IC resets the OPA_MODE bit whenever the boost is deactivated, whether due to a fault or being disabled by setting the HZ_MODE bit. Setting HZ_MODE=1 through I²C won't disable charger but only disable boost function.

Boost Mode

Boost Mode can be enabled if the OTG pin and OPA_MODE bits as indicated in Table 15. The OTG pin ACTIVE state is 1 if OTG_PL=1 and 0 when OTG_PL=0.

If boost is active using the OTG pin, Boost Mode is initiated even if the HZ_MODE=1. The HZ_MODE bit overrides the OPA_MODE bit.

Table 15. Enabling Boost

OTG_EN	OTG Pin	HZ_MODE	OPA_MODE	BOOST
1	ACTIVE	X	X	Enabled
X	X	0	1	Enabled
X	$\overline{\text{ACTIVE}}$	X	0	Disabled
0	X	1	X	Disabled
1	$\overline{\text{ACTIVE}}$	1	1	Disabled
0	ACTIVE	0	0	Disabled

Boost PWM Control

The IC uses a minimum on-time and computed minimum off-time to regulate VBUS. The regulator achieves excellent transient response by employing current-mode modulation. This technique causes the regulator to exhibit a load line. During PWM Mode, the output voltage drops slightly as the input current rises. With a constant V_{BAT}, this appears as a constant output resistance.

PFM Mode

If V_{BUS} > $VREF_{BOOST}$ (nominally 5.15V) when the minimum off-time has ended, the regulator enters PFM Mode. Boost pulses are inhibited until V_{BUS} < $VREF_{BOOST}$. The minimum on-time is increased to enable the output to pump up sufficiently with each PFM boost pulse. Therefore the regulator behaves like a constant on-time regulator, with the bottom of its output voltage ripple at 5.15V in PFM Mode.

Startup

When the boost regulator is shut down, current flow is prevented from V_{BAT} to V_{BUS}, as well as reverse flow from V_{BUS} to V_{BAT}.

SS State

This IC has built-in soft start function to prevent the IC being out of control. The reference voltage is slightly raised to the normal voltage within about 50us. In SS state, peak current is limited as 1.5x of that in normal condition. When SS is done, the current limit is set to 100%.

BST State

This is the normal operating mode of the regulator. The regulator uses a minimum t_{OFF}-minimum t_{ON} modulation scheme. The minimum t_{OFF} is proportional to $\frac{V_{IN}}{V_{OUT}}$ Which keeps the regulator's switching frequency reasonably constant in CCM. $t_{ON(MIN)}$ is proportional to VBAT and is a higher value if the inductor current reached 0 before $t_{OFF(MIN)}$ in the prior cycle.

To ensure the VBUS does not pump significantly above the regulation point, the boost switch remains off as long as FB > V_{REF}.

Boost Faults

If a BOOST fault occurs:

1. The STAT pin pulses.
2. OPA_MODE bit is reset.
3. The power stage is in High-Impedance Mode.
4. The FAULT bits (REG0[2:0]) are set per Table 17.

Restart After Boost Faults

If boost was enabled with the OPA_MODE bit and OTG_EN=0, Boost Mode can only be enabled through subsequent I^2C commands since OPA_MODE is reset on boost faults. If OTG_EN=1 and the OTG pin is still ACTIVE *(see Table 15).*

Table 17. Fault Bits During Boost Mode

Fault Bit			Fault Description
B2	B1	B0	
0	0	0	Normal (No Fault)
0	1	1	V_{BST}<$UVLO_{BST}$
1	0	1	Thermal shutdown

Table 18. MONITOR Register Bit Definitions

BIT#	NAME	STATE		Active When
		0	1	
MONITOR Address 0AH				
7	ITETM_CMP	V_{CSIN}-V_{BAT}<V_{ITERM}	V_{CSIN}-V_{BAT}>V_{ITERM}	Charging with TE=1
		V_{CSIN}-V_{BAT}<1mA	V_{CSIN}-V_{BAT}>1mA	Charging with TE=0
6	VBAT_CMP	V_{BAT}<V_{SHORT}	V_{BAT}>V_{SHORT}	Charging
		V_{BAT}<V_{LOW}	V_{BAT}>V_{LOW}	High-Impedance Mode
		V_{BAT}<$UVLO_{BST}$	V_{BAT}>$UVLO_{BST}$	Boosting
5	LIMCHG	Linear Charging Not Enabled	Linear Charging Enabled	Charging
4	T_120	T_J<120℃	T_J>120℃	
3	ICHG	Charging Current Controlled by I_{CHARGE} Control Loop	Charging Current Not Controlled by I_{CHARGE} Control Loop	Charging
2	IBUS	I_{BUS} Limiting Charging Current	Charge Current Not Limited by I_{BUS}	Charging
1	VBUS_VALID	V_{BUS} Not Valid	V_{BUS} is Valid	V_{BUS} > V_{BAT}
0	CV	Constant Current Charging	Constant Voltage Charging	Charging

I²C Interface

The PSC5415's serial interface is compatible with Standard, Fast, Fast Plus, and High-Speed Mode I²C-Bus® specifications. The PSC5415's SCL line is an input and its SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

Slave Address

Table 19. I²C Slave Address Byte

Part Types	7	6	5	4	3	2	1	0
PSC5415	1	1	0	1	0	1	0	R/ $\overline{W}$

In hex notation, the slave address assumes a 0 LSB. The hex slave address for the PSC5415 is D4H.

Bus Timing

As shown in Figure 43, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

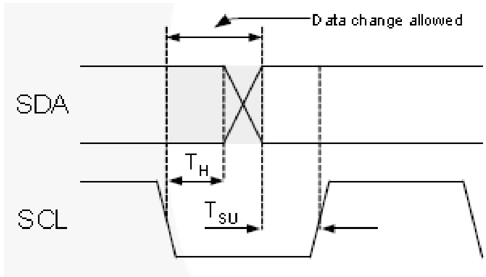


Figure 43. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 44.

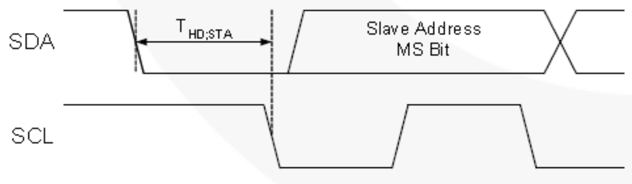


Figure 44. Start Bit

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 45.

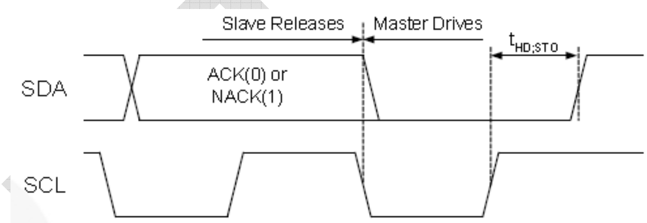


Figure 45. Stop Bit

During a read from the PSC5415 (Figure 48), the master issues a Repeated Start after sending the register address and before resending the slave address. The Repeated Start is a 1-to-0 transition on SDA while SCL is HIGH, as shown in Figure 46.

High-Speed (HS) Mode

The protocols for High-Speed (HS), Low-Speed (LS), and Fast-Speed (FS) Modes are identical except the bus speed for HS Mode is 3.4MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a start condition. The master code is sent in Fast or Fast Plus Mode (less than 1MHz clock); slaves do not ACK this transmission.

The master then generates a repeated start condition (Figure 46) that causes all slaves on the bus to switch to HS Mode. The master then sends I^2C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a stop bit (Figure 45) is sent by the master. While in HS Mode, packets are separated by repeated start conditions (Figure 46).

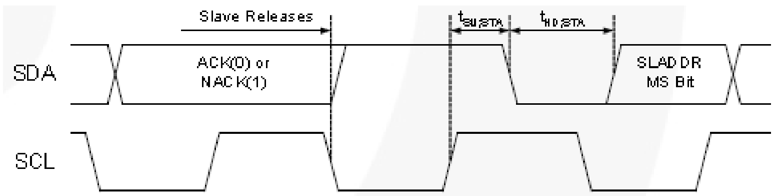


Figure 46. Repeated Start Timing

Read and Write Transactions

The figures below outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as **Master Drives Bus** and **Slave Drives Bus** .

All addresses and data are MSB first.

Table 20. Bit Definitions for Figure 47, Figure 48

Symbol	Definition
S	START, see Figure 44
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	Repeated START, see Figure 46
P	STOP, see Figure 45

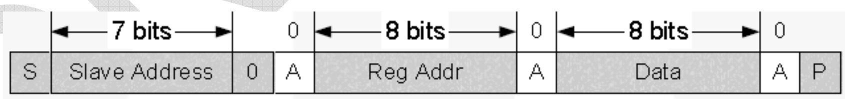


Figure 47. Write Transaction

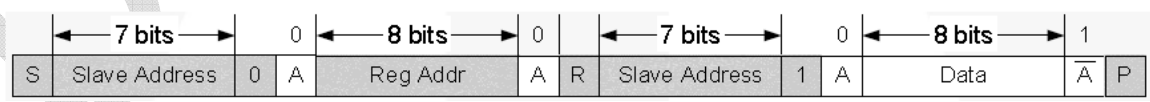


Figure 48. Read Transaction

Register Descriptions

Table 21. I²C Register Address

IC	Register		Address Bits							
	Name	REG#	7	6	5	4	3	2	1	0
PSC5415	CONTROL0	0	0	0	0	0	0	0	0	0
	CONTROL1	1	0	0	0	0	0	0	0	1
	OREG	2	0	0	0	0	0	0	1	0
	IC_INFO	3	0	0	0	0	0	0	1	1
	IBAT	4	0	0	0	0	0	1	0	0
	SP_CHARGER	5	0	0	0	0	0	1	0	1
	SAFETY	6	0	0	0	0	0	1	1	0
	MONITOR	0AH	0	0	0	0	1	0	1	0

Table 22. Register Bit Definitions

This table defines the operation of each register bit for all IC versions. Default values are in bold text.

Bit	Name	Value	Type	Description
CONTROL0				**Register Address:00** **Default Value=X1XX 0XXX**
7:6	-	-	-	Reserved.
5:4	STAT	00	R	Ready
		01		Charge in progress
		10		Charge done
		11		Fault
3	BOOST	0	R	IC is not in Boost Mode
		1		IC is in Boost Mode
2:0	FAULT		R	Fault status bits: *for Charge Mode, see Table 12; for Boost Mode: see Table 17*

<table>
<tr><th>Bit</th><th>Name</th><th>Value</th><th>Type</th><th colspan="2">Description</th></tr>
<tr><td colspan="6">CONTROL1 Register Address:01 Default Value=0111 0000(70H)</td></tr>
<tr><td>7:6</td><td>I_{INLIM}</td><td></td><td>R/W</td><td colspan="2">Input current limit, see Table 7</td></tr>
<tr><td>5:4</td><td>VLOWV</td><td></td><td>R/W</td><td colspan="2">Reserved.</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">TE</td><td>0</td><td>R/W</td><td colspan="2">Disable charge current termination</td></tr>
<tr><td>1</td><td></td><td colspan="2">Enable charge current termination</td></tr>
<tr><td>2</td><td>$\overline{CE}$</td><td>0</td><td>R/W</td><td colspan="2">Set “0”.</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">HZ_MODE</td><td>0</td><td>R/W</td><td>Not High-Impedance Mode</td><td rowspan="4">See Table 15</td></tr>
<tr><td>1</td><td></td><td>High-Impedance Mode</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">OPA_MODE</td><td>0</td><td>R/W</td><td>Charge Mode</td></tr>
<tr><td>1</td><td></td><td>Boost Mode</td></tr>
<tr><td colspan="6">OREG Register Address:02 Default Value=0000 1010(0AH)</td></tr>
<tr><td>7:2</td><td>OREG</td><td></td><td>R/W</td><td colspan="2">Charger output “float” voltage; programmable from 4.2 to 4.4V increments; defaults to 000010 (4.2V), see Table 3</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">OTG_PL</td><td>0</td><td>R/W</td><td colspan="2">OTG pin active LOW</td></tr>
<tr><td>1</td><td></td><td colspan="2">OTG pin active HIGH</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">OTG_EN</td><td>0</td><td>R/W</td><td colspan="2">Disables OTG pin</td></tr>
<tr><td>1</td><td></td><td colspan="2">Enables OTG pin</td></tr>
<tr><td colspan="6">IC_INFO Register Address: 03 or 3B Default Value=1111 0XXX</td></tr>
<tr><td>7:5</td><td>Vendor Code</td><td>111</td><td>R</td><td colspan="2">Identifies Prisemi as the IC supplier</td></tr>
<tr><td>4:3</td><td>PN</td><td>10</td><td>R</td><td colspan="2">10: PSC5415</td></tr>
<tr><td>2:0</td><td>REV</td><td></td><td>R</td><td colspan="2">IC Revision, revision 1.X, where X is the decimal of these three bits</td></tr>
<tr><td colspan="6">IBAT Register Address: 04 Default Value=1000 1001(89H)</td></tr>
<tr><td>7</td><td>-</td><td>1</td><td>W</td><td colspan="2">Reserved.</td></tr>
<tr><td>6:4</td><td>IOCHARGE</td><td>Table 5</td><td>R/W</td><td colspan="2">Programs the maximum charge current, see Table 5</td></tr>
<tr><td>3:0</td><td>-</td><td>-</td><td>R</td><td colspan="2">Reserved.</td></tr>
</table>

Bit	Name	Value	Type	Description
SP_CHARGER				**Register Address: 05** **Default Value=001X X100**
7:6	Reserved	-	-	Reserved
5	IO_LEVEL	0	R/W	Output current is controlled by IOCHARGE bits
		1		Voltage across R_{SENSE} for output current control is set to 34mV (500mA for R_{SENSE}=68mΩ)
4	SP	0	R	Special charger is not active (V_{BUS} is able to stay above V_{SP})
		1		Special charger has been detected and V_{BUS} is being regulated to V_{SP}
3	EN_LEVEL	0	R/W	Reserved.
		1		
2:0	VSP	Table 8	R/W	Special charger input regulation voltage, see Table 8
SAFETY				**Register Address: 06** **Default Value=0100 0000 (40H)**
7	Reserved	0	R	Bit disabled and always returns 0 when read back
6:4	ISAFE	Table 9	R/W	Sets the maximum $I_{OCHARGE}$ value used by the control circuit, see Table 9
3:0	VSAFE	Table 10	R/W	Sets the maximum V_{OREG} used by the control circuit, see Table 10
MONITOR				**Register Address: 0AH (10)** **See Table 18**
7	ITERM_CMP	See Table 18	R	I_{TERM} comparator output, 1 when V_{RSENSE} > I_{TERM} reference
6	VBAT_CMP		R	Output of VBAT comparator
5	LINCHG		R	30mA linear charger ON
4	T_120		R	Thermal regulation comparator;
3	ICHG		R	0 indicates the I_{CHARGE} loop is controlling the battery charge current
2	IBUS		R	0 indicates the I_{BUS} (input current) loop is controlling the battery charge current
1	VBUS_VALID		R	1 indicates V_{BUS} has passed validation and is capable of charging
0	CV		R	1 indicates the constant-voltage loop (OREG) is controlling the charger and all current limiting loops have released

PCB Layout Considerations

1. To obtain optimal performance, the power input capacitors, connected from input to PGND, should be placed as close as possible to the pin. The output inductor should be placed close to the IC and the output capacitor connected between the inductor and PGND of the IC. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin. To prevent high frequency oscillation problems, proper layout to minimize high frequency current path loop is critical. (See Figure 49.) The sense resistor should be adjacent to the junction of the inductor and output capacitor. Route the sense leads connected across the RSNS back to the IC, close to each other (minimize loop area) or on top of each other on adjacent layers (do not route the sense leads through a high-current path). (See Figure 50.)

2. Place all decoupling capacitors close to their respective IC pins and close to PGND (do not place components such that routing interrupts power stage currents). All small control signals should be routed away from the high current paths.

3. The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, two vias for the IC PGND, one via per capacitor for small- signal components). A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is no ground-bounce issue, and having the components segregated minimizes coupling between signals.

4. The high-current charge paths into VBUS, PMID and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins should be connected to the ground plane to return current through the internal low-side FET.

5. Place 22μF input capacitor as close to PMID pin and PGND pin as possible to make high frequency current loop area as small as possible. Place 1μF input capacitor as close to VBUS pin and PGND pin as possible to make high frequency current loop area as small as possible (see Figure 51).

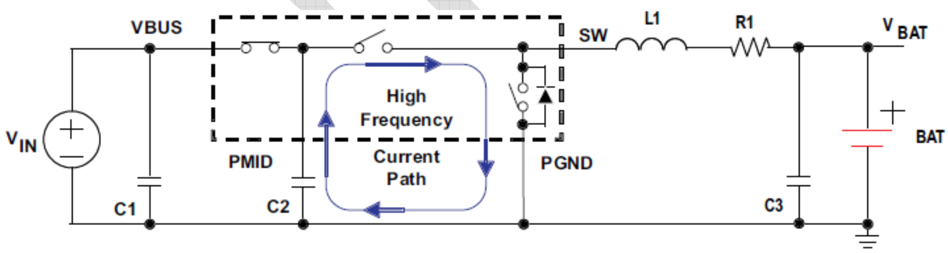


Figure 49. high frequency current path

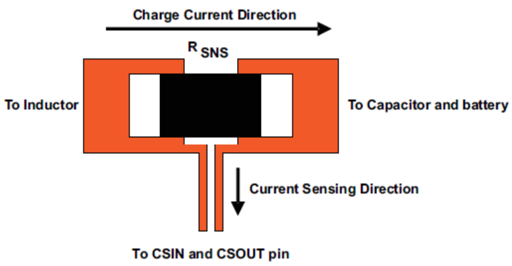


Figure 50. Sensing resistor PCB layout

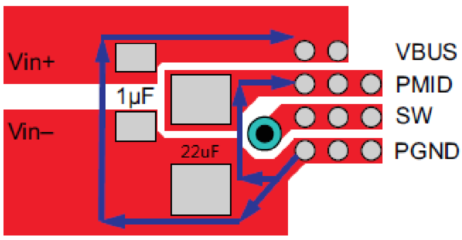
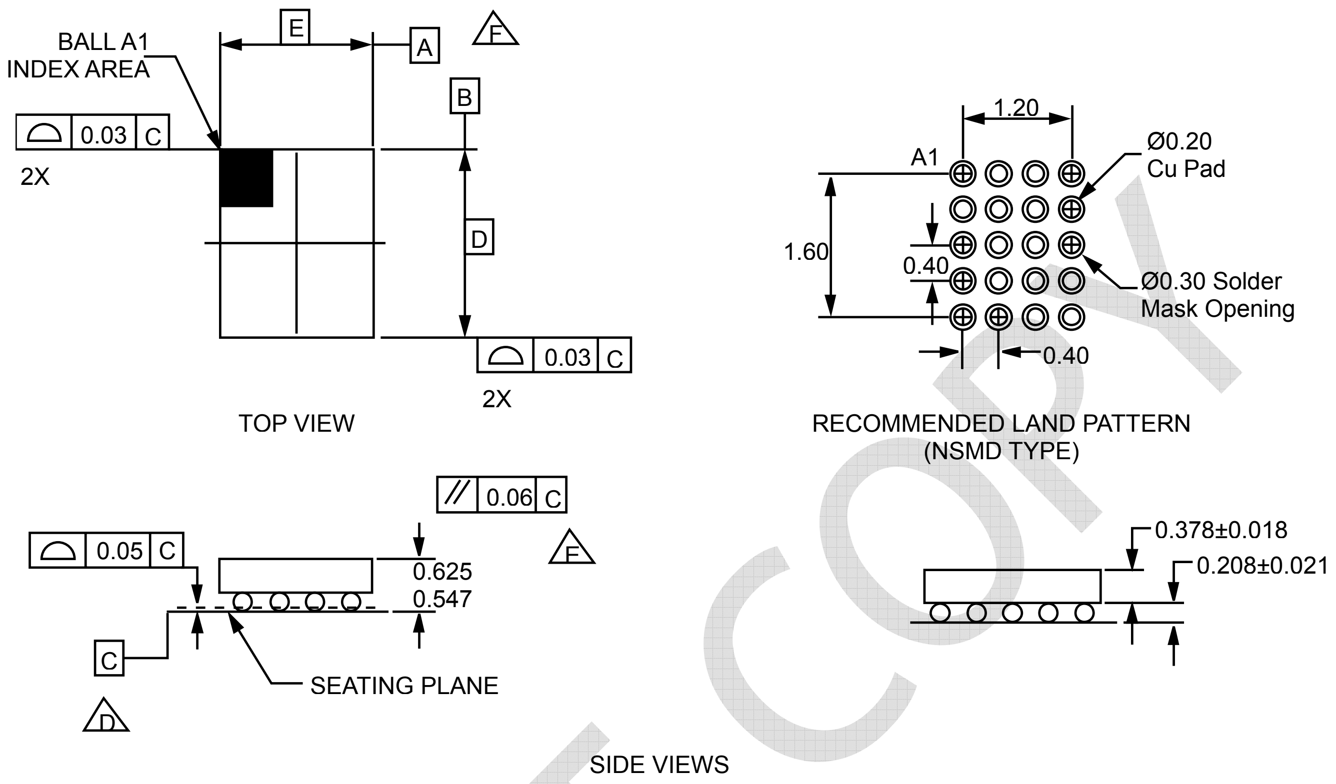
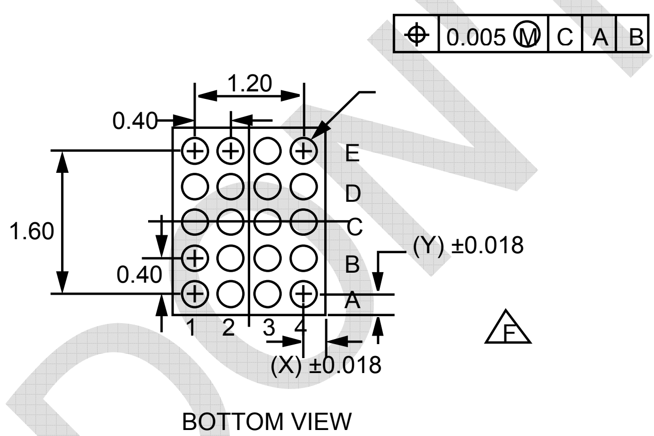


Figure 51. Input capacitor position and PCB layout example

Product dimension





NOTES:

A.NO JEDEC REGISTRATION APPLIES.

B.DIMENSIONS ARE IN MILLIMETERS.

C.DIMENSIONS AND TOLERANCE PER ASMER14.5M,1994.

D.DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E.PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS(547-625 MICRONS).

F.FOR DIMENSIONS D,E,X,AND Y SEE PRODUCT DATASHEET.

G.DRAWING FILNAME:MKT-UC020AArev2.

Figure 50. 20-Ball WLCSP, 4x5 Array, 0.4mm Pitch, 250µm Ball

Product-Specific Dimensions (mm)

Product	D	E	X	Y
PSC5415	2.000±0.030	1.700±0.030	0.335	0.180