



Is Now Part of



**ON Semiconductor®**

To learn more about ON Semiconductor, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (\_), the underscore (\_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (\_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at [www.onsemi.com](http://www.onsemi.com). Please email any questions regarding the system integration to [Fairchild\\_questions@onsemi.com](mailto:Fairchild_questions@onsemi.com).

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.



January 2016

# Single-Channel: 6N137M, HCPL2601M, HCPL2611M Dual-Channel: HCPL2630M, HCPL2631M 8-Pin DIP High-Speed 10 MBit/s Logic Gate Optocouplers

## Features

- Very High Speed – 10 MBit/s
- Superior CMR – 10 kV/μs
- Fan-out of 8 Over -40°C to +85°C
- Logic Gate Output
- Strobable Output
- Wired OR-open Collector
- Safety and Regulatory Approvals
  - UL1577, 5,000 VAC<sub>RMS</sub> for 1 Minute
  - DIN EN/IEC60747-5-5

## Applications

- Ground Loop Elimination
- LSTTL to TTL, LSTTL or 5 V CMOS
- Line Receiver, Data Transmission
- Data Multiplexing
- Switching Power Supplies
- Pulse Transformer Replacement
- Computer-peripheral Interface

## Description

The 6N137M, HCPL2601M, HCPL2611M single-channel and HCPL2630M, HCPL2631M dual-channel optocouplers consist of a 850 nm AlGaAs LED, optically coupled to a very high speed integrated photo-detector logic gate with a strobable output. This output features an open collector, thereby permitting wired OR outputs. The switching parameters are guaranteed over the temperature range of -40°C to +85°C. A maximum input signal of 5 mA will provide a minimum output sink current of 13 mA (fan out of 8).

An internal noise shield provides superior common mode rejection of typically 10 kV/μs. The HCPL2601M and HCPL2631M has a minimum CMR of 5 kV/μs. The HCPL2611M has a minimum CMR of 10 kV/μs.

## Schematics



A 0.1μF bypass capacitor must be connected between pins 8 and 5<sup>(1)</sup>.

Figure 1. Schematics

## Package Outlines



Figure 2. Package Options

## Truth Table (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

## Safety and Insulation Ratings

As per DIN EN/IEC 60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Parameter	Characteristics	
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	< 150 V <sub>RMS</sub>	I-IV
	< 300 V <sub>RMS</sub>	I-IV
	< 450 V <sub>RMS</sub>	I-III
	< 600 V <sub>RMS</sub>	I-III
Climatic Classification	40/100/21	
Pollution Degree (DIN VDE 0110/1.89)	2	
Comparative Tracking Index	175	

Symbol	Parameter	Value	Unit
V <sub>PR</sub>	Input-to-Output Test Voltage, Method A, V <sub>IORM</sub> × 1.6 = V <sub>PR</sub> , Type and Sample Test with t <sub>m</sub> = 10 s, Partial Discharge < 5 pC	1,335	V <sub>peak</sub>
	Input-to-Output Test Voltage, Method B, V <sub>IORM</sub> × 1.875 = V <sub>PR</sub> , 100% Production Test with t <sub>m</sub> = 1 s, Partial Discharge < 5 pC	1,669	V <sub>peak</sub>
V <sub>IORM</sub>	Maximum Working Insulation Voltage	890	V <sub>peak</sub>
V <sub>IOTM</sub>	Highest Allowable Over-Voltage	6,000	V <sub>peak</sub>
	External Creepage	≥ 8.0	mm
	External Clearance	≥ 7.4	mm
	External Clearance (for Option TV, 0.4" Lead Spacing)	≥ 10.16	mm
DTI	Distance Through Insulation (Insulation Thickness)	≥ 0.5	mm
T <sub>S</sub>	Case Temperature <sup>(2)</sup>	150	°C
I <sub>S,INPUT</sub>	Input Current <sup>(2)</sup>	200	mA
P <sub>S,OUTPUT</sub>	Output Power (Duty Factor ≤ 2.7%) <sup>(2)</sup>	300	mW
R <sub>IO</sub>	Insulation Resistance at T <sub>S</sub> , V <sub>IO</sub> = 500 V <sup>(2)</sup>	> 10 <sup>9</sup>	Ω

### Notes:

- The V<sub>CC</sub> supply to each optoisolator must be bypassed by a 0.1 μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V<sub>CC</sub> and GND pins of each device.
- Safety limit value - maximum values allowed in the event of a failure.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Value	Unit	
$T_{STG}$	Storage Temperature	-40 to +125	$^\circ\text{C}$	
$T_{OPR}$	Operating Temperature	-40 to +100	$^\circ\text{C}$	
$T_J$	Junction Temperature	-40 to +125	$^\circ\text{C}$	
$T_{SOL}$	Lead Solder Temperature	260 for 10 sec	$^\circ\text{C}$	
Symbol	Parameter	Device	Value	Unit
<b>EMITTER</b>				
$I_F$ (avg)	DC/Average Forward Input Current Per Channel	Single Channel	50	mA
		Dual Channel	30	
$V_E$	Enable Input Voltage Not to Exceed $V_{CC}$ by more than 500 mV	Single Channel	5.5	V
$V_R$	Reverse Input Voltage Per Channel	All	5.0	V
$P_I$	Input Power Dissipation Per Channel	Single Channel	100	mW
		Dual Channel	45	
<b>DETECTOR</b>				
$V_{CC}$	Supply Voltage	All	-0.5 to 7.0	V
$I_O$ (avg)	Average Output Current Per Channel	All	25	mA
$I_O$ (pk)	Peak Output Current Per Channel	All	50	mA
$V_O$	Output Voltage Per Channel	All	-0.5 to 7.0	V
$P_O$	Output Power Dissipation Per Channel	Single Channel	85	mW
		Dual Channel	60	

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply Voltage	4.5	5.5	V
$I_{FL}$	Input Current, Low Level	0	250	$\mu\text{A}$
$I_{FH}$	Input Current, High Level	6.3 <sup>(3)</sup>	20.0	mA
$V_{EL}$	Enable Voltage, Low Level	0	0.8	V
$V_{EH}$	Enable Voltage, High Level	2.0	$V_{CC}$	V
$T_A$	Ambient Operating Temperature	-40	+85	$^\circ\text{C}$
N	Fan Out (TTL load)		8	

### Note:

- 6.3 mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0 mA or less.

## Electrical Characteristics

**Individual Component Characteristics** ( $V_{CC} = 5.5\text{ V}$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Device	Test Conditions	Min.	Typ.	Max.	Unit
<b>EMITTER</b>							
$V_F$	Input Forward Voltage	All	$I_F = 10\text{ mA}$ , $T_A = 25^\circ\text{C}$		1.45	1.70	V
			$I_F = 10\text{ mA}$			1.80	
$B_{VR}$	Input Reverse Breakdown Voltage	All	$I_R = 10\text{ }\mu\text{A}$	5.0			V
$C_{IN}$	Input Capacitance	All	$V_F = 0$ , $f = 1\text{ MHz}$		60		pF
$\Delta V_F / \Delta T_A$	Temperature Coefficient of Forward Voltage	All	$I_F = 10\text{ mA}$		-1.4		mV/ $^\circ\text{C}$
<b>DETECTOR</b>							
$I_{CCL}$	Logic Low Supply Current	Single Channel	$I_F = 10\text{ mA}$ , $V_O = \text{Open}$ , $V_E = 0.5\text{ V}$		8	13	mA
		Dual Channel	$I_{F1} = I_{F2} = 10\text{ mA}$ , $V_O = \text{Open}$		14	21	
$I_{CCH}$	Logic High Supply Current	Single Channel	$I_F = 0\text{ mA}$ , $V_O = \text{Open}$ , $V_E = 0.5\text{ V}$		6	10	mA
		Dual Channel	$I_F = 0\text{ mA}$ , $V_O = \text{Open}$ ,		10	15	
$I_{EL}$	Low Level Enable Current	Single Channel	$V_E = 0.5\text{ V}$		-0.7	-1.6	mA
$I_{EH}$	High Level Enable Current	Single Channel	$V_E = 2.0\text{ V}$		-0.5	-1.6	mA
$V_{EL}$	Low Level Enable Voltage	Single Channel	$I_F = 10\text{ mA}^{(4)}$			0.8	V
$V_{EH}$	High Level Enable Voltage	Single Channel	$I_F = 10\text{ mA}$	2.0			V

**Note:**

4. Enable Input – No pull up resistor required as the device has an internal pull up resistor.

**Transfer Characteristics** ( $V_{CC} = 5.5\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Device	Test Conditions	Min.	Typ.	Max.	Unit
$I_{FT}$	Input Threshold Current	All	$V_O = 0.6\text{ V}$ , $V_E = 2.0\text{ V}$ , $I_{OL} = 13\text{ mA}$		3	5	mA
$I_{OH}$	HIGH Level Output Current	All	$V_O = 5.5\text{ V}$ , $I_F = 250\text{ }\mu\text{A}$ , $V_E = 2.0\text{ V}$			100	$\mu\text{A}$
$V_{OL}$	LOW Level Output Voltage	All	$I_F = 5\text{ mA}$ , $V_E = 2.0\text{ V}$ , $I_{OL} = 13\text{ mA}$		0.4	0.6	V

## Electrical Characteristics (Continued)

**Switching Characteristics** ( $V_{CC} = 5\text{ V}$ ,  $I_F = 7.5\text{ mA}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Device	Test Conditions	Min.	Typ.	Max.	Unit
$t_{PHL}$	Propagation Delay Time to Logic LOW	All	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$ , $T_A = 25^\circ\text{C}^{(5)}$ (Fig. 14)	25	40	75	ns
			$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}^{(6)}$ (Fig. 14)			100	
$t_{PLH}$	Propagation Delay Time to Logic HIGH	All	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$ , $T_A = 25^\circ\text{C}^{(6)}$ (Fig. 14)	20	40	75	ns
			$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}^{(6)}$ (Fig. 14)			100	
$ t_{PHL} - t_{PLH} $	Pulse Width Distortion	All	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$ (Fig. 14)		1	35	ns
$t_R$	Output Rise Time (10% to 90%)	All	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}^{(7)}$ (Fig. 14)		30		ns
$t_F$	Output Fall Time (90% to 10%)	All	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}^{(8)}$ (Fig. 14)		10		ns
$t_{EHL}$	Enable Propagation Delay Time to Output LOW Level	Single Channel	$V_{EH} = 3.5\text{ V}$ , $R_L = 350\ \Omega$ , $C_L = 15\text{ pF}^{(9)}$ (Fig. 15)		15		ns
$t_{ELH}$	Enable Propagation Delay Time to Output HIGH Level	Single Channel	$V_{EH} = 3.5\text{ V}$ , $R_L = 350\ \Omega$ , $C_L = 15\text{ pF}^{(10)}$ (Fig. 15)		15		ns
$ CM_H $	Common Mode Transient Immunity at Logic High	6N137M, HCPL2630M	$I_F = 0\text{ mA}$ , $V_{CM} = 50\text{ V}_{PEAK}$ , $R_L = 350\ \Omega$ , $T_A = 25^\circ\text{C}^{(11)}$ (Fig. 16)		10,000		V/ $\mu\text{s}$
		HCPL2601M, HCPL2631M		5000	10,000		
		HCPL2611M		10,000	15,000		
$ CM_L $	Common Mode Transient Immunity at Logic Low	6N137M, HCPL2630M	$V_{CM} = 50\text{ V}_{PEAK}$ , $R_L = 350\ \Omega$ , $T_A = 25^\circ\text{C}^{(11)}$ (Fig. 16)		10,000		V/ $\mu\text{s}$
		HCPL2601M, HCPL2631M		5000	10,000		
		HCPL2611M		10,000	15,000		

### Notes:

- $t_{PHL}$  – Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
- $t_{PLH}$  – Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
- $t_R$  – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
- $t_F$  – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
- $t_{EHL}$  – Enable input propagation delay is measured from the 1.5 V level on the LOW to HIGH transition of the input voltage pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
- $t_{ELH}$  – Enable input propagation delay is measured from the 1.5 V level on the HIGH to LOW transition of the input voltage pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
- Common mode transient immunity in logic high level is the maximum tolerable (positive)  $dV_{cm}/dt$  on the leading edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a logic high state (i.e.,  $V_O > 2.0\text{ V}$ ). Common mode transient immunity in logic low level is the maximum tolerable (negative)  $dV_{cm}/dt$  on the trailing edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a logic low state (i.e.,  $V_O < 0.8\text{ V}$ ).

## Electrical Characteristics (Continued)

### Isolation Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified.)

Symbol	Parameter	Device	Test Conditions	Min.	Typ.	Max.	Unit
$V_{\text{ISO}}$	Withstand Insulation Test Voltage	All	Relative Humidity $\leq 50\%$ , $I_{\text{I-O}} \leq 10 \mu\text{A}$ , $t = 1 \text{ min}$ , $f = 50 \text{ Hz}^{(12)(13)}$	5,000			$\text{VAC}_{\text{RMS}}$
$R_{\text{I-O}}$	Resistance (Input to Output)	All	$V_{\text{I-O}} = 500 \text{ V}_{\text{DC}}^{(12)}$		$10^{11}$		$\Omega$
$C_{\text{I-O}}$	Capacitance (Input to Output)	All	$f = 1 \text{ MHz}$ , $V_{\text{I-O}} = 0 \text{ V}_{\text{DC}}^{(12)}$		1		pF
$I_{\text{I-O}}$	Input-Output Insulation Leakage Current	All	Relative Humidity $\leq 45\%$ , $V_{\text{I-I}} = 3000 \text{ V}_{\text{DC}}$ , $t = 5 \text{ sec}^{(12)}$			1.0	$\mu\text{A}$

#### Notes:

12. Device is considered a two terminal device: pins 1, 2, 3 and 4 are shorted together and pins 5, 6, 7 and 8 are shorted together.
13. 5000  $\text{VAC}_{\text{RMS}}$  for 1 minute duration is equivalent to 6000  $\text{VAC}_{\text{RMS}}$  for 1 second duration.

## Typical Performance Curves

For Single-Channel Devices: 6N137M, HCPL2601M, and HCPL2611M



Figure 3. Low Level Output Voltage vs. Ambient Temperature

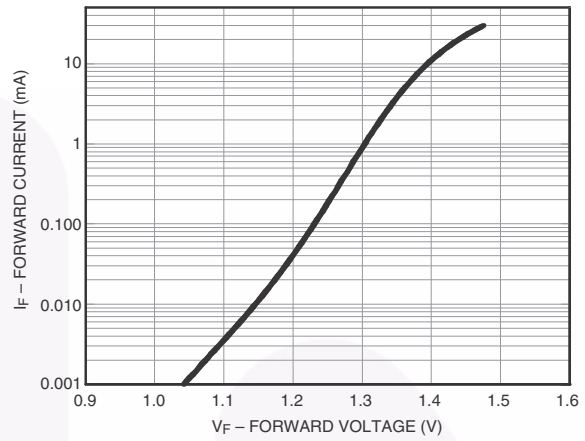


Figure 4. Input Diode Forward Voltage vs. Forward Current

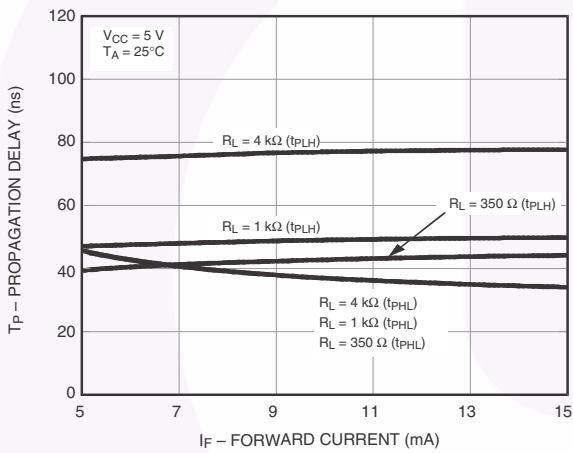


Figure 5. Switching Time vs. Forward Current

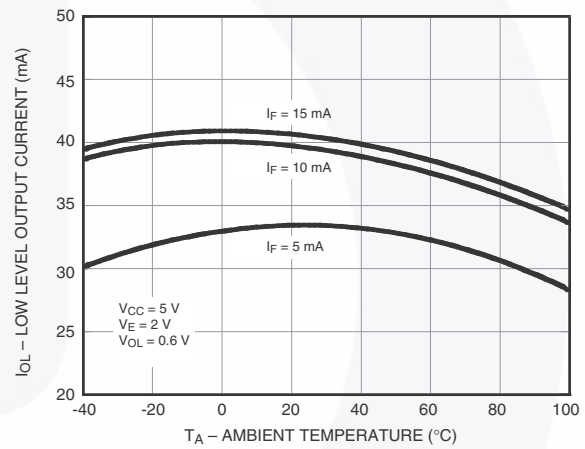


Figure 6. Low Level Output vs. Ambient Temperature

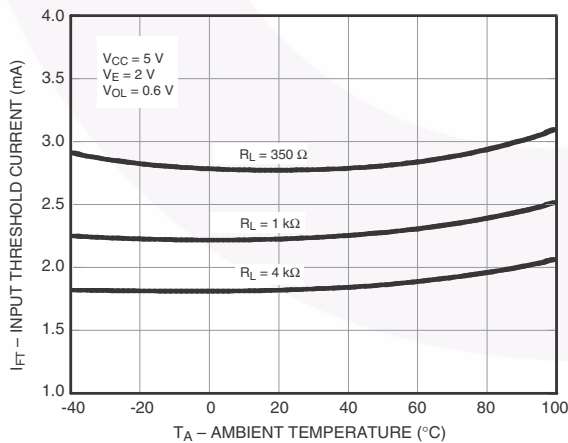


Figure 7. Input Threshold Current vs. Ambient Temperature

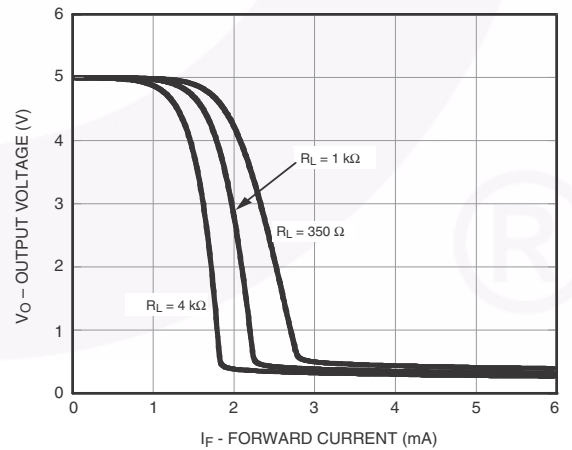


Figure 8. Output Voltage vs. Input Forward Current



## Typical Performance Curves (Continued)

For Single-Channel Devices: 6N137M, HCPL2601M, HCPL2611M



Figure 9. Pulse Width Distortion vs. Temperature



Figure 10. Rise and Fall Time vs. Temperature



Figure 11. Enable Propagation Delay vs. Temperature



Figure 12. Switching Time vs. Temperature

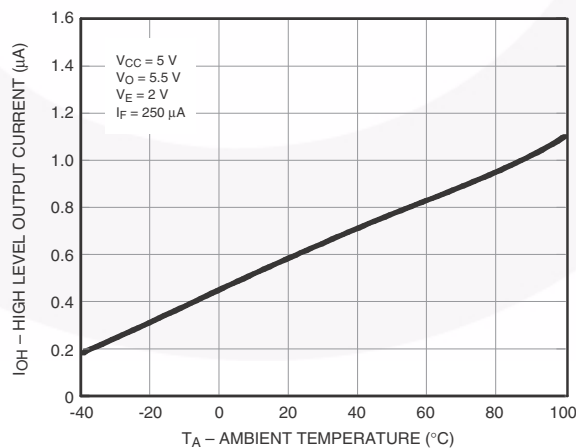


Figure 13. High Level Output Current vs. Temperature

## Typical Performance Curves (Continued)

For Dual-Channel Devices: HCPL2630M and HCPL2631M

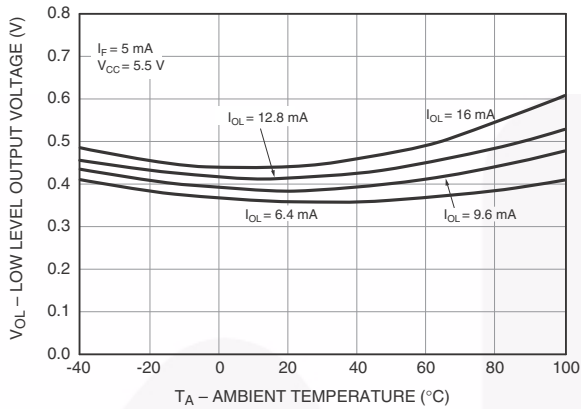


Figure 14. Low Level Output Voltage vs. Ambient Temperature



Figure 15. Input Diode Forward Voltage vs. Forward Current

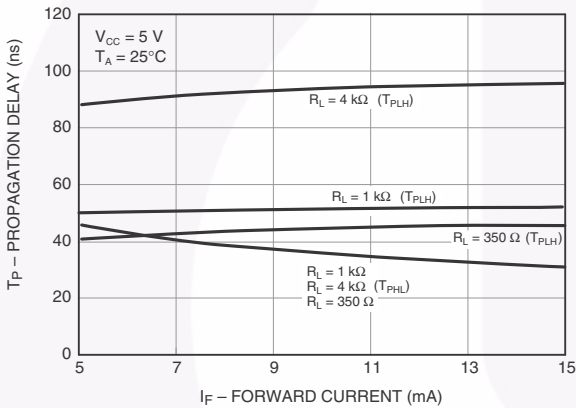


Figure 16. Switching Time vs. Forward Current



Figure 17. Low Level Output Current vs. Ambient Temperature

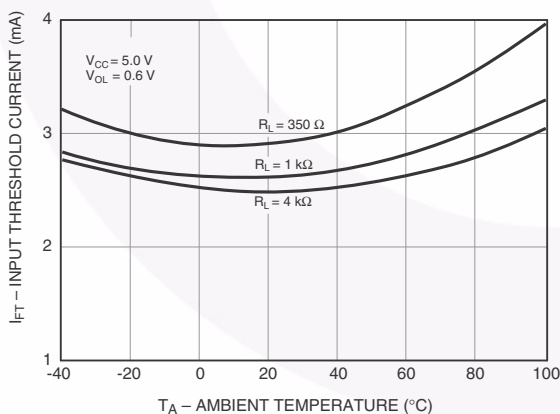


Figure 18. Input Threshold Current vs. Ambient Temperature

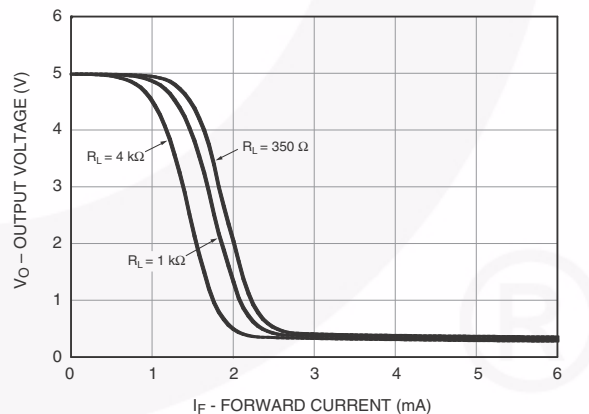


Figure 19. Output Voltage vs. Input Forward Current

## Typical Performance Curves (Continued)

For Dual-Channel Devices: HCPL2630M and HCPL2631M

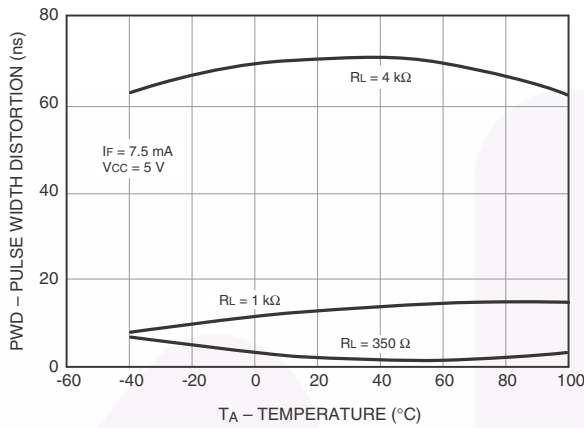


Figure 20. Pulse Width Distortion vs. Temperature



Figure 21. Rise and Fall Time vs. Temperature

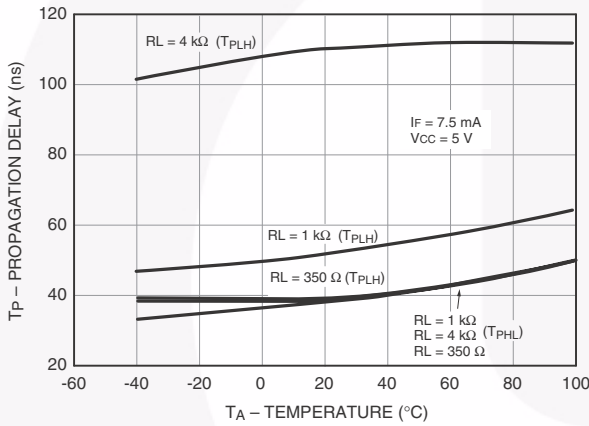


Figure 22. Switching Time vs. Temperature

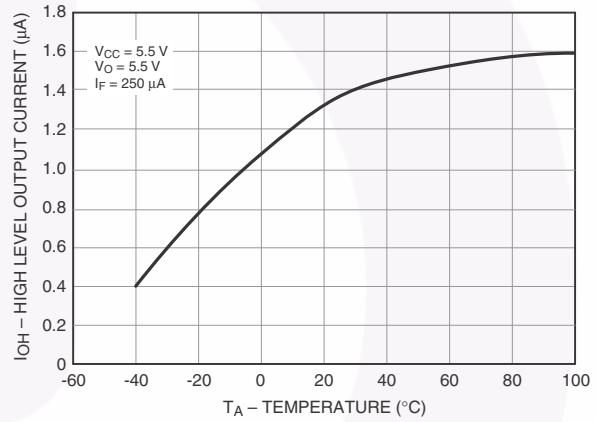


Figure 23. High Level Output Current vs. Temperature

### Test Circuits



Figure 24. Test Circuit and Waveforms for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$  and  $t_f$



Figure 25. Test Circuit  $t_{EHL}$  and  $t_{ELH}$

Test Circuits (Continued)



Figure 26. Test Circuit Common Mode Transient Immunity

## Reflow Profile



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmín)	150°C
Temperature Max. (Tsmáx)	200°C
Time (ts) from (Tsmín to Tsmáx)	60 to 120 s
Ramp-up Rate (tL to tp)	3°C/second maximum
Liquidous Temperature (TL)	217°C
Time (tL) Maintained Above (TL)	60 to 150 s
Peak Body Package Temperature	260°C +0°C / -5°C
Time (tp) within 5°C of 260°C	30 s
Ramp-down Rate (TP to TL)	6°C/s maximum
Time 25°C to Peak Temperature	8 minutes maximum

Figure 27. Reflow Profile

## Ordering Information

Part Number	Package	Packing Method
6N137M	DIP 8-Pin	Tube (50 units per tube)
6N137SM	SMT 8-Pin (Lead Bend)	Tube (50 units per tube)
6N137SDM	SMT 8-Pin (Lead Bend)	Tape and Reel (1,000 units per reel)
6N137VM	DIP 8-Pin, DIN EN/IEC 60747-5-5 Option	Tube (50 units per tube)
6N137SVM	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 Option	Tube (50 units per tube)
6N137SDVM	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 Option	Tape and Reel (1,000 units per reel)
6N137TVM	DIP 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-5 Option	Tube (50 units per tube)
6N137TSVM	SMT 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-5 Option	Tube (50 units per tube)
6N137TSR2VM	SMT 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-5 Option	Tape and Reel (1,000 units per reel)

### Note:

The product orderable part number system listed in this table also applies to the HCPL2601M, HCPL2611M, HCPL2630M and HCPL2631M product families.

## Marking Information

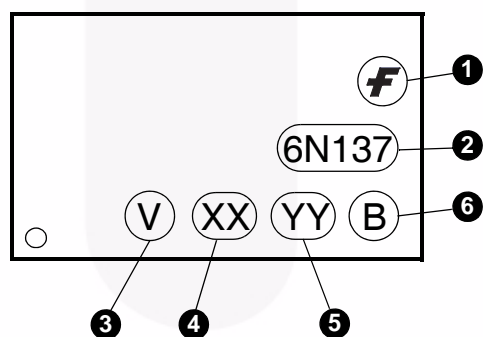
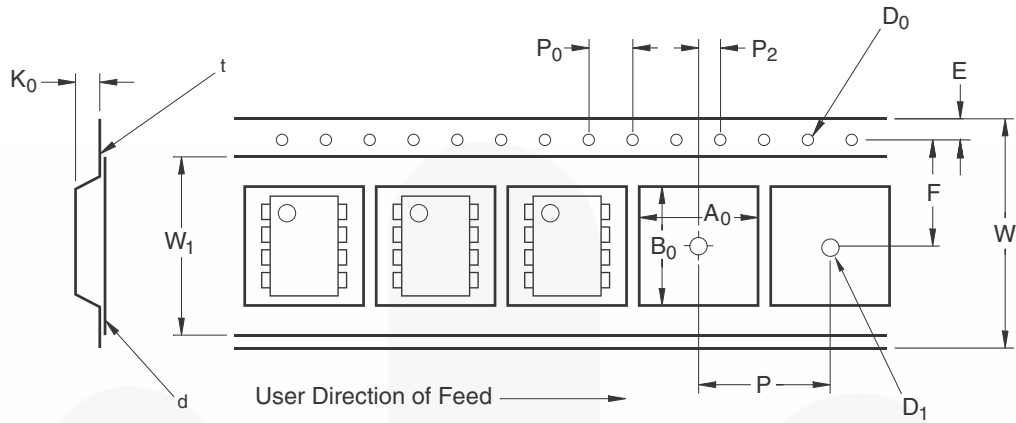


Figure 28. Top Mark

Definitions	
1	Fairchild Logo
2	Device Number
3	DIN EN/IEC60747-5-5 Option (only appears on component ordered with this option)
4	Two Digit Year Code, e.g., '16'
5	Two Digit Work Week Ranging from '01' to '53'
6	Assembly Package Code

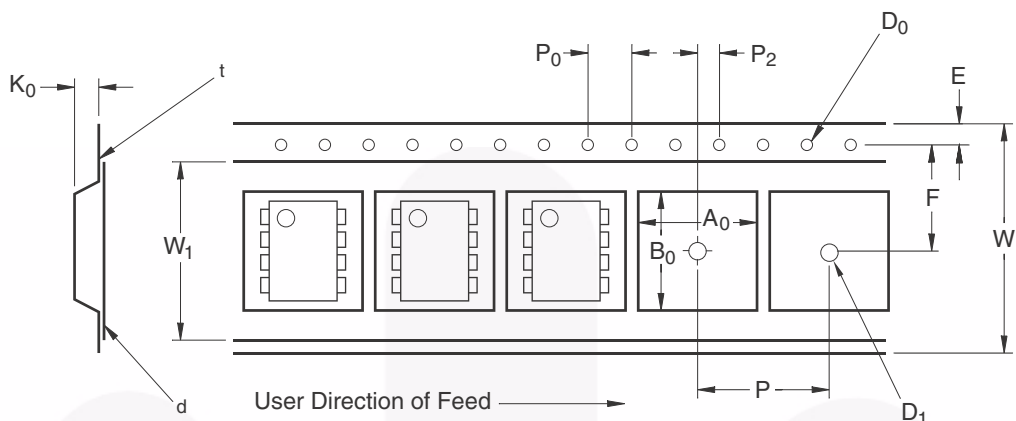
### Carrier Tape Specifications (Option SD)



Symbol	Description	Dimension in mm
W	Tape Width	$16.0 \pm 0.3$
t	Tape Thickness	$0.30 \pm 0.05$
$P_0$	Sprocket Hole Pitch	$4.0 \pm 0.1$
$D_0$	Sprocket Hole Diameter	$1.55 \pm 0.05$
E	Sprocket Hole Location	$1.75 \pm 0.10$
F	Pocket Location	$7.5 \pm 0.1$
$P_2$		$2.0 \pm 0.1$
P	Pocket Pitch	$12.0 \pm 0.1$
$A_0$	Pocket Dimensions	$10.30 \pm 0.20$
$B_0$		$10.30 \pm 0.20$
$K_0$		$4.90 \pm 0.20$
$W_1$	Cover Tape Width	$13.2 \pm 0.2$
d	Cover Tape Thickness	0.1 Maximum
	Maximum Component Rotation or Tilt	$10^\circ$
R	Minimum Bending Radius	30



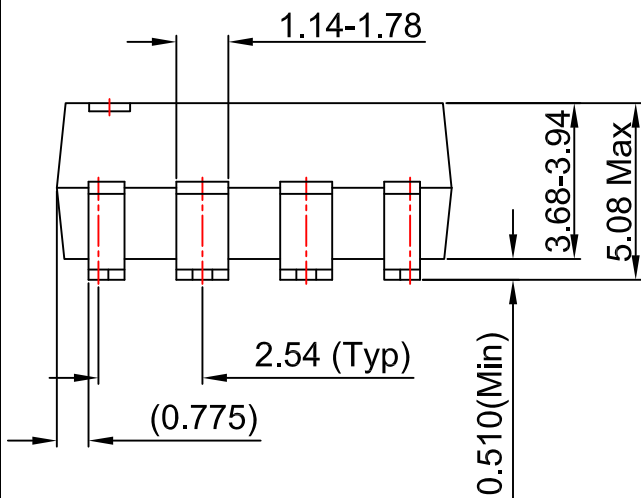
## Carrier Tape Specifications (Option TSR2)



Symbol	Description	Dimension in mm
W	Tape Width	24.0 ± 0.3
t	Tape Thickness	0.40 ± 0.1
P <sub>0</sub>	Sprocket Hole Pitch	4.0 ± 0.1
D <sub>0</sub>	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	11.5 ± 0.1
P <sub>2</sub>		2.0 ± 0.1
P	Pocket Pitch	16.0 ± 0.1
A <sub>0</sub>	Pocket Dimensions	12.80 ± 0.1
B <sub>0</sub>		10.35 ± 0.1
K <sub>0</sub>		5.7 ± 0.1
W <sub>1</sub>	Cover Tape Width	21.0 ± 0.1
d	Cover Tape Thickness	0.1 Maximum
	Maximum Component Rotation or Tilt	10°
R	Minimum Bending Radius	30



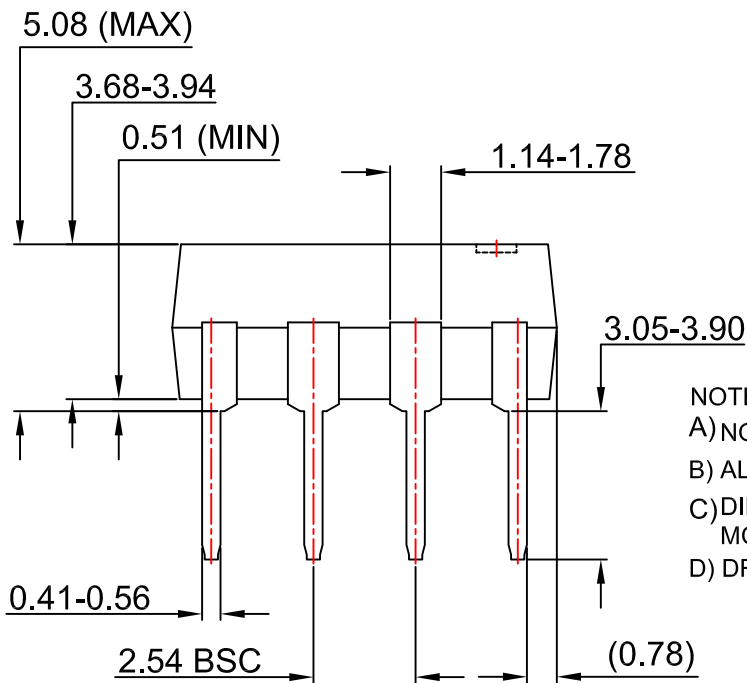
LAND PATTERN RECOMMENDATION



NOTES:

- A) NO STANDARD APPLIES TO THIS PACKAGE
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION
- D) DWG FILENAME AND REVISION: MKT-N08Lrev2.





- NOTES:  
 A) NO STANDARD APPLIES TO THIS PACKAGE  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION  
 D) DRAWING FILENAME AND REVISION: MKT-N08GREV7





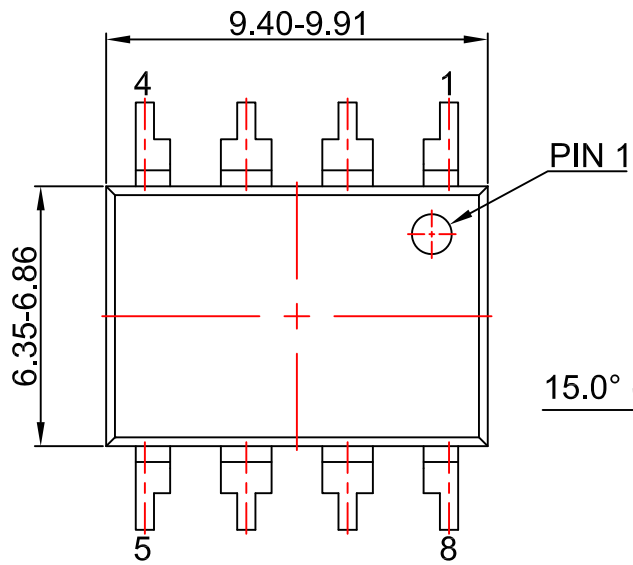
LAND PATTERN RECOMMENDATION



NOTES:

- A) NO STANDARD APPLIES TO THIS PACKAGE
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION
- D) DRAWING FILENAME AND REVISION: MKT-N08Hrev7.



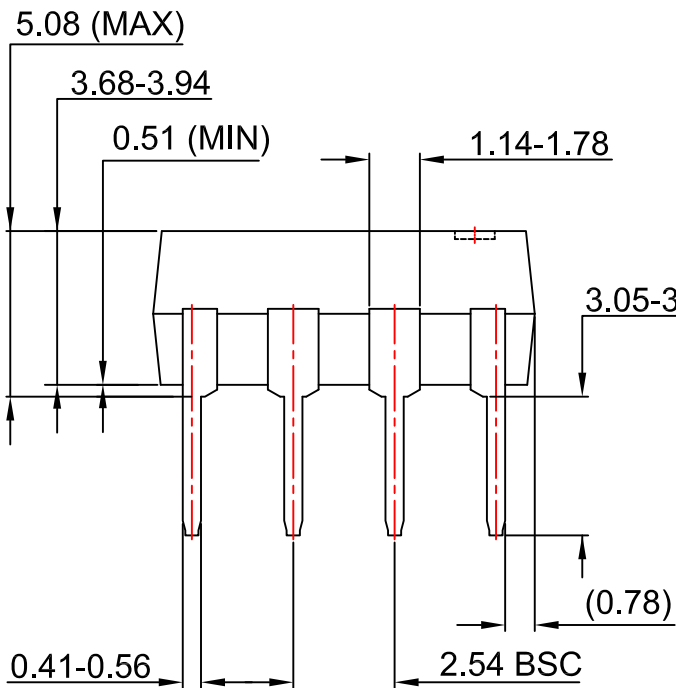


PIN 1

15.0° (MAX)

10.16 (TYP)

0.20-0.40



NOTES:

- A) NO STANDARD APPLIES TO THIS PACKAGE
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION
- D) DRAWING FILENAME AND REVISION: MKT-N08REV7



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative