Low-Noise, 900kHz, RRIO, Precision OPERATIONAL AMPLIFIER Zerø-Drift Series

Check for Samples: OPA378 OPA2378

FEATURES

- LOW NOISE
  - $0.4\mu V_{PP}$, 0.1Hz to 10Hz
  - $20nV/\sqrt{Hz}$ at 1kHz
- ZERØ-DRIFT SERIES
  - LOW OFFSET VOLTAGE: 20μV
  - LOW OFFSET DRIFT: 0.1μV/°C
- QUIESCENT CURRENT: 125μA
- GAIN BANDWIDTH: 900kHz
- RAIL-TO-RAIL INPUT/OUTPUT
- EMI FILTERING
- SUPPLY VOLTAGE: 2.2V to 5.5V
- *micro*SIZE PACKAGES: SC70 and SOT23

APPLICATIONS

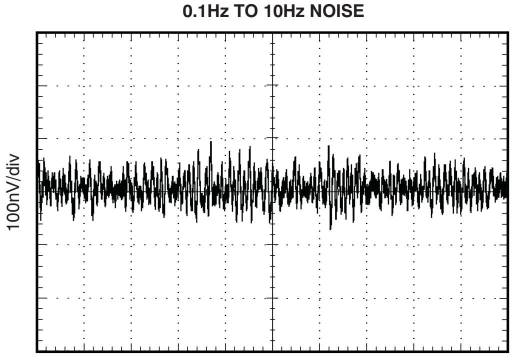
- PORTABLE MEDICAL DEVICES
  - GLUCOSE METERS
  - OXYGEN METERING
  - HEART RATE MONITORS
- WEIGH SCALES
- BATTERY-POWERED INSTRUMENTS
- THERMOPILE MODULES
- HANDHELD TEST EQUIPMENT
- SENSOR SIGNAL CONDITIONING

DESCRIPTION

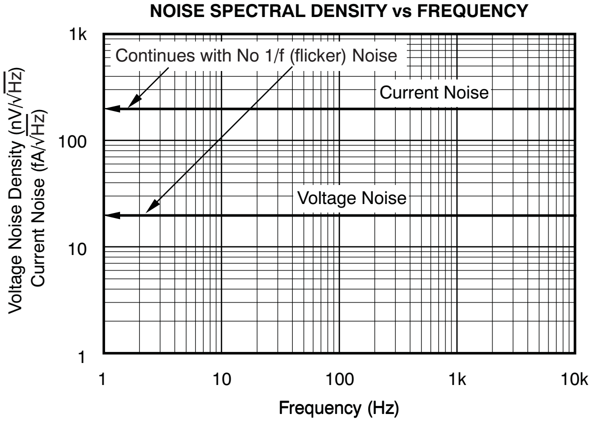
The OPA378 and OPA2378 represent a new generation of Zerø-Drift, microPOWER™ operational amplifiers that use a proprietary auto-calibration technique to provide minimal input offset voltage (20μV) and offset voltage drift (0.1μV/°C). The combination of low input voltage noise, high gain bandwidth (900kHz), and low power (150μA max) enable these devices to achieve optimum performance for low-power precision applications. In addition, the excellent PSRR performance, coupled with a wide input supply range of 2.2V to 5.5V and rail-to-rail input and output, makes it an outstanding choice for single-supply applications that run directly from batteries without regulation.

The OPA378 (single version) is available in both a *micro*SIZE SC70-5 and a SOT23-5 package. The OPA2378 (dual version) is offered in a SOT23-8 package. All versions are specified for operation from –40°C to +125°C.

0.1Hz TO 10Hz NOISE



NOISE SPECTRAL DENSITY vs FREQUENCY



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA378	SOT23-5	DBV	OAZI
OPA378	SC70-5	DCK	BTS
OPA2378	SOT23-8	DCN	OCAI

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

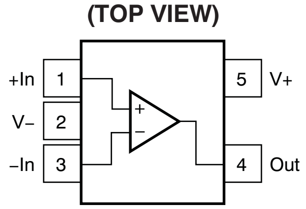
Over operating free-air temperature range (unless otherwise noted).

		OPA378, OPA2378	UNIT
Supply Voltage, V_S = (V+) – (V–)		+7	V
Signal Input Terminals	Voltage(2)	(V–) – 0.3 ≤ V_{IN} ≤ (V+) + 0.3	V
	Current(2)	±10	mA
Output Short-Circuit(3)		Continuous	
Operating Temperature, T_A		–55 to +150	°C
Storage Temperature, T_A		–65 to +150	°C
Junction Temperature, T_J		+150	°C
ESD Ratings	Human Body Model (HBM)	4000	V
	Charged Device Model (CDM)	1000	V
	Machine Model (MM)	200	V

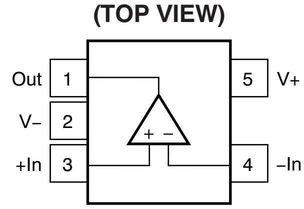
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

PIN CONFIGURATIONS

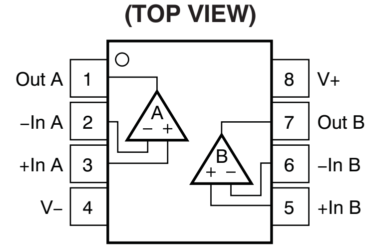
OPA378
SC70-5
(TOP VIEW)



OPA378
SOT23-5
(TOP VIEW)



OPA2378
SOT23-8
(TOP VIEW)



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ELECTRICAL CHARACTERISTICS: V_S = +2.2V to +5.5V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA378, OPA2378 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage, OPA378	V_{OS}	V_{CM} = V–		20	50	µV
vs Temperature	**dV_{OS}/dT**			**0.1**	**0.25**	**µV/°C**
Input Offset Voltage, OPA2378				20	70	µV
vs Temperature	**dV_{OS}/dT**	**-40°C to +125°C**		**0.25**	**0.4**	**µV/°C**
		–40°C to +85°C		0.15	0.25	µV/°C
vs Power Supply, OPA378	PSRR	V_{CM} = 0V, V_S = +2.2V to +5.5V		1.5	5	µV/V
over Temperature		**V_{CM} = 0V, V_S = +2.2V to +5.5V**		**3**	**8**	**µV/V**
vs Power Supply, OPA2378		V_{CM} = 0V, V_S = +2.2V to +5.5V			10	µV/V
over Temperature		**V_{CM} = 0V, V_S = +2.2V to +5.5V**		**3**	**13**	**µV/V**
Channel Separation (Dual Version)		At dc		135		dB
INPUT BIAS CURRENT						
Input Bias Current, OPA378	I_B			±150	±550	pA
Input Bias Current, OPA2378				±150	±670	pA
over Temperature, OPA378 and OPA2378					**±2**	**nA**
Input Offset Current, OPA378	I_{OS}			±0.3	±1.1	nA
Input Offset Current, OPA2378				±0.3	±1.34	nA
NOISE						
Input Voltage Noise	e_n	f = 0.1Hz to 10Hz, V_S = +5.5V		0.4		$µV_{PP}$
Input Voltage Noise Density	e_n	f = 1kHz		20		nV/√Hz
Input Current Noise	i_n	f = 10Hz		200		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) – 0.05		(V+) + 0.05	V
Common-Mode Rejection Ratio	CMRR	(V–) – 0.05V < V_{CM} < (V+) + 0.05V, V_S = 5.5V	100	112		dB
		(V–) – 0.05V < V_{CM} < (V+) + 0.05V, V_S = 2.2V	94	106		dB
over Temperature		**(V–) – 0.05V < V_{CM} < (V+) + 0.05V, V_S = 5.5V**	**96**			**dB**
		(V–) – 0.05V < V_{CM} < (V+) + 0.05V, V_S = 2.2V	**90**			**dB**
INPUT CAPACITANCE						
Differential	C_{IN}			4		pF
Common-Mode				5		pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	50mV < V_O < (V+) – 50mV, R_L = 100kΩ	110	134		dB
		100mV < V_O < (V+) – 100mV, R_L = 10kΩ	110	130		dB
over Temperature		**100mV < V_O < (V+) – 100mV, R_L = 10kΩ**	**106**			**dB**
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW			900		kHz
Slew Rate	SR	G = +1		0.4		V/µs
Settling Time 0.1%	t_S	V_S = 5.5V, 2V Step, G = +1		7		µs
Settling Time 0.01%	t_S	V_S = 5.5V, 2V Step, G = +1		9		µs
Overload Recovery Time		V_{IN} × Gain > V_S		4		µs
THD + Noise	THD + N	V_S = 5V, V_O = $3V_{PP}$, G = +1, f = 1kHz		0.003		%

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ELECTRICAL CHARACTERISTICS: V_S = +2.2V to +5.5V (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA378, OPA2378 MIN	TYP	MAX	UNIT
OUTPUT						
Voltage Output Swing from Rail, OPA378	V_O	R_L = 10kΩ		6	8	mV
over Temperature		**R_L = 10kΩ**		**8**	**13**	**mV**
Voltage Output Swing from Rail, OPA2378	V_O	R_L = 10kΩ		6	10	mV
over Temperature		**R_L = 10kΩ**		**8**	**15**	**mV**
Voltage Output Swing from Rail		R_L = 100kΩ		0.7	2	mV
over Temperature		**R_L = 100kΩ**			**3**	**mV**
Short-Circuit Current	I_{SC}			±30		mA
Capacitive Load Drive	C_{LOAD}			See Figure 18		pF
Open-Loop Output Impedance	Z_O			See Figure 23		Ω
POWER SUPPLY						
Specified Voltage Range	V_S		2.2		5.5	V
Quiescent Current (per Amplifier)	I_Q	I_O = 0mA, V_S = +5.5V		125	150	μA
over Temperature					**165**	**μA**
TEMPERATURE RANGE						
Specified Range			–40		+125	°C
Operating Range			–55		+150	°C
Thermal Resistance	θ_{JA}					°C/W
SOT23-5				200		°C/W
SC70-5				250		°C/W
SOT23-8				100		°C/W

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TYPICAL CHARACTERISTICS

At T_A = +25°C, R_L = 10kΩ, V_S = +5.5V and V_{OUT} = V_S/2, unless otherwise noted.

0.1Hz TO 10Hz NOISE

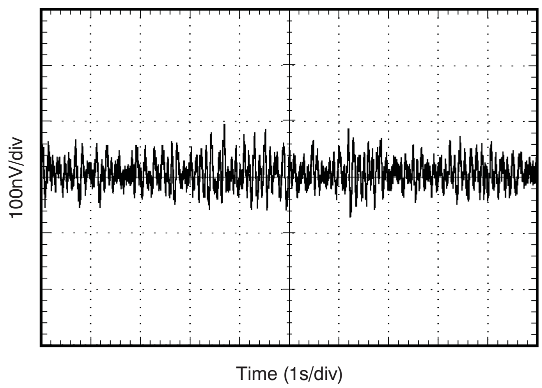

Figure 1.

INPUT CURRENT AND VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

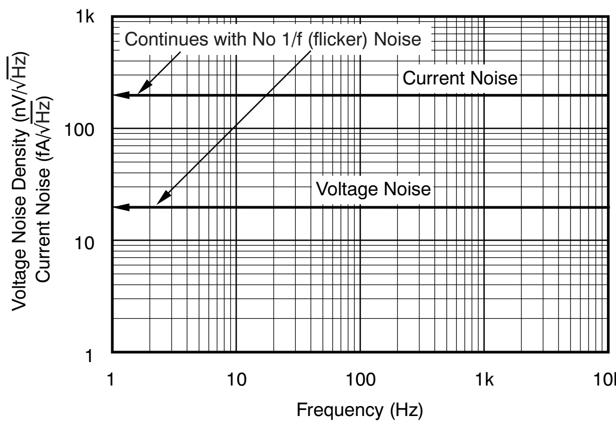

Figure 2.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

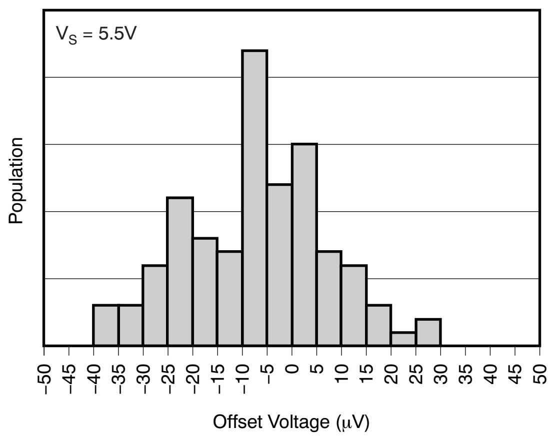

Figure 3.

OFFSET VOLTAGE DRIFT DISTRIBUTION

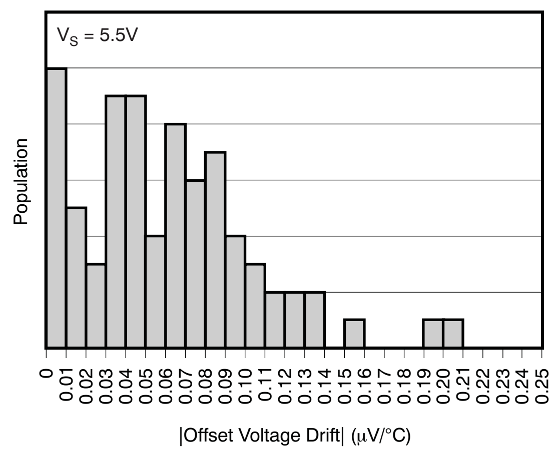

Figure 4.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10kΩ, V_S = +5.5V and V_{OUT} = V_S/2, unless otherwise noted.

OFFSET VOLTAGE vs TEMPERATURE

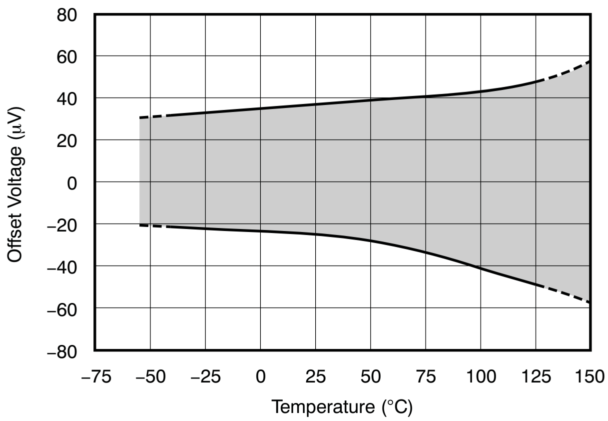

Figure 5.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

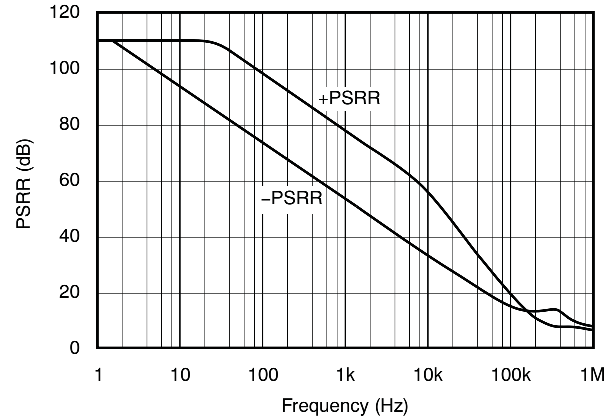

Figure 6.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

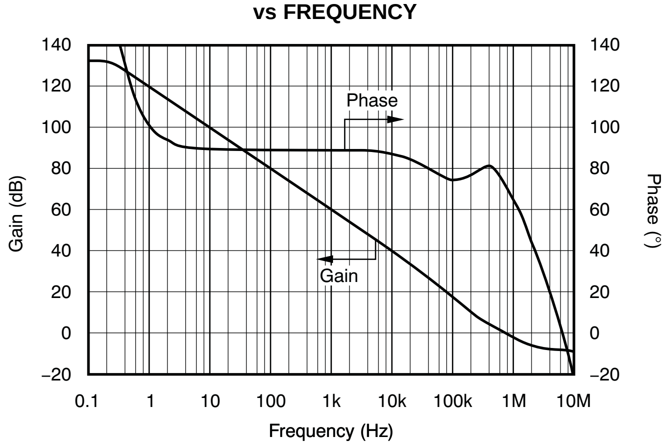

Figure 7.

OPEN-LOOP GAIN vs TEMPERATURE

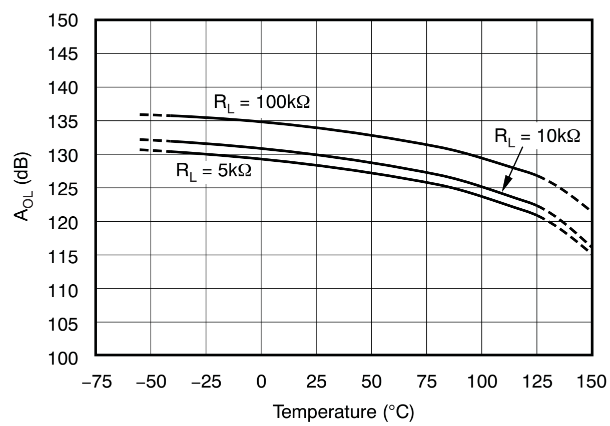

Figure 8.

COMMON-MODE REJECTION RATIO vs FREQUENCY

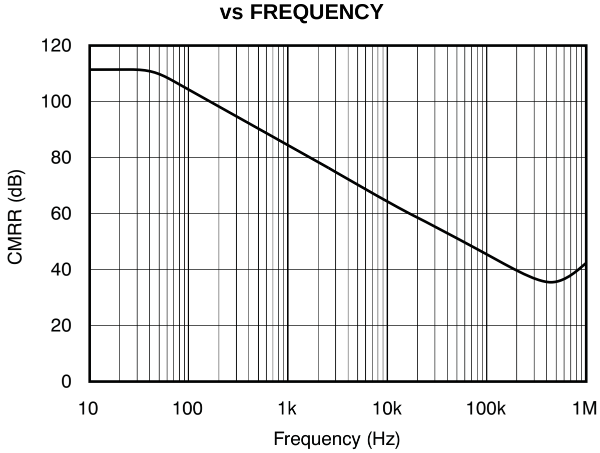

Figure 9.

COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs TEMPERATURE

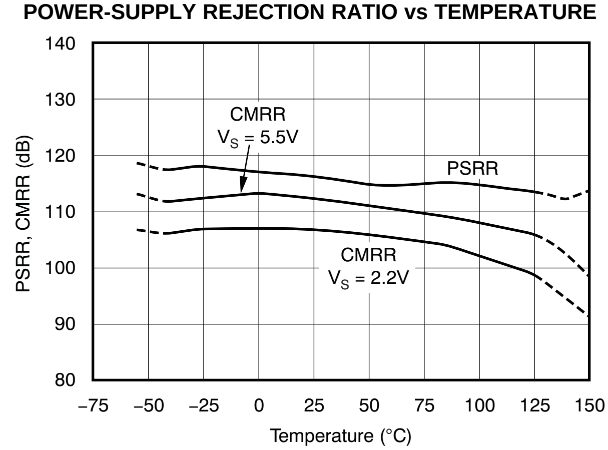

Figure 10.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10kΩ, V_S = +5.5V and V_{OUT} = V_S/2, unless otherwise noted.

INPUT BIAS CURRENT vs INPUT COMMON-MODE VOLTAGE

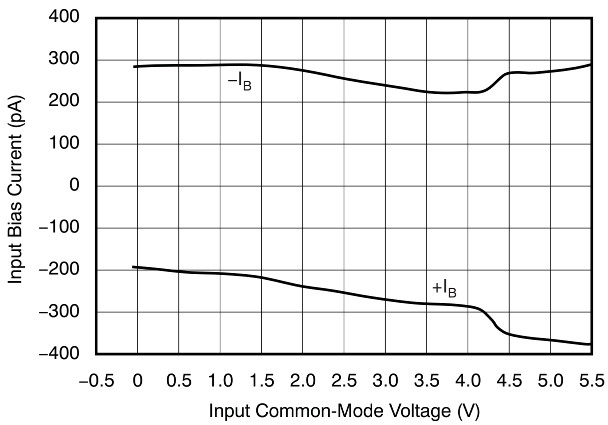

Figure 11.

INPUT BIAS CURRENT vs TEMPERATURE

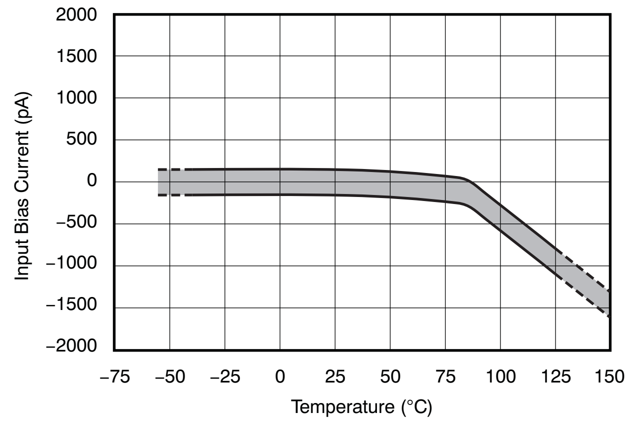

Figure 12.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

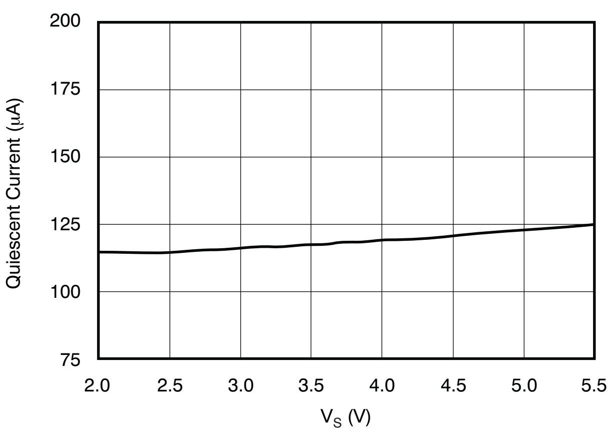

Figure 13.

QUIESCENT CURRENT vs TEMPERATURE

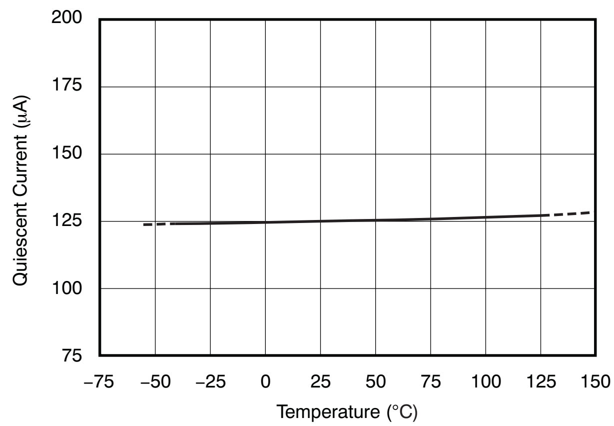

Figure 14.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

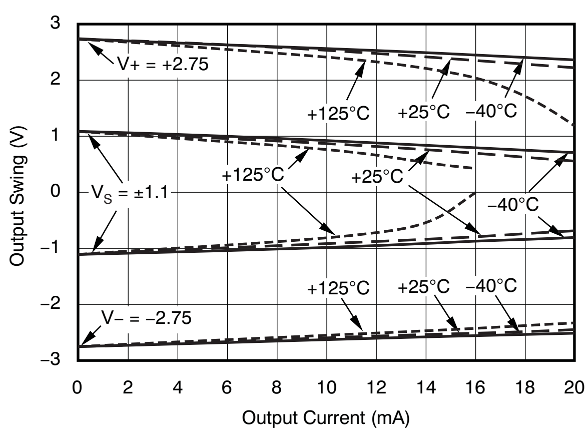

Figure 15.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

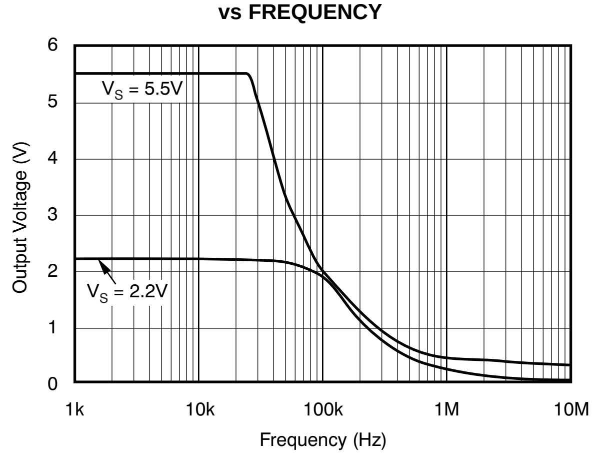

Figure 16.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10kΩ, V_S = +5.5V and V_{OUT} = V_S/2, unless otherwise noted.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

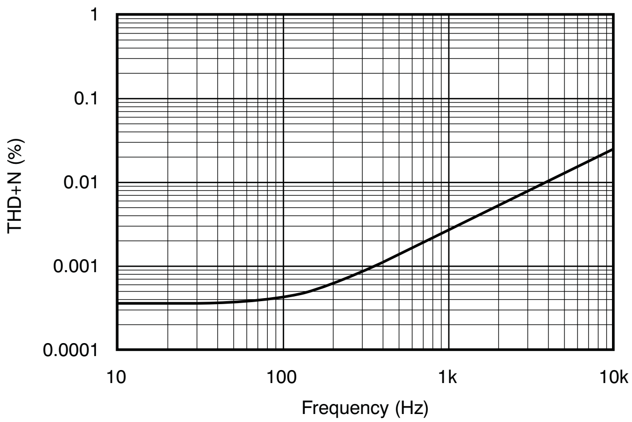

Figure 17.

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

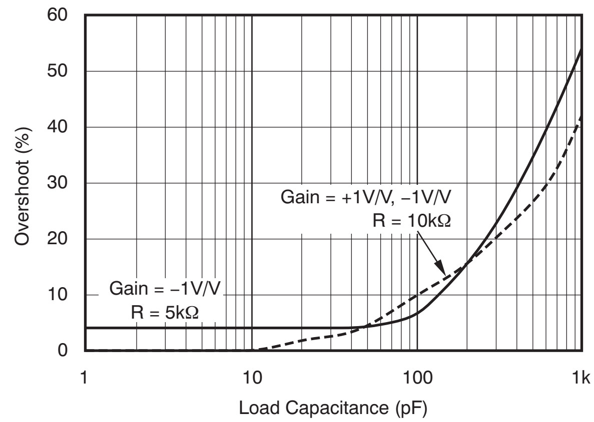

Figure 18.

POSITIVE OVER-VOLTAGE RECOVERY

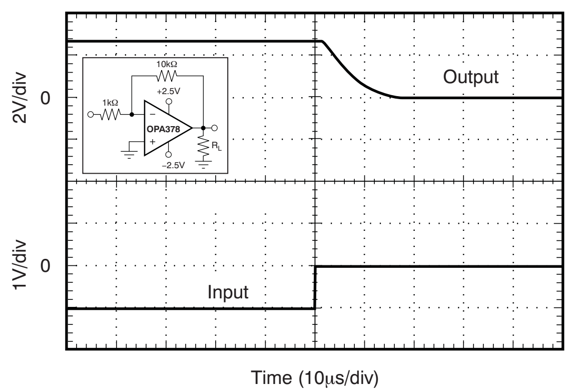

Figure 19.

NEGATIVE OVER-VOLTAGE RECOVERY

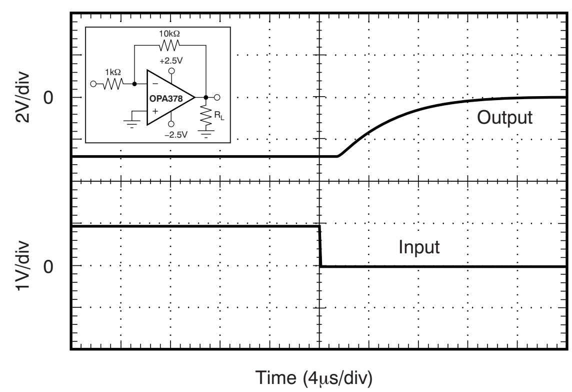

Figure 20.

SMALL-SIGNAL STEP RESPONSE

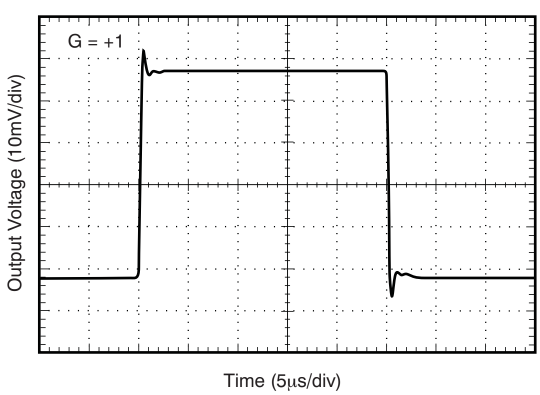

Figure 21.

LARGE-SIGNAL STEP RESPONSE

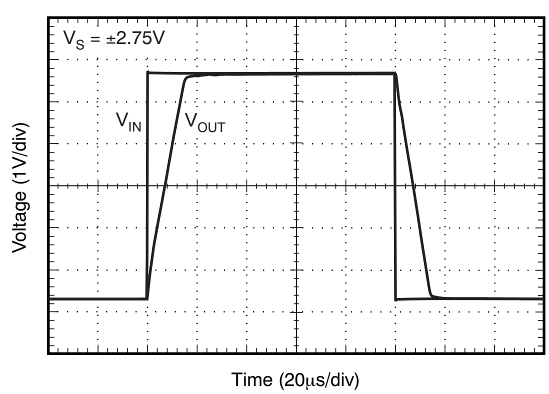

Figure 22.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10kΩ, V_S = +5.5V and V_{OUT} = V_S/2, unless otherwise noted.

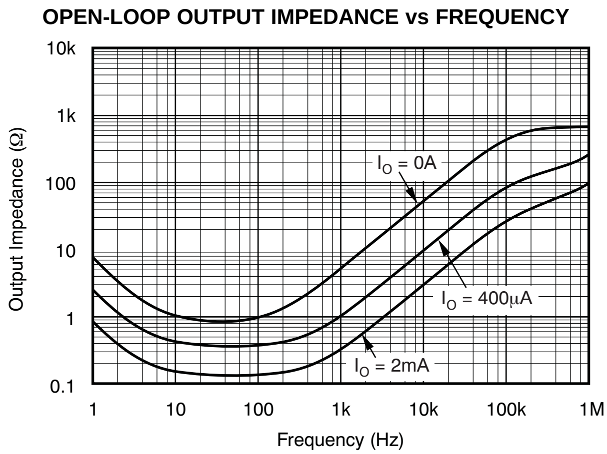

Figure 23.

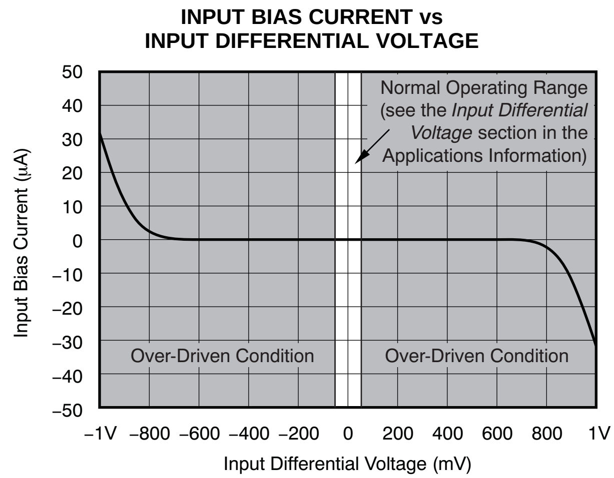

Figure 24.

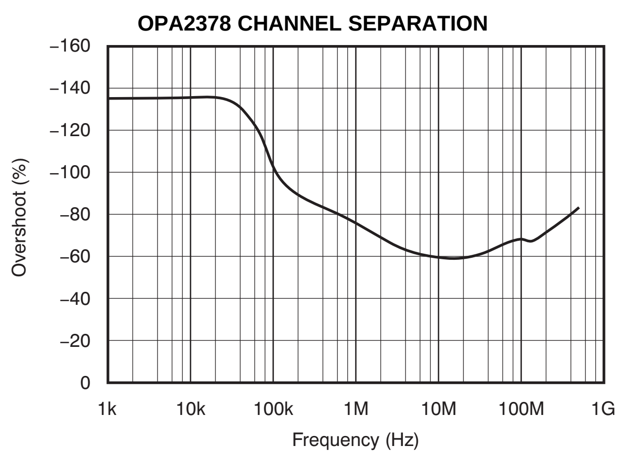

Figure 25.

APPLICATIONS INFORMATION

The OPA378 and OPA2378 are unity-gain stable, precision operational amplifiers that are free from phase reversal. The use of proprietary Zerø-Drift circuitry gives the benefit of low input offset voltage over time and temperature as well as lowering the 1/f noise component. This design provides the optimization of gain, noise, and power, making the OPA378 series one of the best performers in this bandwidth range. As a result of the high PSRR, this device works well in applications that run directly from battery power without regulation. They are optimized for low-voltage, single-supply operation. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100mV beyond the supplies, excellent CMRR, and a rail-to-rail output that swings within 10mV of the supplies. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity.

OPERATING VOLTAGE

The OPA378 and OPA2378 can be used with single or dual supplies from an operating range of V_S = +2.2V (±1.1V) and up to V_S = +5.5V (±2.75V). This device does not require symmetrical supplies, only a differential supply voltage of 2.2V to 5.5V. A power-supply rejection ratio of 1.5μV/V (typical) ensures that the device functions with an unregulated battery source. Supply voltages higher than +7V can permanently damage the device; see the Absolute Maximum Ratings table. Key parameters are assured over the specified temperature range, T_A = –40°C to +125°C. Parameters that vary over the supply voltage or temperature range are shown in the Typical Characteristics section of this data sheet.

INPUT VOLTAGE

The OPA378 and OPA2378 input common-mode voltage range extends 0.05V beyond the supply rails. The OPA378 achieves a common-mode rejection ratio of 112dB (typical) over the common-mode voltage range. Figure 26 shows the variation of offset voltage over the entire specified common-mode range for 10 typical units.

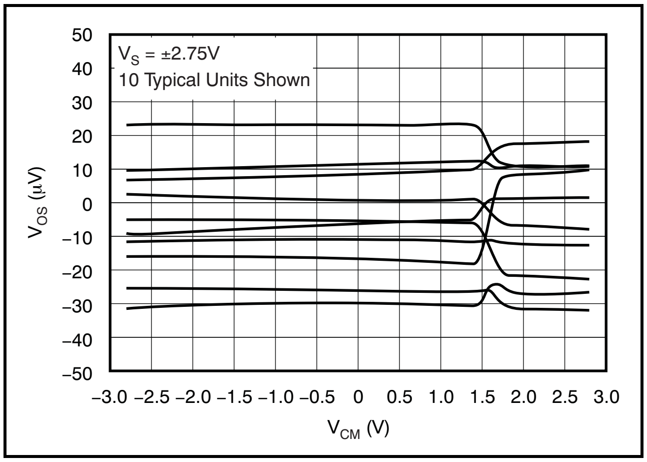

Figure 26. Offset Voltage versus Common-Mode Voltage

Normally, input bias current is about 150pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10mA. This limitation is easily accomplished with an input resistor, as Figure 27 shows.

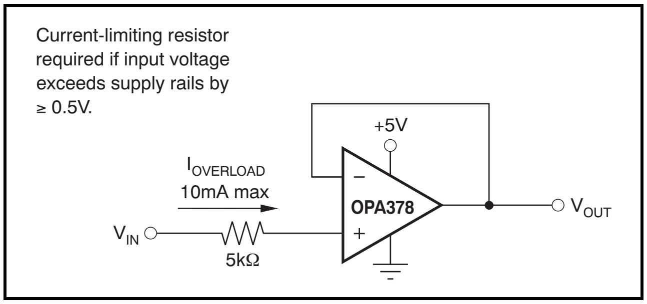

Figure 27. Input Current Protection

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INPUT DIFFERENTIAL VOLTAGE

The typical input bias current of the OPA378 during normal operation is approximately 150pA. In over-driven conditions, the bias current can increase significantly (see Figure 24). The most common cause of an over-driven condition occurs when the op amp is outside of the linear range of operation. When the output of the op amp is driven to one of the supply rails the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front end input chopping switches that combine with 1.5kΩ EMI filter resistors to create the equivalent circuit shown in Figure 28.

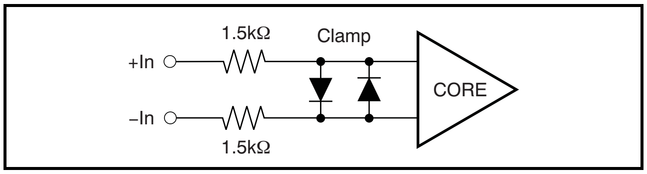

Figure 28. Equivalent Input Circuit

INTERNAL OFFSET CORRECTION

The OPA378 and OPA2378 family of op amps use an auto-calibration technique with a time-continuous 350kHz op amp in the signal path. This amplifier is zero-corrected every 3μs using a proprietary technique. Upon power-up, the amplifier requires approximately 100μs to achieve specified V_{OS} accuracy. This architecture has no aliasing or flicker noise.

NOISE

The OPA378 series of op amps have excellent distortion characteristics. Total harmonic distortion + noise is below 0.003% (G = +1, V_O = $3V_{RMS}$, and f = 1kHz, with a 10kΩ load). Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all the noise components.

EMI SUSCEPTIBILITY AND INPUT FILTERING

Operational amplifiers vary in their susceptibility to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output may shift from its nominal value while the EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA378 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential-mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 25MHz (–3dB), with a roll-off of 20dB per decade. Figure 29 shows the EMI filter.

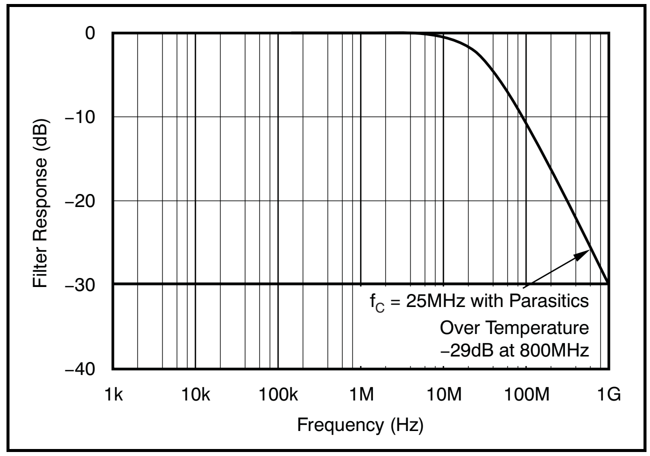

Figure 29. EMI Filter

GENERAL LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1μV/°C or higher, depending on materials used.

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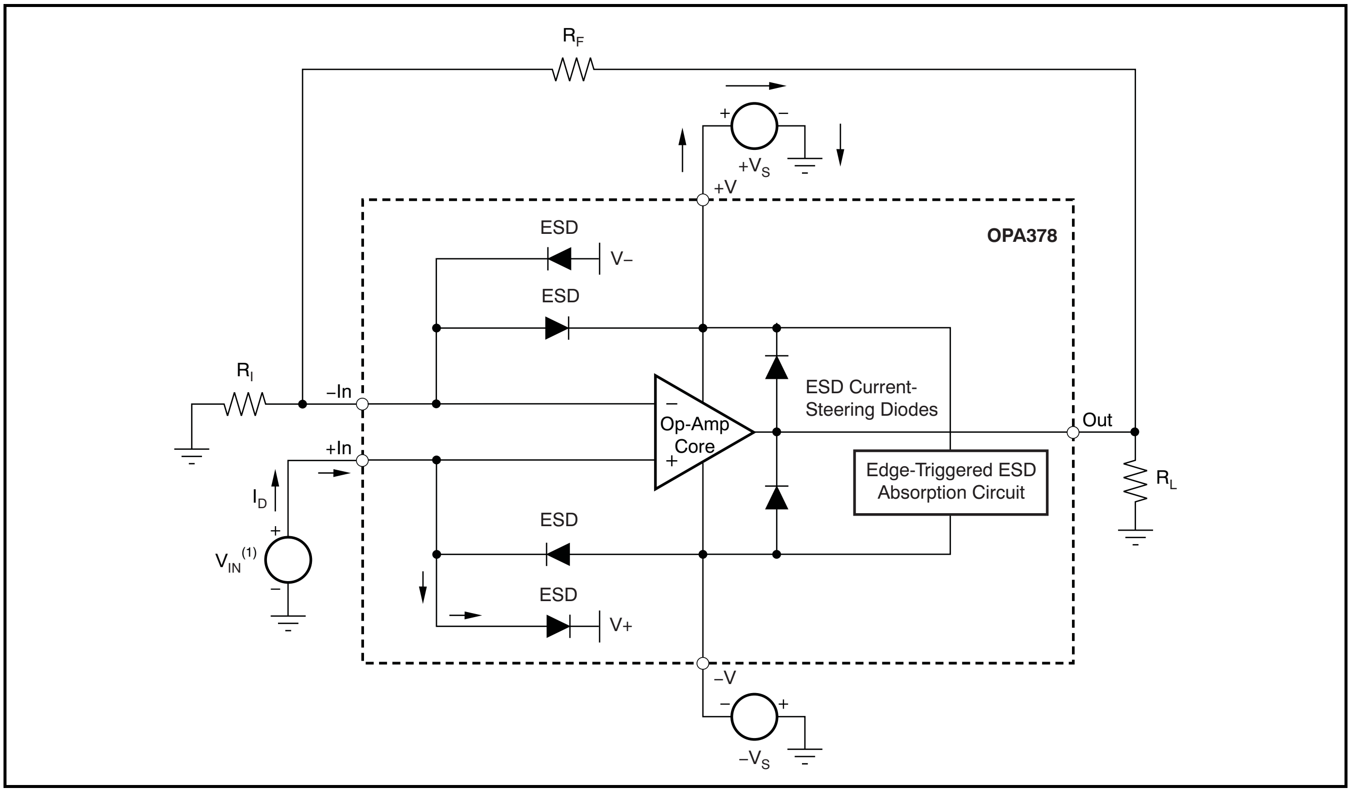
ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 30 shows the ESD circuits contained in the OPA378 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.



(1) $V_{IN} = +V_S + 500mV$.

Figure 30. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

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An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA378 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as that illustrated in Figure 30, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 30 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 300mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while $+V_S$ and $–V_S$ are applied. If this event happens, a direct current path is established between the $+V_S$ and $–V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $–V_S$ are at 0V. Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

APPLICATION IDEAS

Figure 31 shows the basic configuration for a bridge amplifier.

A low-side current shunt monitor is shown in Figure 32. R_N are optional resistors used to isolate the ADS8325 from the noise of the digital two-wire bus. Because the ADS8325 is a 16-bit converter, a precise reference is essential for maximum accuracy. If absolute accuracy is not required, and the 5V power supply is sufficiently stable, the REF3330 may be omitted.

Figure 33 shows a high-side current monitor. The load current develops a voltage drop across R_{SHUNT}. The noninverting input monitors this voltage and is duplicated on the inverting input. R_G then has the same voltage drop as R_{SHUNT}. R_G can be sized to provide whatever current is most convenient to the designer based on design constraints. The current from R_G then flows through the MOSFET and to resistor R_L, creating a voltage that can be read. Note that R_L and R_G set the voltage gain of the circuit.

The supply voltage for the op amp is derived from the zener diode. For the OPA378 V_S must be between 2.2V and 5.5V. Two possible methods to bias the zener are shown in the circuit of Figure 33: the customary resistor bias and the current monitor. The current monitor biasing achieves the lowest possible voltage. Resistor R_1 and the diode on the noninverting input provide short-circuit protection.

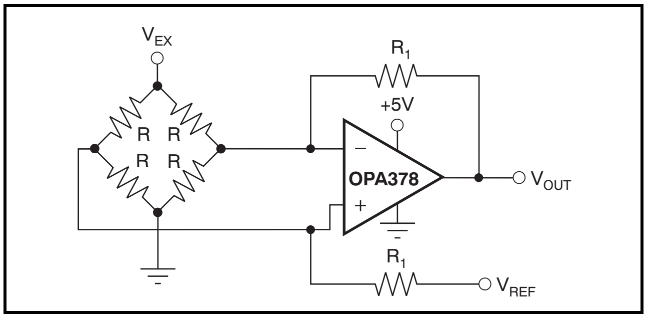
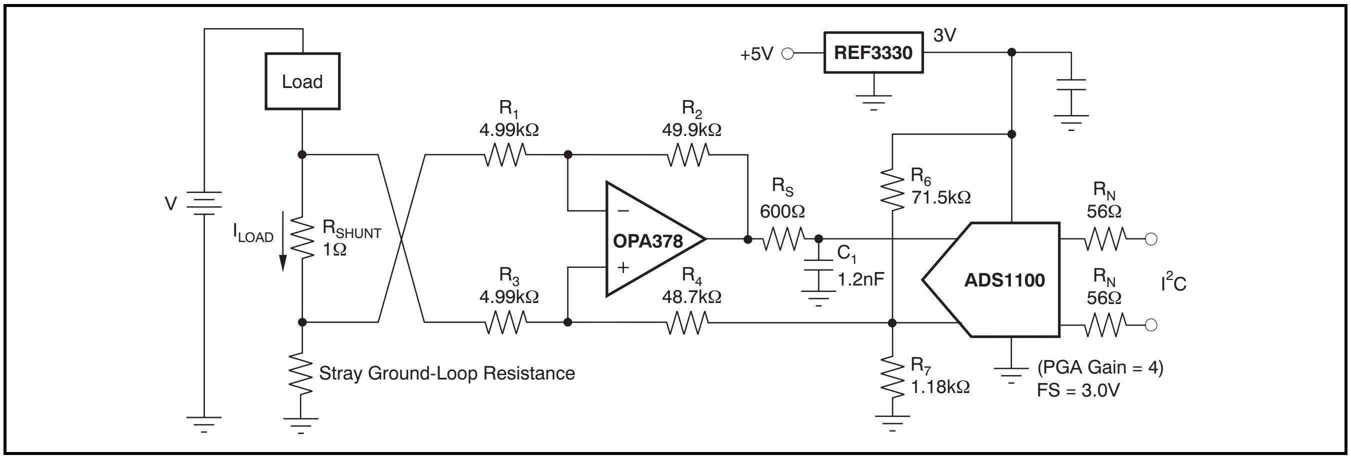
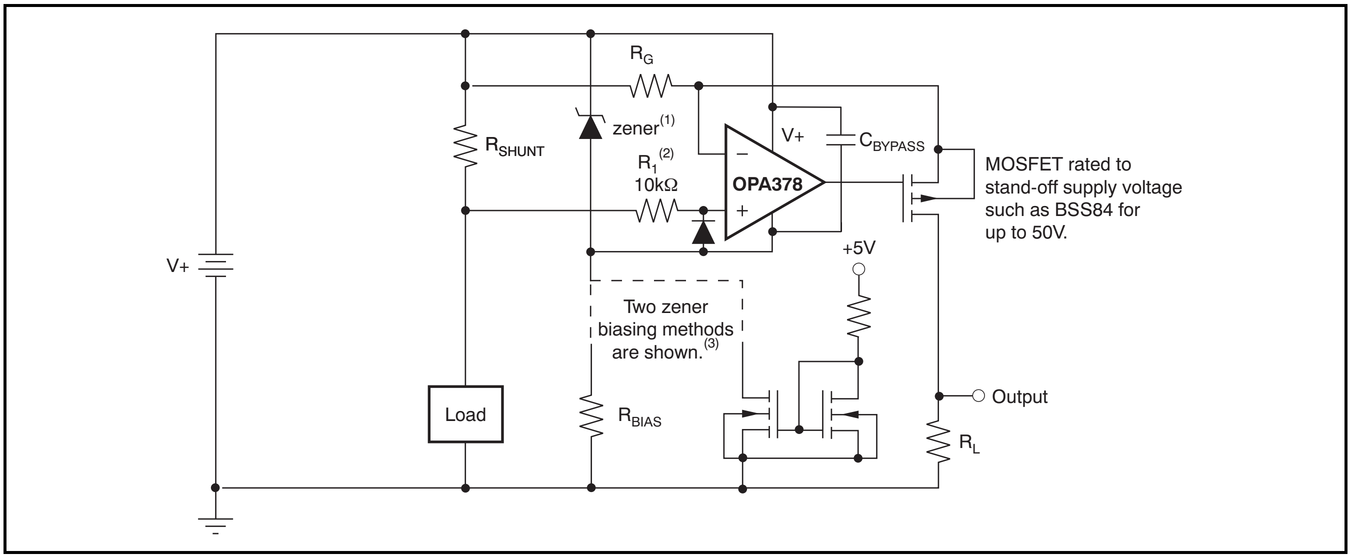


Figure 31. Single Op Amp Bridge Amplifier



NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 32. Low-Side Current Monitor



(1) Zener rated for op amp supply capability (that is, 5.1V for the OPA378).

(2) Current-limiting resistor.

(3) Choose zener biasing resistor or dual NMOSFETs (2N7002, NTZD511ON, SM6K2T110).

Figure 33. High-Side Current Monitor

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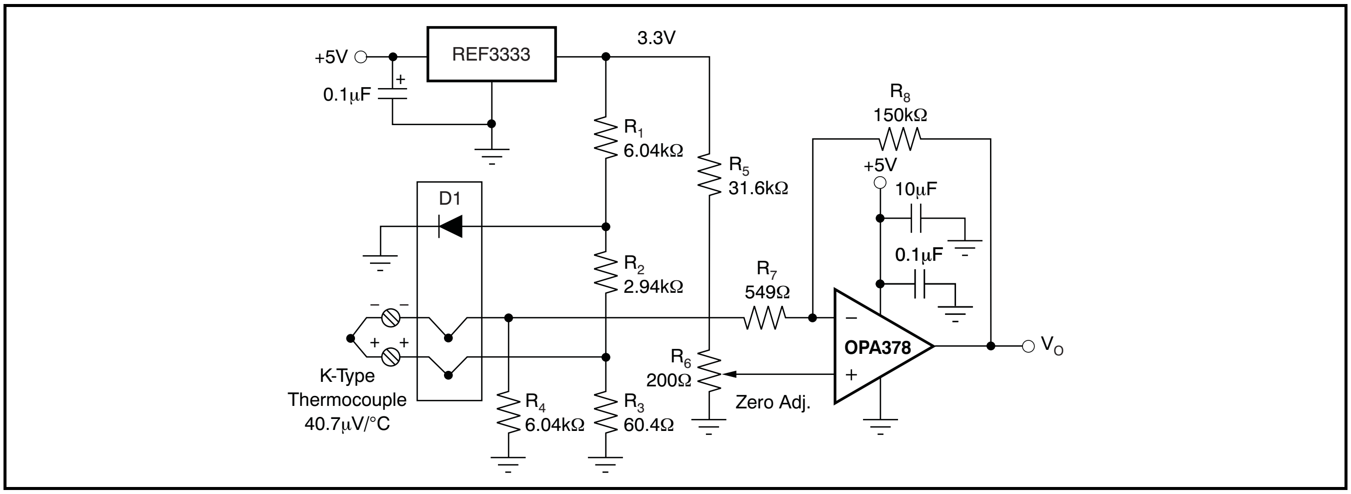


Figure 34. Temperature Measurement

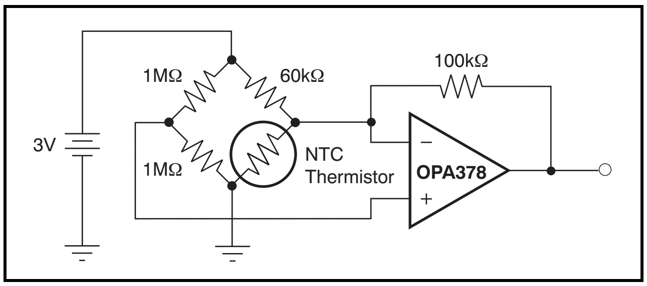


Figure 35. Thermistor Measurement

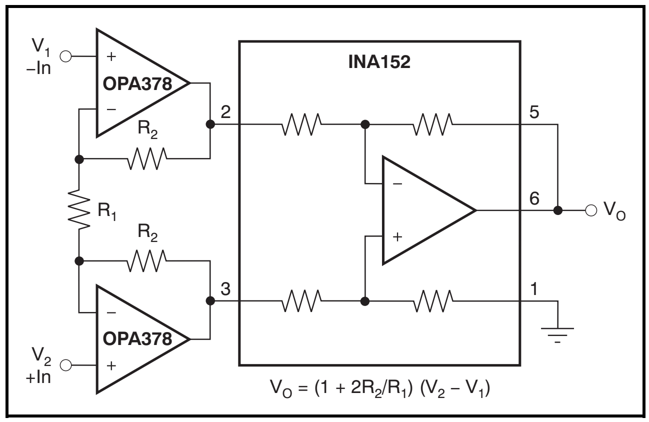
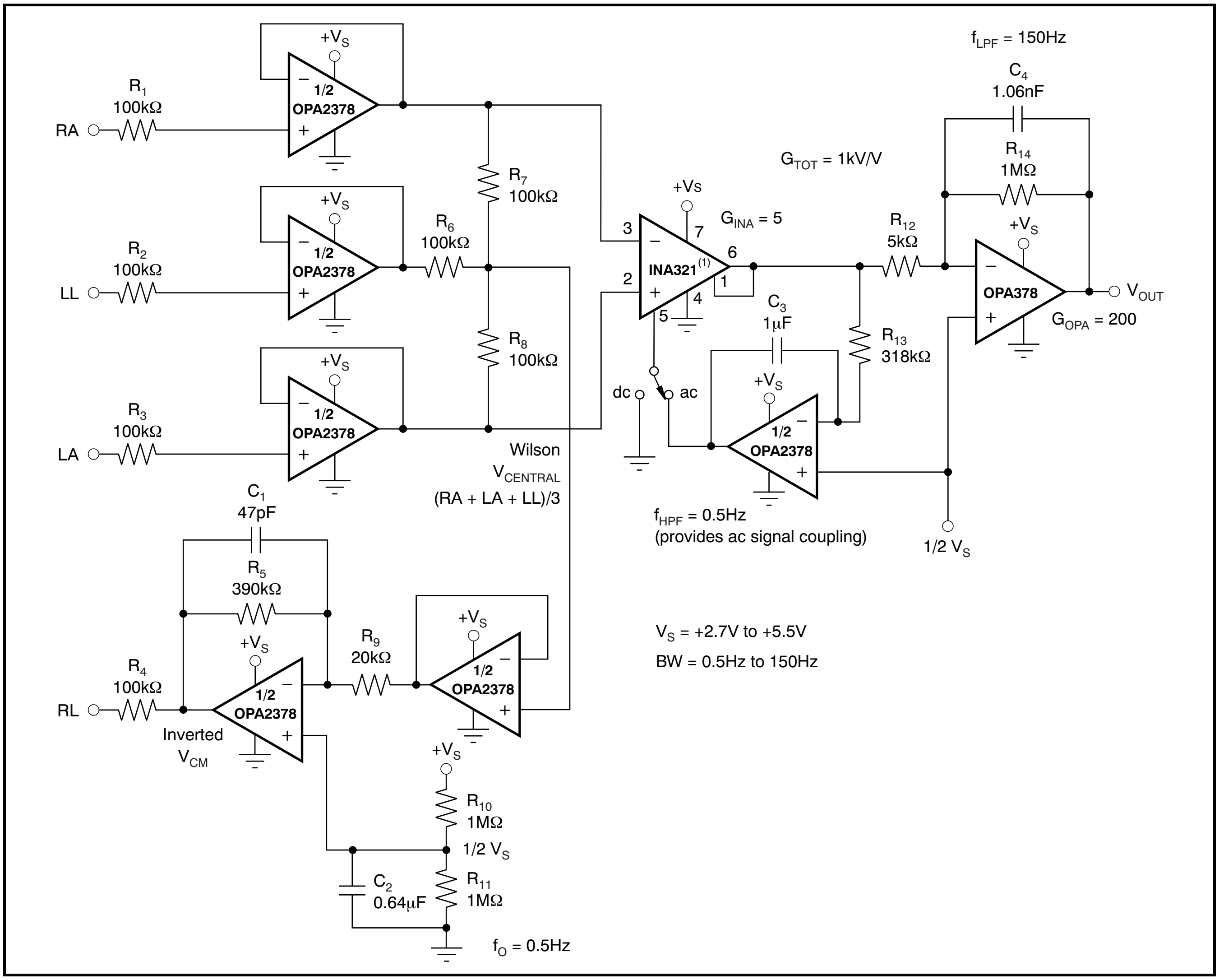


Figure 36. Precision Instrumentation Amplifier



(1) Other instrumentation amplifiers can be used, such as the INA326, which has lower noise but higher quiescent current.

Figure 37. Single-Supply, Very Low Power ECG Circuit

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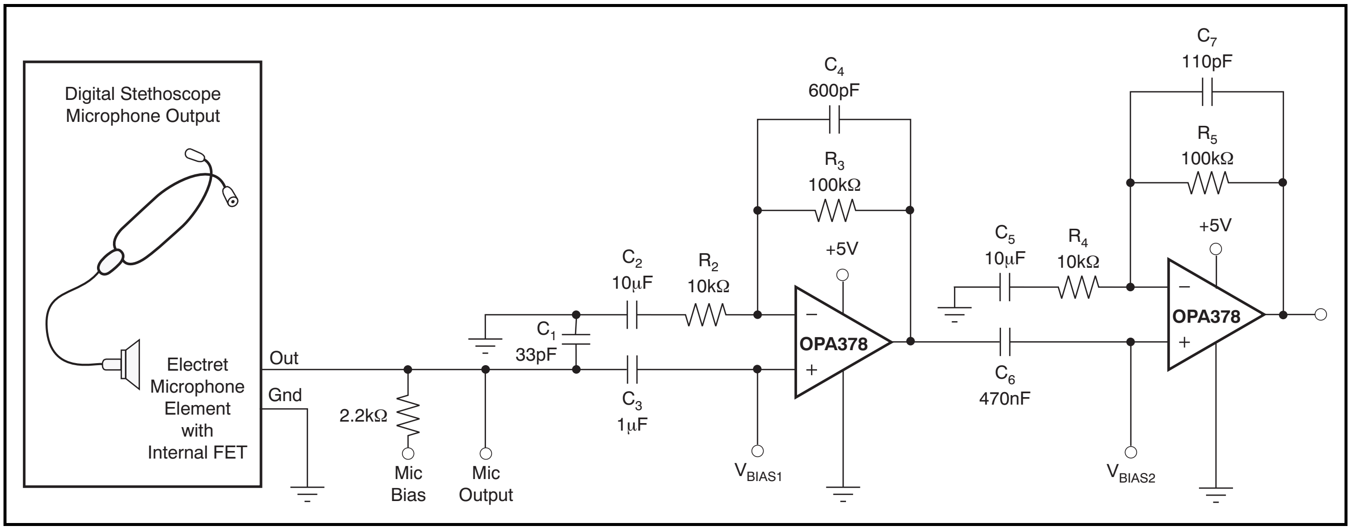

Figure 38. Digital Stethoscope Circuit

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2009) to Revision D **Page**

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2378AIDCNR	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCAI	Samples
OPA2378AIDCNT	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OCAI	Samples
OPA378AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAZI	Samples
OPA378AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAZI	Samples
OPA378AIDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTS	Samples
OPA378AIDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BTS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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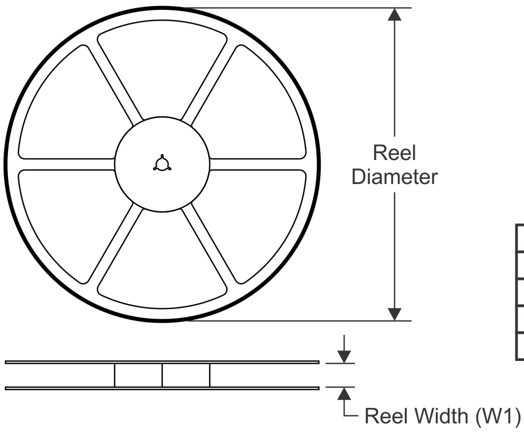
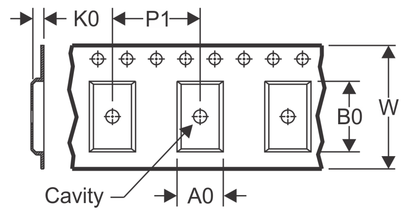
TAPE AND REEL INFORMATION

REEL DIMENSIONS

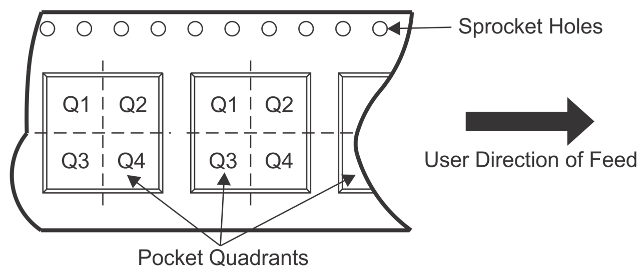


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

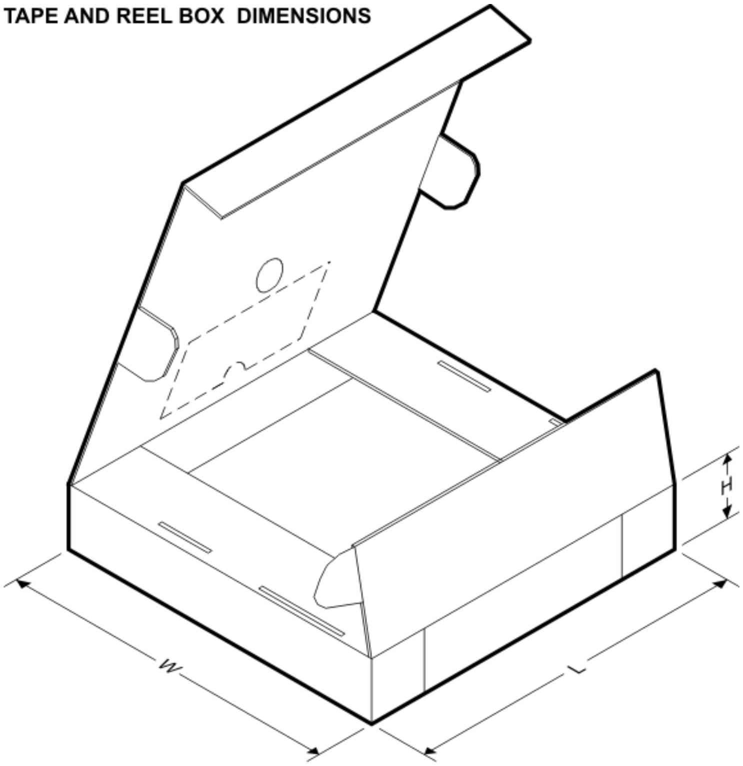
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2378AIDCNR	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2378AIDCNT	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA378AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA378AIDCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA378AIDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA378AIDCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3

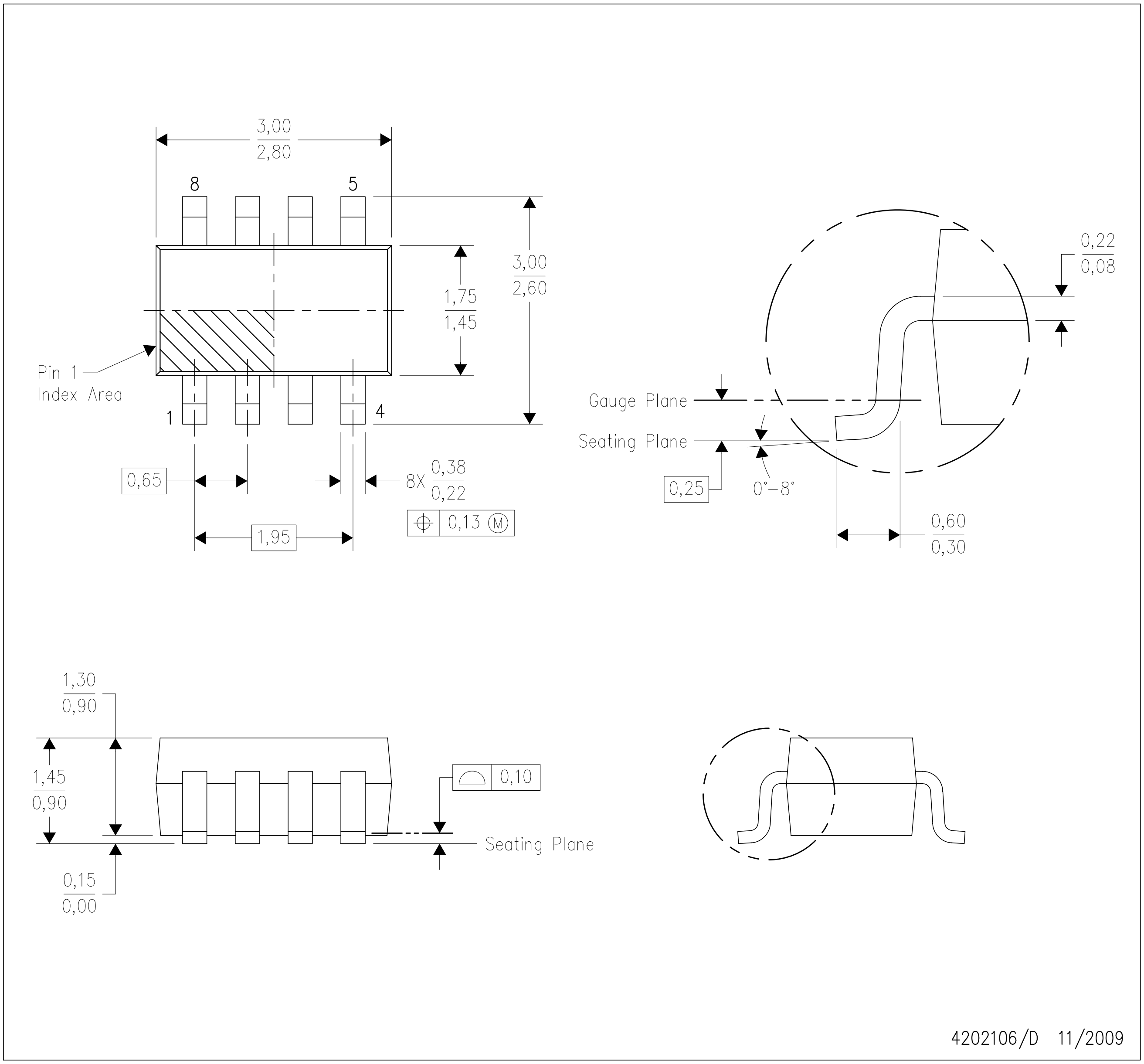
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

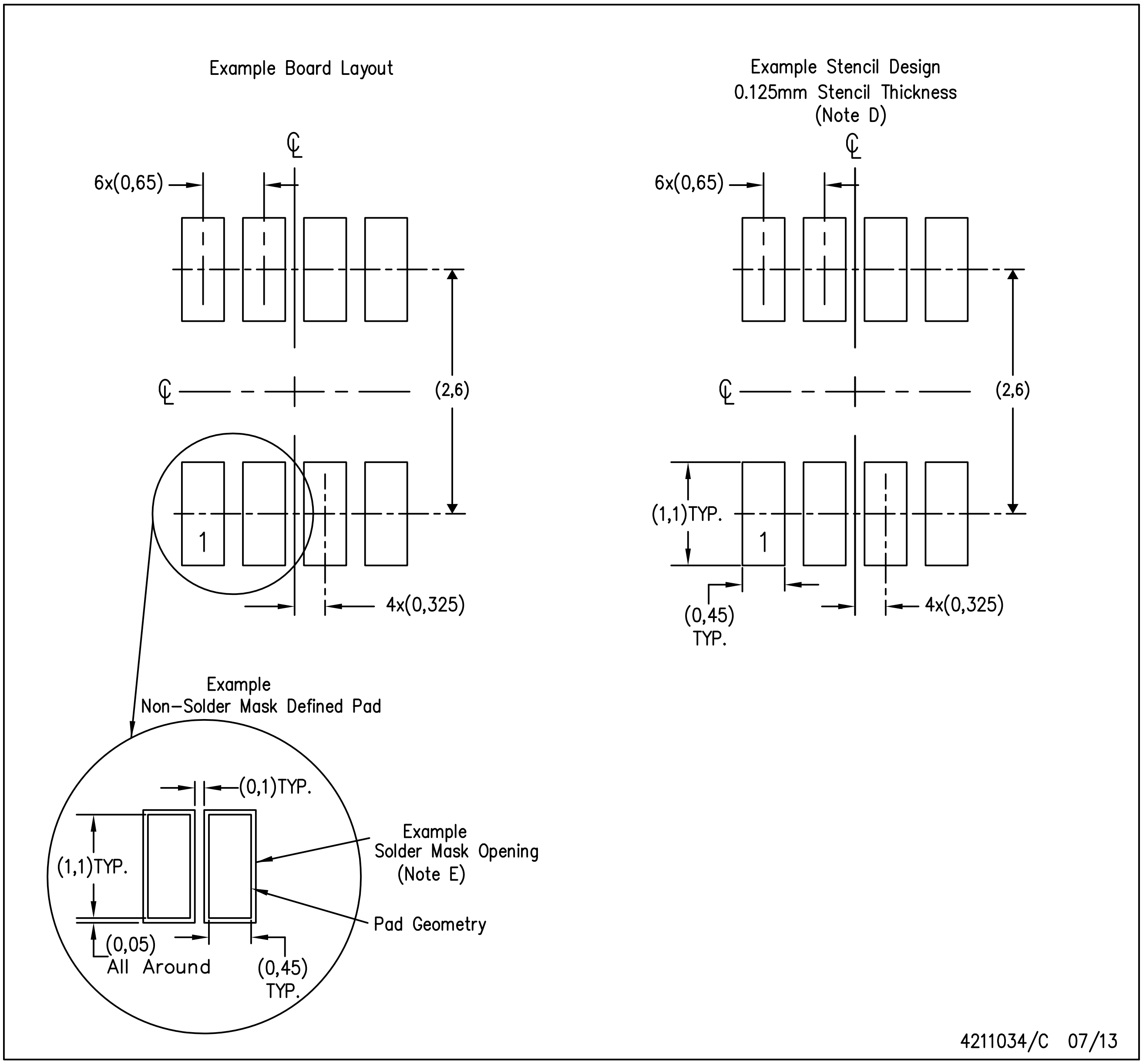
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2378AIDCNR	SOT-23	DCN	8	3000	195.0	200.0	45.0
OPA2378AIDCNT	SOT-23	DCN	8	250	195.0	200.0	45.0
OPA378AIDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
OPA378AIDCKR	SC70	DCK	5	3000	195.0	200.0	45.0
OPA378AIDCKT	SC70	DCK	5	250	180.0	180.0	18.0
OPA378AIDCKT	SC70	DCK	5	250	195.0	200.0	45.0

DCN (R–PDSO–G8)   PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



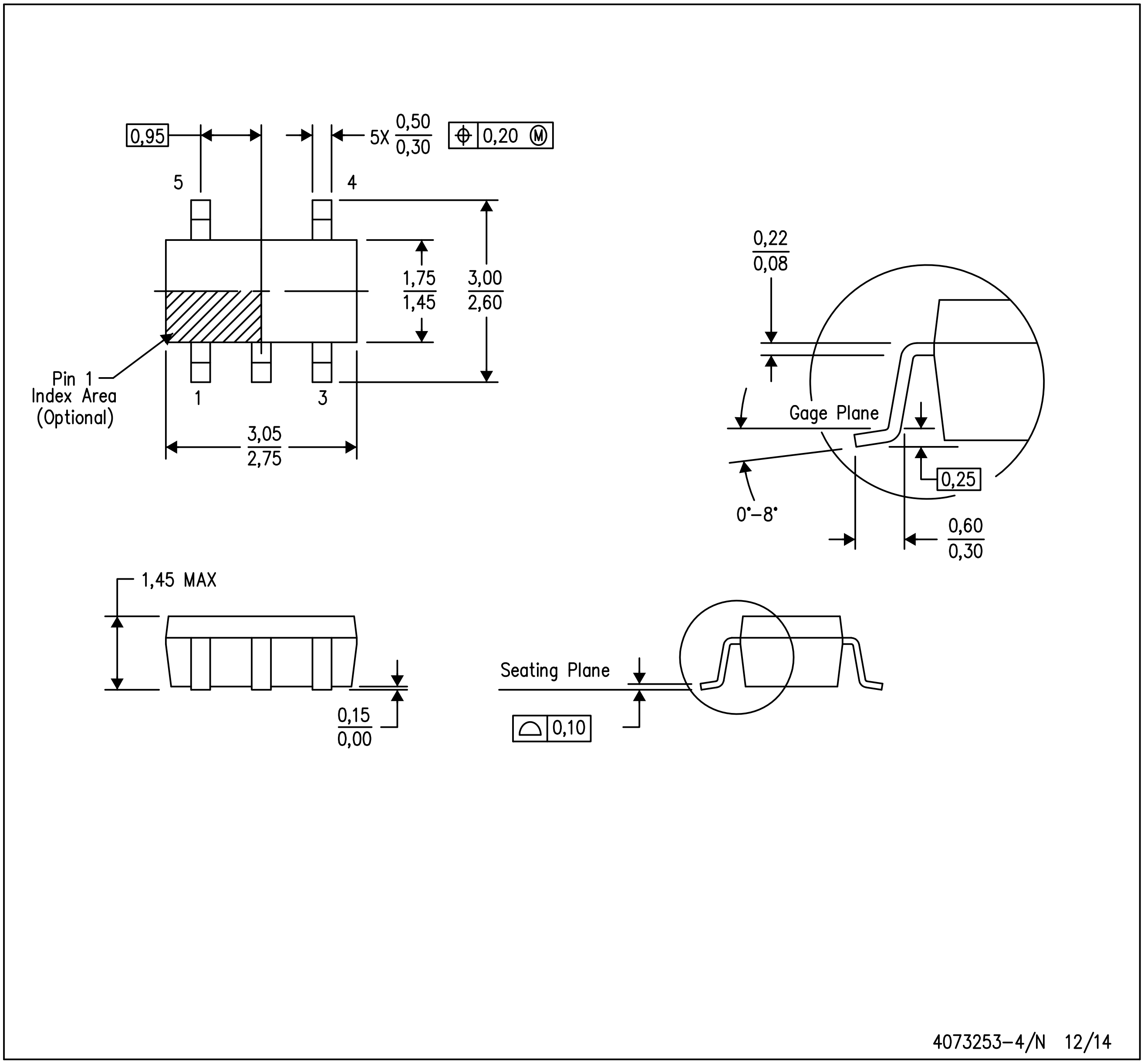
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
- D. Package outline inclusive of solder plating.
- E. A visual index feature must be located within the Pin 1 index area.
- F. Falls within JEDEC MO–178 Variation BA.
- G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



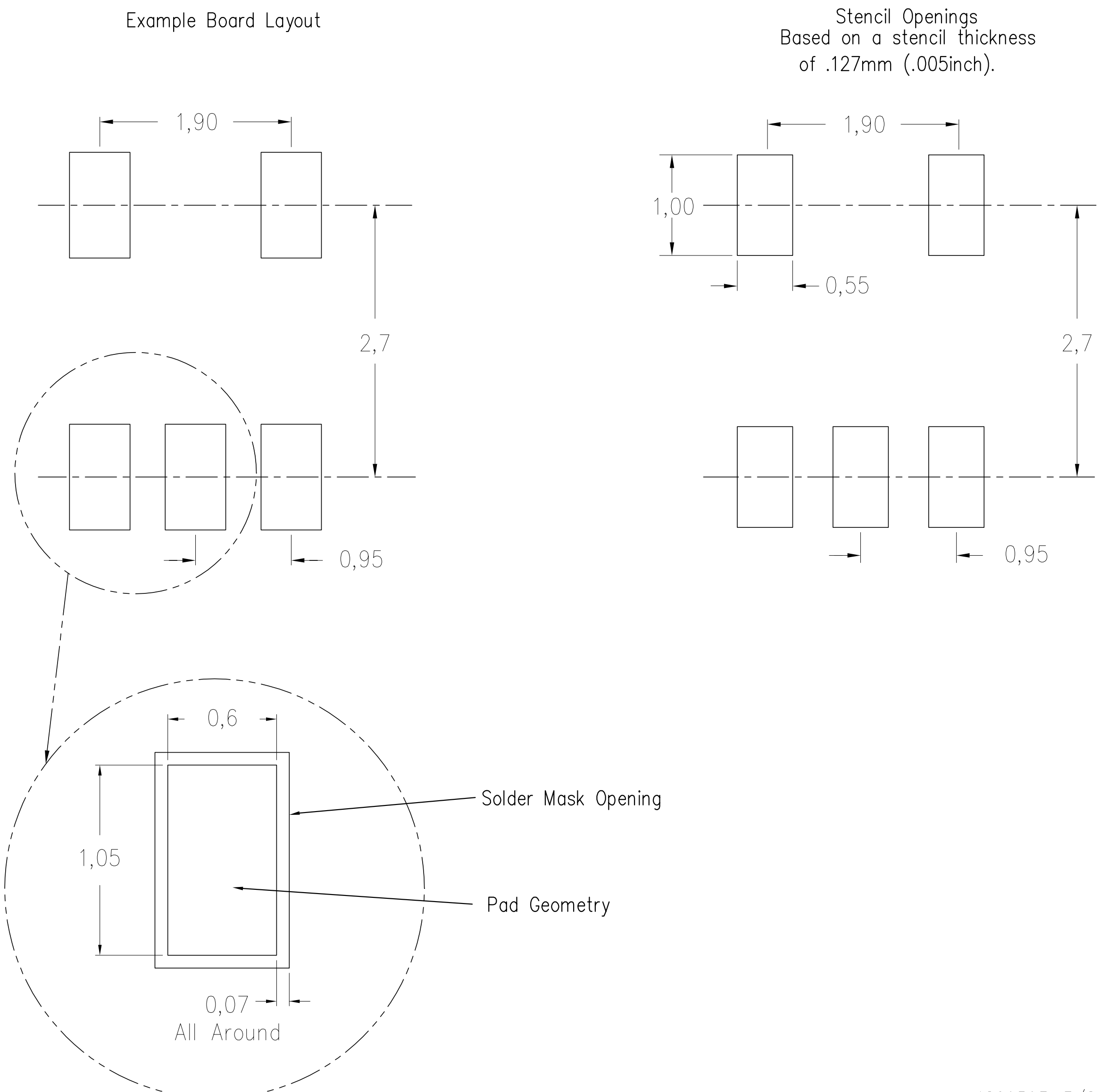
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

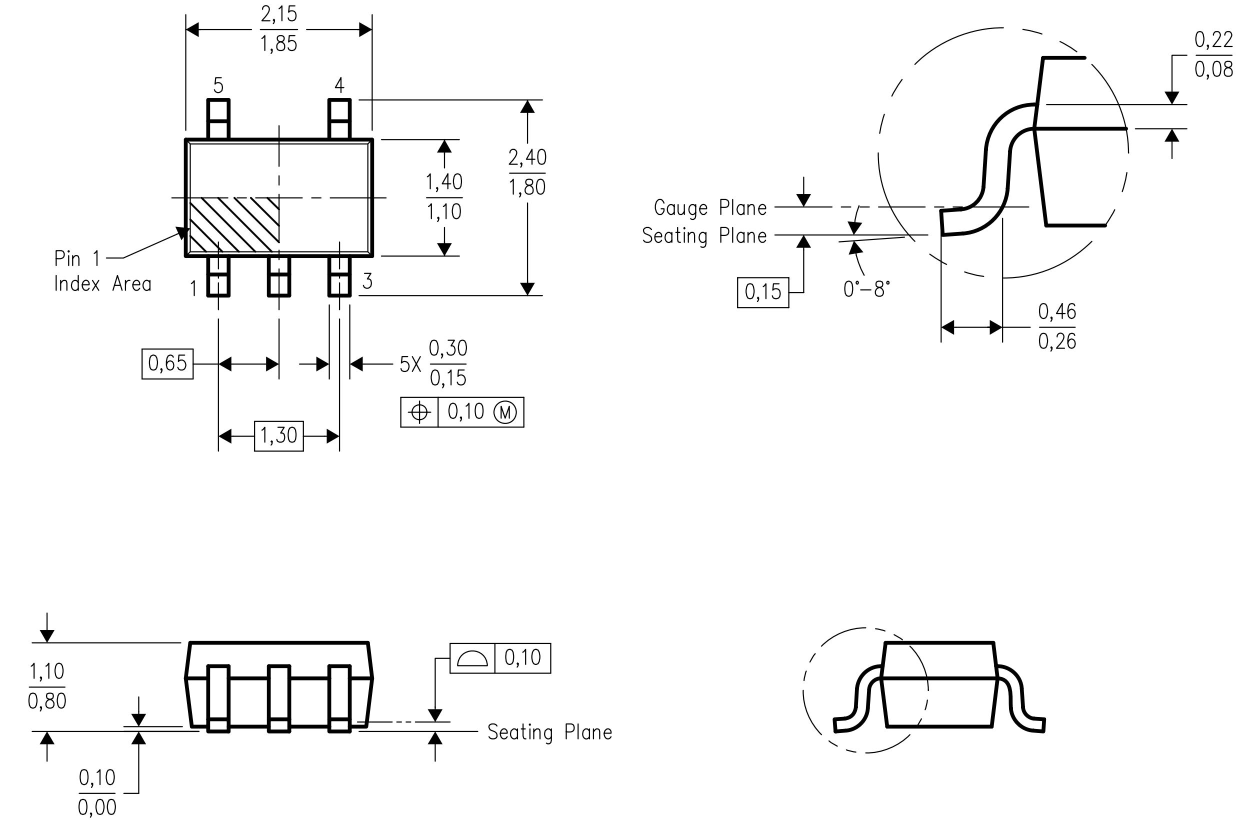
DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE



4209593-3/C 08/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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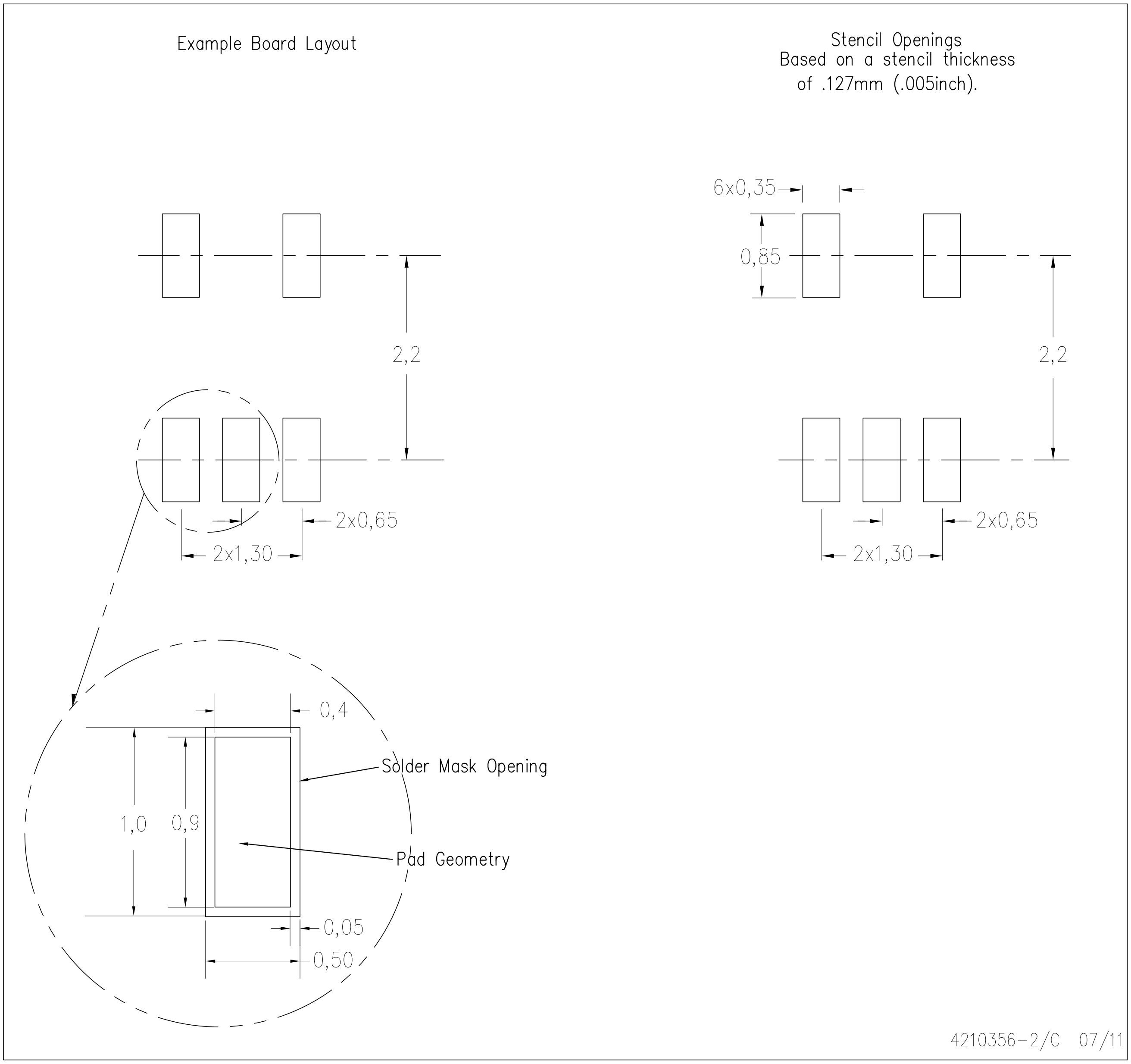
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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