

TLVx170 面向成本敏感型系统的 36V 单电源、抗 EMI 型低功耗运算放大器

1 特性

- 电源电压范围：2.7V 至 36V， $\pm 1.35V$ 至 $\pm 18V$
- 低噪声：22 nV/ \sqrt{Hz}
- 抗电磁干扰 (EMI) 并过滤射频干扰 (RFI) 的输入
- 输入范围包括负电源
- 单位增益稳定：200pF 容性负载
- 轨到轨输出
- 增益带宽：1.2MHz
- 低静态电流：每个放大器 125 μA
- 高共模抑制：110dB
- 低偏置电流：10pA（典型值）

2 应用

- 点钞机
- AC-DC 转换器
- 电源模块内的跟踪放大器
- 服务器电源
- 逆变器
- 测试设备
- 电池供电的仪器
- 变频器放大器
- 线路驱动器或线路接收器

3 说明

TLVx170 系列是抗电磁干扰 (EMI) 型、36V 单电源低噪声运算放大器 (op amp)，1kHz 下的总谐波失真 + 噪声 (THD+N) 为 0.0002%，能够在 2.7V ($\pm 1.35V$) 至 36V ($\pm 18V$) 的电源电压范围内运行。这些特性结合低噪声和超高电源抑制比 (PSRR) 使得单通道 TLV170、双通道 TLV2170 和四通道 TLV4170 成为毫伏级信号放大的理想选择。TLVx170 系列器件还具有良好的偏移、漂移和带宽以及低静态电流特性。

大多数运算放大器仅有一个指定的电源电压，TLVx170 系列运算放大器则有所不同，其可在 2.7V 至 36V 的电压范围内额定运行，超过电源轨的输入信号摆幅不会导致反相。TLVx170 系列同时也是单位增益稳定的精密运算放大器，容性负载为 200pF，带宽为 1.2MHz，转换率为 0.4V/ μs ，非常适用于电流-电压转换器。

器件输入可在负电源轨以下 100mV 以及正电源轨 2V 之内正常运行，但满轨到轨输入的性能会受到影响。TLVx170 器件的额定运行温度范围为 $-40^{\circ}C$ 至 $+125^{\circ}C$ 。

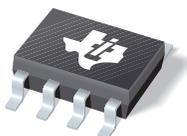
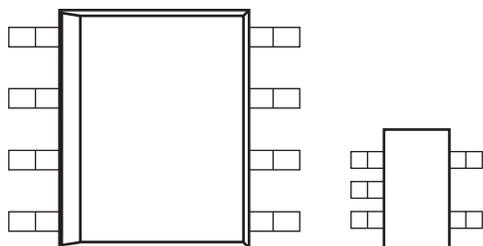
器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TLV170	SOIC (8)	4.90mm x 3.91mm
	SOT-23 (5)	2.90mm x 1.60mm
TLV2170	SOIC (8)	4.90mm x 3.91mm
	VSSOP (8)	3.00mm x 3.00mm
TLV4170	SOIC (14)	8.65mm x 3.91mm
	TSSOP (14)	5.00mm x 4.40mm

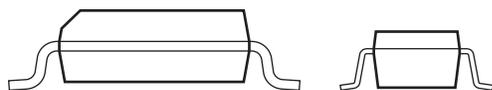
(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

36V 运算放大器的最小封装

Package Footprint Comparison (to Scale)



Package Height Comparison (to Scale)



D (SO-8)

DBV (SOT23-5)



目录

1	特性	1	8.4	Device Functional Modes.....	19
2	应用	1	9	Application and Implementation	20
3	说明	1	9.1	Application Information.....	20
4	修订历史记录	2	9.2	Typical Application	20
5	Device Comparison Table	3	10	Power Supply Recommendations	22
6	Pin Configuration and Functions	3	11	Layout.....	22
7	Specifications.....	6	11.1	Layout Guidelines	22
7.1	Absolute Maximum Ratings	6	11.2	Layout Example	23
7.2	ESD Ratings.....	6	12	器件和文档支持	24
7.3	Recommended Operating Conditions.....	6	12.1	器件支持	24
7.4	Thermal Information: TLV170	7	12.2	文档支持	25
7.5	Thermal Information: TLV2170	7	12.3	相关链接	25
7.6	Thermal Information: TLV4170	7	12.4	接收文档更新通知	25
7.7	Electrical Characteristics.....	8	12.5	社区资源	25
7.8	Typical Characteristics	9	12.6	商标	25
8	Detailed Description	15	12.7	静电放电警告	25
8.1	Overview	15	12.8	Glossary	25
8.2	Functional Block Diagram	15	13	机械、封装和可订购信息	25
8.3	Feature Description.....	15			

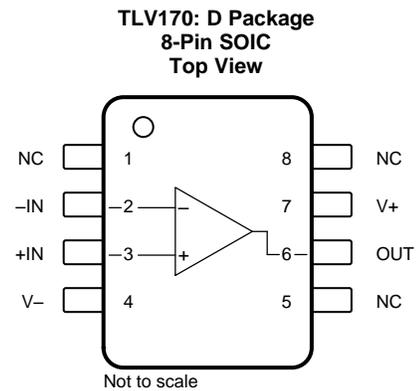
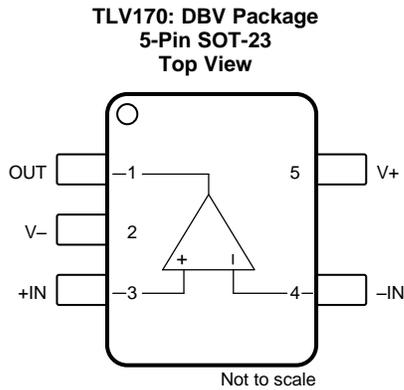
4 修订历史记录

日期	修订版本	注释
2016 年 11 月	*	最初发布。

5 Device Comparison Table

DEVICE	NO OF CHANNELS	PACKAGE-LEAD			
		SOT23-5	D	VSSOP (micro size)	TSSOP
TLV170	1	5	8	—	—
TLV2170	2	—	8	8	—
TLV4170	4	—	14	—	14

6 Pin Configuration and Functions

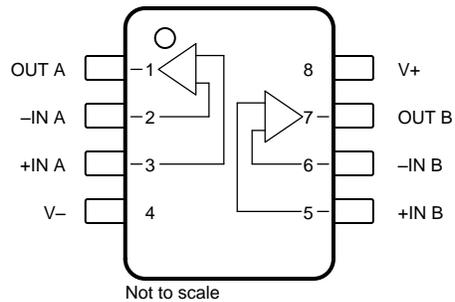


Pin Functions: TLV170

NAME	PIN		I/O	DESCRIPTION
	TLV170			
	SOT-23	D		
-IN	4	2	I	Negative (inverting) input
+IN	3	3	I	Positive (noninverting) input
NC ⁽¹⁾	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	1	6	O	Output
V-	2	4	—	Negative (lowest) power supply
V+	5	7	—	Positive (highest) power supply

(1) NC indicates no internal connection.

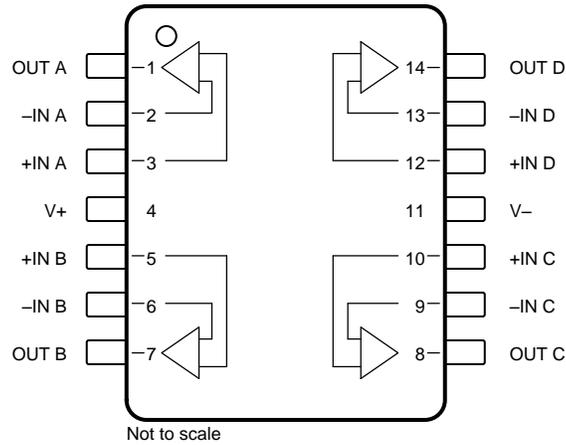
**TLV2170: D and DGK Packages
8-Pin SOIC and VSSOP
Top View**



Pin Functions: TLV2170

NAME	PIN		I/O	DESCRIPTION
	TLV2170			
	SOIC	VSSOP (micro size)		
-IN A	2	2	I	Inverting input, channel A
-IN B	6	6	I	Inverting input, channel B
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
V-	4	4	—	Negative (lowest) power supply
V+	8	8	—	Positive (highest) power supply

**TLV4170: D and PW Packages
14-Pin SOIC and TSSOP
Top View**



Pin Functions: TLV4170

NAME	PIN		I/O	DESCRIPTION
	SOIC	TSSOP		
-IN A	2	2	I	Inverting input, channel A
-IN B	6	6	I	Inverting input, channel B
-IN C	9	9	I	Inverting input, channel C
-IN D	13	13	I	Inverting input, channel D
+IN A	3	3	I	Noninverting input, channel A
+IN B	5	5	I	Noninverting input, channel B
+IN C	10	10	I	Noninverting input, channel C
+IN D	12	12	I	Noninverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	8	O	Output, channel C
OUT D	14	14	O	Output, channel D
V-	11	11	—	Negative (lowest) power supply
V+	4	4	—	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply voltage, V+ to V-	-20	20	V
	Single-supply voltage		40	
	Signal input pin	(V-) - 0.5	(V+) + 0.5	
Current	Signal input pin	-10	10	mA
	Output short-circuit ⁽²⁾	Continuous		
Temperature	Operating, T _A	-55	150	°C
	Junction, T _J		150	
	Storage, T _{stg}	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	Supply, V _S = (V+) - (V-)	2.7	36	V
T _A	Specified temperature	-40	125	°C
T _A	Operating temperature	-55	150	°C

7.4 Thermal Information: TLV170

THERMAL METRIC ⁽¹⁾		TLV170		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	149.5	245.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.9	133.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87.7	83.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	35.5	18.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	89.5	83.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Thermal Information: TLV2170

THERMAL METRIC ⁽¹⁾		TLV2170		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.3	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.1	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.6	130	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.2	5.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	53.8	120	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.6 Thermal Information: TLV4170

THERMAL METRIC ⁽¹⁾		TLV4170		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.8	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	59.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.5	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.2	54.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.7 Electrical Characteristics

 at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	$T_A = 25^\circ\text{C}$		0.5	± 2.5	mV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			± 2.7	
dV_{OS}/dT	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 2		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_S = 4\text{ V}$ to 36 V , $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	90	105		dB
	Channel separation, dc			5		$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT						
I_B	Input bias current	$T_A = 25^\circ\text{C}$		± 10		pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 1		nA
I_{OS}	Input offset current	$T_A = 25^\circ\text{C}$		± 10		pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		± 50		
NOISE						
	Input voltage noise	$f = 0.1\text{ Hz}$ to 10 Hz		2		μV_{PP}
e_n	Input voltage noise density	$f = 100\text{ Hz}$		27		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		22		
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range ⁽¹⁾		$(V-) - 0.1$		$(V+) - 2$	V
CMRR	Common-mode rejection ratio	$V_S = \pm 2\text{ V}$, $(V-) - 0.1\text{ V} < V_{CM} < (V+) - 2\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		100		dB
		$V_S = \pm 18\text{ V}$, $(V-) - 0.1\text{ V} < V_{CM} < (V+) - 2\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	95	110		
INPUT IMPEDANCE						
	Differential			$100 \parallel 3$		$\text{M}\Omega \parallel \text{pF}$
	Common-mode			$6 \parallel 3$		$10^{12}\ \Omega \parallel \text{pF}$
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	$V_S = 36\text{ V}$, $(V-) + 0.35\text{ V} < V_O < (V+) - 0.35\text{ V}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	94	130		dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product			1.2		MHz
SR	Slew rate	$G = +1$		0.4		$\text{V}/\mu\text{s}$
t_S	Settling time	To 0.1%, $V_S = \pm 18\text{ V}$, $G = +1$, 10-V step		20		μs
		To 0.01% (12-bit), $V_S = \pm 18\text{ V}$, $G = +1$, 10-V step		28		
THD+N	Total harmonic distortion + noise	$G = +1$, $f = 1\text{ kHz}$, $V_O = 3\text{ V}_{RMS}$		0.0002%		
OUTPUT						
V_O	Voltage output swing from rail	$V_S = \pm 18\text{ V}$, $R_L = 10\text{ k}\Omega$; $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$(V-) + 0.2$		$(V+) - 0.3$	V
		$R_L = 10\text{ k}\Omega$, $A_{OL} \geq 94\text{ dB}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$(V-) + 0.35$		$(V+) - 0.35$	
I_{SC}	Short-circuit current		-20		17	mA
C_{LOAD}	Capacitive load drive			See Typical Characteristics		pF
R_O	Open-loop output resistance	$f = 1\text{ MHz}$, $I_O = 0\text{ A}$		900		Ω
POWER SUPPLY						
V_S	Specified voltage range		2.7		36	V
I_Q	Quiescent current per amplifier	$I_O = 0\text{ A}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		125	175	μA

- (1) The input range can be extended beyond $(V+) - 2\text{ V}$ up to $V+$. See the [Typical Characteristics](#) and [Application and Implementation](#) sections for additional information.

7.8 Typical Characteristics

at $V_S = \pm 18\text{ V}$, $V_{CM} = V_S / 2$, $R_{LOAD} = 10\text{ k}\Omega$ connected to $V_S / 2$, and $C_L = 100\text{ pF}$ (unless otherwise noted)

Table 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage vs Common-Mode Voltage	Figure 2
Offset Voltage vs Common-Mode Voltage (Upper Stage)	Figure 3
Input Bias Current vs Temperature	Figure 4
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 5
CMRR and PSRR vs Frequency (Referred-to-Input)	Figure 6
0.1-Hz to 10-Hz Noise	Figure 7
Input Voltage Noise Spectral Density vs Frequency	Figure 8
Quiescent Current vs Supply Voltage	Figure 9
Open-Loop Gain and Phase vs Frequency	Figure 10
Closed-Loop Gain vs Frequency	Figure 11
Open-Loop Gain vs Temperature	Figure 12
Open-Loop Output Impedance vs Frequency	Figure 13
Small-Signal Overshoot vs Capacitive Load	Figure 14 , Figure 15
No Phase Reversal	Figure 16
Small-Signal Step Response (100 mV)	Figure 17 , Figure 18
Large-Signal Step Response	Figure 19 , Figure 20
Large-Signal Settling Time	Figure 21 , Figure 22
Short-Circuit Current vs Temperature	Figure 23
Maximum Output Voltage vs Frequency	Figure 24
EMIRR IN+ vs Frequency	Figure 25

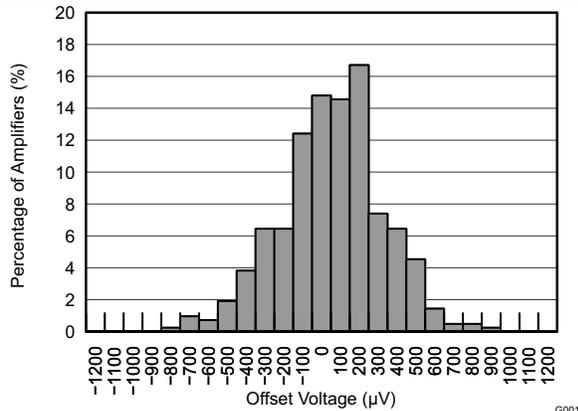


Figure 1. Offset Voltage Production Distribution

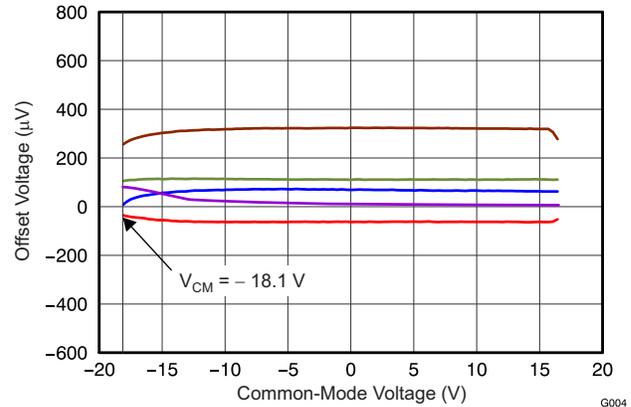


Figure 2. Offset Voltage vs Common-Mode Voltage

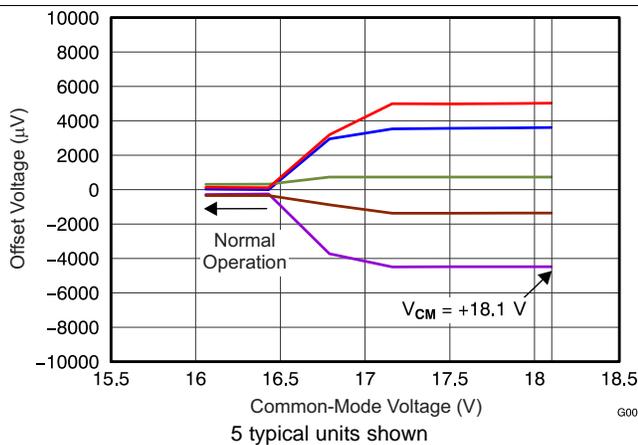


Figure 3. Offset Voltage vs Common-Mode Voltage (Upper Stage)

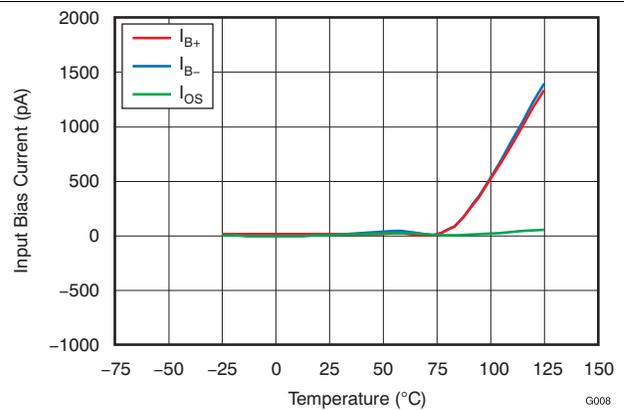


Figure 4. Input Bias Current vs Temperature

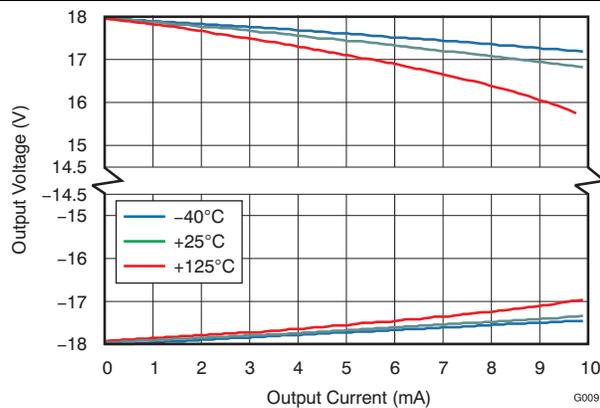


Figure 5. Output Voltage Swing vs Output Current (Maximum Supply)

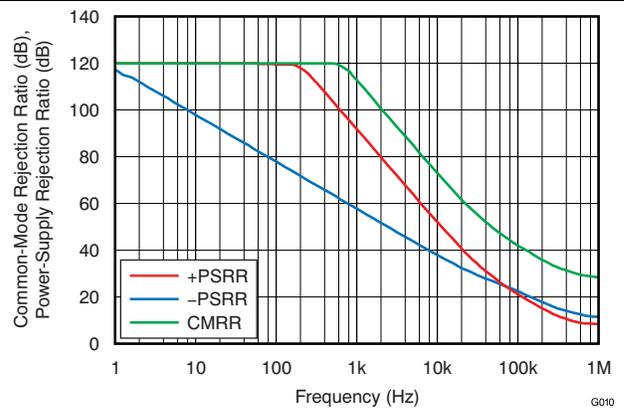


Figure 6. CMRR and PSRR vs Frequency (Referred-to Input)

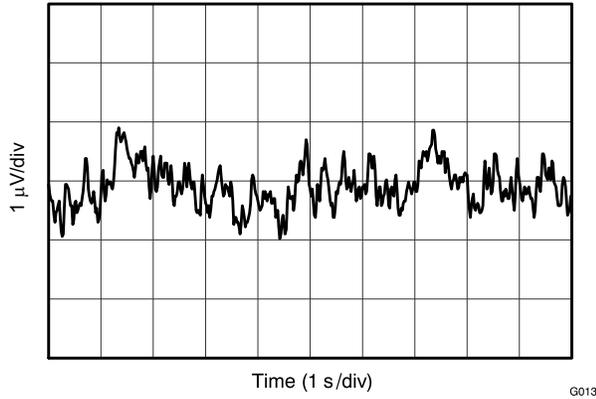


Figure 7. 0.1-Hz to 10-Hz Noise

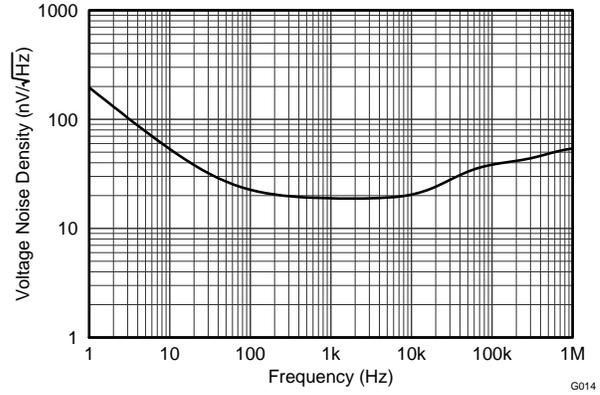


Figure 8. Input Voltage Noise Spectral Density vs Frequency

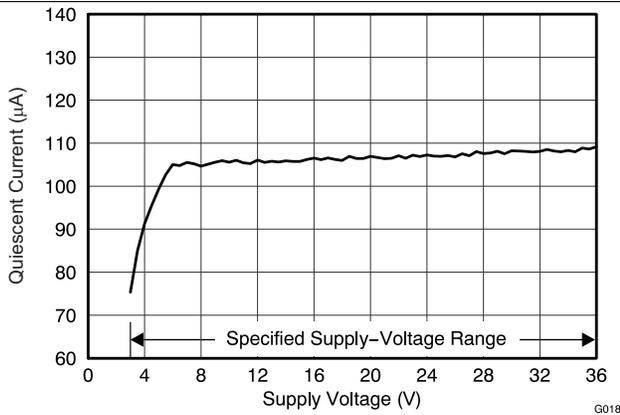


Figure 9. Quiescent Current vs Supply Voltage

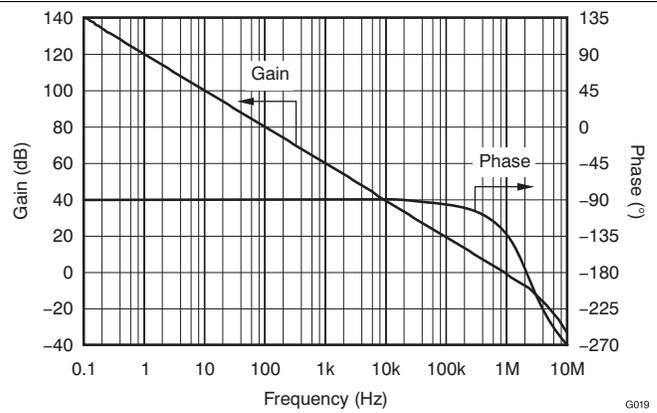


Figure 10. Open-Loop Gain and Phase vs Frequency

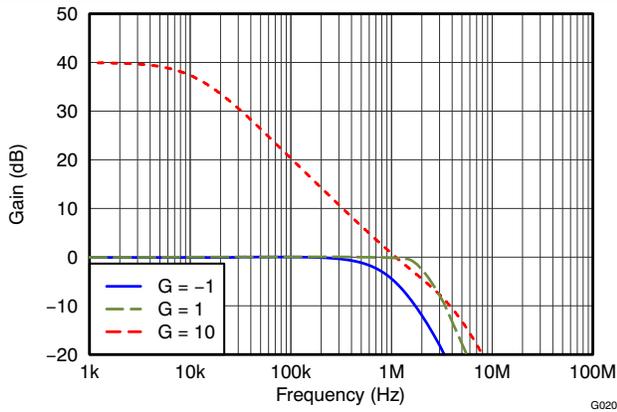


Figure 11. Closed-Loop Gain vs Frequency

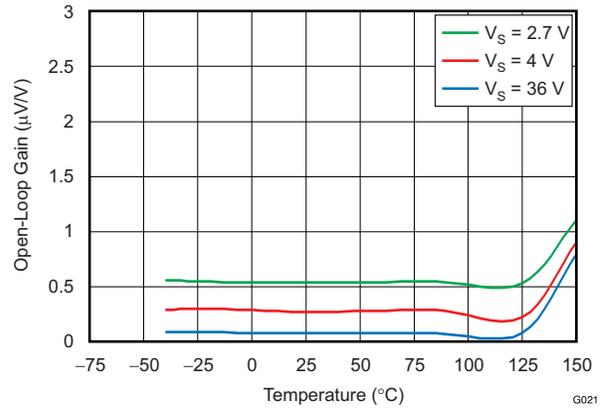


Figure 12. Open-Loop Gain vs Temperature

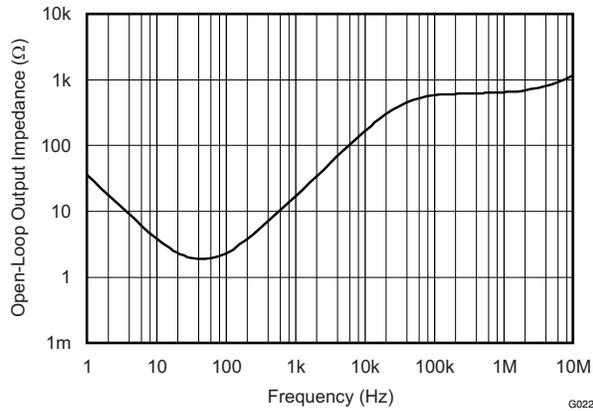


Figure 13. Open-Loop Output Impedance vs Frequency

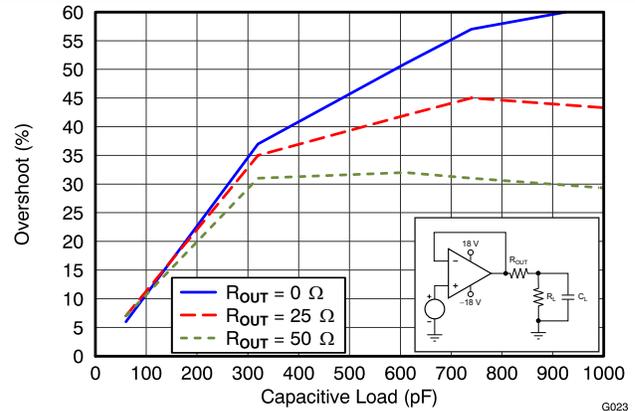


Figure 14. Small-Signal Overshoot vs Capacitive Load

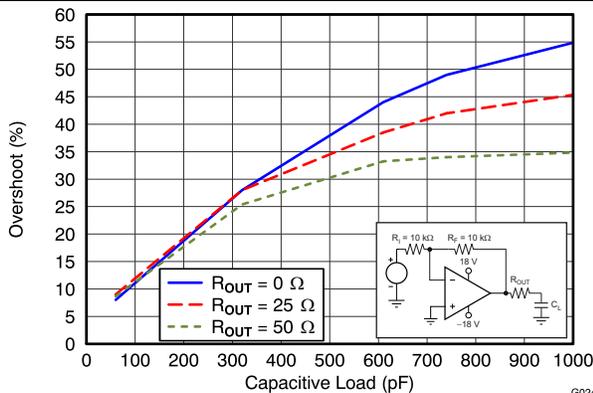


Figure 15. Small-Signal Overshoot vs Capacitive Load

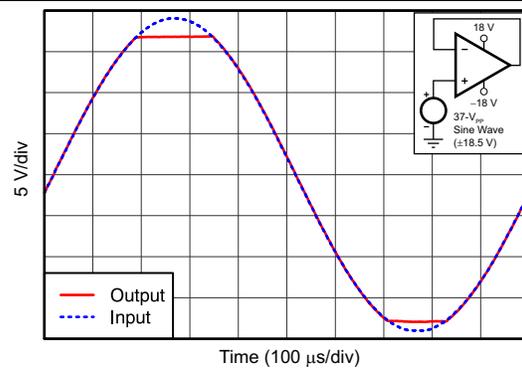


Figure 16. No Phase Reversal

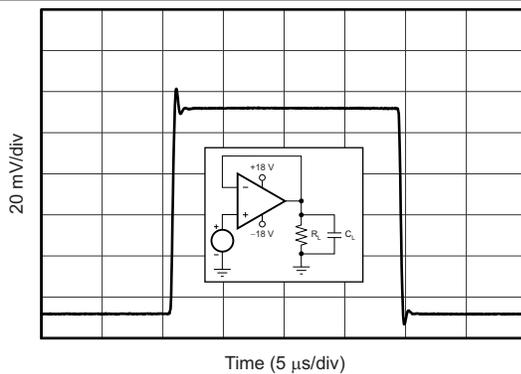


Figure 17. Small-Signal Step Response (100 mV)

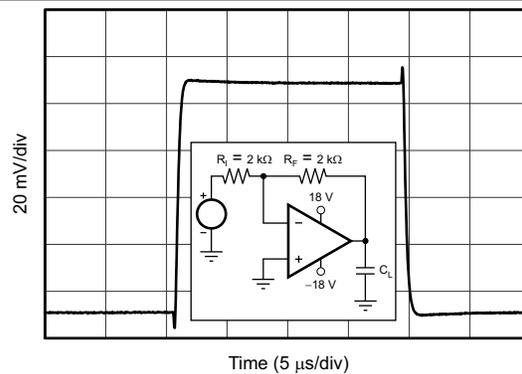
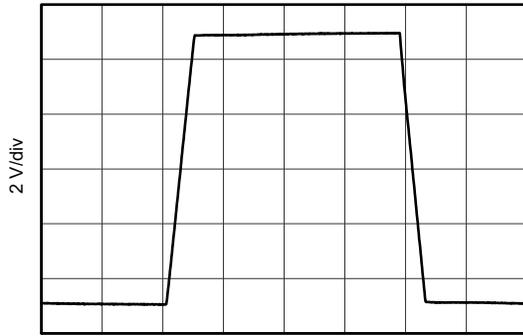


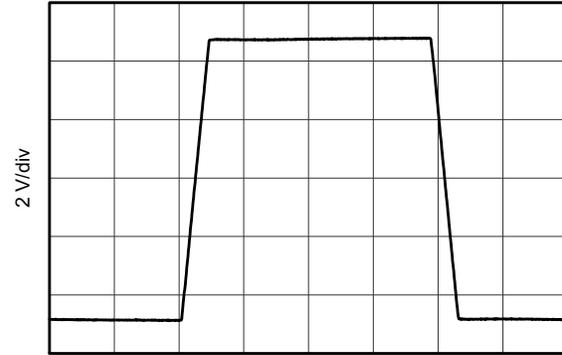
Figure 18. Small-Signal Step Response (100 mV)



$G = +1, R_L = 10 \text{ k}\Omega, C_L = 10 \text{ pF}$

G030

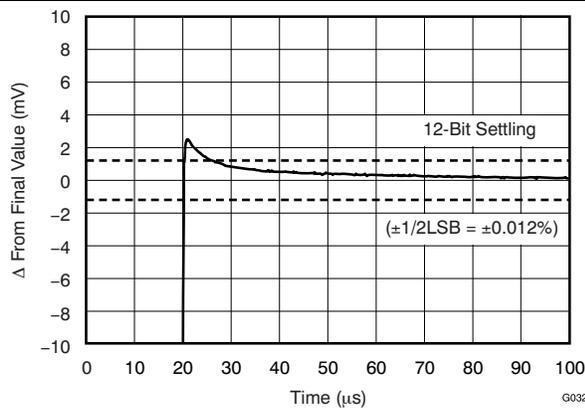
Figure 19. Large-Signal Step Response



$G = -1, R_L = 10 \text{ k}\Omega, C_L = 10 \text{ pF}$

G031

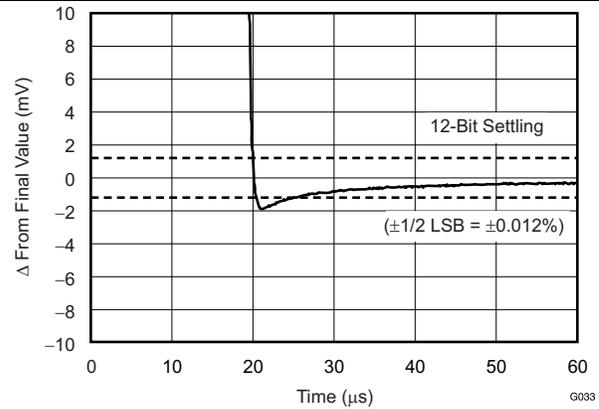
Figure 20. Large-Signal Step Response



10-V positive step, $G = +1$

G032

Figure 21. Large-Signal Settling Time



10-V negative step, $G = -1$

G033

Figure 22. Large-Signal Settling Time

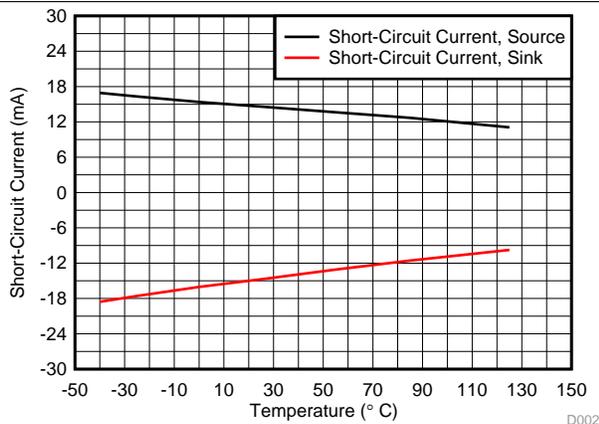


Figure 23. Short-Circuit Current vs Temperature

D002

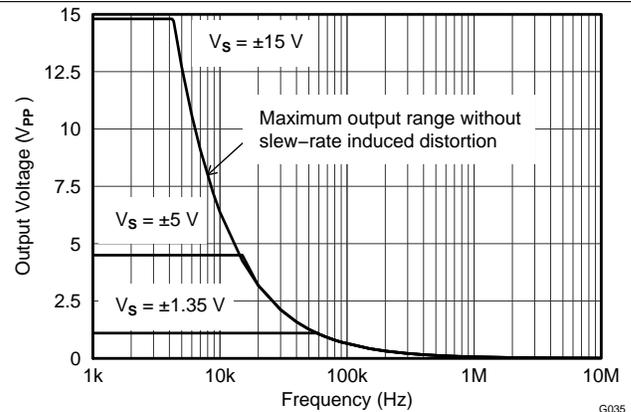
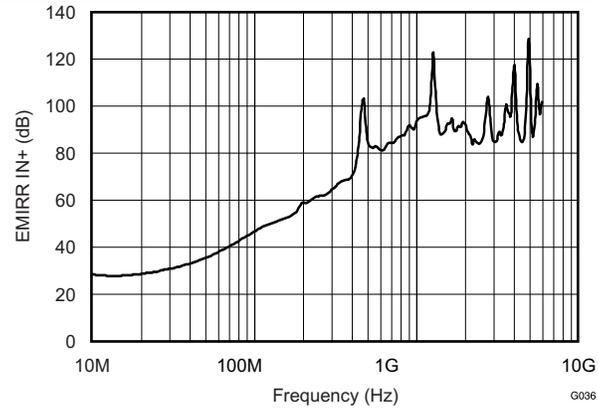


Figure 24. Maximum Output Voltage vs Frequency

G035



PRP = -10 dBm, VS = ±18 V, VCM = 0 V

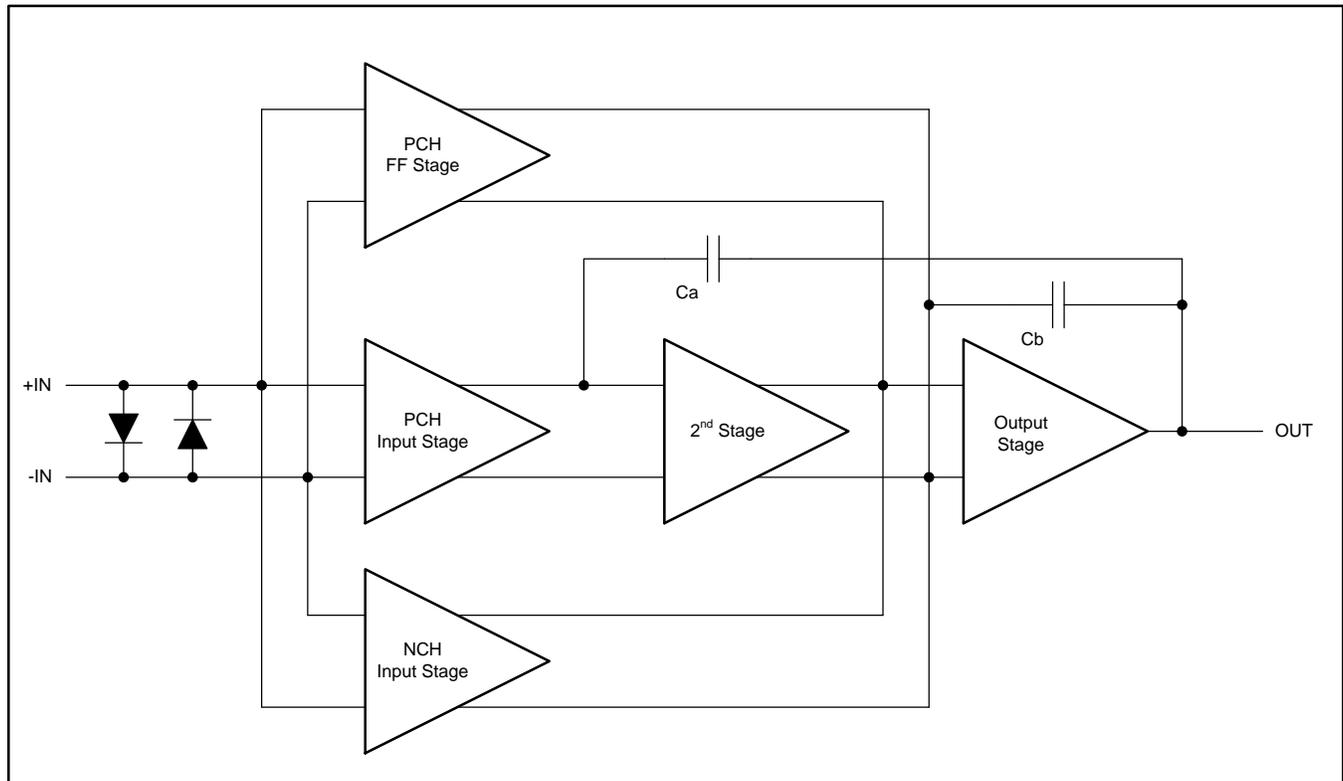
Figure 25. EMIRR IN+ vs Frequency

8 Detailed Description

8.1 Overview

The TLVx170 family of op amps provides high overall performance, making the devices ideal for many general-purpose applications. The excellent offset drift of only $2 \mu\text{V}/^\circ\text{C}$ provides excellent stability over the entire temperature range. In addition, the family offers very good overall performance with high CMRR, PSRR, and A_{OL} .

8.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

8.3 Feature Description

8.3.1 Operating Characteristics

The TLVx170 family of amplifiers is specified for operation from 2.7 V to 36 V ($\pm 1.35 \text{ V}$ to $\pm 18 \text{ V}$). Many of the specifications apply from -40°C to $+125^\circ\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#) section.

Feature Description (continued)

8.3.2 Phase-Reversal Protection

The TLVx170 family has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the TLVx170 prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in [Figure 26](#).

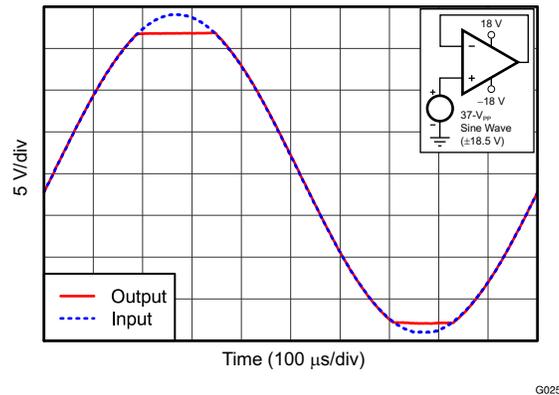


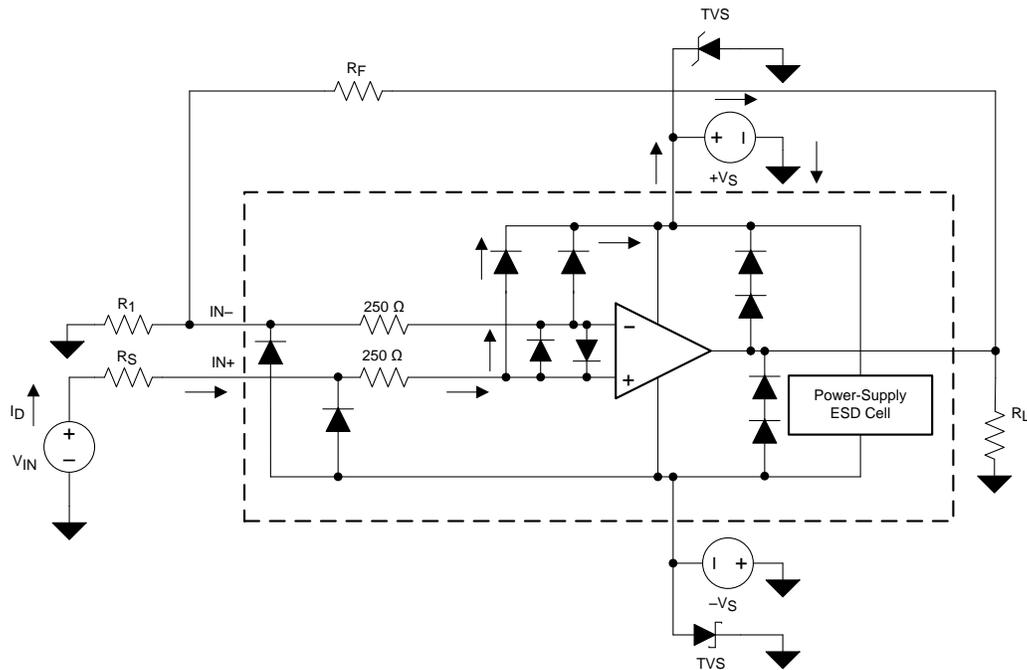
Figure 26. No Phase Reversal

8.3.3 Electrical Overstress

Designers often ask questions about the capability of an op amp to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits for protection from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. [Figure 27](#) illustrates the ESD circuits contained in the TLVx170 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the op amp. This protection circuitry is intended to remain inactive during normal circuit operation.

Feature Description (continued)



Copyright © 2016, Texas Instruments Incorporated

Figure 27. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the op amp core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the TLVx170 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the op amp connects into a circuit, as shown in [Figure 27](#), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

[Figure 27](#) shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($V+$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $V+$ can sink the current, then one of the upper input steering diodes conducts and directs current to $V+$. Excessively high current levels can flow with increasingly higher V_{IN} . As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the op amp and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the op amp absolute maximum ratings.

Feature Description (continued)

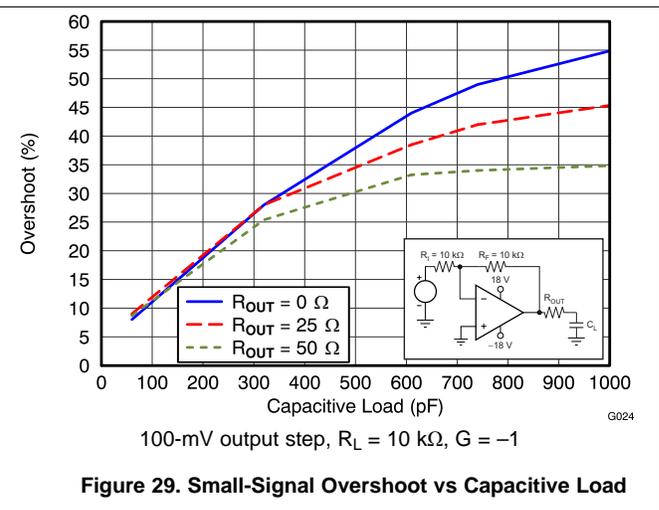
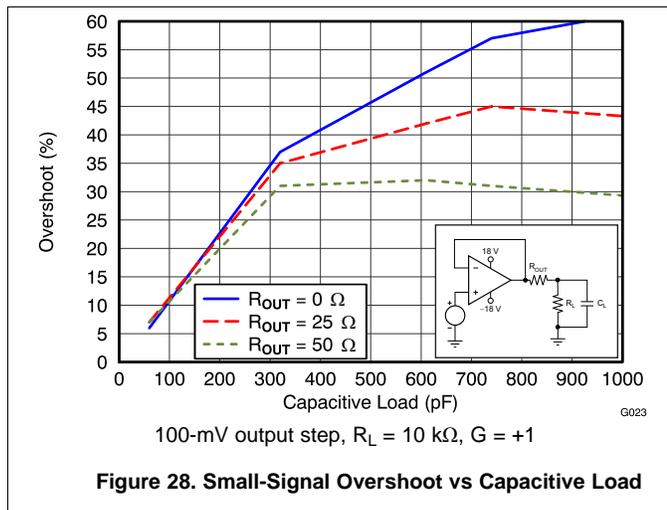
Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies ($V+$ or $V-$) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the op amp current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see [Figure 27](#). Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The TLVx170 input pins are protected from excessive differential voltage with back-to-back diodes; see [Figure 27](#). In most circuit applications, the input protection circuitry has no effect. However, in low-gain or $G = 1$ circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the TLVx170. [Figure 27](#) illustrates an example configuration that implements a current-limiting feedback resistor.

8.3.4 Capacitive Load and Stability

The dynamic characteristics of the TLVx170 are optimized for common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_{OUT} equal to 50 Ω) in series with the output. [Figure 28](#) and [Figure 29](#) show graphs of small-signal overshoot versus capacitive load for several values of R_{OUT} . Also, see the [Feedback Plots Define Op Amp AC Performance](#) application report for details of analysis techniques and application circuits.



8.4 Device Functional Modes

8.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the TLVx170 family extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in [Table 2](#).

Table 2. Typical Performance for Common-Mode Voltages Within 2 V of the Positive Supply

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	$(V+) - 2$		$(V+) + 0.1$	V
Offset voltage		7		mV
Offset voltage vs temperature		12		$\mu\text{V}/^\circ\text{C}$
Common-mode rejection ratio		65		dB
Open-loop gain		60		dB
Gain-bandwidth product		0.3		MHz
Slew rate		0.3		V/ μs

8.4.2 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from the saturated state to the linear state. The output devices of the op amp enter the saturation region when the output voltage exceeds the rated operating voltage, either resulting from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLVx170 is approximately 2 μs .

9 Application and Implementation

NOTE

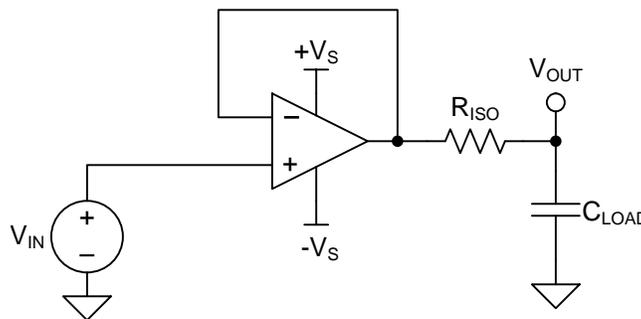
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLVx170 family of op amps provides high overall performance in a large number of general-purpose applications. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1- μ F capacitors are adequate. Follow the additional recommendations in the [Layout Guidelines](#) section in order to achieve the maximum performance from this device. Many applications can introduce capacitive loading to the output of the amplifier (potentially causing instability). One method of stabilizing the amplifier in such applications is to add an isolation resistor between the amplifier output and the capacitive load. The design process for selecting this resistor is given in the [Typical Application](#) section.

9.2 Typical Application

This circuit can be used to drive capacitive loads (such as cable shields, reference buffers, MOSFET gates, and diodes). The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system to ensure the circuit has sufficient phase margin.



Copyright © 2016, Texas Instruments Incorporated

Figure 30. Unity-Gain Buffer With R_{ISO} Stability Compensation

9.2.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (± 15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 μ F, 0.1 μ F, and 1 μ F
- Phase margin: 45° and 60°

9.2.2 Detailed Design Procedure

Figure 30 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 30. Not shown in Figure 30 is the open-loop output resistance of the op amp, R_o .

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + (R_o + R_{ISO}) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole (f_p) is determined by $(R_o + R_{ISO})$ and C_{LOAD} . Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and $1/\beta$ is 20 dB per decade; see Figure 31. The $1/\beta$ curve for a unity-gain buffer is 0 dB.

Typical Application (continued)

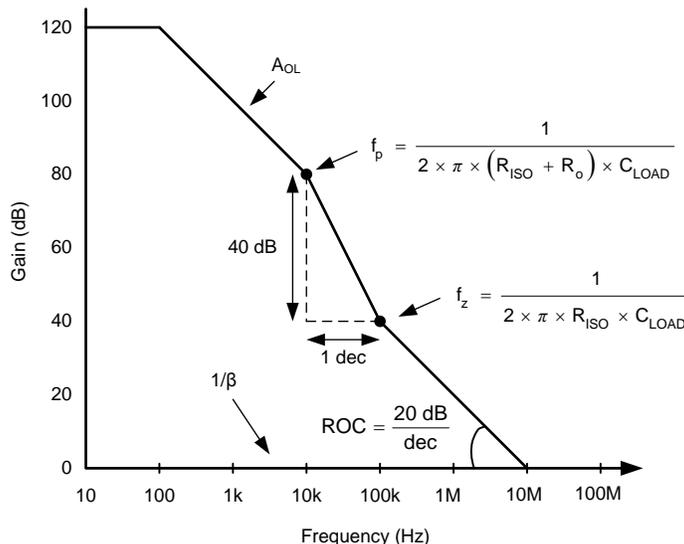


Figure 31. T1PD128 Unity-Gain Amplifier With RISO Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o . In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and ac gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 3 shows the overshoot percentage and ac gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the TLV170, see the [Capacitive Load Drive Solution Using an Isolation Resistor](#) precision design.

Table 3. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

9.2.3 Application Curve

Using the described methodology, the values of R_{ISO} that yield phase margins of 45° and 60° for various capacitive loads were determined. The results are shown in Figure 32.

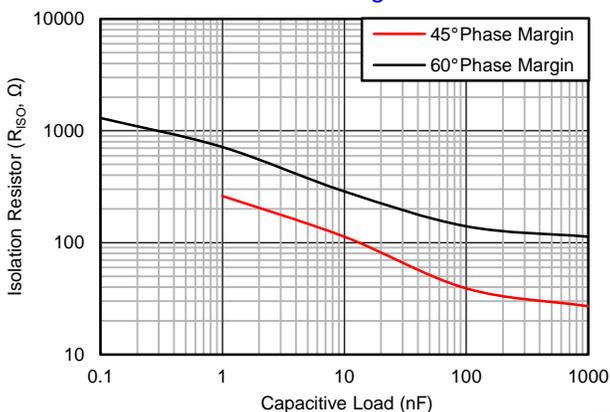


Figure 32. Isolation Resistor Required for Various Capacitive Loads to Achieve a Target Phase Margin

10 Power Supply Recommendations

The TLVx170 is specified for operation from 2.7 V to 36 V (± 1.35 V to ± 18 V); many specifications apply from -40°C to $+125^{\circ}\text{C}$. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#) section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the [Absolute Maximum Ratings](#).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout](#) section.

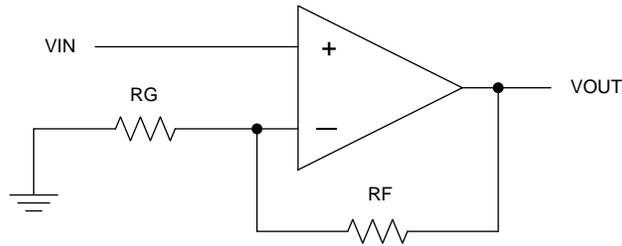
11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [Figure 34](#), keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example



Copyright © 2016, Texas Instruments Incorporated

Figure 33. Schematic Representation

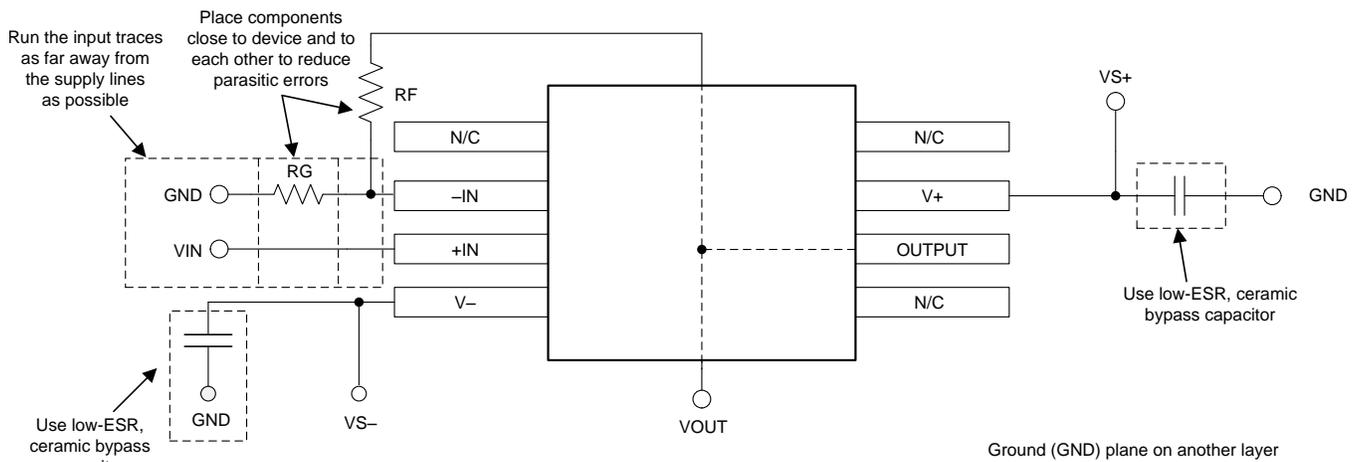


Figure 34. Op Amp Board Layout for a Noninverting Configuration

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 TINA-TI™ (免费软件下载)

TINA-TI™ 是一款基于 SPICE 引擎的电路仿真程序，简单易用并且功能强大。TINA-TI™ 是 TINA-TI™ 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI™ 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI™ 提供全面的后处理能力，便于用户以多种方式获得结果，用户可从 Analog eLab Design Center (模拟电子实验室设计中心) [免费下载](#)。虚拟仪器提供选择输入波形和探测电路节点、电压以及波形的功能，从而构建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件 (由 DesignSoft™ 提供) 或者 TINA-TI™ 软件。请下载 [TINA-TI™ 文件夹](#) 中的免费 TINA-TI™ 软件。

12.1.1.2 DIP 适配器 EVM

DIP 适配器 EVM 工具为小型表面贴装器件的原型设计提供了一种简易的低成本方法。评估工具使用以下 TI 封装: D 或 U (SOIC-8)、PW (TSSOP-8)、DGK (VSSOP-8)、DBV (SOT23-6、SOT23-5 和 SOT23-3)、DCK (SC70-6 和 SC70-5) 以及 DRL (SOT563-6)。DIP 适配器 EVM 也可搭配引脚排使用，或者直接与现有电路相连。

12.1.1.3 通用运放 EVM

通用运放 EVM 是一系列通用空白电路板，可简化采用各种器件封装类型的电路板原型设计。借助评估模块电路板设计，可以轻松快速地构造多种不同电路。共有 5 个模型可供选用，每个模型都对应一种特定封装类型。支持 PDIP、SOIC、VSSOP、TSSOP 和 SOT23 封装。

注

这些电路板均为空白电路板，用户必须自行提供相关器件。TI 建议您在订购通用运放 EVM 时申请几个运放器件样品。

12.1.1.4 TI 高精度设计

TI 高精度设计是由 TI 公司高精度模拟应用专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。TI 高精度设计可从 www.ti.com/ww/en/analog/precision-designs/ 在线获取。

12.1.1.5 WEBENCH® 滤波器设计器

WEBENCH® 滤波器设计器 是一款简单、功能强大且便于使用的有源滤波器设计程序。此 WEBENCH® Filter Designer 通过选择 TI 运算放大器以及 TI 供应商合作伙伴的无源组件来构建优化滤波器设计方案。

WEBENCH® 设计中心以基于网络的工具形式提供 WEBENCH® 滤波器设计器。用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

12.2 文档支持

12.2.1 相关文档

相关文档如下：

[《反馈曲线图定义运算放大器交流性能》](#)（文献编号：SBOA015）

12.3 相关链接

表 4 列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 4. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TLV170	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV2170	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV4170	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 接收文档更新通知

如需接收文档更新通知，请访问 ti.com 上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.5 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 商标

TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
DesignSoft is a trademark of DesignSoft, Inc.

12.7 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI)及其下属子公司有权根据 JESD46 最新标准,对所提供的产品和服务进行更正、修改、增强、改进或其它更改,并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息,并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内,且 TI 认为有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定,否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险,客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息,不能构成从 TI 获得使用这些产品或服务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可,或是 TI 的专利权或其它知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分,仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时,如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分,则会失去相关 TI 组件或服务的所有明示或暗示授权,且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意,尽管任何应用相关信息或支持仍可能由 TI 提供,但他们将独立负责满足与其产品及其在应用中使用的 TI 产品相关的所有法律、法规和安全相关要求。客户声明并同意,他们具备制定与实施安全措施所需的全部专业技术和知识,可预见故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中,为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此,此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备)的授权许可,除非各方授权官员已经达成了专门管控此类使用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同意,对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用,其风险由客户单独承担,并且由客户独立负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品,这些产品主要用于汽车。在任何情况下,因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址: 上海市浦东新区世纪大道1568号, 中建大厦32楼邮政编码: 200122
Copyright © 2016, 德州仪器半导体技术(上海)有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV170IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	14QT	Samples
TLV170IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	14QT	Samples
TLV170IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV170	Samples
TLV2170IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	14NV	Samples
TLV2170IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	14NV	Samples
TLV2170IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL2170	Samples
TLV4170ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TLV4170	Samples
TLV4170IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TLV4170	Samples
TLV4170IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4170	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

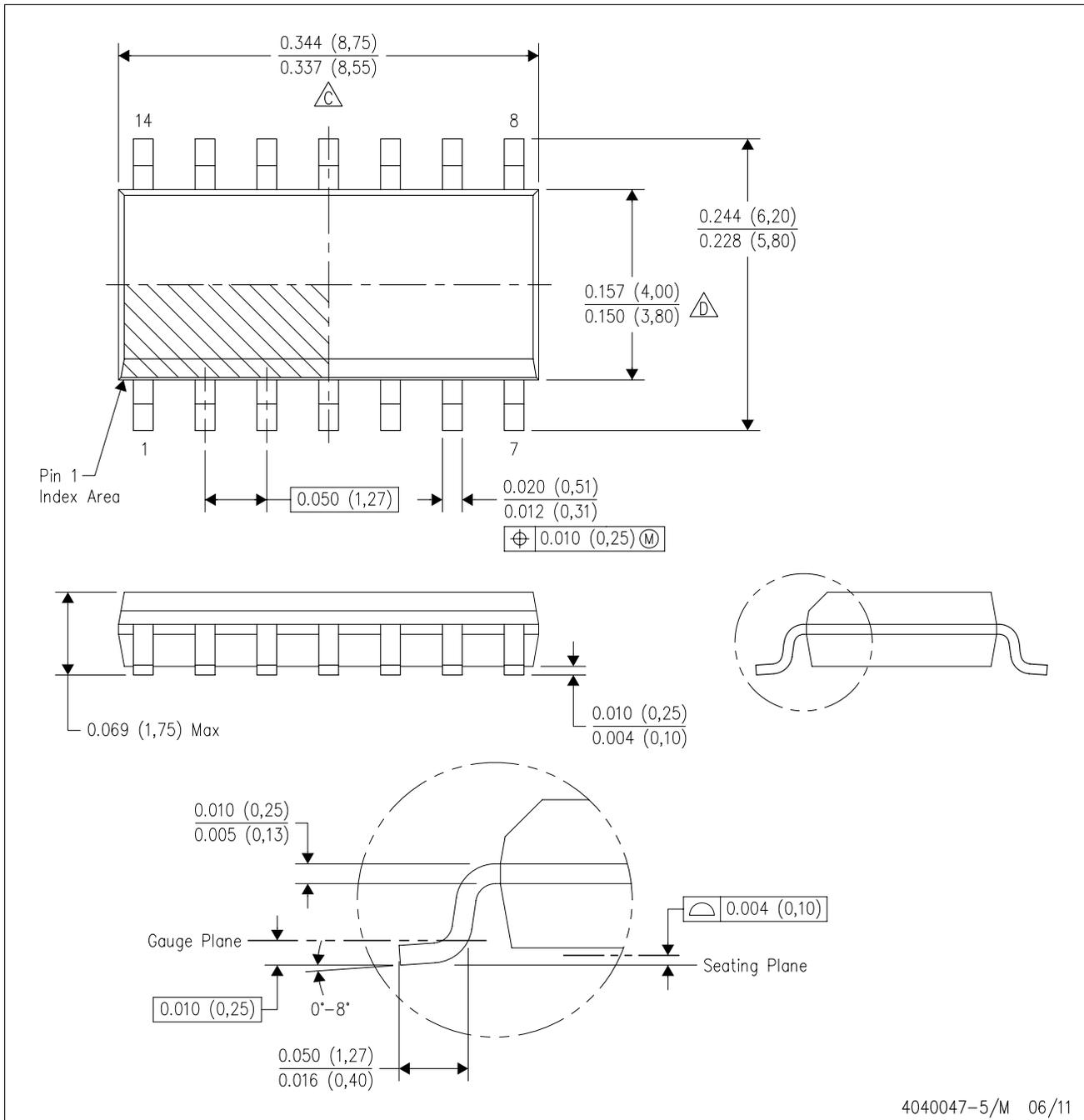
- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

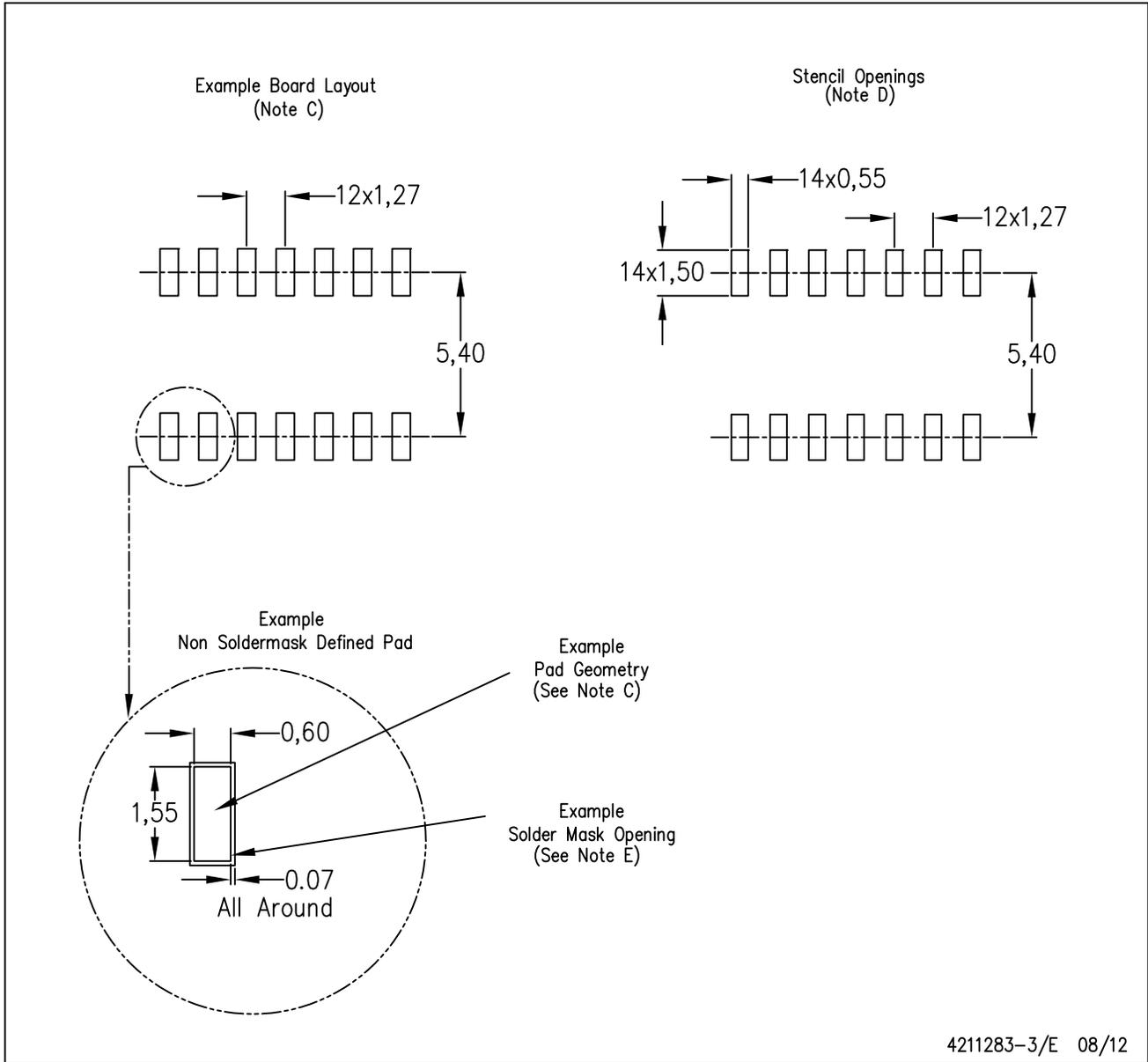


4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

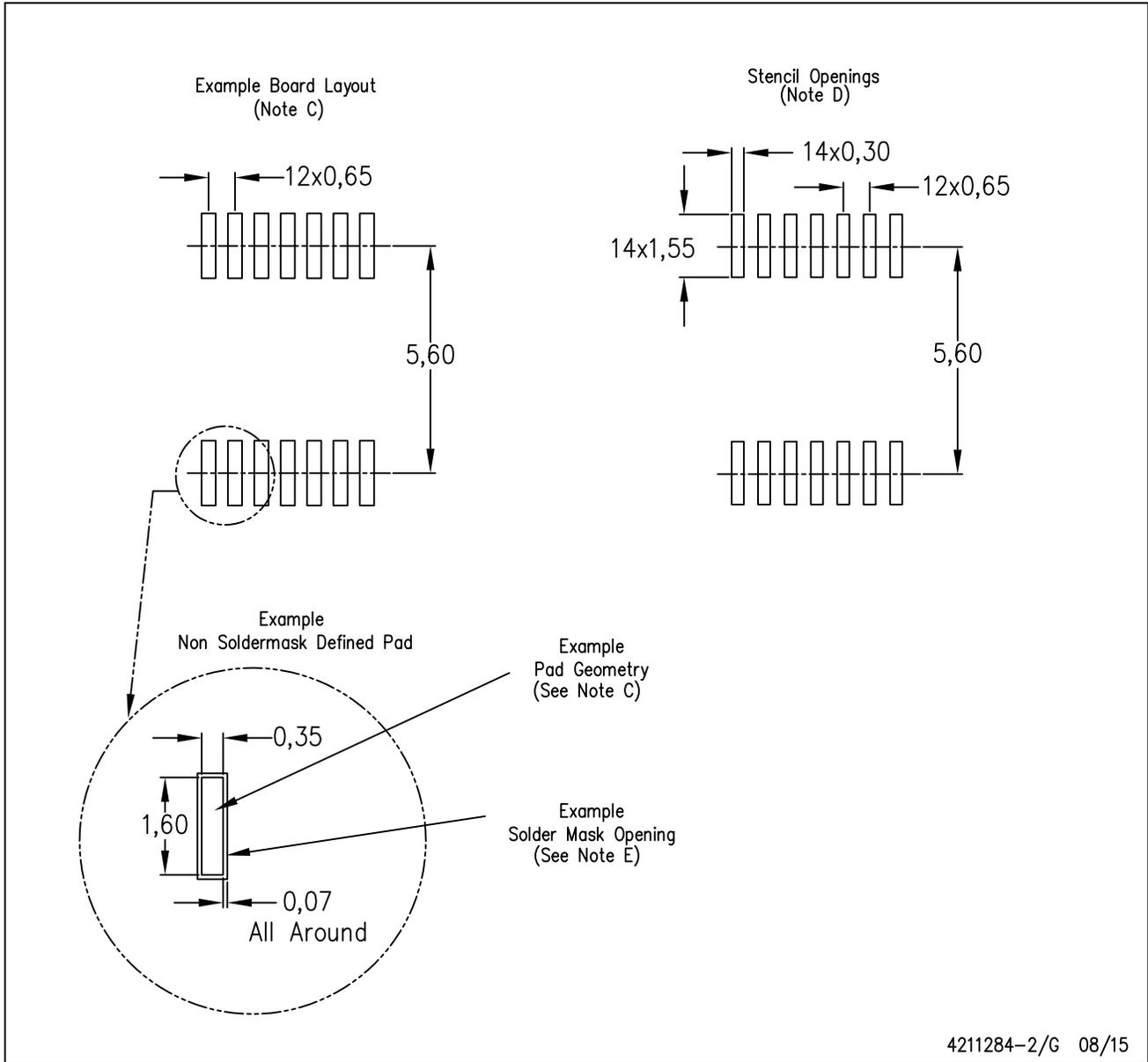
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

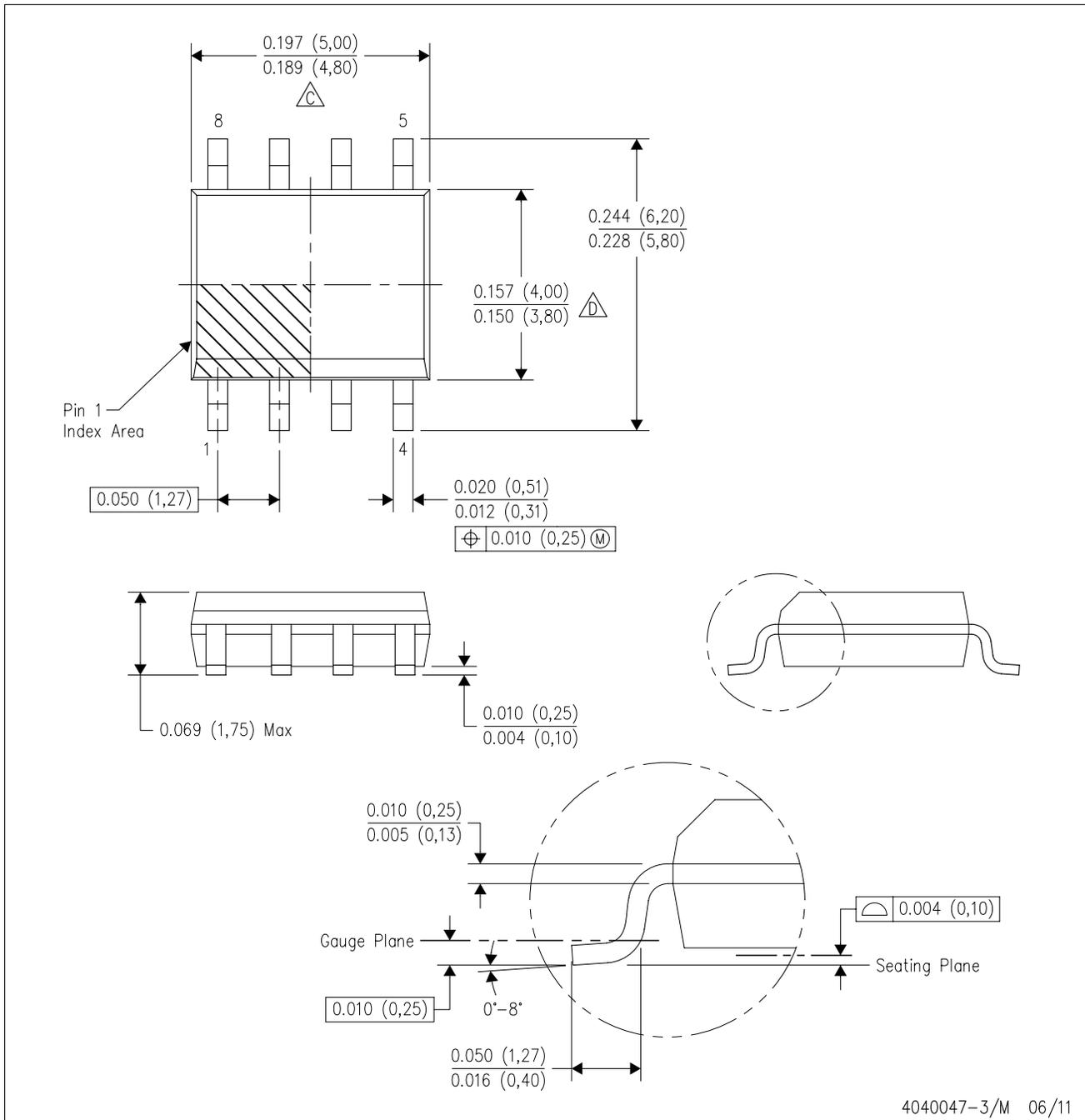
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

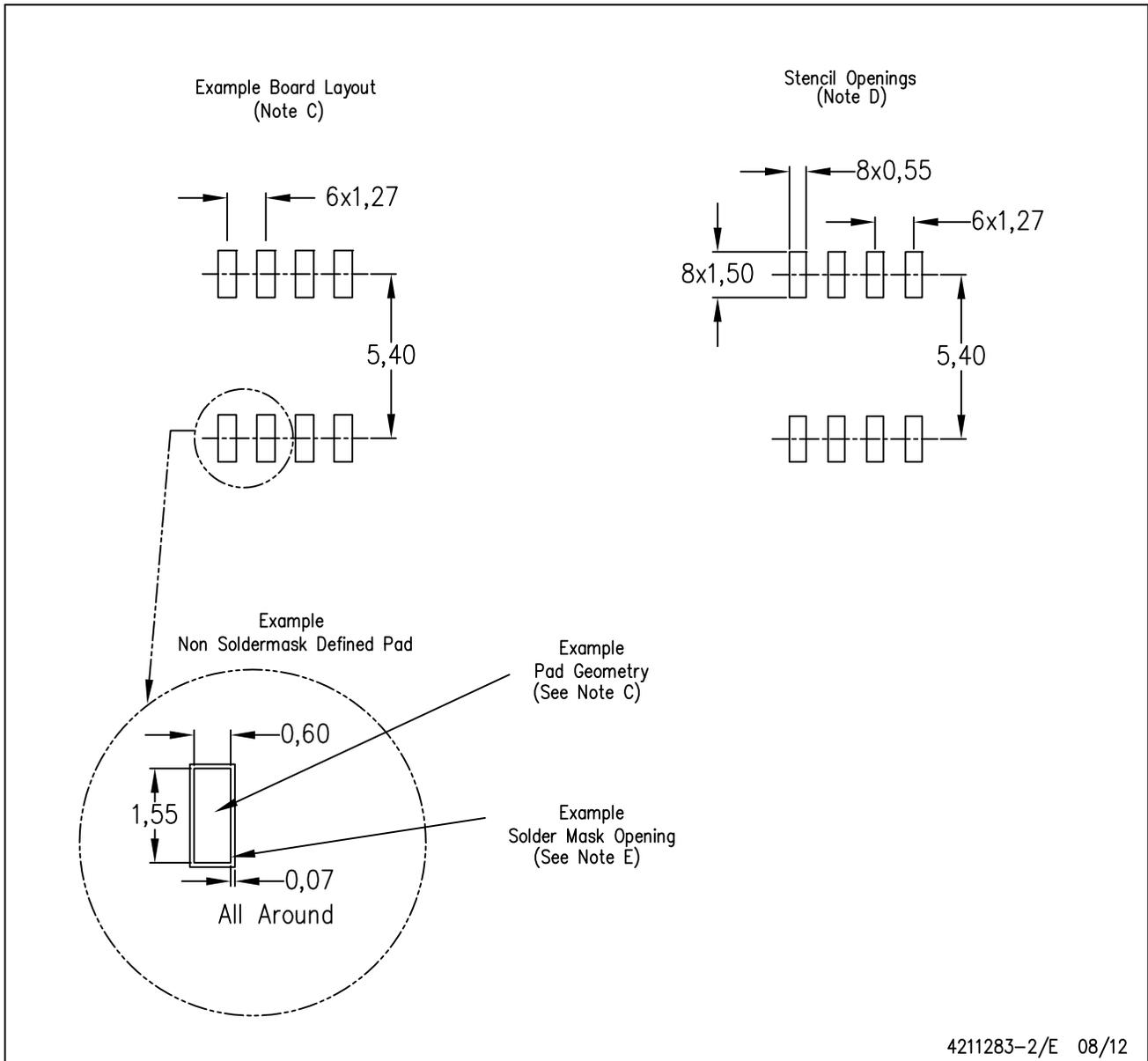
PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

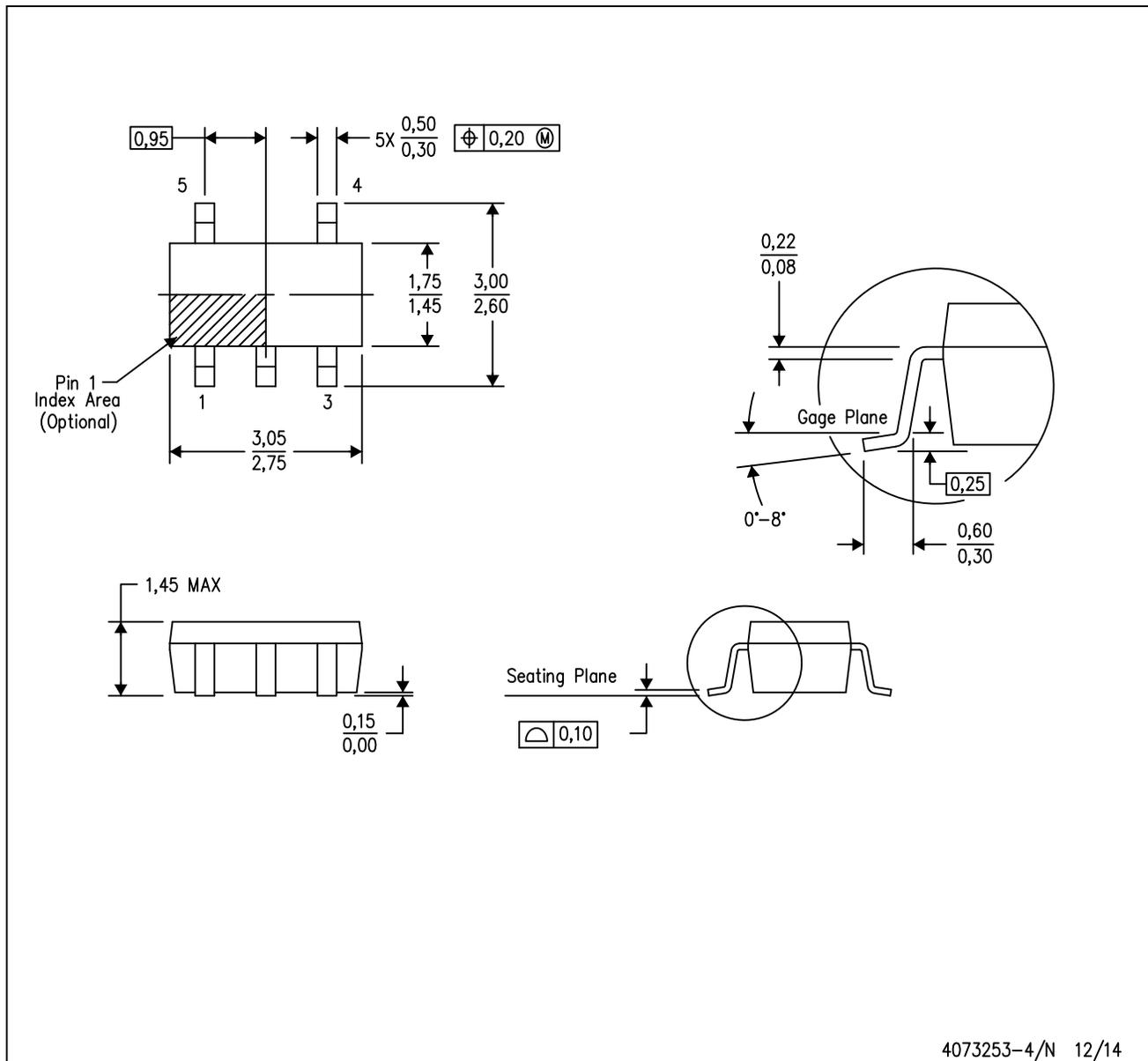
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBV (R-PDSO-G5)

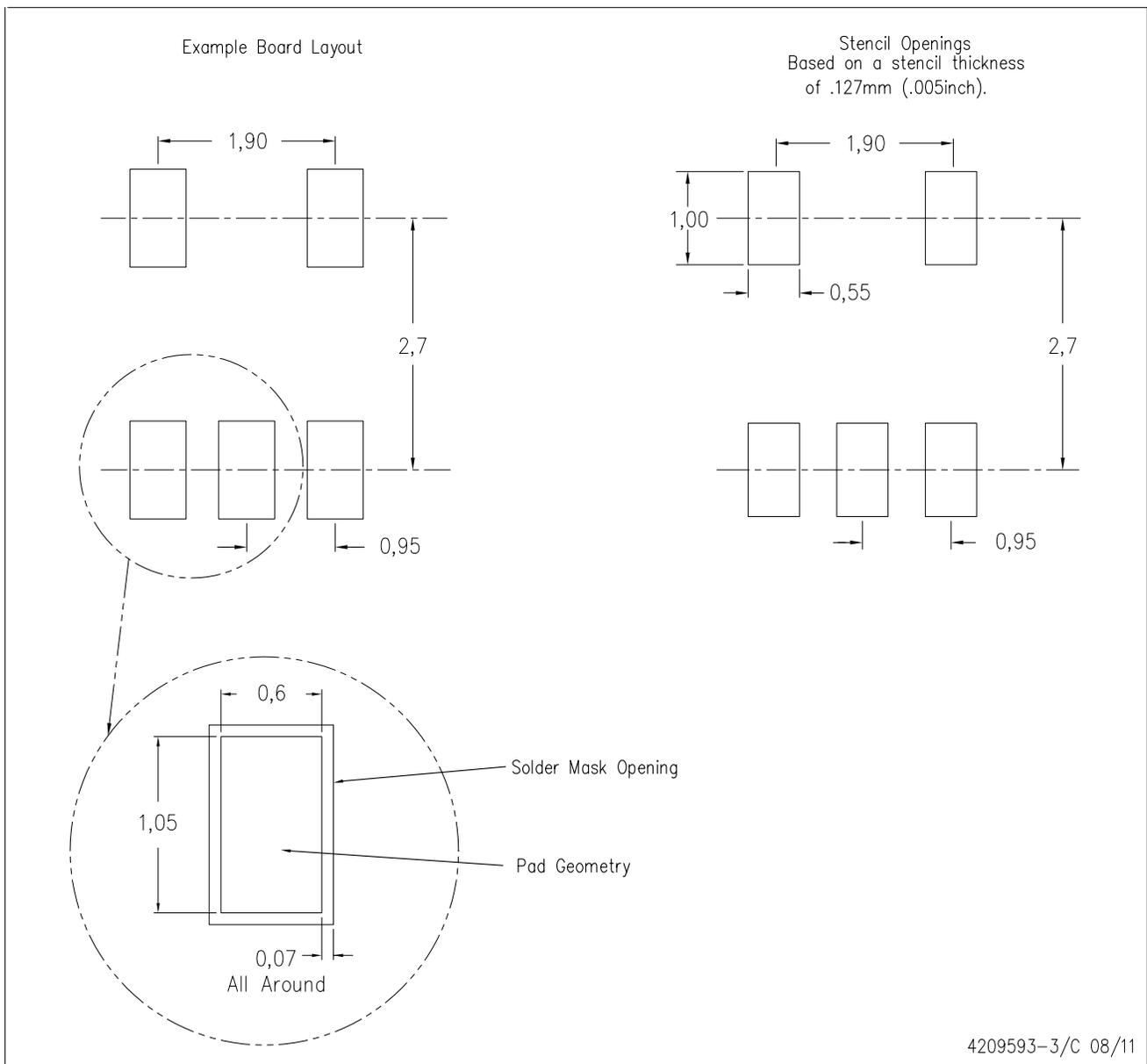
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

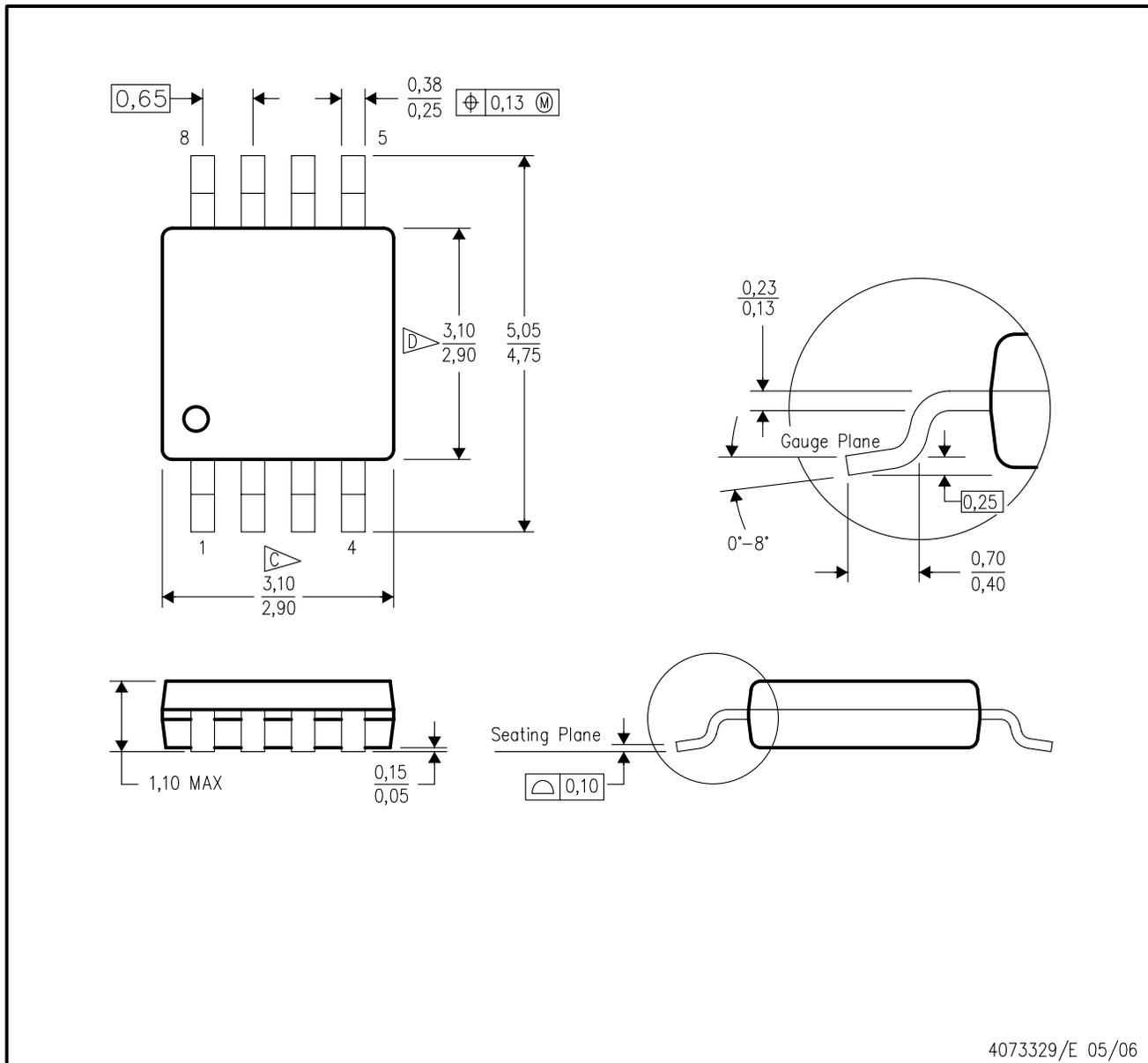
PLASTIC SMALL OUTLINE



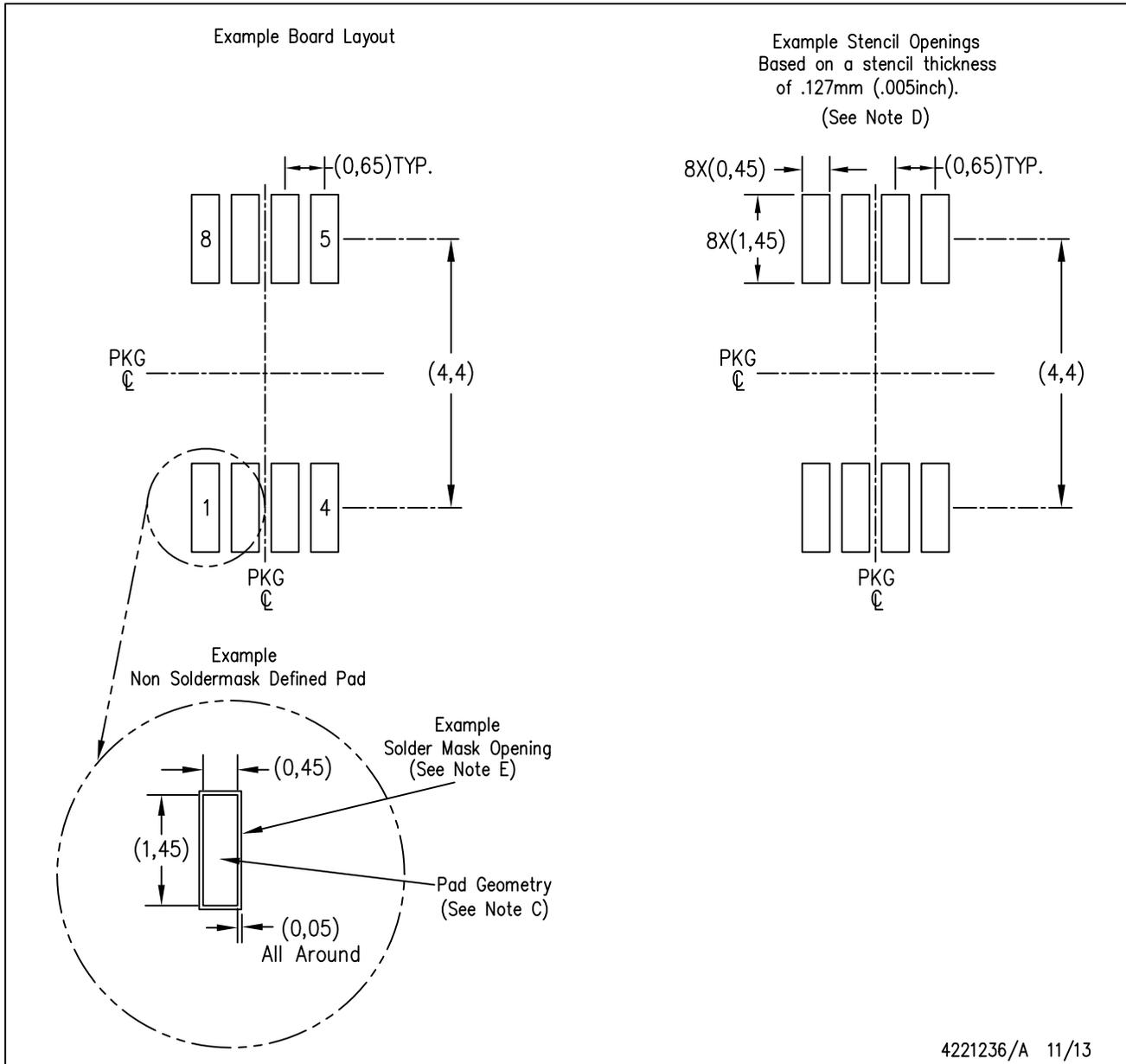
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (<http://www.ti.com/sc/docs/stdterms.htm>) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权负责并确保应用的安全性，及设计人员的应用（包括应用中使用的 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何应用前，将彻底测试该等应用和该等应用中所用 TI 产品的功能。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的应用，如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的应用时，才被授权使用、复制和修改任何相关 TI 资源。但并未依据禁止反言原则或其他法律授予您任何 TI 知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等许可包括但不限于任何专利权、版权、屏蔽作品权或与美国 TI 产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默示的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的符合相关功能安全标准和要求的的应用。在应用内使用产品的行为本身不会配有安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和标准。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的产品，并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2017 德州仪器半导体技术（上海）有限公司