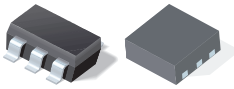


# 精密可调节限流配电开关

查询样品: **TPS2553-Q1**

## 特性

- 符合汽车应用要求
- 具有符合 **AEC-Q100** 的下列结果:
  - 器件温度 **1** 级: **-40°C** 至 **125°C** 的环境运行温度范围
  - 器件人体模型 **(HBM)** 静电放电 **(ESD)** 分类等级 **H2**
  - 器件充电器件模型 **(CDM) ESD** 分类等级 **C3B**
- 高达 **1.5A** 最大负载电流
- **1.7A** 电流下 **±6%** 限流精度（典型值）
- 满足 **USB** 限流要求
- 与 **TPS2550/51** 向后兼容
- 可调节电流限制，**75mA-1300mA**（典型值）
- 恒定电流 **(TPS2553-Q1)**
- 快速过流响应 **-2μs**（典型值）
- **85mΩ** 高侧金属氧化物半导体场效应晶体管 **(MOSFET)**（**DBV** 封装）
- 反向输入**-**输出电压保护
- 工作范围: **2.5V** 至 **6.5V**
- 内置软启动
- 符合 **IEC 61000-4-2** 标准的 **15kV** 静电放电 **(ESD)** 保护（用外部电容实现）
- **UL**列表 **-** 文件号**E169910** 和 **NEMKO IEC60950-1-am1 ed2.0**
- 请见**TI** 开关系列产品

## 应用范围

- 车载应用
- 配电
- 限流

## 说明

TPS2553-Q1 配电开关用于要求精确限流或者遇到高电容和短路的应用并提供高达 1.5A 的持续负载电流。 这些器件借助一个外部电阻器提供一个 75mA至 1.7A（典型值）间的可编程电流限制阀值。 在更高电流限制设置上可实现严格至 ±6% 的电流限制精度。 对电源开关的上升和下降次数进行控制以大大降低接通/切断期间的电流冲击。

当输出负载超过限流阀值时，TPS2553-Q1 器件借助于恒定电流模式来将输出电流限制在安全的水平上。 当输出电压被驱动至高于输入时，一个内部反向电压比较器将电源开关禁用来保护开关输入端上的器件。 在过流和反向电压情况下，$\overline{\text{FAULT}}$输出被置为低电平。

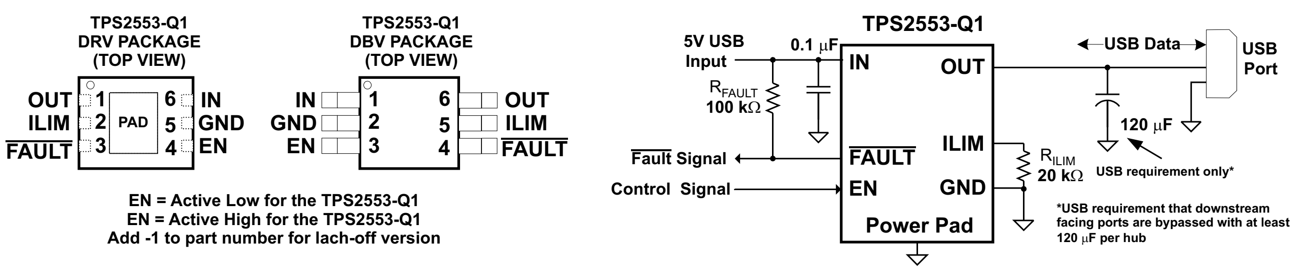



图 **1.** 作为 **USB** 电源开关的典型应用



English Data Sheet: SLVSBD0

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**GENERAL SWITCH CATALOG**

| 33 mΩ, single | 80 mΩ, single | 80 mΩ, dual | 80 mΩ, dual | 80 mΩ, triple | 80 mΩ, quad | 80 mΩ, quad |
|---|---|---|---|---|---|---|
| TPS201xA 0.2 A - 2 A<br>TPS202x 0.2 A - 2 A<br>TPS203x 0.2 A - 2 A | TPS2014 600 mA<br>TPS2015 1 A<br>TPS2041B 500 mA<br>TPS2051B 500 mA<br>TPS2045A 250 mA<br>TPS2049 100 mA<br>TPS2055A 250 mA<br>TPS2061 1 A<br>TPS2065 1 A<br>TPS2068 1.5 A<br>TPS2069 1.5 A | TPS2042B 500 mA<br>TPS2052B 500 mA<br>TPS2046B 250 mA<br>TPS2056 250 mA<br>TPS2062 1 A<br>TPS2066 1 A<br>TPS2060 1.5 A<br>TPS2064 1.5 A | TPS2080 500 mA<br>TPS2081 500 mA<br>TPS2082 500 mA<br>TPS2090 250 mA<br>TPS2091 250 mA<br>TPS2092 250 mA | TPS2043B 500 mA<br>TPS2053B 500 mA<br>TPS2047B 250 mA<br>TPS2057A 250 mA<br>TPS2063 1 A<br>TPS2067 1 A | TPS2044B 500 mA<br>TPS2054B 500 mA<br>TPS2048A 250 mA<br>TPS2058 250 mA | TPS2085 500 mA<br>TPS2086 500 mA<br>TPS2087 500 mA<br>TPS2095 250 mA<br>TPS2096 250 mA<br>TPS2097 250 mA |

## ORDERING INFORMATION(1)

| $T_A$ (2) | ENABLE | ORDERABLE PART NUMBER | TOP-SIDE MARKING | RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT(2) | CURRENT-LIMIT PROTECTION |
|---|---|---|---|---|---|
| –40°C to 125°C | Active high | TPS2553QDRVRQ1 | Preview | 1.5 A | Constant-Current |
| | | TPS2553QDBVRQ1 | PYEQ | | |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Maximum ambient temperature is a function of device junction temperature and system level considerations, such as load current, power dissipation and board layout. See *dissipation rating table* and *recommended operating conditions* for specific information related to these devices.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1] [2]

| | | VALUE | UNIT |
|---|---|---|---|
| | Voltage range on IN, OUT, EN or $\overline{EN}$, ILIM, $\overline{FAULT}$ | –0.3 to 7 | V |
| | Voltage range from IN to OUT | –7 to 7 | V |
| $I_O$ | Continuous output current | Internally Limited | |
| | Continuous $\overline{FAULT}$ sink current | 25 | mA |
| | ILIM source current | 1 | mA |
| ESD Ratings | Human Body Model Classification Level H2 | 2 | kV |
| | Charged Device Model ESD Classification Level C3B | 750 | V |
| | IEC system level (contact/air)[3] | 8 / 15 | kV |
| $T_J$ | Maximum junction temperature | –40 to 150 | °C |
| $T_{stg}$ | Storage temperature | –65 to 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are referenced to GND unless otherwise noted.
(3) Surges per EN61000-4-2. 1999 applied to output terminals of EVM. These are passing test levels, not failure threshold.

## THERMAL INFORMATION

| THERMAL METRIC[1] | | TPS2553-Q1 | TPS2553-Q1 | UNIT |
|---|---|---|---|---|
| | | DBV (6 PINS) | DRV (6 PINS) | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 182.6 | 72 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 122.2 | 85.3 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 29.4 | 41.3 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 20.8 | 1.7 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 28.9 | 41.7 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | n/a | 11.1 | |

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage, IN | | 2.5 | 6.5 | V |
| $V_{EN}$ | Enable voltage | | 0 | 6.5 | V |
| $V_{IH}$ | High-level input voltage on EN or $\overline{EN}$ | | 1.1 | | V |
| $V_{IL}$ | Low-level input voltage on EN or $\overline{EN}$ | | | 0.66 | V |
| $I_{OUT}$ | Continuous output current, OUT | –40 °C ≤ $T_J$ ≤ 125 °C | 0 | 1.2 | A |
| | | –40 °C ≤ $T_J$ ≤ 105 °C | 0 | 1.5 | A |
| $R_{ILIM}$ | Current-limit threshold resistor range (nominal 1%) from ILIM to GND | | 15 | 232 | kΩ |
| $I_O$ | Continuous $\overline{FAULT}$ sink current | | 0 | 10 | mA |
| | Input de-coupling capacitance, IN to GND | | 0.1 | | μF |
| $T_J$ | Operating virtual junction temperature(1) | $I_{OUT}$ ≤ 1.2 A | –40 | 125 | °C |
| | | $I_{OUT}$ ≤ 1.5 A | -40 | 105 | °C |

(1) See "Dissipation Rating Table" and "Power Dissipation and Junction Temperature" sections for details on how to calculate maximum junction temperature for specific applications and packages.

## ELECTRICAL CHARACTERISTICS

over recommended operating conditions, $V_{\overline{EN}}$ = 0 V, or $V_{EN}$ = $V_{IN}$, $R_{FAULT}$ = 10 kΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS(1) | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **POWER SWITCH** | | | | | | | | |
| $r_{DS(on)}$ | Static drain-source on-state resistance | DBV package, $T_A$ = 25°C | | | | 85 | 95 | mΩ |
| | | DBV package, –40°C ≤$T_A$ ≤125°C | | | | | 135 | mΩ |
| | | DRV package, $T_A$ = 25°C | | | | 100 | 115 | mΩ |
| | | DRV package, –40°C ≤$T_A$ ≤105°C | | | | | 140 | mΩ |
| | | DRV package, –40°C ≤$T_A$ ≤125°C | | | | | 150 | mΩ |
| $t_r$ | Rise time, output | $V_{IN}$ = 6.5 V | $C_L$ = 1 μF, $R_L$ = 100 Ω, (see Figure 2) | | | 1.1 | 1.5 | ms |
| | | $V_{IN}$ = 2.5 V | | | | 0.7 | 1 | ms |
| $t_f$ | Fall time, output | $V_{IN}$ = 6.5 V | | | 0.2 | | 0.5 | ms |
| | | $V_{IN}$ = 2.5 V | | | 0.2 | | 0.5 | ms |
| **ENABLE INPUT EN OR $\overline{EN}$** | | | | | | | | |
| | Enable pin turn on/off threshold | | | | 0.66 | | 1.1 | V |
| $I_{EN}$ | Input current | $V_{EN}$ = 0 V or 6.5 V, $V_{\overline{EN}}$ = 0 V or 6.5 V | | | –0.5 | | 0.5 | μA |
| $t_{on}$ | Turnon time | $C_L$ = 1 μF, $R_L$ = 100 Ω, (see Figure 2) | | | | | 3 | ms |
| $t_{off}$ | Turnoff time | | | | | | 3 | ms |
| **CURRENT-LIMIT** | | | | | | | | |
| $I_{OS}$ | Current-limit threshold (Maximum DC output current $I_{OUT}$ delivered to load) and Short-circuit current, OUT connected to GND | | $R_{ILIM}$ = 15 kΩ | –40°C ≤$T_A$ ≤105°C | 1610 | 1700 | 1800 | mA |
| | | | $R_{ILIM}$ = 20 kΩ | $T_A$ = 25°C | 1215 | 1295 | 1375 | mA |
| | | | | –40°C ≤$T_A$ ≤125°C | 1200 | 1295 | 1375 | mA |
| | | | $R_{ILIM}$ = 49.9 kΩ | $T_A$ = 25°C | 490 | 520 | 550 | mA |
| | | | | –40°C ≤$T_A$ ≤125°C | 475 | 520 | 565 | mA |
| | | | $R_{ILIM}$ = 210 kΩ | | 100 | 130 | 150 | mA |
| | | | ILIM shorted to IN | | 50 | 75 | 100 | mA |
| $t_{IOS}$ | Response time to short circuit | $V_{IN}$ = 5 V (see Figure 3) | | | | 2 | | μs |
| **REVERSE-VOLTAGE PROTECTION** | | | | | | | | |
| | Reverse-voltage comparator trip point ($V_{OUT}$ – $V_{IN}$) | | | | 95 | 135 | 190 | mV |
| | Time from reverse-voltage condition to MOSFET turn off | $V_{IN}$ = 5 V | | | 3 | 5 | 7 | ms |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

## ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions, $V_{\overline{EN}}$ = 0 V, or $V_{EN}$ = $V_{IN}$, $R_{FAULT}$ = 10 kΩ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS (1) | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | |
| $I_{IN\_off}$ | Supply current, low-level output | $V_{IN}$ = 6.5 V, No load on OUT, $V_{\overline{EN}}$ = 6.5 V or $V_{EN}$ = 0 V | | | 0.1 | 1 | μA |
| $I_{IN\_on}$ | Supply current, high-level output | $V_{IN}$ = 6.5 V, No load on OUT | $R_{ILIM}$ = 20 kΩ | | 120 | 140 | μA |
| | | | $R_{ILIM}$ = 210 kΩ | | 100 | 120 | μA |
| $I_{REV}$ | Reverse leakage current | $V_{OUT}$ = 6.5 V, $V_{IN}$ = 0 V | $T_A$ = 25 °C | | 0.01 | 1 | μA |
| **UNDERVOLTAGE LOCKOUT** | | | | | | | |
| UVLO | Low-level input voltage, IN | $V_{IN}$ rising | | | 2.35 | 2.45 | V |
| | Hysteresis, IN | $T_A$ = 25 °C | | | 25 | | mV |
| **$\overline{FAULT}$ FLAG** | | | | | | | |
| $V_{OL}$ | Output low voltage, $\overline{FAULT}$ | $I_{/FAULT}$ = 1 mA | | | | 180 | mV |
| | Off-state leakage | $V_{/FAULT}$ = 6.5 V | | | | 1 | μA |
| | $\overline{FAULT}$ deglitch | $\overline{FAULT}$ assertion or de-assertion due to overcurrent condition | | 5 | 8 | 11 | ms |
| | | $\overline{FAULT}$ assertion or de-assertion due to reverse-voltage condition | | 2 | 4 | 6 | ms |
| **THERMAL SHUTDOWN** | | | | | | | |
| | Thermal shutdown threshold | | | 155 | | | °C |
| | Thermal shutdown threshold in current-limit | | | 135 | | | °C |
| | Hysteresis | | | | 10 | | °C |

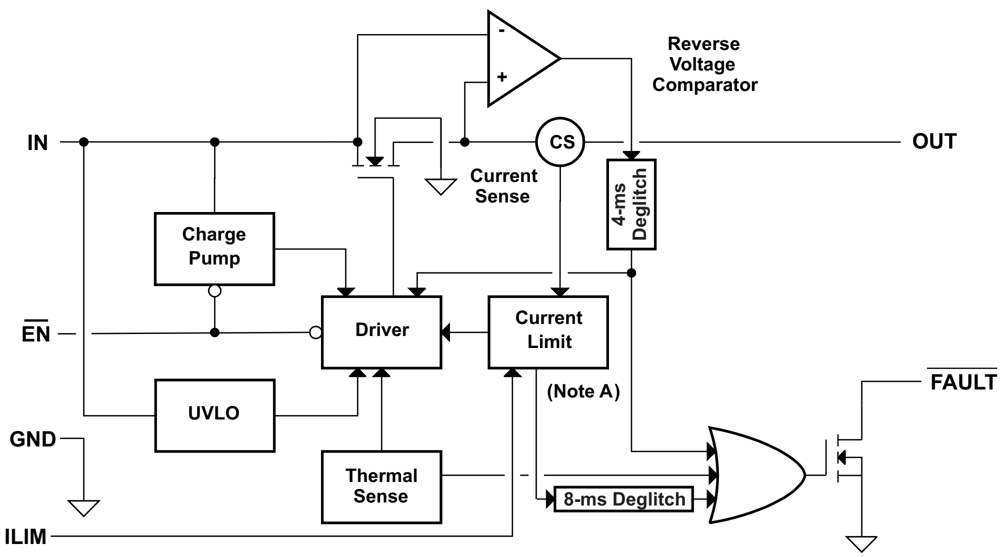
# DEVICE INFORMATION

## Pin Functions

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | TPS2553-Q1DBV NO. | TPS2553-Q1DRV NO. | | |
| $\overline{EN}$ | – | – | I | Enable input, logic low turns on power switch |
| EN | 3 | 4 | I | Enable input, logic high turns on power switch |
| GND | 2 | 5 | | Ground connection; connect externally to PowerPAD |
| IN | 1 | 6 | I | Input voltage; connect a 0.1 µF or greater ceramic capacitor from IN to GND as close to the IC as possible. |
| $\overline{FAULT}$ | 4 | 3 | O | Active-low open-drain output, asserted during overcurrent, overtemperature, or reverse-voltage conditions. |
| OUT | 6 | 1 | O | Power-switch output |
| ILIM | 5 | 2 | O | External resistor used to set current-limit threshold; recommended 15 kΩ ≤ $R_{ILIM}$ ≤ 232 kΩ. |
| PowerPAD™ | – | PAD | | Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND pin externally. |

Add -1 for Latch-Off version

## FUNCTIONAL BLOCK DIAGRAM




Note A: TPS255x parts enter constant current mode during current limit condition; TPS255x-1 parts latch off

## PARAMETER MEASUREMENT INFORMATION

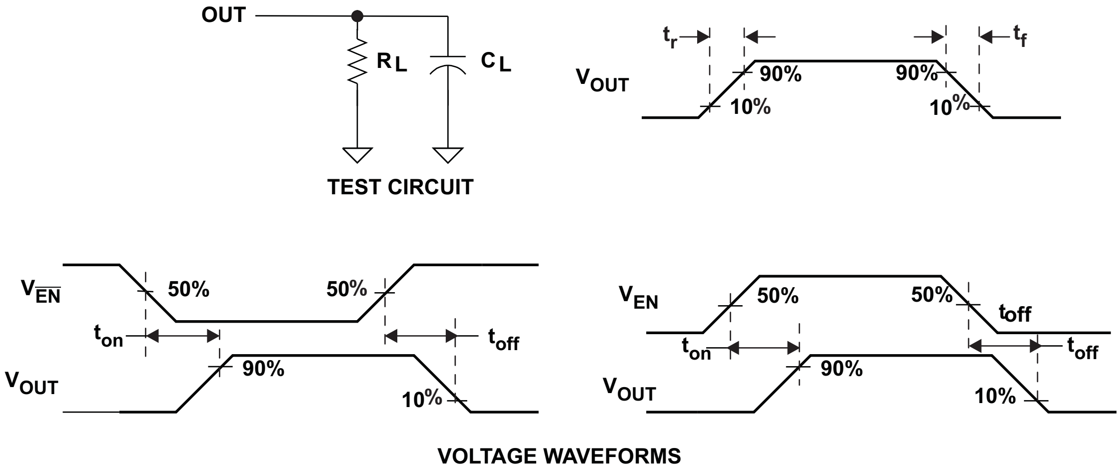



**Figure 2. Test Circuit and Voltage Waveforms**

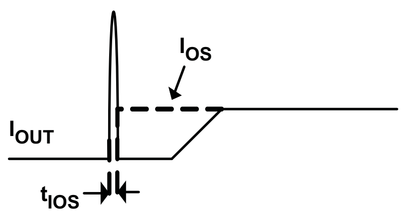



**Figure 3. Response Time to Short Circuit Waveform**

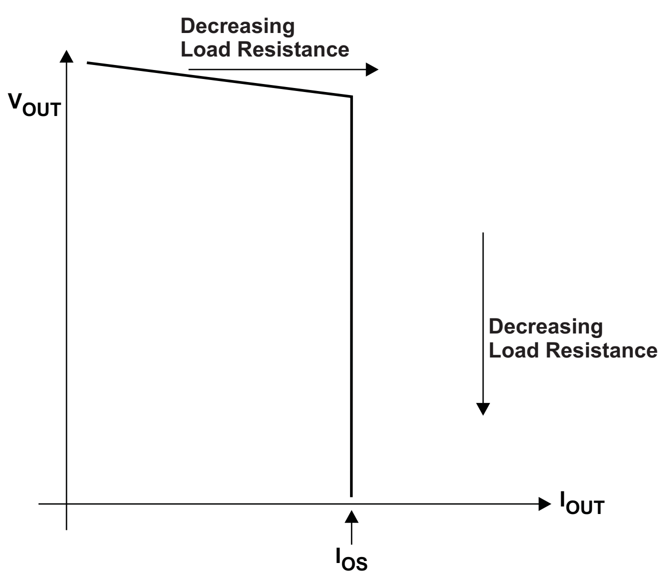



**Figure 4. Output Voltage vs. Current-Limit Threshold**

## TYPICAL CHARACTERISTICS

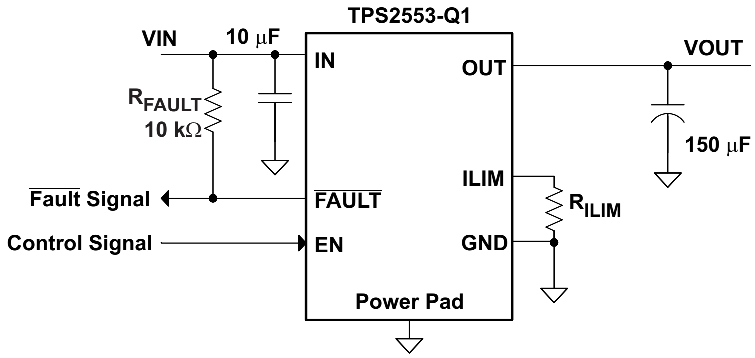



**Figure 5. Typical Characteristics Reference Schematic**

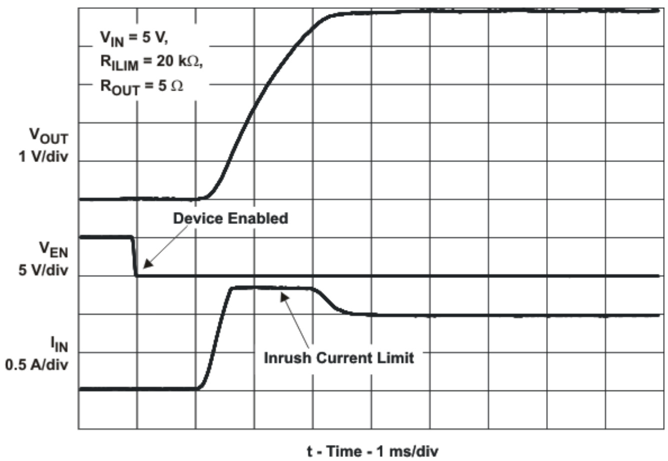



**Figure 6. Turnon Delay and Rise Time**

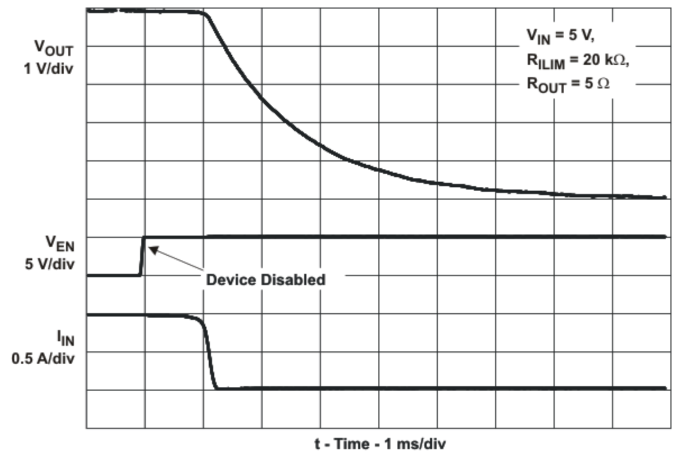



**Figure 7. Turnoff Delay and Fall Time**

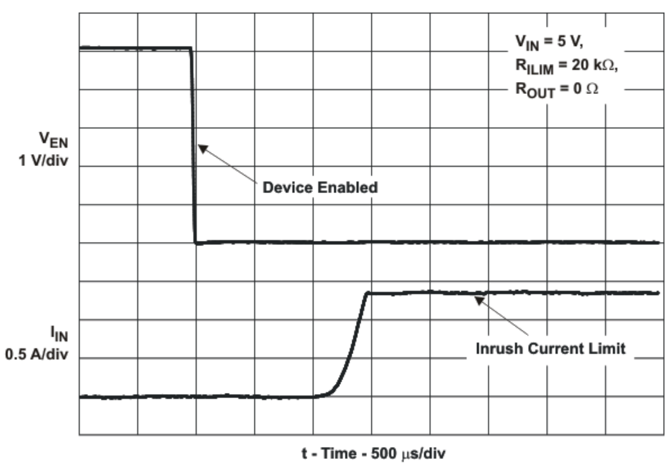



**Figure 8. Device Enabled into Short-Circuit**

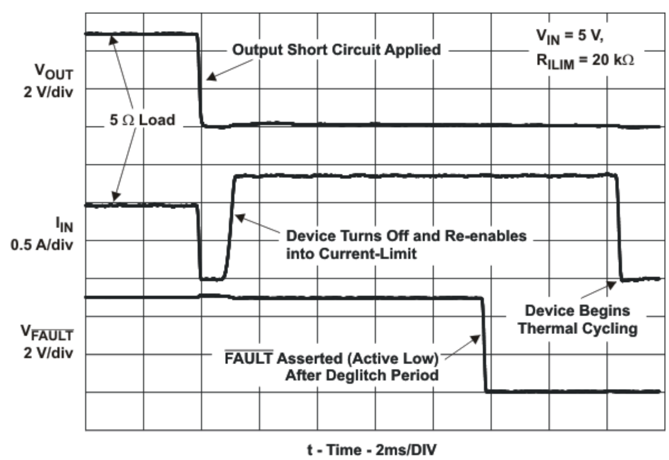



**Figure 9. Full-Load to Short-Circuit Transient Response**

## TYPICAL CHARACTERISTICS (continued)

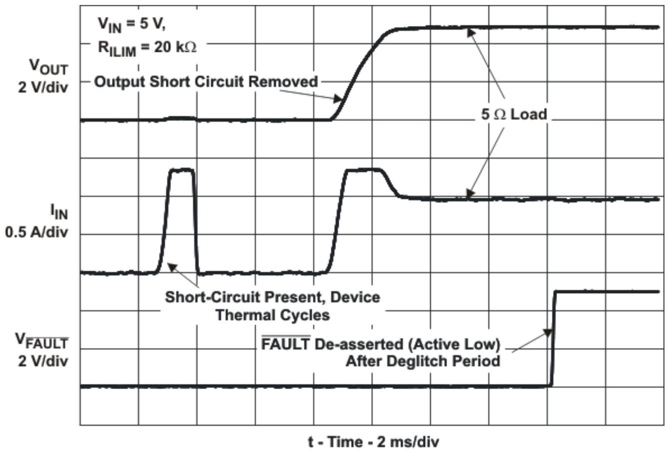



Figure 10. Short-Circuit to Full-Load Recovery Response

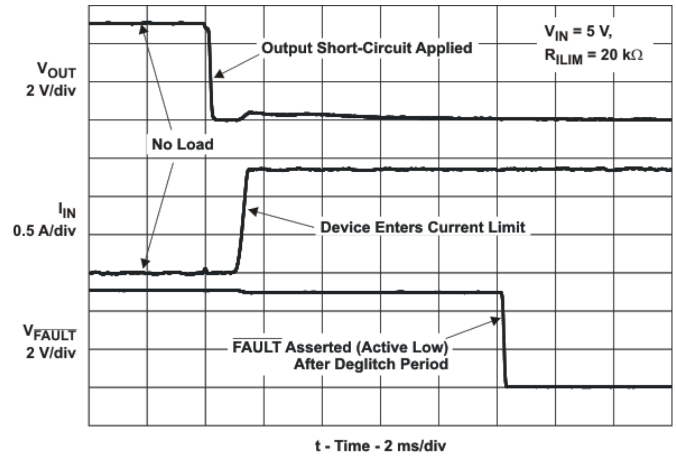



Figure 11. No-Load to Short-Circuit Transient Response

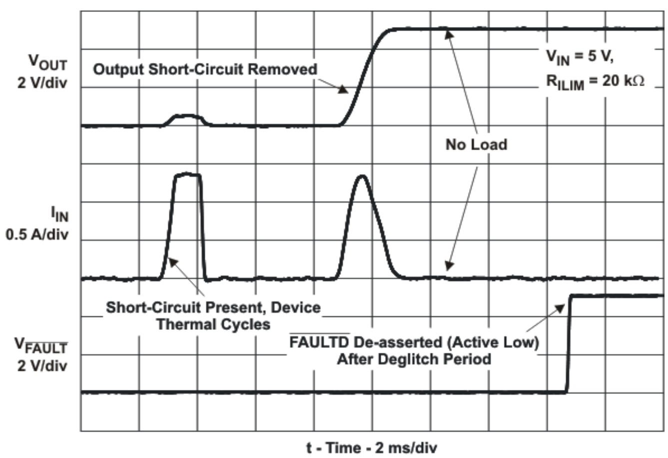



Figure 12. Short-Circuit to No-Load Recovery Response

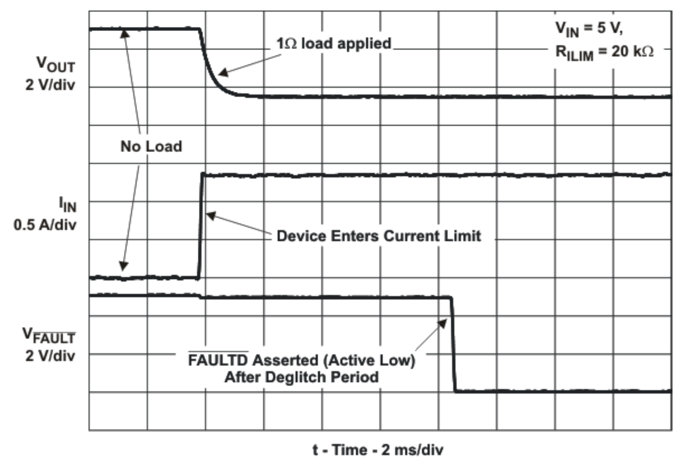



Figure 13. No Load to 1Ω Transient Response

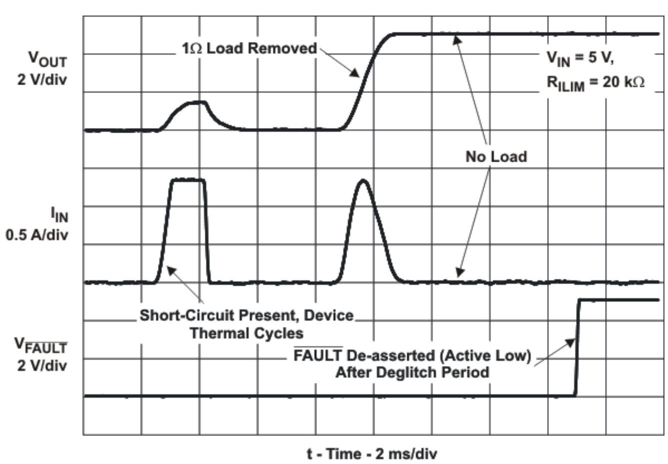



Figure 14. 1Ω to No Load Transient Response

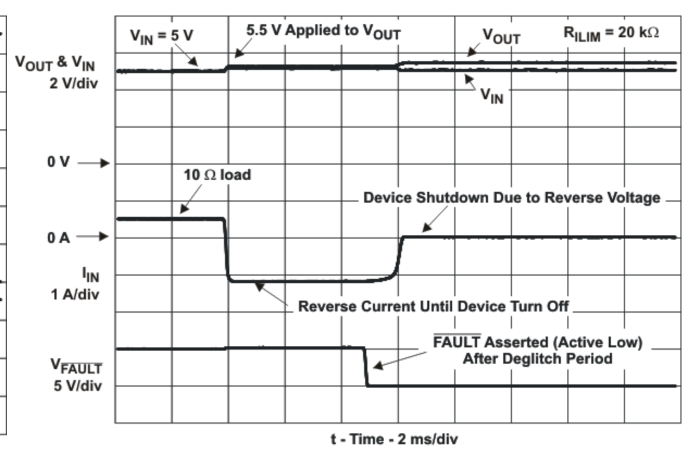



Figure 15. Reverse-Voltage Protection Response

## TYPICAL CHARACTERISTICS (continued)

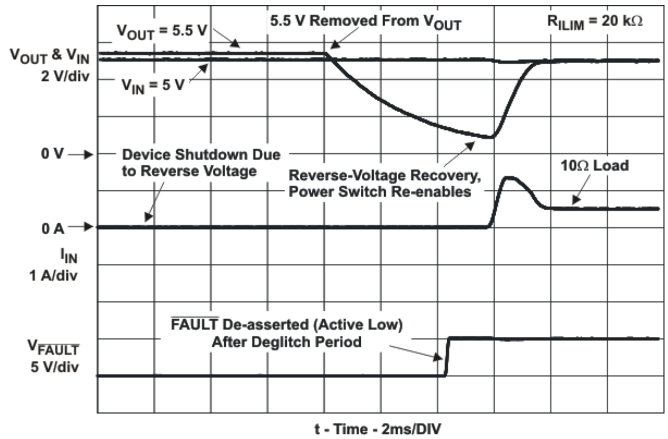



**Figure 16. Reverse-Voltage Protection Recovery**

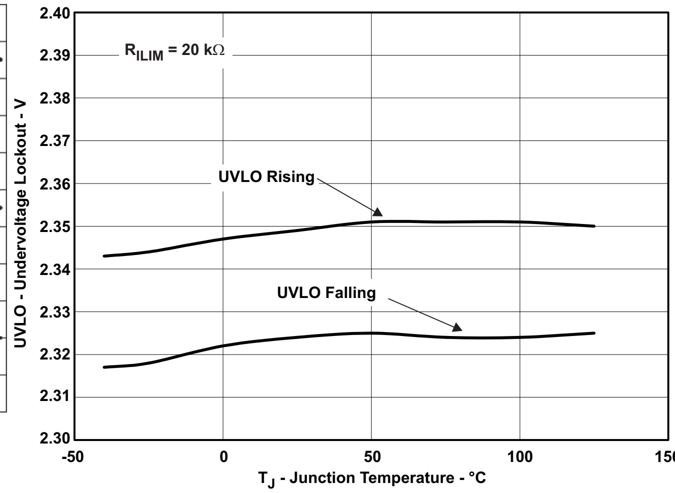



**Figure 17. UVLO – Undervoltage Lockout – V**

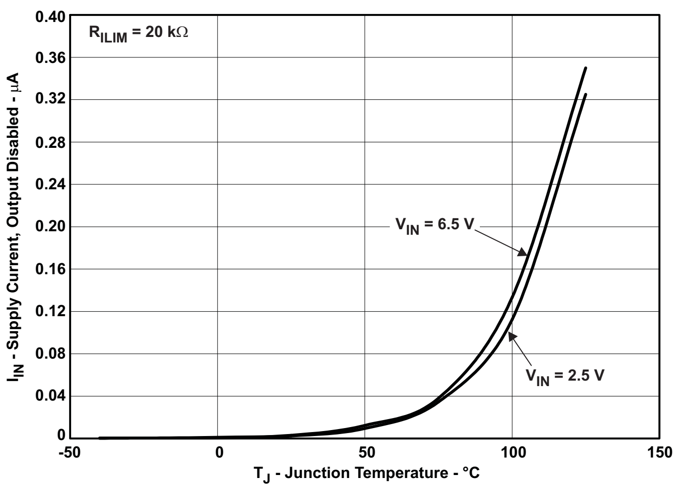



**Figure 18. $I_{IN}$ – Supply Current, Output Disabled – μA**

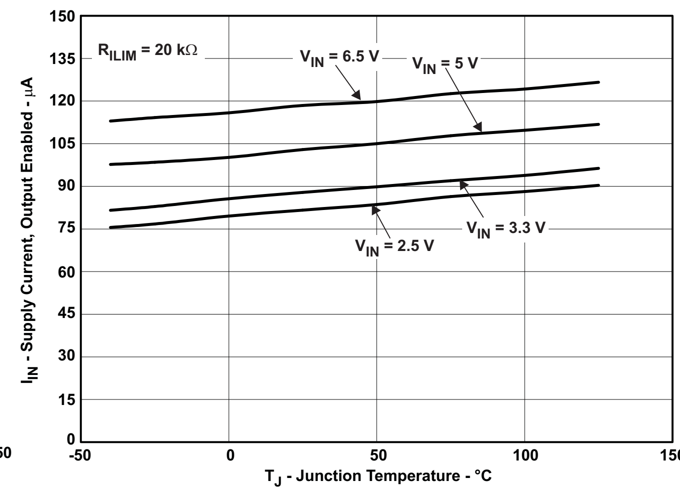



**Figure 19. $I_{IN}$ – Supply Current, Output Enabled – μA**

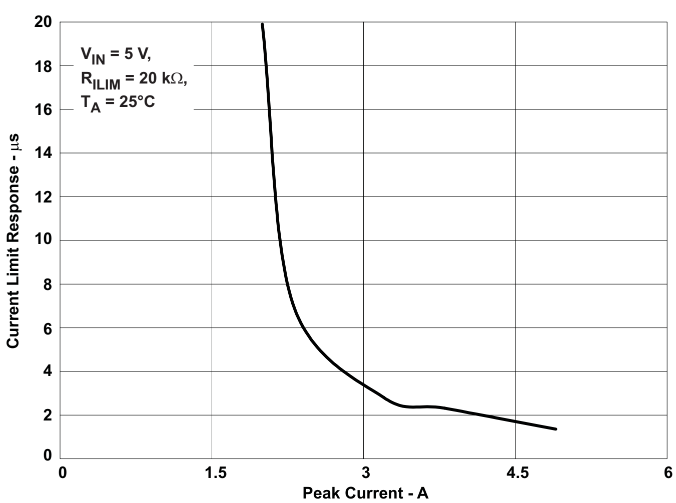



**Figure 20. current-limit Response – μs**

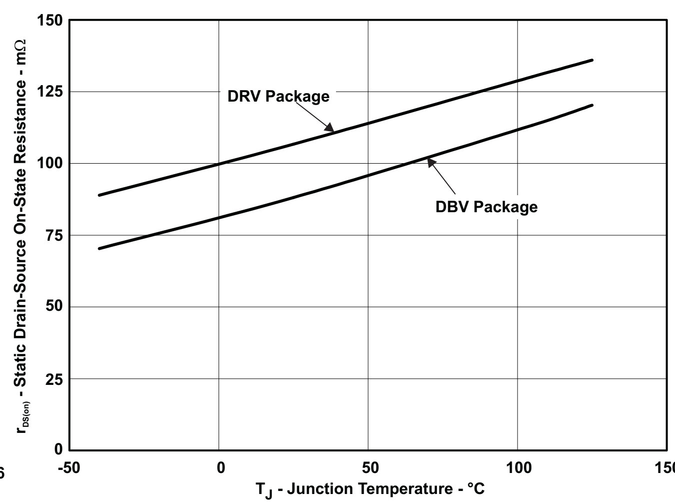



**Figure 21. MOSFET $r_{DS(on)}$ Vs. Junction Temperature**

## TYPICAL CHARACTERISTICS (continued)

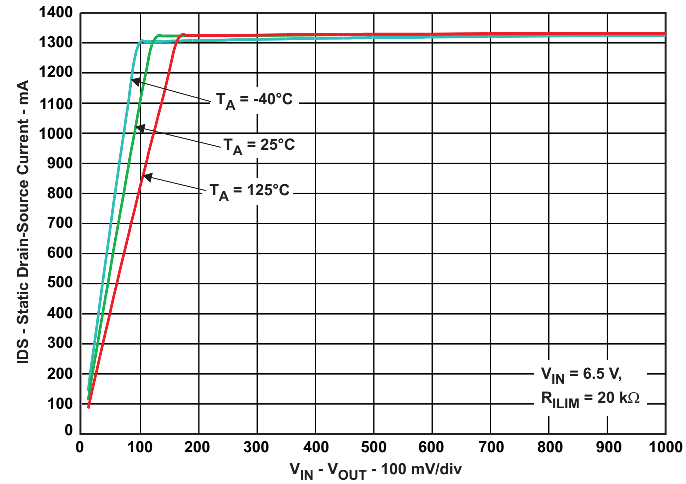



**Figure 22. Switch Current Vs. Drain-Source Voltage Across Switch**

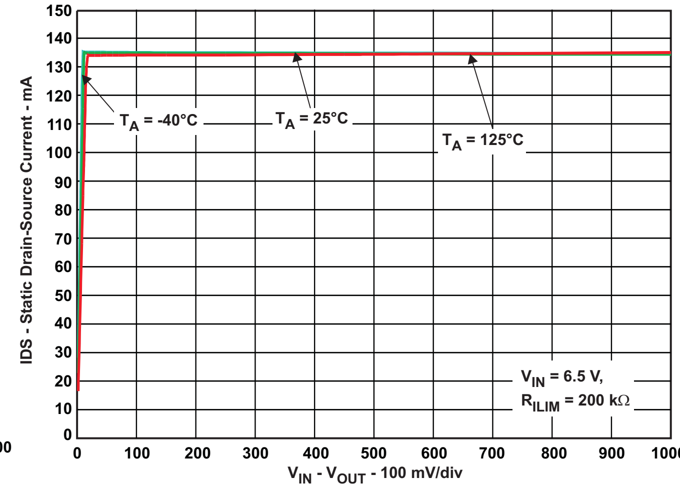



**Figure 23. Switch Current Vs. Drain-Source Voltage Across Switch**

# DETAILED DESCRIPTION

## OVERVIEW

The TPS2553-Q1 is current-limited. Power-distribution switches using N-channel MOSFETs for applications where short circuits or heavy capacitive loads will be encountered and provide up to 1.5 A of continuous load current. These devices allow the user to program the current-limit threshold between 75 mA and 1.7 A (typ) via an external resistor. Additional device shutdown features include overtemperature protection and reverse-voltage protection. The device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.5 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provides built-in soft-start functionality. The TPS2553-Q1 enters constant-current mode when the load exceeds the current-limit threshold.

## OVERCURRENT CONDITIONS

The TPS2553-Q1 responds to overcurrent conditions by limiting the output current to the $I_{OS}$ levels shown in Figure 24. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS2553-Q1 ramps the output current to $I_{OS}$. The TPS2553-Q1 device will limit the current to $I_{OS}$ until the overload condition is removed or the device begins to thermal cycle. The device will remain off until power is cycled or the device enable is toggled.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time $t_{IOS}$ (see Figure 3). The current-sense amplifier is overdriven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier recovers and limits the output current to $I_{OS}$. Similar to the previous case, the TPS2553-Q1 will limit the current to $I_{OS}$ until the overload condition is removed or the device begins to thermal cycle.

The TPS2553-Q1 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. The device turns off when the junction temperature exceeds 135°C (typ) while in current-limit. The device remains off until the junction temperature cools 10°C (typ) and then restarts. The TPS2553-Q1 cycles on/off until the overload is removed (see Figure 10 and Figure 12) .

## REVERSE-VOLTAGE PROTECTION

The reverse-voltage protection feature turns off the N-channel MOSFET whenever the output voltage exceeds the input voltage by 135 mV (typ) for 4-ms (typ).A reverse current of $(V_{OUT} – V_{IN})/r_{DS(on)}$) will be present when this occurs. This prevents damage to devices on the input side of the TPS2553-Q1 by preventing significant current from sinking into the input capacitance. The TPS2553-Q1 device allows the N-channel MOSFET to turn on once the output voltage goes below the input voltage for the same 4-ms deglitch time.

## $\overline{\text{FAULT}}$ RESPONSE

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an overcurrent, overtemperature or reverse-voltage condition. The TPS2553-Q1 asserts the $\overline{\text{FAULT}}$ signal until the fault condition is removed and the device resumes normal operation. The TPS2553-Q1 is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal delay "deglitch" circuit for overcurrent (7.5-ms typ) and reverse-voltage (4-ms typ) conditions without the need for external circuitry. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving fault conditions. Overtemperature conditions are not deglitched and assert the $\overline{\text{FAULT}}$ signal immediately.

## UNDERVOLTAGE LOCKOUT (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage drop from large current surges.

## ENABLE ($\overline{\text{EN}}$ OR EN)

The logic enable controls the power switch, bias for the charge pump, driver, and other circuits to reduce the supply current. The supply current is reduced to less than 1-μA when a logic high is present on $\overline{\text{EN}}$ or when a logic low is present on EN. A logic low input on $\overline{\text{EN}}$ or a logic high input on EN enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

## THERMAL SENSE

The TPS2553-Q1 has a self-protection feature using two independent thermal sensing circuits that monitor the operating temperature of the power switch. It disables the operation if the temperature exceeds recommended operating conditions. The TPS2553-Q1 device operates in constant-current mode during an overcurrent condition, which increases the voltage drop across the power-switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor turns off the power switch when the die temperature exceeds 135°C (min) and the part is in current-limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 10 °C.

The TPS2553-Q1 also has a second ambient thermal sensor. The ambient thermal sensor turns off the power-switch when the die temperature exceeds 155°C (min) regardless of whether the power switch is in current-limit and will turn on the power switch after the device has cooled approximately 10 °C. The TPS2553-Q1 continues to cycle off and on until the fault is removed.

The open-drain fault reporting output $\overline{\text{FAULT}}$ is asserted (active low) immediately during an overtemperature shutdown condition.

# APPLICATION INFORMATION

## INPUT AND OUTPUT CAPACITANCE

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.1μF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise de-coupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power-supply.

Placing a high-value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output.

## PROGRAMMING THE CURRENT-LIMIT THRESHOLD

The overcurrent threshold is user programmable via an external resistor. The TPS2553-Q1 uses an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for $R_{ILIM}$ is 15 kΩ ≤ $R_{ILIM}$ ≤ 232 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current-limit is above a certain current level or that the maximum current-limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for $R_{ILIM}$. The following equations and Figure 24 can be used to calculate the resulting overcurrent threshold for a given external resistor value ($R_{ILIM}$). Figure 24 includes current-limit tolerance due to variations caused by temperature and process. However, the equations do not account for tolerance due to external resistor variation, so it is important to account for this tolerance when selecting $R_{ILIM}$. The traces routing the $R_{ILIM}$ resistor to the TPS2553-Q1 should be as short as possible to reduce parasitic effects on the current-limit accuracy.

$R_{ILIM}$ can be selected to provide a current-limit threshold that occurs 1) above a minimum load current or 2) below a maximum load current.

To design above a minimum current-limit threshold, find the intersection of $R_{ILIM}$ and the maximum desired load current on the $I_{OS(min)}$ curve and choose a value of $R_{ILIM}$ below this value. Programming the current-limit above a minimum threshold is important to ensure start up into full load or heavy capacitive loads. The resulting maximum current-limit threshold is the intersection of the selected value of $R_{ILIM}$ and the $I_{OS(max)}$ curve.

To design below a maximum current-limit threshold, find the intersection of $R_{ILIM}$ and the maximum desired load current on the $I_{OS(max)}$ curve and choose a value of $R_{ILIM}$ above this value. Programming the current-limit below a maximum threshold is important to avoid current-limiting upstream power supplies causing the input voltage bus to droop. The resulting minimum current-limit threshold is the intersection of the selected value of $R_{ILIM}$ and the $I_{OS(min)}$ curve.

Current-Limit Threshold Equations ($I_{OS}$):

$$I_{OSmax}(mA) = \frac{22980V}{R_{ILIM}{}^{0.94} k\Omega}$$

$$I_{OSnom}(mA) = \frac{23950V}{R_{ILIM}{}^{0.977} k\Omega}$$

$$I_{OSmin}(mA) = \frac{25230V}{R_{ILIM}{}^{1.016} k\Omega} \quad (1)$$

where 15 kΩ ≤ $R_{ILIM}$ ≤ 232 kΩ.

While the maximum recommended value of RILIM is 232 kΩ, there is one additional configuration that allows for a lower current-limit threshold. The ILIM pin may be connected directly to IN to provide a 75 mA (typ) current-limit threshold. Additional low-ESR ceramic capacitance may be necessary from IN to GND in this configuration to prevent unwanted noise from coupling into the sensitive ILIM circuitry.

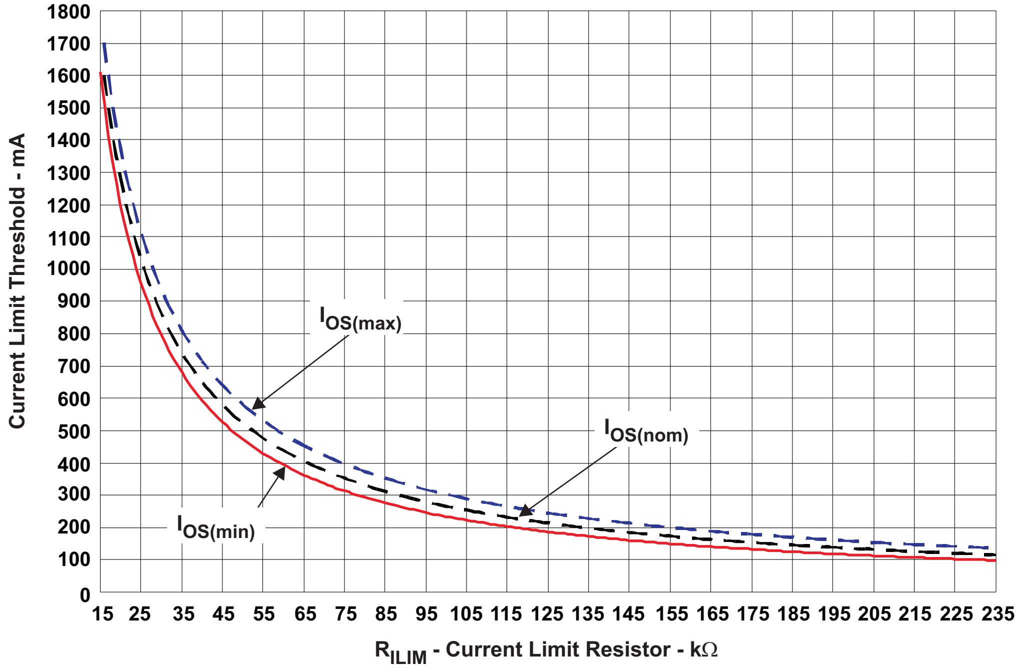



**Figure 24. Current-Limit Threshold vs $R_{ILIM}$**

## APPLICATION 1: DESIGNING ABOVE A MINIMUM current-limit

Some applications require that current-limiting cannot occur below a certain threshold. For this example, assume that 1 A must be delivered to the load so that the minimum desired current-limit threshold is 1000 mA. Use the $I_{OS}$ equations and Figure 24 to select $R_{ILIM}$.

$$I_{OSmin}(mA) = 1000mA$$
$$I_{OSmin}(mA) = \frac{25230V}{R_{ILIM}^{1.016}k\Omega}$$
$$R_{ILIM}(k\Omega) = \left(\frac{25230V}{I_{OSmin}mA}\right)^{\frac{1}{1.016}}$$
$$R_{ILIM}(k\Omega) = 24k\Omega \quad (2)$$

Select the closest 1% resistor less than the calculated value: $R_{ILIM}$ = 23.7 kΩ. This sets the minimum current-limit threshold at 1 A . Use the $I_{OS}$ equations, Figure 24, and the previously calculated value for $R_{ILIM}$ to calculate the maximum resulting current-limit threshold.

$$R_{ILIM}(k\Omega) = 23.7k\Omega$$
$$I_{OSmax}(mA) = \frac{22980V}{R_{ILIM}^{0.94}k\Omega}$$
$$I_{OSmax}(mA) = \frac{22980V}{23.7^{0.94}k\Omega}$$
$$I_{OSmax}(mA) = 1172.4mA \quad (3)$$

The resulting maximum current-limit threshold is 1172.4 mA with a 23.7 kΩ resistor.

## APPLICATION 2: DESIGNING BELOW A MAXIMUM current-limit

Some applications require that current-limiting must occur below a certain threshold. For this example, assume that the desired upper current-limit threshold must be below 500 mA to protect an up-stream power supply. Use the $I_{OS}$ equations and Figure 24 to select $R_{ILIM}$.

$$I_{OSmax}(mA) = 500mA$$
$$I_{OSmax}(mA) = \frac{22980V}{R_{ILIM}^{0.94}k\Omega}$$
$$R_{ILIM}(k\Omega) = \left(\frac{22980V}{I_{OSmax}mA}\right)^{\frac{1}{0.94}}$$
$$R_{ILIM}(k\Omega) = 58.7k\Omega \quad (4)$$

Select the closest 1% resistor greater than the calculated value: $R_{ILIM}$ = 59 kΩ. This sets the maximum current-limit threshold at 500 mA . Use the $I_{OS}$ equations, Figure 24, and the previously calculated value for $R_{ILIM}$ to calculate the minimum resulting current-limit threshold.

$$R_{ILIM}(k\Omega) = 59k\Omega$$
$$I_{OSmin}(mA) = \frac{25230V}{R_{ILIM}^{1.016}k\Omega}$$
$$I_{OSmin}(mA) = \frac{25230V}{59^{1.016}k\Omega}$$
$$I_{OSmin}(mA) = 400.6mA \quad (5)$$

The resulting minimum current-limit threshold is 400.6 mA with a 59 kΩ resistor.

## ACCOUNTING FOR RESISTOR TOLERANCE

The previous sections described the selection of $R_{ILIM}$ given certain application requirements and the importance of understanding the current-limit threshold tolerance. The analysis focused only on the TPS2553-Q1 performance and assumed an exact resistor value. However, resistors sold in quantity are not exact and are bounded by an upper and lower tolerance centered around a nominal resistance. The additional $R_{ILIM}$ resistance tolerance directly affects the current-limit threshold accuracy at a system level. The following table shows a process that accounts for worst-case resistor tolerance assuming 1% resistor values. Step one follows the selection process outlined in the application examples above. Step two determines the upper and lower resistance bounds of the selected resistor. Step three uses the upper and lower resistor bounds in the $I_{OS}$ equations to calculate the threshold limits. It is important to use tighter tolerance resistors, e.g. 0.5% or 0.1%, when precision current-limiting is desired.

**Table 1. Common $R_{ILIM}$ Resistor Selections**

| Desired Nominal current-limit (mA) | | Ideal Resistor (kΩ) | Closest 1% Resistor (kΩ) | Resistor Tolerance | | | Actual Limits | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | 1% low (kΩ) | 1% high (kΩ) | | IOS MIN (mA) | IOS Nom (mA) | IOS MAX (mA) |
| 75 | | SHORT ILIM to IN | | | | | 50.0 | 75.0 | 100.0 |
| 120 | | 226.1 | 226 | 223.7 | 228.3 | | 101.3 | 120.0 | 142.1 |
| 200 | | 134.0 | 133 | 131.7 | 134.3 | | 173.7 | 201.5 | 233.9 |
| 300 | | 88.5 | 88.7 | 87.8 | 89.6 | | 262.1 | 299.4 | 342.3 |
| 400 | | 65.9 | 66.5 | 65.8 | 67.2 | | 351.2 | 396.7 | 448.7 |
| 500 | | 52.5 | 52.3 | 51.8 | 52.8 | | 448.3 | 501.6 | 562.4 |
| 600 | | 43.5 | 43.2 | 42.8 | 43.6 | | 544.3 | 604.6 | 673.1 |
| 700 | | 37.2 | 37.4 | 37.0 | 37.8 | | 630.2 | 696.0 | 770.8 |
| 800 | | 32.4 | 32.4 | 32.1 | 32.7 | | 729.1 | 800.8 | 882.1 |
| 900 | | 28.7 | 28.7 | 28.4 | 29.0 | | 824.7 | 901.5 | 988.7 |
| 1000 | | 25.8 | 26.1 | 25.8 | 26.4 | | 908.3 | 989.1 | 1081.0 |
| 1100 | | 23.4 | 23.2 | 23.0 | 23.4 | | 1023.7 | 1109.7 | 1207.5 |
| 1200 | | 21.4 | 21.5 | 21.3 | 21.7 | | 1106.0 | 1195.4 | 1297.1 |
| 1300 | | 19.7 | 19.6 | 19.4 | 19.8 | | 1215.1 | 1308.5 | 1414.9 |
| 1400 | | 18.3 | 18.2 | 18.0 | 18.4 | | 1310.1 | 1406.7 | 1517.0 |
| 1500 | | 17.0 | 16.9 | 16.7 | 17.1 | | 1412.5 | 1512.4 | 1626.4 |
| 1600 | | 16.0 | 15.8 | 15.6 | 16.0 | | 1512.5 | 1615.2 | 1732.7 |
| 1700 | | 15.0 | 15.0 | 14.9 | 15.2 | | 1594.5 | 1699.3 | 1819.4 |

## CONSTANT-CURRENT VS. LATCH-OFF OPERATION AND IMPACT ON OUTPUT VOLTAGE

During normal operation the constant-current device (TPS2553-Q1) has a load current that is less than the current-limit threshold and the device is not limiting current. During normal operation the N-channel MOSFET is fully enhanced, and $V_{OUT} = V_{IN} - (I_{OUT} \times r_{DS(on)})$. The voltage drop across the MOSFET is relatively small compared to $V_{IN}$, and $V_{OUT} \not\approx V_{IN}$.

During the initial onset of an overcurrent event, the constant-current device (TPS2553-Q1) limits current to the programmed current-limit threshold set by $R_{ILIM}$ by operating the N-channel MOSFET in the linear mode. During current-limit operation, the N-channel MOSFET is no longer fully-enhanced and the resistance of the device increases. This allows the device to effectively regulate the current to the current-limit threshold. The effect of increasing the resistance of the MOSFET is that the voltage drop across the device is no longer negligible ($V_{IN} \neq V_{OUT}$), and $V_{OUT}$ decreases. The amount that $V_{OUT}$ decreases is proportional to the magnitude of the overload condition. The expected $V_{OUT}$ can be calculated by $I_{OS} \times R_{LOAD}$, where $I_{OS}$ is the current-limit threshold and $R_{LOAD}$ is the magnitude of the overload condition. For example, if $I_{OS}$ is programmed to 1 A and a 1 Ω overload condition is applied, the resulting $V_{OUT}$ is 1 V.

The constant-current device (TPS2553-Q1) operates during the initial onset of an overcurrent event, if the overcurrent event lasts longer than the internal delay "deglitch" circuit (7.5-ms typ). The constant-current device (TPS2553-Q1) asserts the $\overline{FAULT}$ flag after the deglitch period and continues to regulate the current to the current-limit threshold indefinitely. In practical circuits, the power dissipation in the package will increase the die temperature above the overtemperature shutdown threshold (135°C min), and the device will turn off until the die temperature decreases by the hysteresis of the thermal shutdown circuit (10°C typ). The device will turn on and continue to thermal cycle until the overload condition is removed. The constant-current devices resume normal operation once the overload condition is removed.

## POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated by:

$$P_D = r_{DS(on)} \times I_{OUT}{}^2$$

Where:

$P_D$ = Total power dissipation (W)

$r_{DS(on)}$ = Power switch on-resistance (Ω)

$I_{OUT}$ = Maximum current-limit threshold (A)

This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature:

$$T_J = P_D \times \theta_{JA} + T_A$$

Where:

$T_A$ = Ambient temperature (°C)

$\theta_{JA}$ = Thermal resistance (°C/W)

$P_D$ = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined" $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance $\theta_{JA}$, and thermal resistance is highly dependent on the individual package and board layout. The Thermal Information Table provides example thermal resistance for specific packages and board layouts.

## UNIVERSAL SERIAL BUS (USB) POWER-DISTRIBUTION REQUIREMENTS

One application for this device is for current-limiting in universal serial bus (USB) applications. The original USB interface was a 12-Mb/s or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). As the demand for more bandwidth increased, the USB 2.0 standard was introduced increasing the maximum data rate to 480-Mb/s. The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply. The USB specification classifies two different classes of devices depending on its maximum current draw. A device classified as low-power can draw up to 100 mA as defined by the standard. A device classified as high-power can draw up to 500 mA. It is important that the minimum current-limit threshold of the current-limiting power-switch exceed the maximum current-limit draw of the intended application. The latest USB standard should always be referenced when considering the current-limit threshold

The USB specification defines two types of devices as hubs and functions. A USB hub is a device that contains multiple ports for different USB devices to connect and can be self-powered (SPH) or bus-powered (BPH). A function is a USB device that is able to transmit or receive data or control information over the bus. A USB function can be embedded in a USB hub. A USB function can be one of three types included in the list below.

- Low-power, bus-powered function
- High-power, bus-powered function
- Self-powered function

SPHs and BPHs distribute data and power to downstream functions. The TPS2553-Q1 has higher current capability than required for a single USB port allowing it to power multiple downstream ports.

## SELF-POWERED AND BUS-POWERED HUBS

A SPH has a local power supply that powers embedded functions and downstream ports. This power supply must provide between 4.75 V to 5.25 V to downstream facing devices under full-load and no-load conditions. SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

A BPH obtains all power from an upstream port and often contains an embedded function. It must power up with less than 100 mA. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This is accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than 100 mA. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

## LOW-POWER BUS-POWERED AND HIGH-POWER BUS-POWERED FUNCTIONS

Both low-power and high-power bus-powered functions obtain all power from upstream ports. Low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 μF at power up, the device must implement inrush current-limiting.

## USB POWER-DISTRIBUTION REQUIREMENTS

USB can be implemented in several ways regardless of the type of USB device being developed. Several power-distribution features must be implemented.

- SPHs must:
  – current-limit downstream ports
  – Report overcurrent conditions
- BPHs must:
  – Enable/disable power to downstream ports
  – Power up at <100 mA
  – Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  – Limit inrush currents
  – Power up at <100 mA

The feature set of the TPS2553-Q1 meets each of these requirements. The integrated current-limiting and overcurrent reporting is required by self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs and the input ports for bus-powered functions.

## AUTO-RETRY FUNCTIONALITY

Some applications require that an overcurrent condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This *auto-retry* functionality can be implemented with an external resistor and capacitor. During a fault condition, $\overline{\text{FAULT}}$ pulls low disabling the part. The part is disabled when EN is pulled low, and $\overline{\text{FAULT}}$ goes high impedance allowing $C_{RETRY}$ to begin charging. The part re-enables when the voltage on EN reaches the turnon threshold, and the auto-retry time is determined by the resistor/capacitor time constant. The part will continue to cycle in this manner until the fault condition is removed.

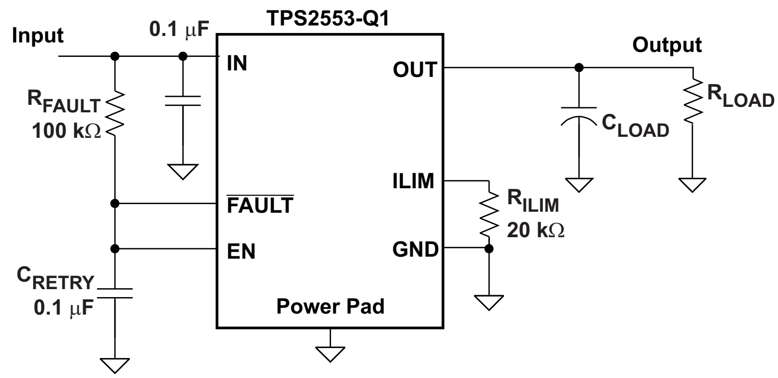



**Figure 25. Auto-Retry Functionality**

Some applications require auto-retry functionality and the ability to enable/disable with an external logic signal. The figure below shows how an external logic signal can drive EN through $R_{FAULT}$ and maintain auto-retry functionality. The resistor/capacitor time constant determines the auto-retry time-out period.

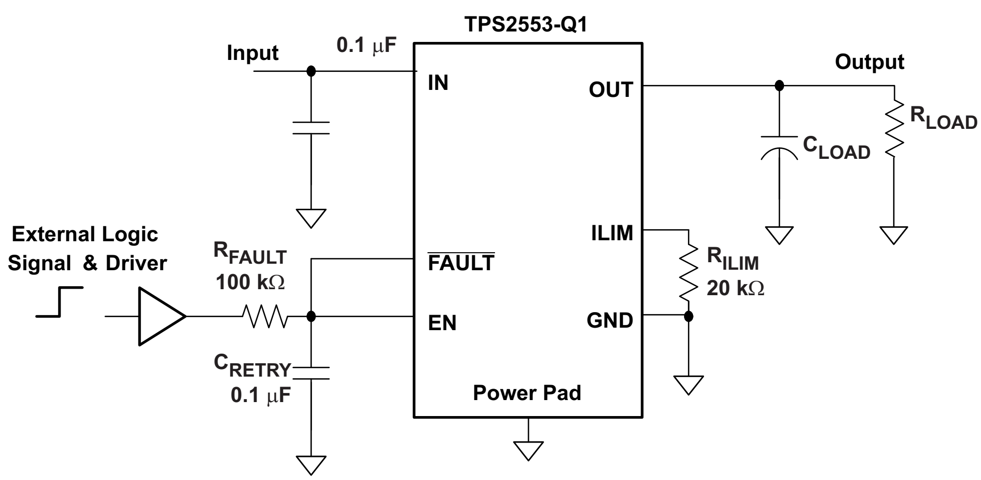



**Figure 26. Auto-Retry Functionality With External EN Signal**

## TWO-LEVEL CURRENT-LIMIT CIRCUIT

Some applications require different current-limit thresholds depending on external system conditions. Figure 27 shows an implementation for an externally controlled, two-level current-limit circuit. The current-limit threshold is set by the total resistance from ILIM to GND (see the Programming the Current-Limit Threshold section). A logic-level input enables/disables MOSFET Q1 and changes the current-limit threshold by modifying the total resistance from ILIM to GND. Additional MOSFET/resistor combinations can be used in parallel to Q1/R2 to increase the number of additional current-limit levels.

**NOTE**

ILIM should never be driven directly with an external signal.

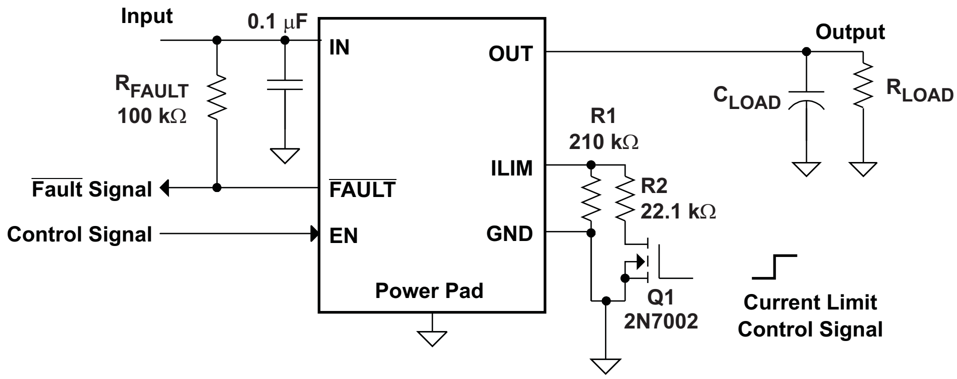



**Figure 27. Two-Level Current-Limit Circuit**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2553QDBVRQ1 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | PYEQ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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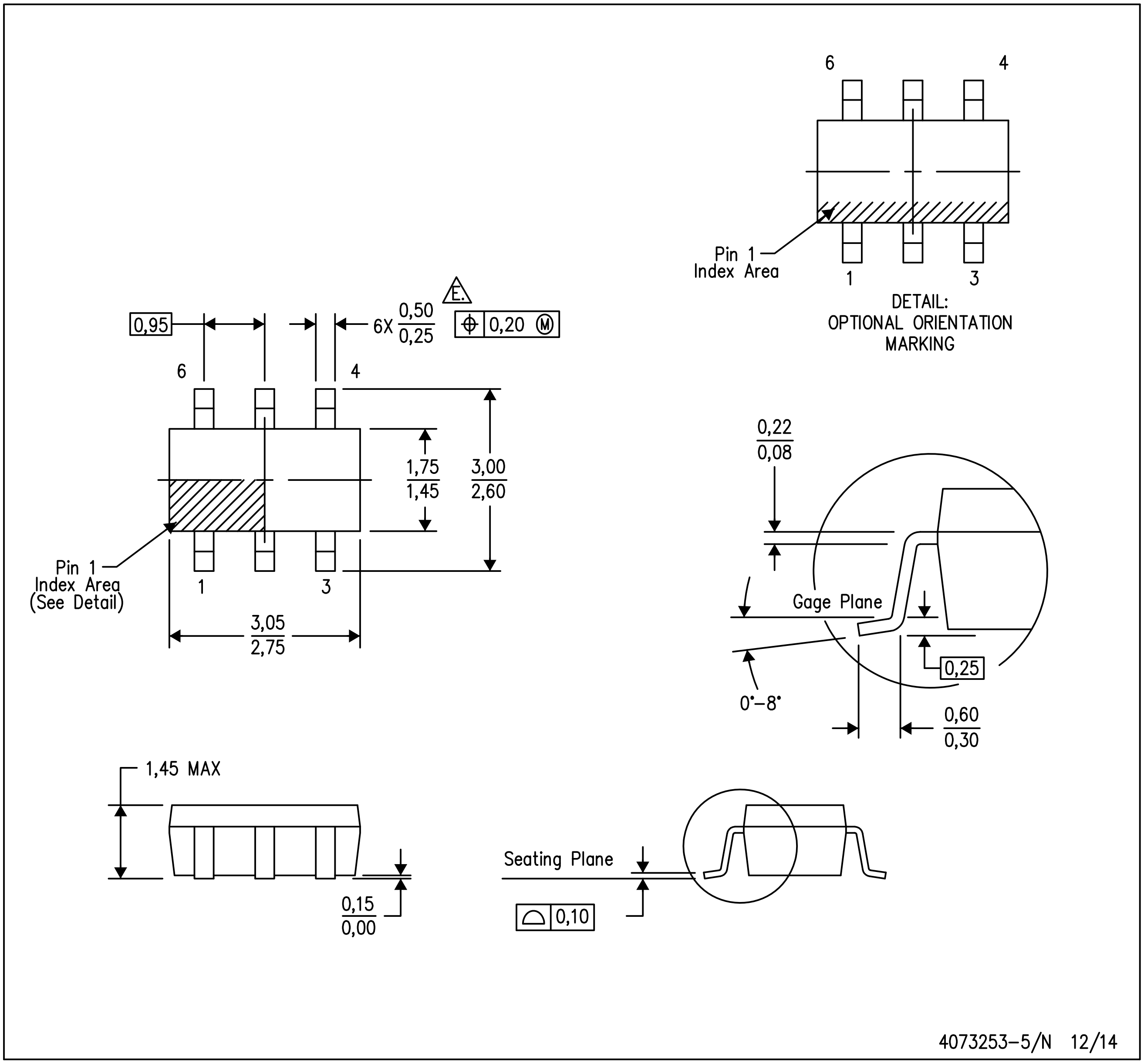
**OTHER QUALIFIED VERSIONS OF TPS2553-Q1 :**

- Catalog: TPS2553

NOTE: Qualified Version Definitions:

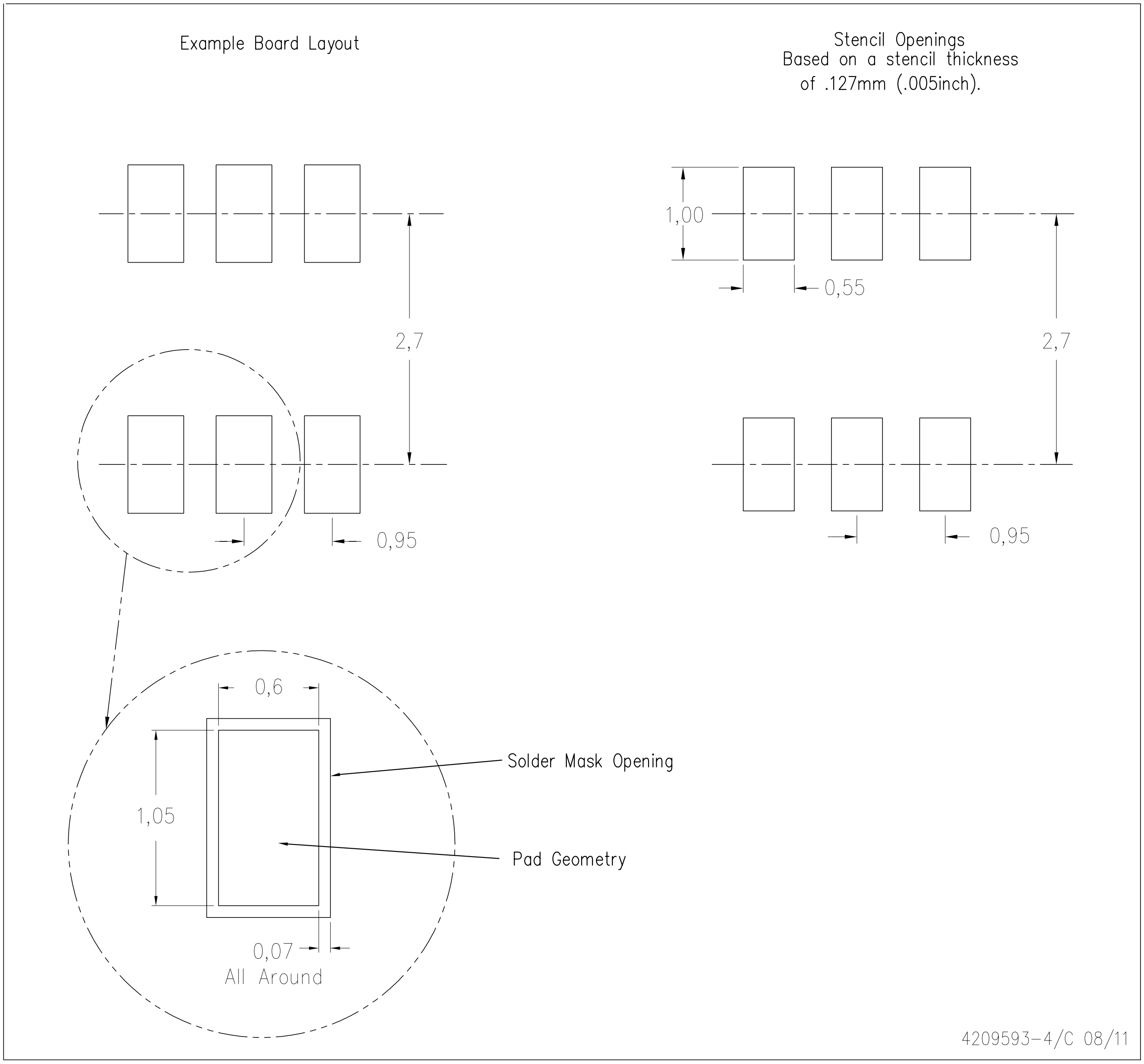
- Catalog - TI's standard catalog product

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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