

## TPS6217x 采用 DCS-Control™ 拓扑的 3V 至 17V、0.5A、降压转换器

### 1 特性

- DCS-Control™ 拓扑
- 输入电压范围为 3V 至 17V
- 输出电流高达 500mA
- 可调输出电压范围为 0.9V 至 6V
- 固定输出电压版本
- 无缝省电模式转换
- 静态电流典型值为 17 $\mu$ A
- 电源正常输出
- 100% 占空比模式
- 短路保护
- 过温保护
- 与 TPS62160 和 TPS62125 引脚兼容
- 采用 2mm x 2mm、8 引脚晶圆级小外形无引线 (WSON) 封装

### 2 应用

- 标准 12V 导轨式电源
- 单一或者多个锂离子电池供电的负载点 (POL) 电源
- 低压差稳压器 (LDO) 替代产品
- 嵌入式系统
- 数码相机、数码摄像机
- 移动电脑、平板电脑、调制解调器

### 3 说明

TPS6217x 器件系列是易于使用的同步降压 DC-DC 转换器，针对高功率密度的应用进行了优化。该系列器件的开关频率典型值高达 2.25MHz，允许使用小型电感器，通过利用 DCS-Control™ 拓扑技术提供快速瞬态响应并实现高输出电压精度。

该系列器件具有 3V 至 17V 宽运行输入电压范围，非常适用于由锂离子或其他电池以及 12V 中间电源轨供电的系统。其输出电压为 0.9V 至 6V，支持高达 0.5A 的持续输出电流（使用 100% 占空比模式）。

此外，还可以通过配置使能引脚和开漏电源正常状态引脚实现电源排序。

在节能模式下，器件可根据输入电压 (VIN) 生成约 17 $\mu$ A 的静态电流。负载较小时可自动且无缝进入节能模式，同时该模式可保持整个负载范围内的高效率。该器件在关断模式下处于关断状态，期间的流耗低于 2 $\mu$ A。

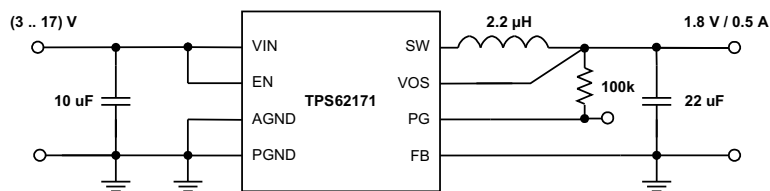
TPS6217x 器件在自然通风环境下的额定工作温度范围为 -40°C 至 85°C。此类器件划分为可调节和固定输出电压两种版本。该系列器件采用 2mm x 2mm、8 引脚 WSON 封装 (DSG)。

#### 器件信息(1)

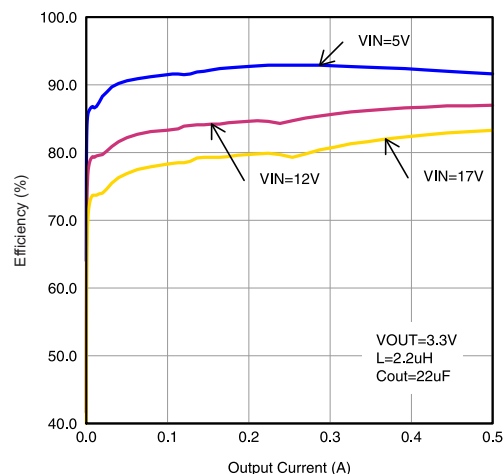
器件型号	封装	封装尺寸 (标称值)
TPS6217x	WSON (8)	2.00mm x 2.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路原理图



效率与输出电流间的关系



## 目录

<b>1</b>	特性 .....	<b>1</b>	<b>9</b>	<b>Application and Implementation</b> .....	<b>11</b>
<b>2</b>	应用 .....	<b>1</b>	9.1	Application Information.....	11
<b>3</b>	说明 .....	<b>1</b>	9.2	Typical Application .....	11
<b>4</b>	修订历史记录 .....	<b>2</b>	9.3	System Examples .....	19
<b>5</b>	<b>Voltage Options</b> .....	<b>3</b>	<b>10</b>	<b>Power Supply Recommendations</b> .....	<b>22</b>
<b>6</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	<b>11</b>	<b>Layout</b> .....	<b>23</b>
<b>7</b>	<b>Specifications</b> .....	<b>4</b>	11.1	Layout Guidelines .....	23
7.1	Absolute Maximum Ratings .....	4	11.2	Layout Example .....	23
7.2	ESD Ratings.....	4	11.3	Thermal Considerations .....	24
7.3	Recommended Operating Conditions.....	4	<b>12</b>	<b>器件和文档支持</b> .....	<b>25</b>
7.4	Thermal Information .....	4	12.1	器件支持 .....	25
7.5	Electrical Characteristics.....	5	12.2	文档支持 .....	25
7.6	Typical Characteristics .....	6	12.3	相关链接 .....	25
<b>8</b>	<b>Detailed Description</b> .....	<b>7</b>	12.4	社区资源 .....	25
8.1	Overview .....	7	12.5	商标 .....	25
8.2	Functional Block Diagram .....	7	12.6	静电放电警告 .....	25
8.3	Feature Description.....	8	12.7	Glossary .....	26
8.4	Device Functional Modes.....	9	<b>13</b>	<b>机械、封装和可订购信息</b> .....	<b>26</b>

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

<b>Changes from Revision C (August 2013) to Revision D</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>已添加 引脚配置和功能部分, ESD 额定值表, 特性 描述 部分, 器件功能模式, 应用和 实施部分, 电源相关建议部 分, 布局部分, 器件和文档支持部分以及机械、封装和可订购信息部分 .....</li> </ul>	1

<b>Changes from Revision B (August 2013) to Revision C</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Changed 50mV/μs to 50mV/s in Enable and Shutdown (EN) section .....</li> </ul>	8

<b>Changes from Revision A (April 2012) to Revision B</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Added diode to <a href="#">Figure 41</a> .....</li> </ul>	22

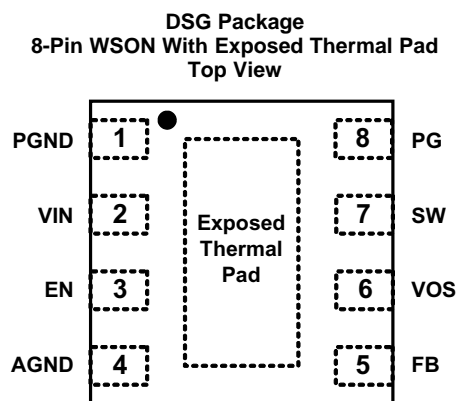
<b>Changes from Original (November 2011) to Revision A</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Changed <a href="#">Table 1</a> .....</li> </ul>	12

## 5 Voltage Options

OUTPUT VOLTAGE	PART NUMBER <sup>(1)</sup>	PACKAGE
adjustable	TPS62170	WSON (8)
1.8 V	TPS62171	
3.3 V	TPS62172	
5.0 V	TPS62173	

(1) Contact the factory to check availability of other fixed output voltage versions.

## 6 Pin Configuration and Functions



### Pin Functions

PIN <sup>(1)</sup>		I/O	DESCRIPTION
NAME	NO.		
PGND	1	—	Power ground
VIN	2	IN	Supply voltage
EN	3	IN	Enable input (High = enabled, Low = disabled)
AGND	4	—	Analog ground
FB	5	IN	Voltage feedback of adjustable version. Connect resistive voltage divider to this pin. It is recommended to connect FB to AGND on fixed output voltage versions for improved thermal performance.
VOS	6	IN	Output voltage sense pin and connection for the control loop circuitry.
SW	7	OUT	Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.
PG	8	OUT	Output power good (High = VOUT ready, Low = VOUT below nominal regulation); open drain (requires pull-up resistor; goes high impedance, when device is switched off)
Exposed Thermal Pad		—	Must be connected to AGND. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see [Detailed Description](#) and [Application Information](#) sections.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Pin voltage range <sup>(2)</sup>	V <sub>IN</sub>	-0.3	20	V
	EN, SW	-0.3	V <sub>IN</sub> + 0.3	V
	FB, PG, VOS	-0.3	7	V
Power good sink current	PG		10	mA
Operating junction temperature, T <sub>J</sub>		-40	125	°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground terminal.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage, V <sub>IN</sub>	3		17	V
Operating free air temperature, T <sub>A</sub>	-40		85	°C
Operating junction temperature, T <sub>J</sub>	-40		125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS6217x	UNIT
		DSG (WSON)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	61.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	61.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	15.5	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	15.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	8.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/zip/Spra953).

## 7.5 Electrical Characteristics

Over free-air temperature range ( $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ), typical values at  $V_{IN} = 12\text{ V}$  and  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
$V_{IN}$	Input voltage range <sup>(1)</sup>		3		17	V
$I_Q$	Operating quiescent current	EN = High, $I_{OUT} = 0\text{ mA}$ , device not switching		17	25	$\mu\text{A}$
$I_{SD}$	Shutdown current <sup>(2)</sup>	EN = Low		1.5	4	$\mu\text{A}$
$V_{UVLO}$	Undervoltage lockout threshold	Falling input voltage	2.6	2.7	2.82	V
		Hysteresis		180		mV
$T_{SD}$	Thermal shutdown temperature	rising temperature		160		$^{\circ}\text{C}$
	Thermal shutdown hysteresis	falling temperature		20		
<b>CONTROL (EN, PG)</b>						
$V_{EN\_H}$	High level input threshold voltage (EN)		0.9	0.6		V
$V_{EN\_L}$	Low level input threshold voltage (EN)			0.56	0.3	V
$I_{LKG\_EN}$	Input leakage current (EN)	EN = $V_{IN}$ or GND		0.01	1	$\mu\text{A}$
$V_{TH\_PG}$	Power good threshold voltage	Rising (% $V_{OUT}$ )	92%	95%	98%	
		Falling (% $V_{OUT}$ )	87%	90%	93%	
$V_{OL\_PG}$	Power good output low voltage	$I_{PG} = -2\text{ mA}$		0.07	0.3	V
$I_{LKG\_PG}$	Input leakage current (PG)	$V_{PG} = 1.8\text{ V}$		1	400	nA
<b>POWER SWITCH</b>						
$R_{DS(ON)}$	High-side MOSFET ON-resistance	$V_{IN} \geq 6\text{ V}$		300	600	m $\Omega$
		$V_{IN} = 3\text{ V}$		430		
	Low-side MOSFET ON-resistance	$V_{IN} \geq 6\text{ V}$		120	200	m $\Omega$
		$V_{IN} = 3\text{ V}$		165		
$I_{LIMF}$	High-side MOSFET forward current limit <sup>(3)</sup>	$V_{IN} = 12\text{ V}$ , $T_A = 25^{\circ}\text{C}$	0.85	1.05	1.35	A
<b>OUTPUT</b>						
$V_{REF}$	Internal reference voltage <sup>(4)</sup>			0.8		V
$I_{LKG\_FB}$	Pin leakage current (FB)	TPS62170, $V_{FB} = 1.2\text{ V}$		5	400	nA
$V_{OUT}$	Output voltage range (TPS62170)	$V_{IN} \geq V_{OUT}$	0.9		6.0	V
	Initial output voltage accuracy <sup>(5)</sup>	PWM mode operation, $V_{IN} \geq V_{OUT} + 1\text{ V}$	-3%		3%	
		Power save mode operation, $C_{OUT} = 22\text{ }\mu\text{F}$	-3.5%		4%	
	DC output voltage load regulation	$V_{IN} = 12\text{ V}$ , $V_{OUT} = 3.3\text{ V}$ , PWM mode operation		0.05		
DC output voltage line regulation	$3\text{ V} \leq V_{IN} \leq 17\text{ V}$ , $V_{OUT} = 3.3\text{ V}$ , $I_{OUT} = 0.5\text{ A}$ , PWM mode operation		0.02			%/V

(1) The device is still functional down to under voltage lockout (see parameter  $V_{UVLO}$ ).

(2) Current into VIN pin.

(3) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see [Current Limit and Short Circuit Protection](#)).

(4) This is the voltage regulated at the FB pin.

(5) This is the accuracy provided by the device itself (line and load regulation effects are not included). For fixed voltage versions, the (internal) resistive feedback divider is included.

## 7.6 Typical Characteristics

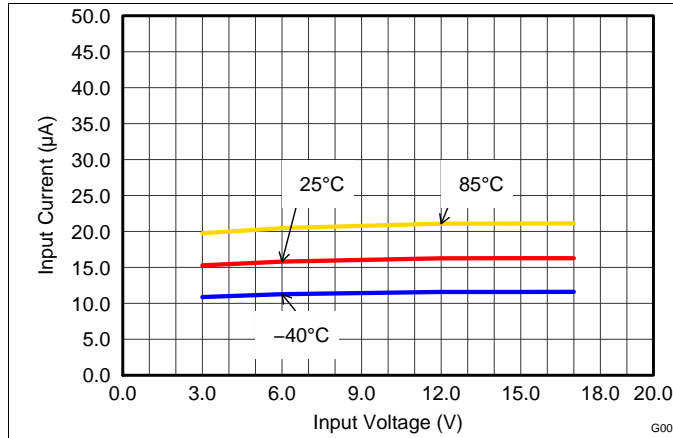


Figure 1. Quiescent Current

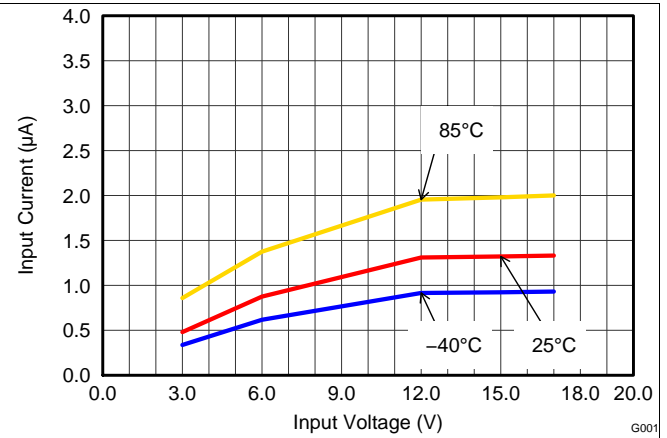


Figure 2. Shutdown Current

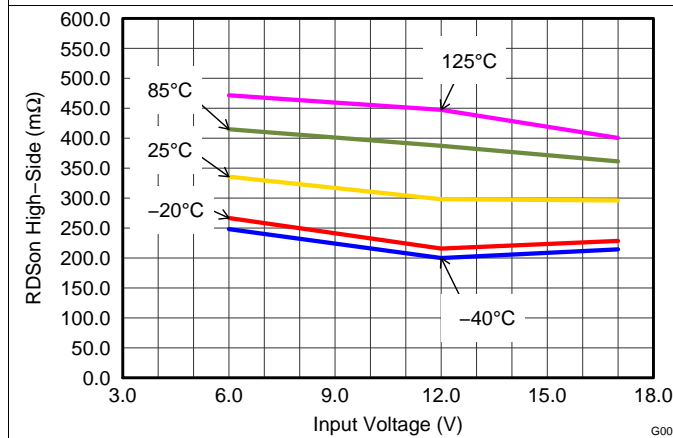


Figure 3. High-Side Switch

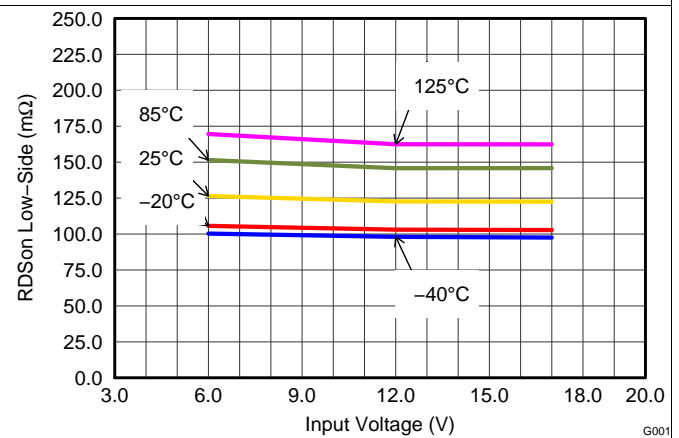


Figure 4. Low-Side Switch

## 8 Detailed Description

### 8.1 Overview

The TPS6217x synchronous step-down DC-DC converters are based on DCS-Control™ (Direct Control with Seamless transition into power save mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports pulse width modulation (PWM) mode for medium and heavy load conditions and a power save mode at light loads. During PWM mode, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.25 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters power save mode to sustain high efficiency down to very light loads. In power save mode, the switching frequency decreases linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to power save mode is seamless without effects on the output voltage.

Fixed output voltage versions provide smallest solution size and lowest current consumption, requiring only 3 external components. An internal current limit supports nominal output currents of up to 500 mA.

The TPS6217x family offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

### 8.2 Functional Block Diagram

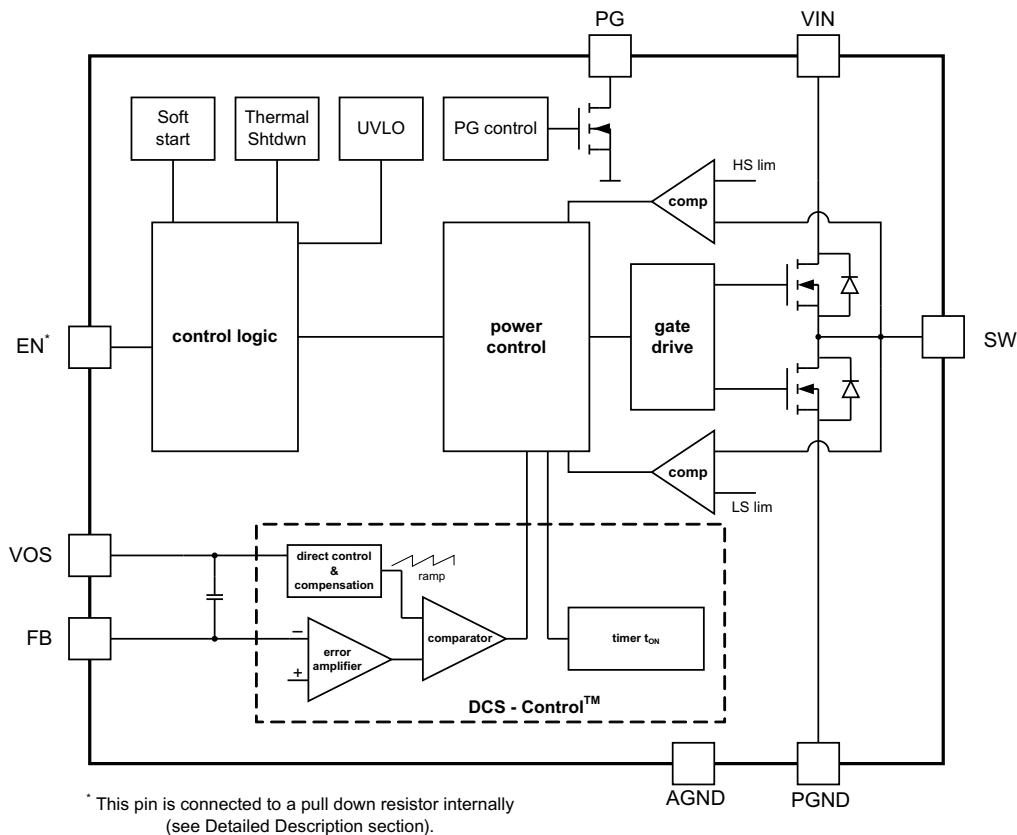
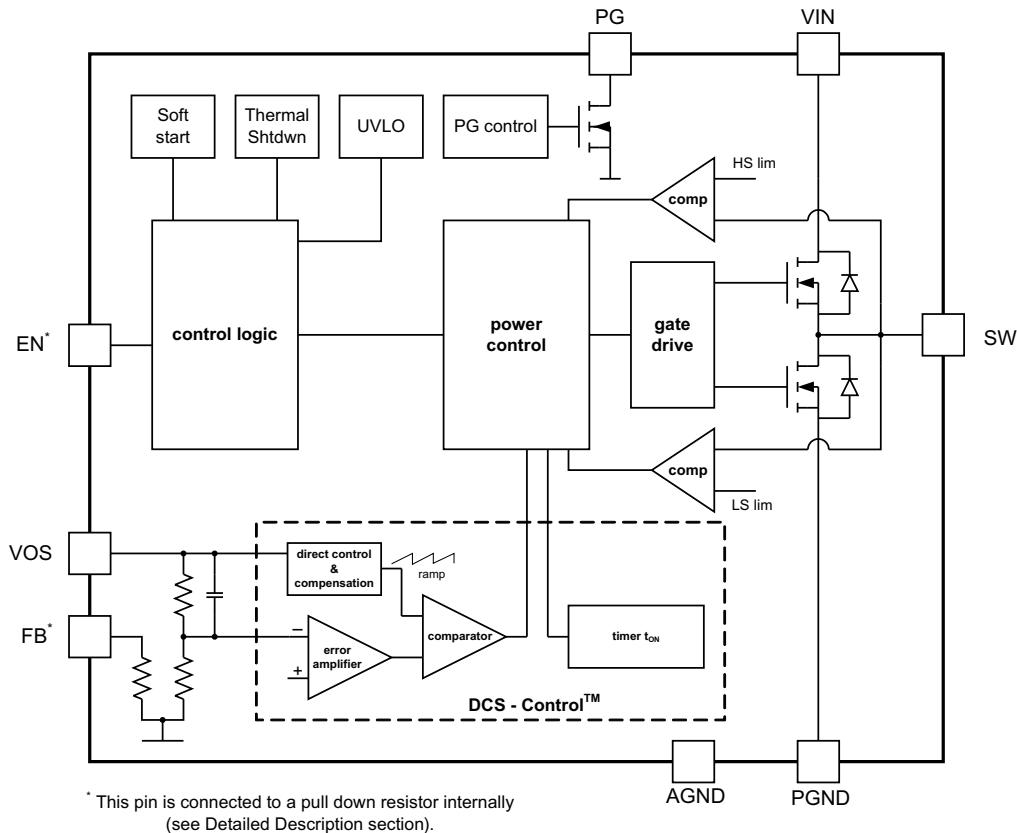


Figure 5. TPS62170 (Adjustable Output Voltage)

**Functional Block Diagram (continued)**

**Figure 6. TPS62171/TPS62172/TPS62173 (Fixed Output Voltage)**

### 8.3 Feature Description

#### 8.3.1 Enable and Shutdown (EN)

When enable (EN) is set high, the device starts operation.

Shutdown is forced if EN is pulled low with a shutdown current of typically 1.5  $\mu$ A. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. If the EN pin is low, an internal pull-down resistor of about 400 k $\Omega$  is connected and keeps it low, to avoid bouncing.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

#### 8.3.2 Current Limit and Short Circuit Protection

The TPS6217x devices are protected against heavy load and short circuit events. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET is turned off. Avoiding shoot-through current, the low-side FET is switched on to allow the inductor current to decrease. The high-side FET turns on again, only if the current in the low-side FET decreases below the low-side current limit threshold.

The output current of the device is limited by the current limit (see [Electrical Characteristics](#)). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit is calculated as follows:



## Feature Description (continued)

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD}$$

where

- $I_{LIMF}$  is the static current limit, specified in [Electrical Characteristics](#)
- L is the inductor value
- $V_L$  is the voltage across the inductor
- $t_{PD}$  is the internal propagation delay

(1)

The dynamic high-side switch peak current is calculated as follows:

$$I_{peak(typ)} = I_{LIMF\_HS} + \frac{(V_{IN} - V_{OUT})}{L} \cdot 30ns$$

(2)

Take care with the current limit, if the input voltage is high and very small inductances are used.

### 8.3.3 Power Good (PG)

The TPS6217x has a built in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor (to any voltage below 7 V). It can sink 2 mA of current and maintain its specified logic low level. It is high impedance when the device is turned off due to EN, UVLO or thermal shutdown.

### 8.3.4 Undervoltage Lockout (UVLO)

If the input voltage drops, the under voltage lockout prevents misoperation of the device by switching off both the power FETs. The under voltage lockout threshold is set typically to 2.7 V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 180 mV.

### 8.3.5 Thermal Shutdown

The junction temperature ( $T_j$ ) of the device is monitored by an internal temperature sensor. If  $T_j$  exceeds 160°C (typical), the device goes into thermal shut down. Both the high-side and low-side power FETs are turned off and PG goes high impedance. When  $T_j$  decreases below the hysteresis amount, the converter resumes normal operation, beginning with soft start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shut down temperature.

## 8.4 Device Functional Modes

### 8.4.1 Soft Start

The internal soft start circuitry controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50  $\mu$ s and  $V_{OUT}$  rises with a slope of about 25 mV/ $\mu$ s. See [Figure 30](#) and [Figure 31](#) for typical startup operation.

The TPS6217x can start into a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to turn on until the device's internal ramp sets an output voltage above the pre-bias voltage.

## Device Functional Modes (continued)

### 8.4.2 Pulse Width Modulation (PWM) Operation

The TPS6217x operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of about 2.25 MHz. The frequency variation in PWM is controlled and depends on  $V_{IN}$ ,  $V_{OUT}$  and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters power save mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor's ripple current.

### 8.4.3 Power Save Mode Operation

The TPS6217x's built in power save mode is entered seamlessly, if the load current decreases. This secures a high efficiency in light load operation. The device remains in power save mode as long as the inductor current is discontinuous.

In power save mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of power save mode happens within the entire regulation scheme and is seamless in both directions.

TPS6217x includes a fixed on-time circuitry. This on-time, in steady-state operation, is estimated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 420ns \quad (3)$$

For very small output voltages, the on-time increases beyond the result of [Equation 3](#), to stay above an absolute minimum on-time,  $t_{ON(min)}$ , which is around 80 ns, to limit switching losses. The peak inductor current in PSM is approximated by:

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \cdot t_{ON} \quad (4)$$

When  $V_{IN}$  decreases to typically 15% above  $V_{OUT}$ , the TPS6217x does not enter power save mode, regardless of the load current. The device maintains output regulation in PWM mode.

### 8.4.4 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by  $D = V_{OUT}/V_{IN}$  and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal setpoint. This allows the conversion of small input to output voltage differences, such as for the longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, is calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} (R_{DS(on)} + R_L)$$

where

- $I_{OUT}$  is the output current
  - $R_{DS(on)}$  is the  $R_{DS(on)}$  of the high-side FET
  - $R_L$  is the DC resistance of the inductor used
- (5)

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPS6217x device family are easy to use synchronous step-down DC-DC converters optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response as well as high output voltage accuracy by utilization of the DCS-Control™ topology. With its wide operating input voltage range of 3 V to 17 V, the devices are ideally suited for systems powered from either a Li-Ion or other battery as well as from 12-V intermediate power rails. It supports up to 0.5-A continuous output current at output voltages between 0.9 V and 6 V (with 100% duty cycle mode).

### 9.2 Typical Application

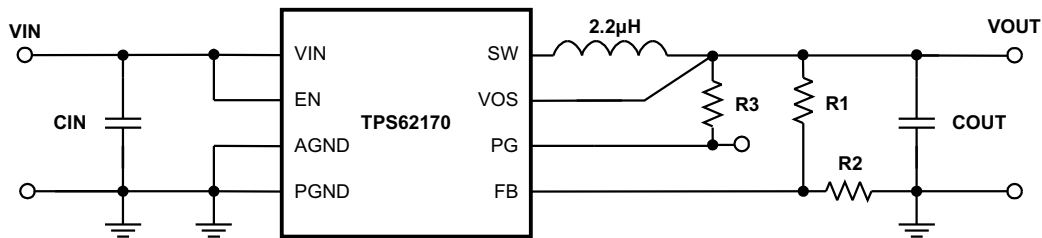


Figure 7. TPS62170 Adjustable Power Supply

#### 9.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the [Recommended Operating Conditions](#).

#### 9.2.2 Detailed Design Procedure

##### 9.2.2.1 Programming the Output Voltage

While the output voltage of the TPS62170 is adjustable, the TPS62171/TPS62172/TPS62173 are programmed to fixed output voltages. For fixed output versions, the FB pin is pulled down internally and may be left floating. It is recommended to connect it to AGND to improve thermal resistance. The adjustable version can be programmed for output voltages from 0.9 V to 6 V by using a resistive divider from VOUT to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from [Equation 6](#). It is recommended to choose resistor values which allow a current of at least 2 µA, meaning the value of R2 should not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design. For applications requiring lowest current consumption, the use of fixed output voltage versions is recommended.

$$R_1 = R_2 \left( \frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (6)$$

In case the FB pin gets opened, the device clamps the output voltage at the VOS pin to about 7.4 V.

## Typical Application (continued)

### 9.2.2.2 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS6217x is optimized to work within a range of external components. The LC output filter's inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter (see [Output Filter and Loop Stability](#)). [Table 1](#) can be used to simplify the output filter component selection.

**Table 1. Recommended LC Output Filter Combinations<sup>(1)</sup>**

	4.7µF	10µF	22µF	47µF	100µF	200µF	400µF
1µH							
2.2µH		√	√ <sup>(2)</sup>	√	√	√	
3.3µH		√	√	√	√		
4.7µH							

(1) The values in the table are nominal values. Variations of typically ±20% due to tolerance, saturation and DC bias are assumed.

(2) This LC combination is the standard value and recommended for most applications.

More detailed information on further LC combinations can be found in [SLVA463](#).

#### 9.2.2.2.1 Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). [Equation 7](#) and [Equation 8](#) calculate the maximum inductor current under static load conditions.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \quad (7)$$

$$\Delta I_{L(\max)} = V_{OUT} \cdot \left( \frac{1 - \frac{V_{OUT}}{V_{IN(\max)}}}{L_{(\min)} \cdot f_{SW}} \right)$$

where

- $I_L(\max)$  is the maximum inductor current
  - $\Delta I_L$  is the peak-to-peak inductor ripple current
  - $L(\min)$  is the minimum effective inductor value
  - $f_{SW}$  is the actual PWM switching frequency
- (8)

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. [Table 2](#) lists inductors that are recommended for use with the TPS6217x.

**Table 2. List of Inductors**

Type	Inductance [µH]	Current [A] <sup>(1)</sup>	Dimensions [L x B x H] mm	MANUFACTURER
VLF3012ST-2R2M1R4	2.2 µH, ±20%	1.9 A	3.0 x 2.8 x 1.2	TDK
VLF302512MT-2R2M	2.2 µH, ±20%	1.9 A	3.0 x 2.5 x 1.2	TDK
VLS252012-2R2	2.2 µH, ±20%	1.3 A	2.5 x 2.0 x 1.2	TDK
XFL3012-222MEC	2.2 µH, ±20%	1.9 A	3.0 x 3.0 x 1.2	Coilcraft
XFL3012-332MEC	3.3 µH, ±20%	1.6 A	3.0 x 3.0 x 1.2	Coilcraft
XPL2010-222MLC	2.2 µH, ±20%	1.3 A	1.9 x 2.0 x 1.0	Coilcraft

(1)  $I_{RMS}$  at 40°C rise or  $I_{SAT}$  at 30% drop.

**Table 2. List of Inductors (continued)**

Type	Inductance [ $\mu\text{H}$ ]	Current [A] <sup>(1)</sup>	Dimensions [L x B x H] mm	MANUFACTURER
XPL2010-332MLC	3.3 $\mu\text{H}$ , $\pm 20\%$	1.1 A	1.9 x 2.0 x 1.0	Coilcraft
LPS3015-332ML	3.3 $\mu\text{H}$ , $\pm 20\%$	1.4 A	3.0 x 3.0 x 1.4	Coilcraft
PFL2512-222ME	2.2 $\mu\text{H}$ , $\pm 20\%$	1.0 A	2.8 x 2.3 x 1.2	Coilcraft
PFL2512-333ME	3.3 $\mu\text{H}$ , $\pm 20\%$	0.78 A	2.8 x 2.3 x 1.2	Coilcraft
744028003	3.3 $\mu\text{H}$ , $\pm 30\%$	1.0 A	2.8 x 2.8 x 1.1	Wuerth
PSI25201B-2R2MS	2.2 $\mu\text{H}$ , $\pm 20\%$	1.3 A	2.0 x 2.5 x 1.2	Cyntec
NR3015T-2R2M	2.2 $\mu\text{H}$ , $\pm 20\%$	1.5 A	3.0 x 3.0 x 1.5	Taiyo Yuden
BRC2012T2R2MD	2.2 $\mu\text{H}$ , $\pm 20\%$	1.0 A	2.0 x 1.25 x 1.4	Taiyo Yuden
BRC2012T3R3MD	3.3 $\mu\text{H}$ , $\pm 20\%$	0.87 A	2.0 x 1.25 x 1.4	Taiyo Yuden

TPS6217x can operate with an inductor as low as 2.2  $\mu\text{H}$ . However, for applications running with low input voltages, 3.3  $\mu\text{H}$  is recommended, to allow the full output current. The inductor value also determines the load current at which power save mode is entered:

$$I_{load(PSM)} = \frac{1}{2} \Delta I_L \quad (9)$$

Using [Equation 8](#), this current level is adjusted by changing the inductor value.

#### 9.2.2.2.2 Capacitor Selection

##### 9.2.2.2.2.1 Output Capacitor

The recommended value for the output capacitor is 22  $\mu\text{F}$ . The architecture of the TPS6217x allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use an X7R or X5R dielectric. Using a higher value can have some advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode (see [SLVA463](#)).

Note: In power save mode, the output voltage ripple depends on the output capacitance, its ESR and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

##### 9.2.2.2.2.2 Input Capacitor

For most applications, 10  $\mu\text{F}$  is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between VIN and PGND as close as possible to those pins.

#### 9.2.2.3 Output Filter and Loop Stability

The devices of the TPS6217x family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency calculated with [Equation 10](#):

$$f_{LC} = \frac{1}{2\pi \sqrt{L \cdot C}} \quad (10)$$

Proven nominal values for inductance and ceramic capacitance are given in [Table 1](#) and are recommended for use. Different values may work, but care has to be taken on the loop stability which is affected. More information including a detailed L-C stability matrix is found in [SLVA463](#).

The TPS6217x devices, both fixed and adjustable versions, include an internal 25 pF feed forward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per [Equation 11](#) and [Equation 12](#):

$$f_{zero} = \frac{1}{2\pi \cdot R_1 \cdot 25 pF} \quad (11)$$

$$f_{pole} = \frac{1}{2\pi \cdot 25 pF} \cdot \left( \frac{1}{R_1} + \frac{1}{R_2} \right) \quad (12)$$

Though the TPS6217x devices are stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in power save mode and/or improved transient response. An external feed-forward capacitor can also be added. A more detailed discussion on the optimization for stability vs. transient response can be found in [SLVA289](#) and [SLVA466](#).

If using ceramic capacitors, the DC bias effect has to be considered. The DC bias effect results in a drop in effective capacitance as the voltage across the capacitor increases (see **NOTE** in Capacitor selection section).

#### NOTE

**DC bias effect:** High capacitance ceramic capacitors have a DC bias effect, which has a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

#### 9.2.2.4 TPS6216x Components List

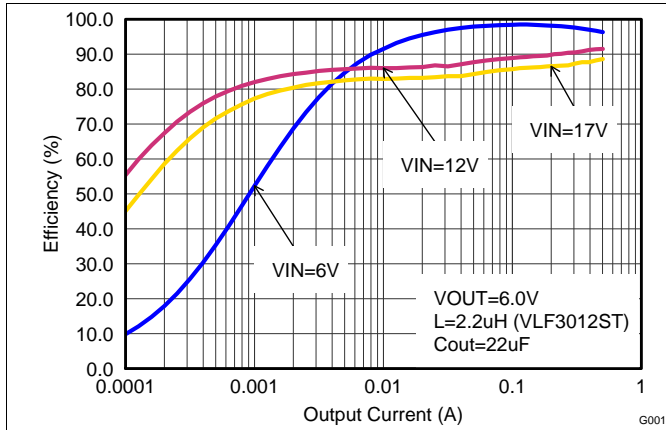
[Table 3](#) shows the list of components for the [Application Curves](#).

**Table 3. List of Components**

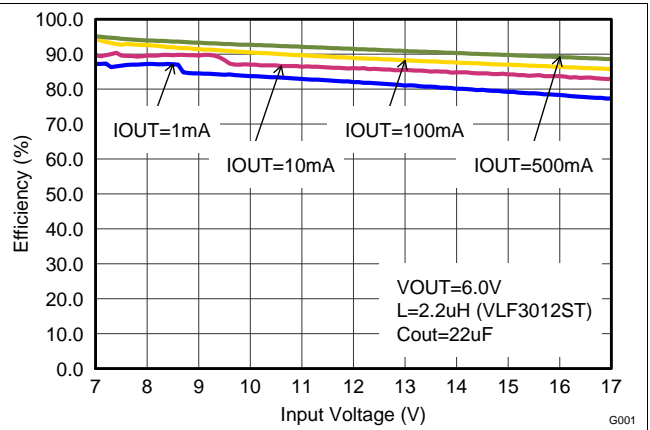
REFERENCE	DESCRIPTION	MANUFACTURER
IC	17 V, 0.5A Step-Down Converter, WSON	TPS62170DSG, Texas Instruments
L1	2.2 uH, 1.4 A, 3 mm x 2.8 mm x 1.2 mm	VLF3012ST-2R2M1R4, TDK
Cin	10 μF, 25 V, Ceramic	Standard
Cout	22 μF, 6.3 V, Ceramic	Standard
R1	depending on V <sub>OUT</sub>	
R2	depending on V <sub>OUT</sub>	
R3	100 kΩ, Chip, 0603, 1/16 W, 1%	Standard

**9.2.3 Application Curves**

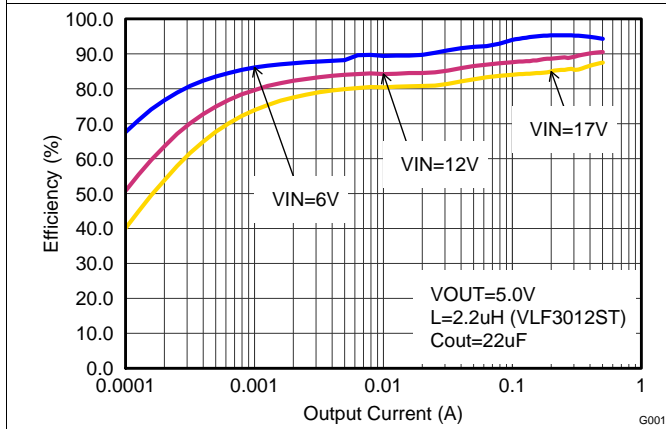
$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $T_A = 25^\circ C$ , (unless otherwise noted)



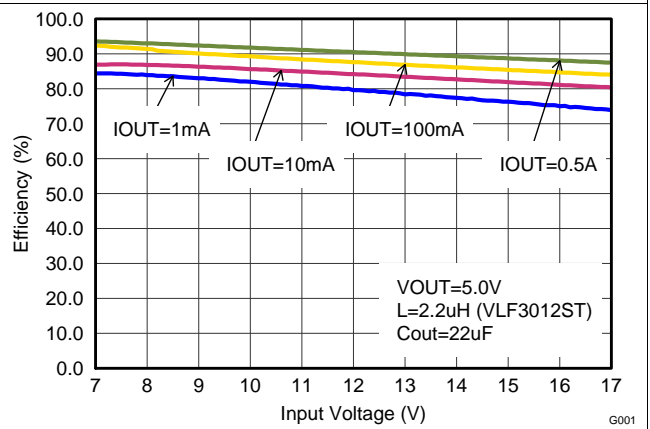
**Figure 8. Efficiency vs Output Current,  $V_{OUT} = 6 V$**



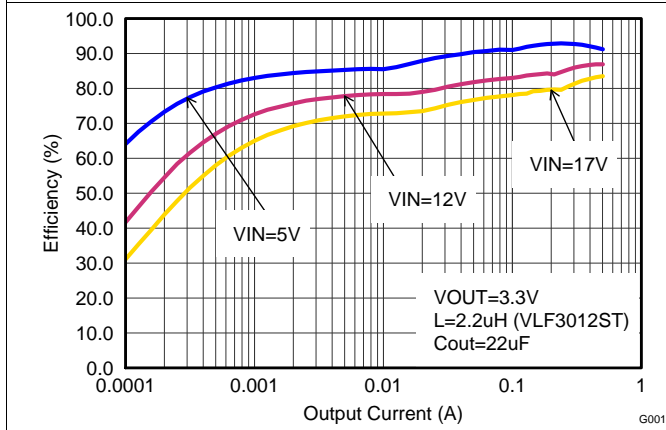
**Figure 9. Efficiency vs Input Voltage,  $V_{OUT} = 6 V$**



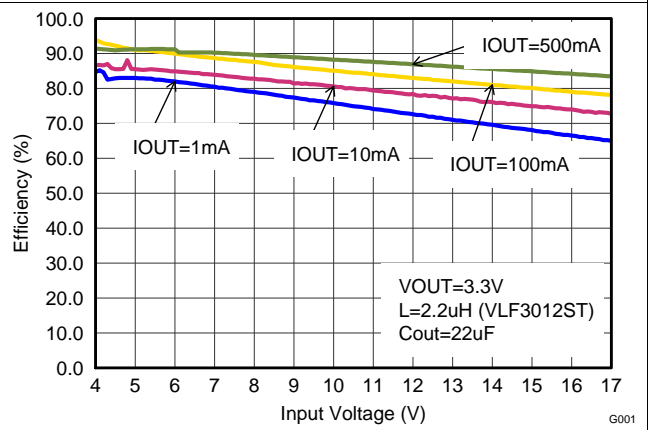
**Figure 10. Efficiency vs Output Current,  $V_{OUT} = 5 V$**



**Figure 11. Efficiency vs Input Voltage,  $V_{OUT} = 5 V$**



**Figure 12. Efficiency vs Output Current,  $V_{OUT} = 3.3 V$**



**Figure 13. Efficiency vs Input Voltage,  $V_{OUT} = 3.3 V$**

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $T_A = 25^\circ C$ , (unless otherwise noted)

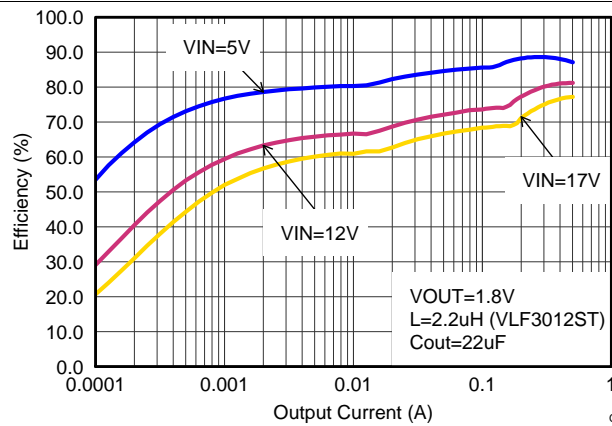


Figure 14. Efficiency vs Output Current,  $V_{OUT} = 1.8 V$

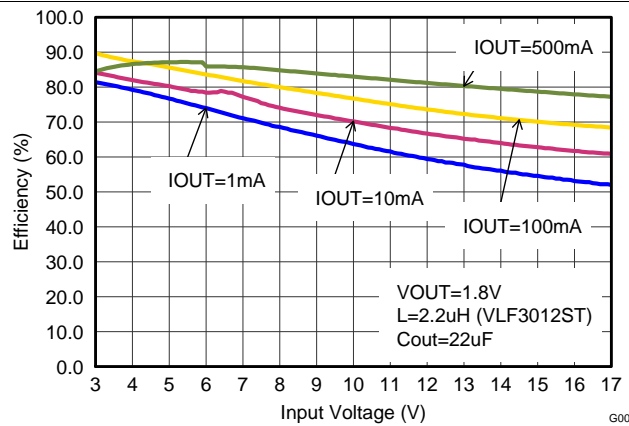


Figure 15. Efficiency vs Input Voltage,  $V_{OUT} = 1.8 V$

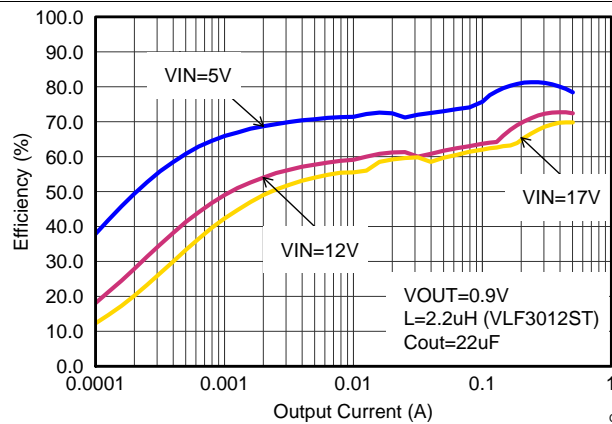


Figure 16. Efficiency vs Output Current,  $V_{OUT} = 0.9 V$

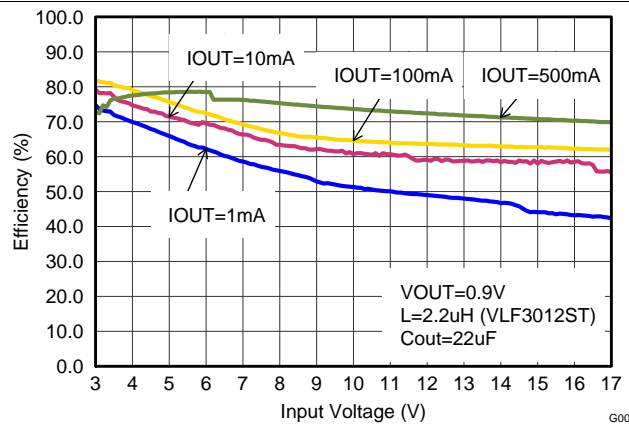


Figure 17. Efficiency vs Input Voltage,  $V_{OUT} = 0.9 V$

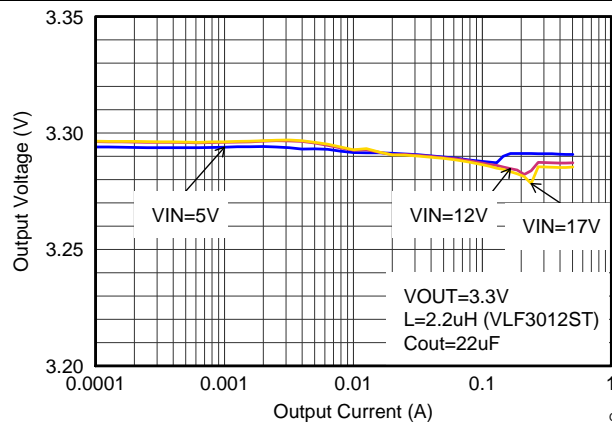


Figure 18. Output Voltage Accuracy (Load Regulation)

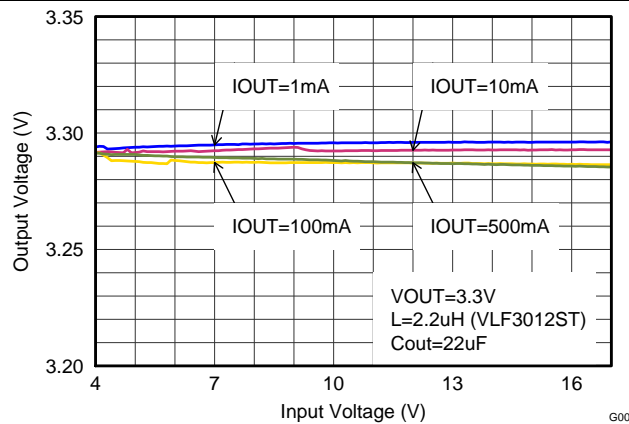
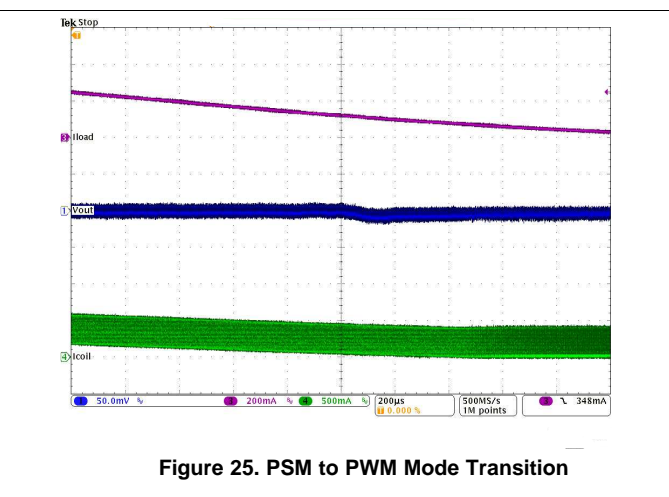
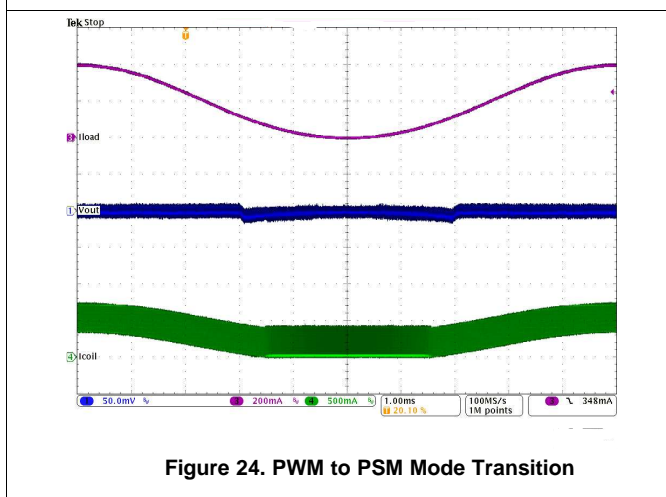
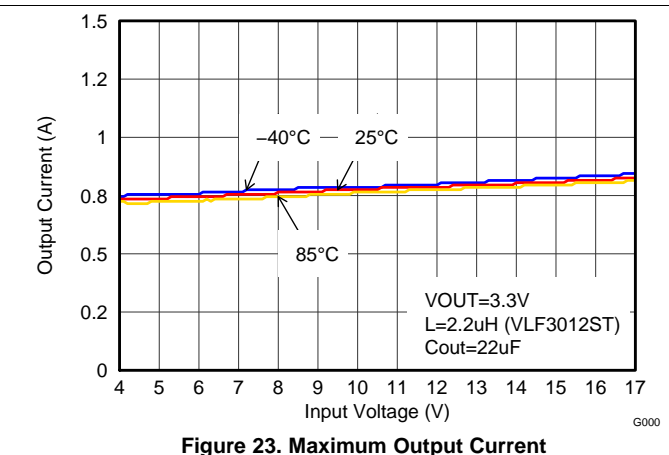
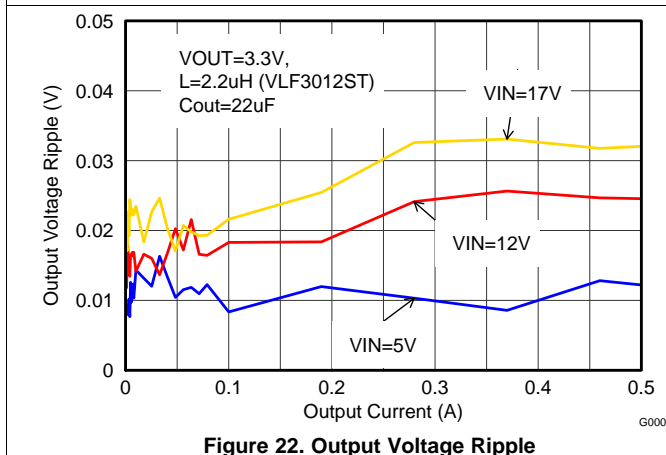
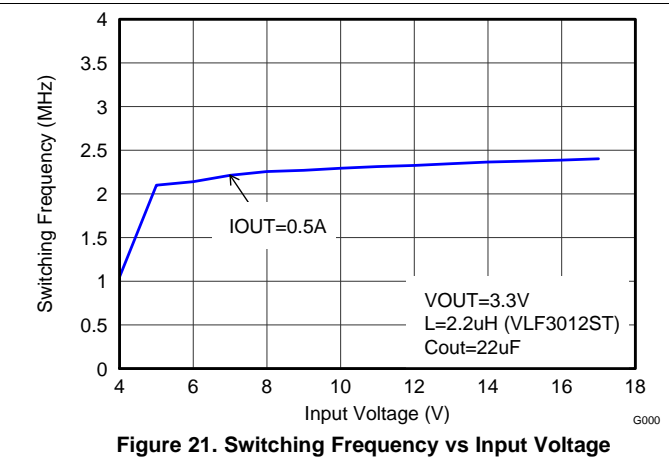
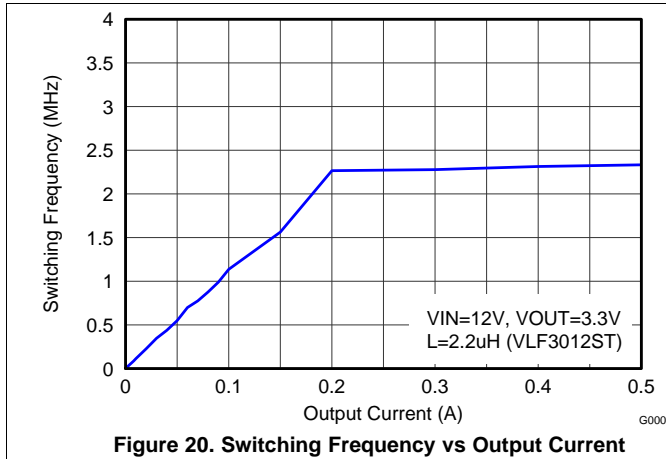


Figure 19. Output Voltage Accuracy (Line Regulation)



$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $T_A = 25^\circ C$ , (unless otherwise noted)



$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $T_A = 25^\circ C$ , (unless otherwise noted)

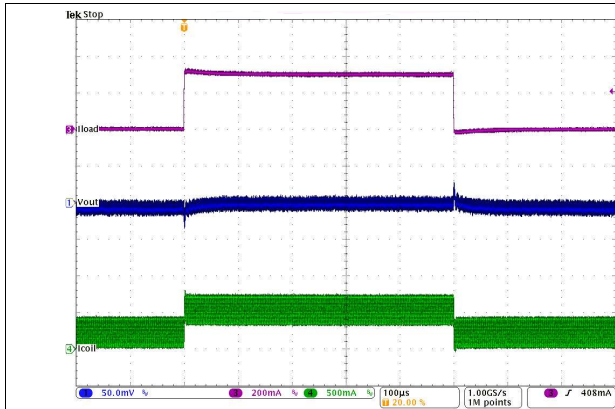


Figure 26. Load Transient Response in PWM Mode (200 mA to 500 mA)

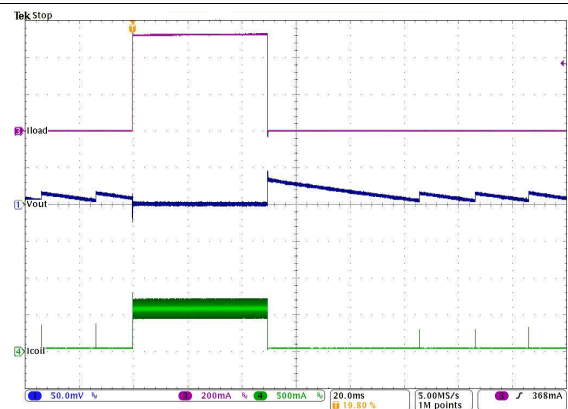


Figure 27. Load Transient Response from Power Save Mode (100 mA to 500 mA)

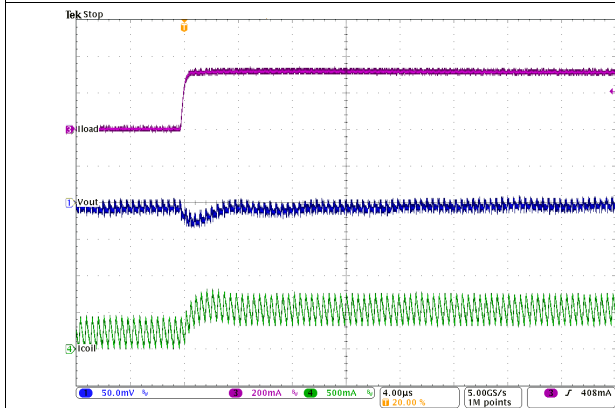


Figure 28. Load Transient Response in PWM Mode (200 mA to 500 mA), Rising Edge

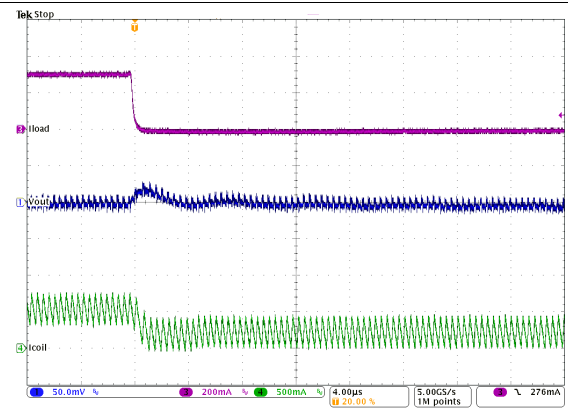


Figure 29. Load Transient Response in PWM Mode (200 mA to 500 mA), Falling Edge

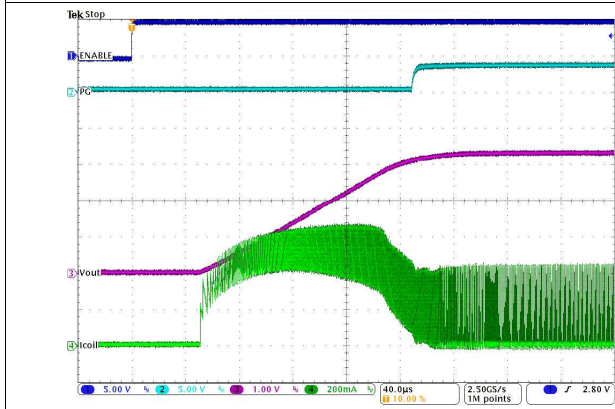


Figure 30. Startup with  $I_{OUT} = 500\text{ mA}$ ,  $V_{OUT} = 3.3\text{ V}$

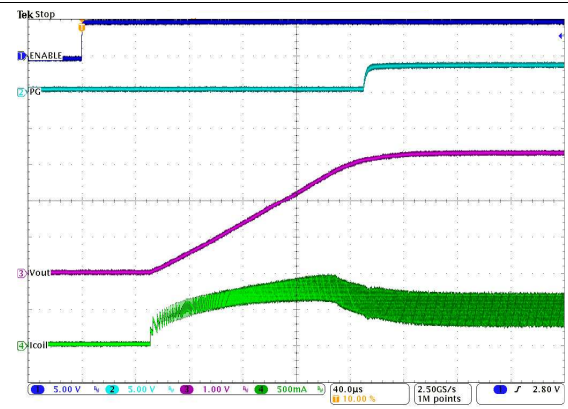
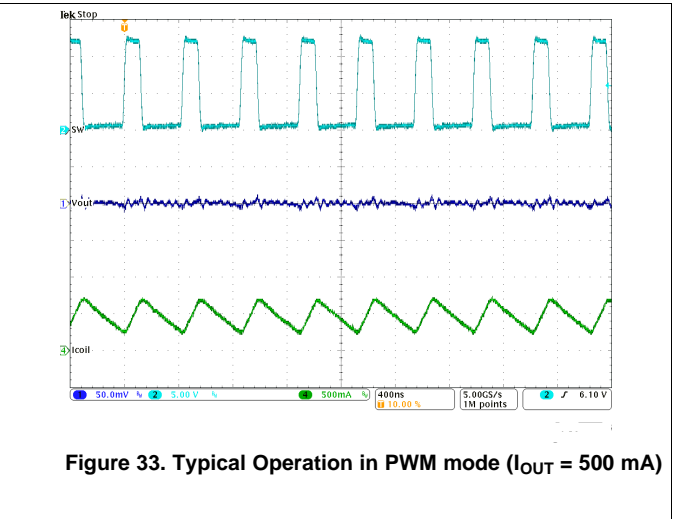
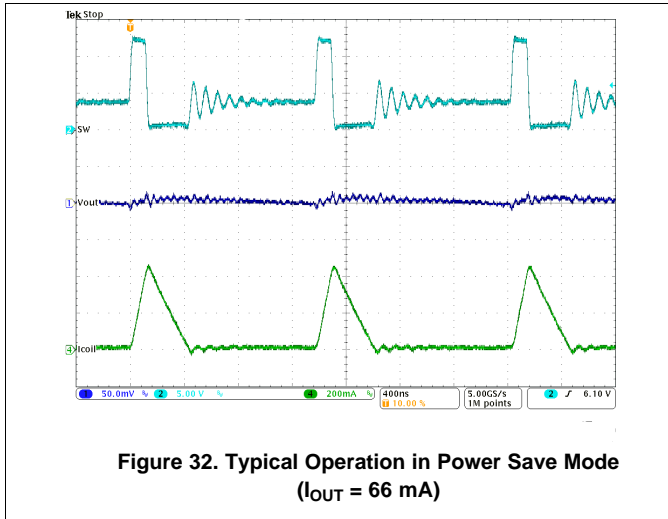


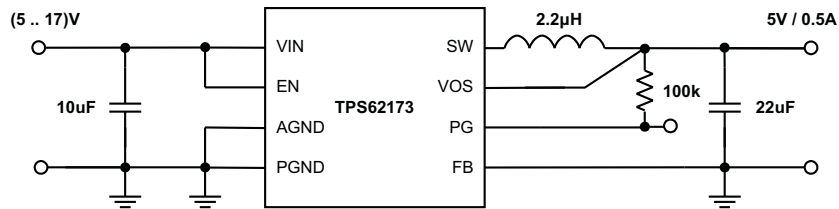
Figure 31. Startup with  $I_{OUT} = 500\text{ mA}$ ,  $V_{OUT} = 3.3\text{ V}$

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $T_A = 25^\circ C$ , (unless otherwise noted)

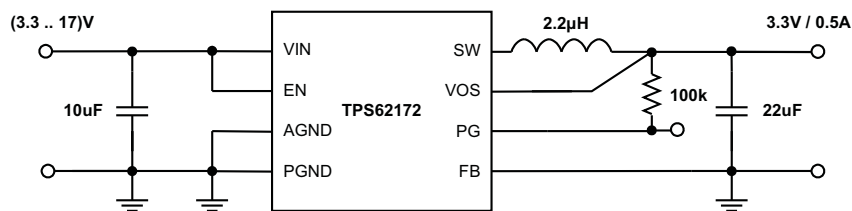


### 9.3 System Examples

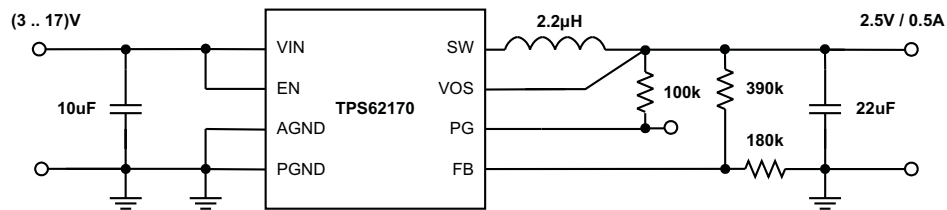
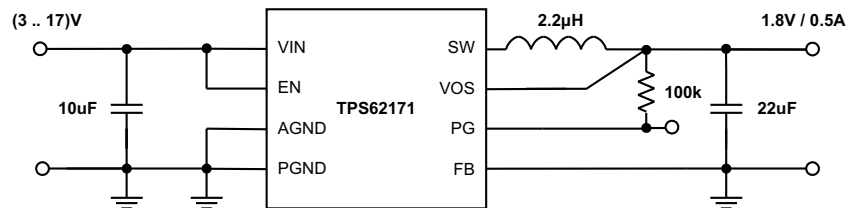
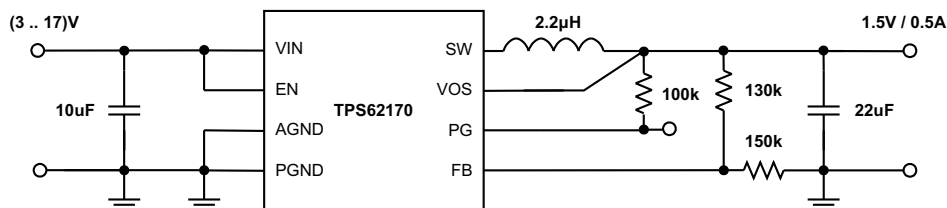
Figure 34 through Figure 40 show various TPS6217x devices and input voltages that provide a 0.5-A power supply with output voltage options.



**Figure 34. 5-V and 0.5-A Power Supply**



**Figure 35. 3.3-V and 0.5-A Power Supply**

**System Examples (continued)**

**Figure 36. 2.5-V and 0.5-A Power Supply**

**Figure 37. 1.8-V and 0.5-A Power Supply**

**Figure 38. 1.5-V and 0.5-A Power Supply**

System Examples (continued)

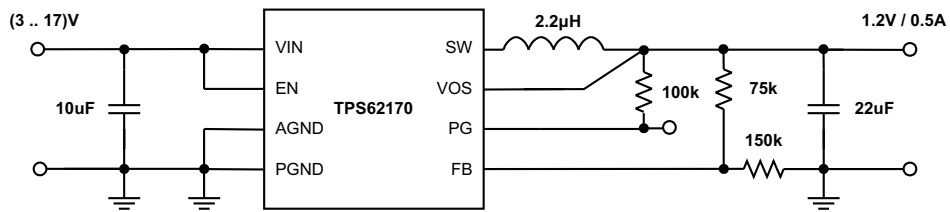


Figure 39. 1.2-V and 0.5-A Power Supply

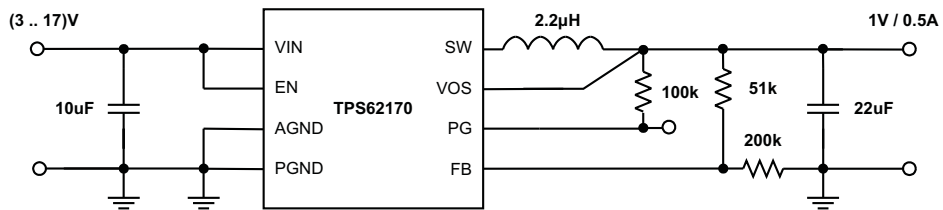


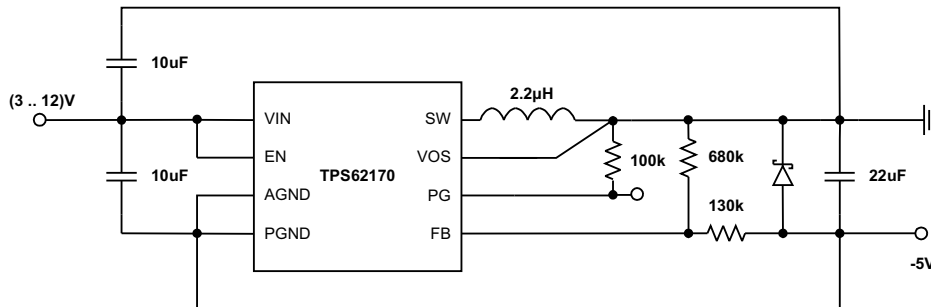
Figure 40. 1-V and 0.5-A Power Supply

## System Examples (continued)

### 9.3.1 Inverting Power Supply

The TPS6217x can be used as inverting power supply by rearranging external circuitry as shown in [Figure 41](#). As the former GND node now represents a voltage level below system ground, the voltage difference between  $V_{IN}$  and  $V_{OUT}$  has to be limited for operation to the maximum supply voltage of 17 V (see [Equation 13](#)).

$$V_{IN} + |V_{OUT}| \leq V_{INmax} \quad (13)$$



**Figure 41. –5-V Inverting Power Supply**

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a right half plane zero additionally. The loop stability has to be adapted and an output capacitance of at least 22  $\mu\text{F}$  is recommended. A detailed design example is given in [SLVA469](#).

## 10 Power Supply Recommendations

The TPS6217x device family has no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TPS6217x.

## 11 Layout

### 11.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TPS6217x demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation and noise sensitivity.

Provide low inductive and resistive paths to ground for loops with high  $di/dt$ . Therefore paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high  $dv/dt$ . Therefore the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Also sensitive nodes like FB and VOS should be connected with short wires, not nearby high  $dv/dt$  signals (such as SW). As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). Signals not assigned to power transmission (such as the feedback divider) should refer to the signal ground (AGND) and always be separated from the power ground (PGND).

In summary, the input capacitor should be placed as close as possible to the VIN and PGND pin of the IC. This connections should be done with wide and short traces. The output capacitor should be placed such that its ground is as close as possible to the IC's PGND pins - avoiding additional voltage drop in traces. This connection should also be made short and wide. The inductor should be placed close to the SW pin and connect directly to the output capacitor - minimizing the loop area between the SW pin, inductor, output capacitor and PGND pin. The feedback resistors,  $R_1$  and  $R_2$ , should be placed close to the IC and connect directly to the AGND and FB pins. Those connections (including VOUT) to the resistors and even more to the VOS pin should stay away from noise sources, such as the inductor. The VOS pin should connect in the shortest way to VOUT at the output capacitor, while the VOUT connection to the feedback divider can connect at the load.

A single point grounding scheme should be implemented with all grounds (AGND, PGND and the thermal pad) connecting at the IC's exposed thermal pad. See [Figure 42](#) for the recommended layout of the TPS6217x. More detailed information can be found in the EVM Users Guide, [SLVU483](#).

The exposed thermal pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation. Although the exposed thermal pad can be connected to a floating circuit board trace, the device has better thermal performance if it is connected to a larger ground plane. The exposed thermal pad is electrically connected to AGND.

### 11.2 Layout Example

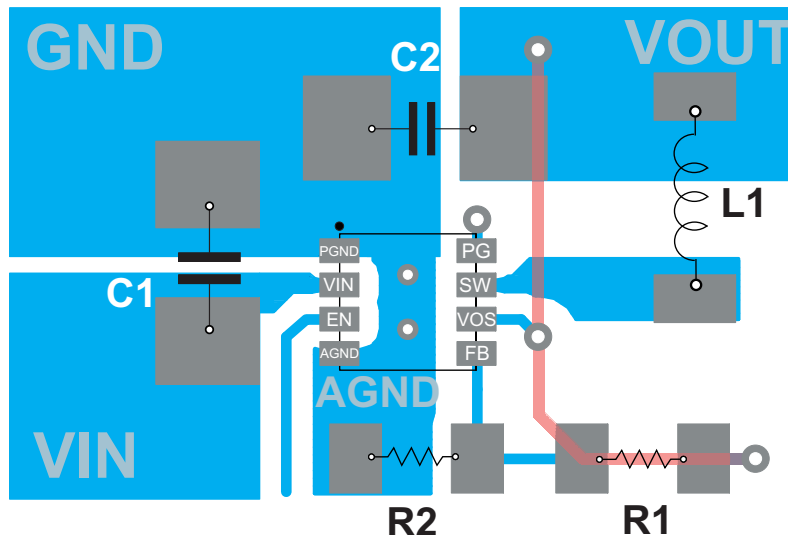


Figure 42. Layout Example

### 11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the exposed thermal pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Note [SZZA017](#), and [SPRA953](#).

The TPS6217x is designed for a maximum operating junction temperature ( $T_j$ ) of 125°C. Therefore the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. If the thermal resistance of the package is given, the size of the surrounding copper area and a proper thermal connection of the IC can reduce the thermal resistance. To get an improved thermal behavior, it is recommended to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.



## 12 器件和文档支持

### 12.1 器件支持

#### 12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 12.2 文档支持

#### 12.2.1 相关文档

相关文档如下:

- [TPS62160](#), 《采用 DCS-Control™ 拓扑的 3V 至 17V、1A、降压转换器》, [TPS62160](#)
- [TPS62125](#), 《具有可调节启用阈值和迟滞的 3V 至 17V、300mA 降压转换器》, [TPS62125](#)
- 《优化 TPS62130/40/50/60/70 输出滤波器》, [SLVA463](#)
- 《采用前馈电容优化内部补偿 DC-DC 转换器的瞬态响应》, [SLVA289](#)
- 《采用前馈电容提升 TPS62130/40/50/60/70 的稳定性和带宽》, [SLVA466](#)
- 《在反向降压-升压拓扑中使用 TPS6215x》, [SLVA469](#)
- 《TPS62160EVM 和 TPS62170EVM-627 评估模块》, [SLVU483](#)
- 《采用 JEDEC PCB 设计的线性和逻辑封装散热特性》, [SZZA017](#)

### 12.3 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，以及样片与购买的快速访问。

表 4. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS62170	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
TPS62171	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
TPS62172	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
TPS62173	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>

### 12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 商标

DCS-Control, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.6 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## 重要声明

德州仪器(TI)及其下属子公司有权根据 JESD46 最新标准,对所提供的产品和服务进行更正、修改、增强、改进或其它更改,并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息,并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内,且 TI 认为有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定,否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险,客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息,不能构成从 TI 获得使用这些产品或服务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可,或是 TI 的专利权或其它知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分,仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时,如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分,则会失去相关 TI 组件或服务的所有明示或暗示授权,且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意,尽管任何应用相关信息或支持仍可能由 TI 提供,但他们将独立负责满足与其产品及其在应用中使用的 TI 产品相关的所有法律、法规和安全相关要求。客户声明并同意,他们具备制定与实施安全措施所需的全部专业技术和知识,可预见故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中,为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此,此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III (或类似的生命攸关医疗设备)的授权许可,除非各方授权官员已经达成了专门管控此类使用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同意,对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用,其风险由客户单独承担,并且由客户独立负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品,这些产品主要用于汽车。在任何情况下,因使用非指定产品而无法达到 ISO/TS16949 要求, TI 不承担任何责任。

	产品		应用
数字音频	<a href="http://www.ti.com.cn/audio">www.ti.com.cn/audio</a>	通信与电信	<a href="http://www.ti.com.cn/telecom">www.ti.com.cn/telecom</a>
放大器和线性器件	<a href="http://www.ti.com.cn/amplifiers">www.ti.com.cn/amplifiers</a>	计算机及周边	<a href="http://www.ti.com.cn/computer">www.ti.com.cn/computer</a>
数据转换器	<a href="http://www.ti.com.cn/dataconverters">www.ti.com.cn/dataconverters</a>	消费电子	<a href="http://www.ti.com.cn/consumer-apps">www.ti.com.cn/consumer-apps</a>
DLP® 产品	<a href="http://www.dlp.com">www.dlp.com</a>	能源	<a href="http://www.ti.com.cn/energy">www.ti.com.cn/energy</a>
DSP - 数字信号处理器	<a href="http://www.ti.com.cn/dsp">www.ti.com.cn/dsp</a>	工业应用	<a href="http://www.ti.com.cn/industrial">www.ti.com.cn/industrial</a>
时钟和计时器	<a href="http://www.ti.com.cn/clockandtimers">www.ti.com.cn/clockandtimers</a>	医疗电子	<a href="http://www.ti.com.cn/medical">www.ti.com.cn/medical</a>
接口	<a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
逻辑	<a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
电源管理	<a href="http://www.ti.com.cn/power">www.ti.com.cn/power</a>	视频和影像	<a href="http://www.ti.com.cn/video">www.ti.com.cn/video</a>
微控制器 (MCU)	<a href="http://www.ti.com.cn/microcontrollers">www.ti.com.cn/microcontrollers</a>		
RFID 系统	<a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a>		
OMAP应用处理器	<a href="http://www.ti.com/omap">www.ti.com/omap</a>		
无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>

邮寄地址: 上海市浦东新区世纪大道1568号, 中建大厦32楼邮政编码: 200122  
Copyright © 2016, 德州仪器半导体技术(上海)有限公司

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62170DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUE	<a href="#">Samples</a>
TPS62170DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUE	<a href="#">Samples</a>
TPS62171DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUF	<a href="#">Samples</a>
TPS62171DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUF	<a href="#">Samples</a>
TPS62172DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUG	<a href="#">Samples</a>
TPS62172DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUG	<a href="#">Samples</a>
TPS62173DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUH	<a href="#">Samples</a>
TPS62173DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QUH	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS62170, TPS62172 :**

- Automotive: [TPS62170-Q1](#), [TPS62172-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62170DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62170DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62170DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62170DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62171DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62171DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62172DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62172DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62173DSGR	WSON	DSG	8	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62173DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62173DSGT	WSON	DSG	8	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS62173DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

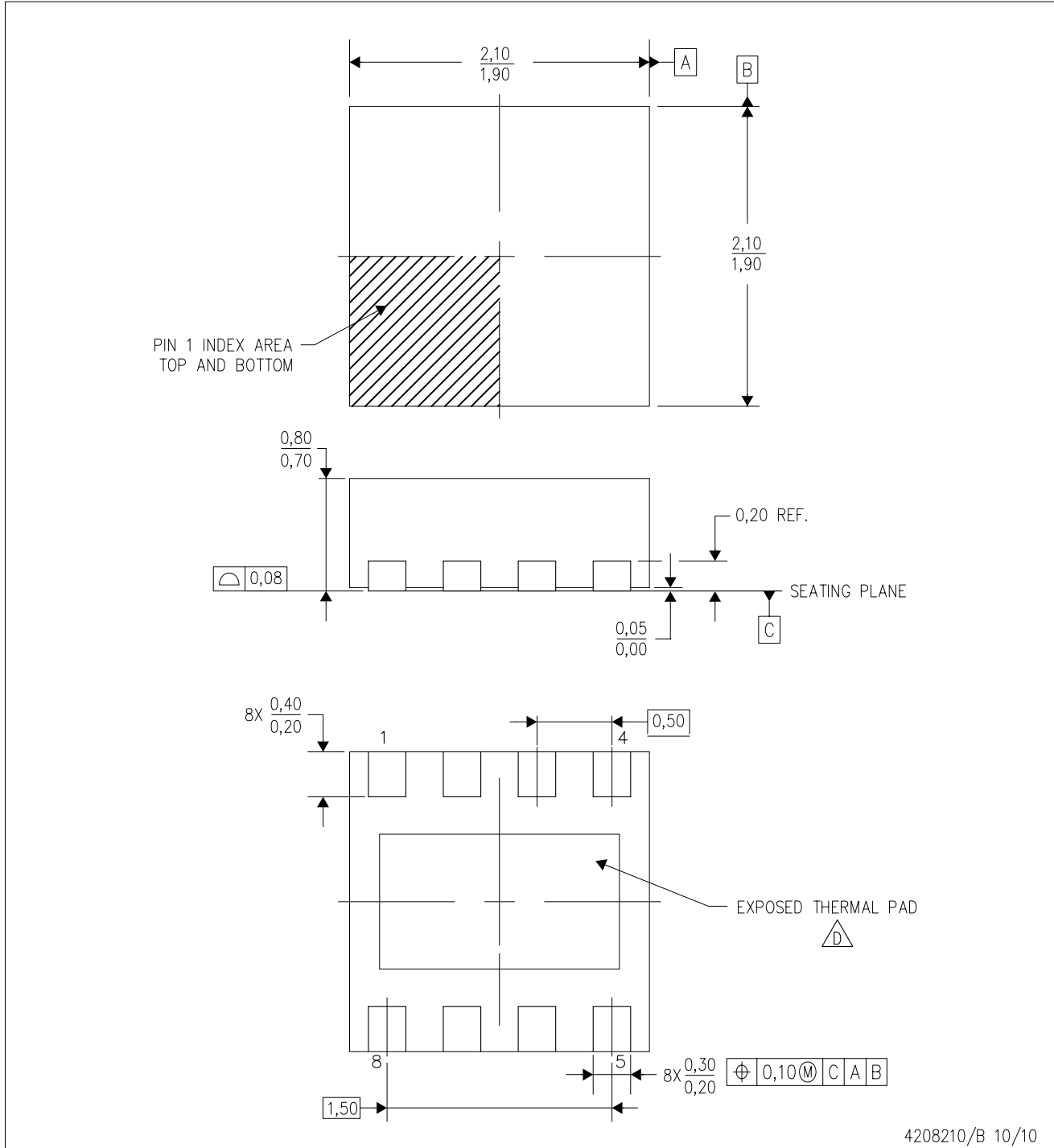
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62170DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62170DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62170DSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS62170DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS62171DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62171DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS62172DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62172DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS62173DSGR	WSON	DSG	8	3000	205.0	200.0	33.0
TPS62173DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62173DSGT	WSON	DSG	8	250	205.0	200.0	33.0
TPS62173DSGT	WSON	DSG	8	250	210.0	185.0	35.0

DSG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4208210/B 10/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-Leads (QFN) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-229.



## THERMAL PAD MECHANICAL DATA

DSG (S-PWSON-N8)

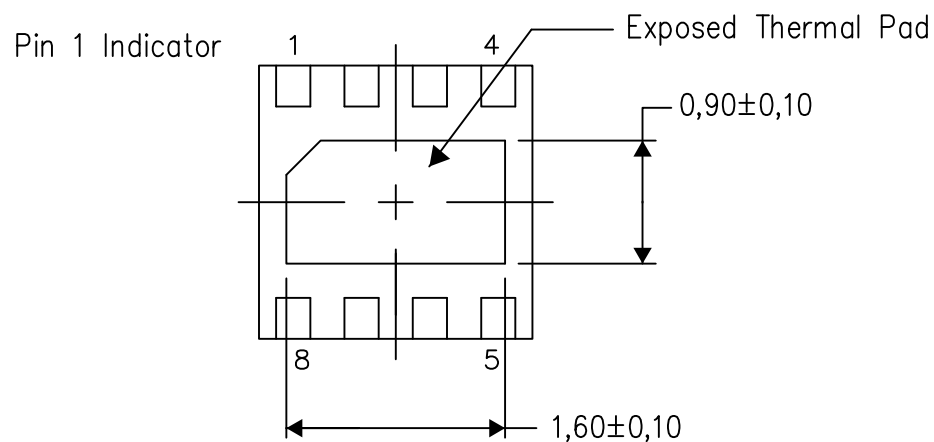
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

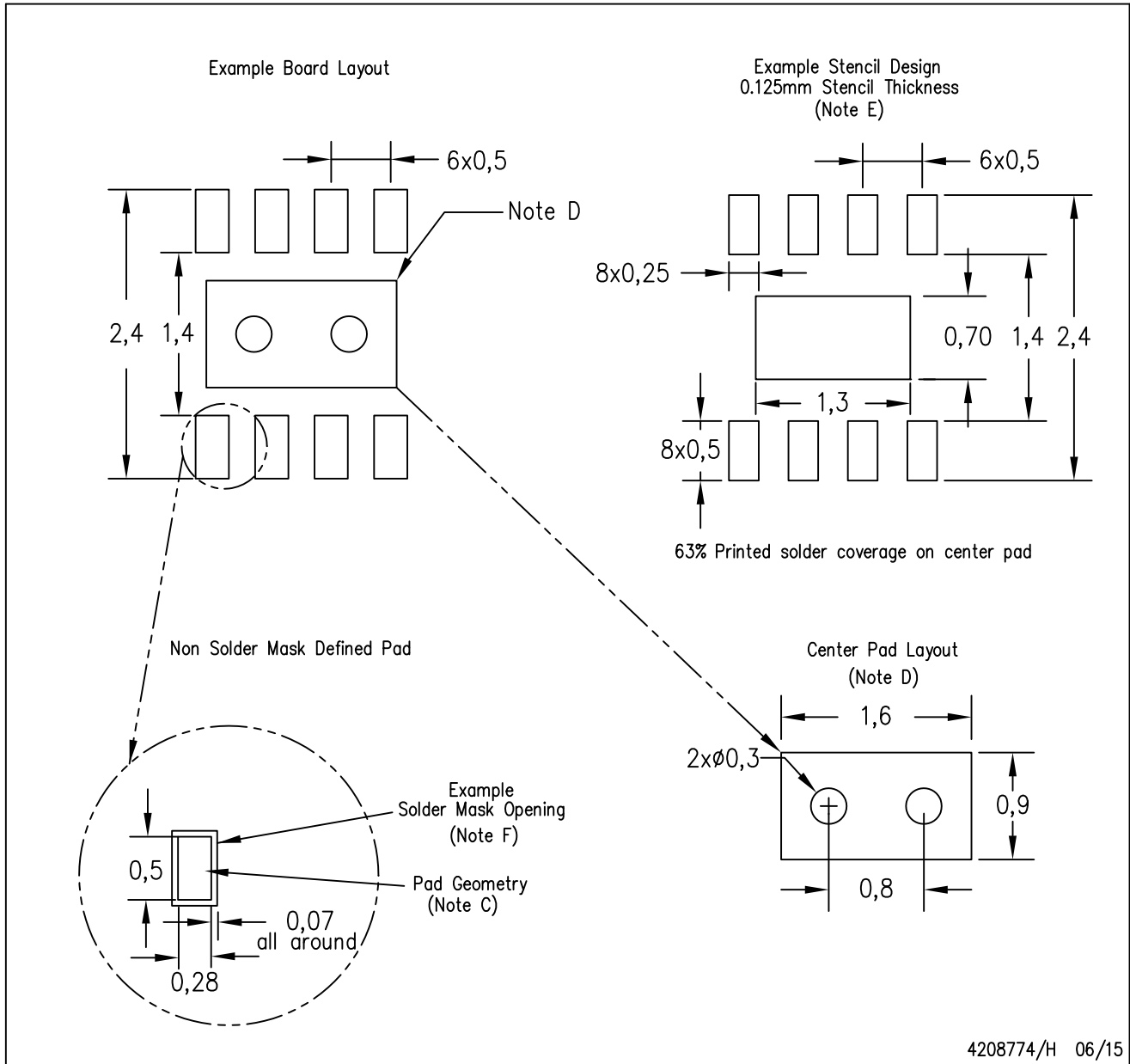


Bottom View

Exposed Thermal Pad Dimensions

4208347/1 06/15

NOTE: All linear dimensions are in millimeters



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for solder mask tolerances.

## 重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (<http://www.ti.com/sc/docs/stdterms.htm>) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权负责并确保应用的安全性，及设计人员的应用（包括应用中使用的 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何应用前，将彻底测试该等应用和该等应用中所用 TI 产品的功能。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的应用，如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的应用时，才被授权使用、复制和修改任何相关 TI 资源。但并未依据禁止反言原则或其他法律授予您任何 TI 知识产权的任何其他明示或暗示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等许可包括但不限于任何专利权、版权、屏蔽作品权或与美国 TI 产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默认为的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的符合相关功能安全标准和要求的的应用。在应用内使用产品的行为本身不会配有安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和标准。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的产品，并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122  
Copyright © 2017 德州仪器半导体技术（上海）有限公司