TXB0304 具有自动方向感应的 4 位双向电平转换器/电压转换器

1 特性

- 完全对称的电源电压，A 端口和 B 端口上均为 0.9V 到 3.6V
- V_{CC} 隔离特性 – 如果任一 V_{CC} 输入接地，则所有输出处于高阻态
- 以 V_{CCA} 为基准的输出使能 (OE) 输入电路
- 低功耗，最大 5μA（I_{CCA} 或 I_{CCB}）
- $I_{关闭}$ 支持部分断电模式工作
- 锁断性能超过 100mA （符合 JESD 78 II 类规范的要求）
- 静电放电 (ESD) 保护性能超过 JESD 22 规范要求
  - 8000V 人体放电模式 (A114-A)
  - 1000V 组件充电模式 (C101)

2 应用

- 个人电子产品
- 工业
- 企业
- 电信

3 说明

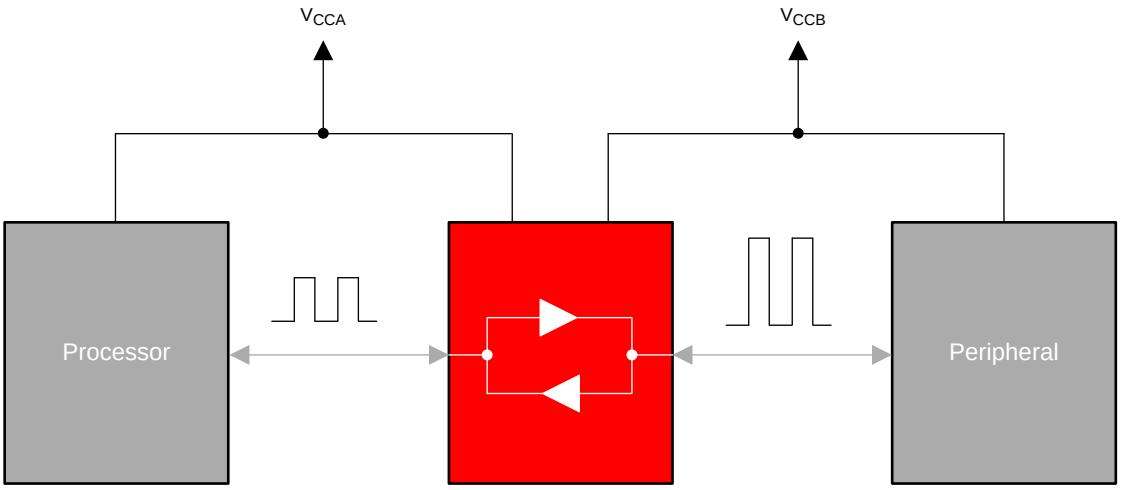
这个 4 位非反向转换器使用两个独立的可配置电源轨。A 端口设计用于跟踪 V_{CCA}。V_{CCA}可接受从 0.9V 到 3.6V 范围内的任意电源电压。B 端口设计用于跟踪 V_{CCB}。V_{CCB} 可接受 0.9V 到 3.6V 范围内的任意电源电压。这可以实现 1V、1.2V、1.5V、1.8V、2.5V 和 3V 电压节点之间的任意低压双向转换。对于 TXB0304，当输出使能 (OE) 输入为低时，所有输出均处于高阻态。为确保在上电或掉电期间均处于高阻态，应将 OE 通过下拉电阻连接至 GND；该电阻的最小值取决于驱动器的拉电流能力。OE 器件控制引脚输入电路由 V_{CCA} 供电。该器件完全 适用于 使用 I_{off} 的局部掉电应用。I_{off} 电路会禁用输出，从而在器件掉电时防止电流回流损坏器件。TXB0304 和 TXBN0304 唯一的区别在于 OE 信号分别为高电平有效和低电平有效。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TXB0304	RUT UQFN (12)	2.00mm × 1.70mm
	RSV UQFN (16)	2.60mm x 1.80mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用方框图**(TXB0304)**



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (August 2014) to Revision F — **Page**

- 已更改*说明*部分 ... 1
- 已更改*Absolute Maximum Ratings*、*Recommended Operating Conditions*(1)(2)、*Switching Characteristics*和*Electrical Characteristics*表。 ... 1

Changes from Revision D (October 2012) to Revision E — **Page**

- 已添加 *ESD 额定值*表，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分。 ... 1
- Changed VCCA and VCCB in the ABS MAX table to V_{CCA} and V_{CCB} in 3 places ... 4
- Changed in ELEC CHARAC table the 0.9 x V_{CCA} and 0.9 x V_{CCB} from MAX column into the MIN column ... 5
- Changed in ELEC CHARAC table 0.2 (2 places) in the MIN column to the MAX ... 5

Changes from Revision C (May 2012) to Revision D — **Page**

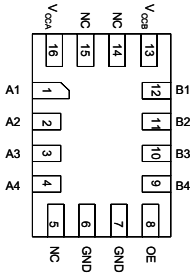
- Added *Application Information* section ... 12

Changes from Revision B (September 2011) to Revision C — **Page**

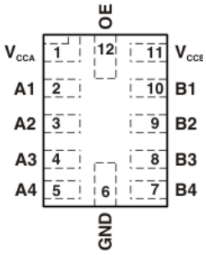
- Added package pin out diagram notes. ... 3

5 Pin Configuration and Functions

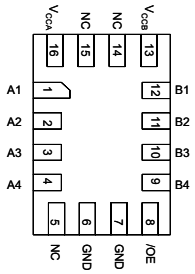
RSV Package
16-Pin UQFN
TXB0304 Top View



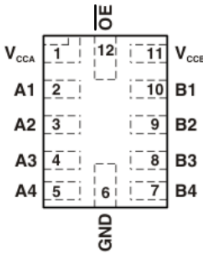
RUT Package
12-Pin UQFN
TXB0304 Top View



RSV Package
16-Pin UQFN
TXBN0304 Top View



RUT Package
12-Pin UQFN
TXBN0304 Top View



A. See *Layout Guidelines* for notes about package pin out diagrams.

Pin Functions

PIN					TYPE	DESCRIPTION	
NAME	TXB0304		TXBN0304				
	RSV	RUT	RSV	RUT			
A1	1	2	1	2	I/O	Input/output 1	Referenced to V_{CCA}
A2	2	3	2	3	I/O	Input/output 2	
A3	3	4	3	4	I/O	Input/output 3	
A4	4	5	4	5	I/O	Input/output 4	
B1	12	10	12	10	I/O	Input/output 4	Referenced to V_{CCB}
B2	11	9	11	9	I/O	Input/output 3	
B3	10	8	10	8	I/O	Input/output 2	
B4	9	7	9	7	I/O	Input/output 1	
GND	6, 7	6	6,7	6	GND	Ground	
NC	5, 14, 15	—	5, 14, 15	—	—	No connection; not internally connected	
OE	8	12	—	—	I	3-state output-mode enable. Pull OE (TXB0304) low to place all outputs in 3-state mode. Referenced to V_{CCA}.	
$\overline{OE}$	—	—	8	12	I	3-state output-mode enable. Pull $\overline{OE}$ (TXBN0304) high to place all outputs in 3-state mode. Referenced to V_{CCA}.	
V_{CCA}	16	1	16	1	—	A-port supply voltage 0.9 V ≤ V_{CCA} ≤ 3.6 V	
V_{CCB}	13	11	13	11	—	B-port supply voltage 0.9 V ≤ V_{CCB} ≤ 3.6 V	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		–0.5	4.6	V
V_{CCB}			–0.5	4.6	
V_I	Input voltage	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state (2)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C
T_J	Junction temperature		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions (1) (2)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				0.9	3.6	V
V_{CCB}							
V_{IH}	High-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	V_{CCI} × 0.65	V_{CCI}	V
		OE/$\overline{OE}$	0.9 V to 3.6 V	0.9 V to 3.6 V	V_{CCA} × 0.65	3.6	
V_{IL}	Low-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	0	V_{CCI} × 0.35	V
		OE/$\overline{OE}$	0.9 V to 1.2 V	0.9 V to 3.6 V	0	V_{CCA} × 0.3	
			1.2 V to 3.6 V	0.9 V to 3.6 V	0	V_{CCA} × 0.35	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	3.6	V
		B-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	3.6	
Δt/Δv	Input transition rise or fall rate	A-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V		40	ns/V
		B-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V		40	
T_A	Operating free-air temperature				–40	85	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, such as, both at V_{CCI} or both at GND.
(2) V_{CCI} is the supply voltage associated with the input port.

6.4 Thermal Information

THERMAL METRIC[1]		TXB0304		UNIT
		RUT (UQFN)	RSV (UQFN)	
		12 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.4	131.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.7	55.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.9	55.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.9	55.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OHA}	High-level output voltage	I_{OH} = –20 µA	T_A = 25°C	0.9 V to 3.6 V		0.9 x V_{CCA}			V
V_{OLA}	Low-level output voltage	I_{OL} = 20 µA	–40°C to 85°C	0.9 V to 3.6 V				0.2	V
V_{OHB}	High-level output voltage	I_{OH} = –20 µA	T_A = 25°C		0.9 V to 3.6 V	0.9 x V_{CCB}			V
V_{OLB}	Low-level output voltage	I_{OL} = 20 µA	–40°C to 85°C		0.9 V to 3.6 V			0.2	V
I_I	OE	V_I = V_{CCI} or GND	T_A = 25°C	0.9 V to 3.6 V	0.9 V to 3.6 V			±1	µA
			–40°C to 85°C					±2	
I_{off}	A port	V_I or V_O = 0 to 3.6 V	T_A = 25°C	0 V	0 V to 3.6 V			±1	µA
			–40°C to 85°C					±2	
	B port	V_I or V_O = 0 to 3.6 V	T_A = 25°C	0.9 V to 3.6 V	0 V			±1	
			–40°C to 85°C					±2	
I_{OZ}	A or B port	OE = GND	T_A = 25°C	0.9 V to 3.6 V	0.9 V to 3.6 V			±1	µA
			–40°C to 85°C					±2	
I_{CCA}		V_I = V_{CCI} or GND, I_O = 0	–40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V			5	µA
I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	–40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V			5	µA
I_{CCA} + I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	–40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V			10	µA
I_{CCZA}	High-Z state supply current	V_I = V_{CCI} or GND, I_O = 0, OE = GND	–40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V			5	µA
I_{CCZB}	High-Z state supply current	V_I = V_{CCI} or GND, I_O = 0, OE = GND	–40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V			5	µA
C_i	OE	T_A = 25°C		0.9 V to 3.6 V	0.9 V to 3.6 V		3		pF
C_{io}	A port	T_A = 25°C, OE = GND		0.9 V to 3.6 V	0.9 V to 3.6 V		6.7		pF
	B port						6.7		

6.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	LOAD	V_{CCA}	V_{CCB}	MIN	MAX	UNIT
Data rate	C_L = 15 pF	0.9 to 3.6 V	0.9 to 3.6 V		50	Mbps
	C_L = 15 pF	1.2 to 3.6 V	1.2 to 3.6 V		100	Mbps
	C_L = 15 pF	1.8 to 3.6 V	1.8 to 3.6 V		140	Mbps
	C_L = 30 pF	0.9 to 3.6 V	0.9 to 3.6 V		40	Mbps
	C_L = 30 pF	1.2 to 3.6 V	1.2 to 3.6 V		90	Mbps
	C_L = 30 pF	1.8 to 3.6 V	1.8 to 3.6 V		130	Mbps
	C_L = 50 pF	1.2 to 3.6 V	1.2 to 3.6 V		80	Mbps
	C_L = 50 pF	1.8 to 3.6 V	1.8 to 3.6 V		120	Mbps
	C_L = 100 pF	1.2 to 3.6 V	1.2 to 3.6 V		70	Mbps
	C_L = 100 pF	1.8 to 3.6 V	1.8 to 3.6 V		100	Mbps

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted). (For parameter descriptions, see Figure 2 and Figure 3.)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	V_{CCA}	V_{CCB}	MIN	TYP(1)	MAX	UNIT
t_{pd}	A	B	C_L = 15	0.9-3.6	0.9-3.6		18.9	30	ns
	A	B	C_L = 15	1.2-3.6	1.2-3.6		7.5	11.5	
	A	B	C_L = 15	1.8-3.6	1.8-3.6		3.7	4.8	
	A	B	C_L = 30	0.9-3.6	0.9-3.6		19.5	34	
	A	B	C_L = 30	1.2-3.6	1.2-3.6		7.8	11.9	
	A	B	C_L = 30	1.8-3.6	1.8-3.6		3.8	5.2	
	A	B	C_L = 50	1.2-3.6	1.2-3.6		8	12.3	
	A	B	C_L = 50	1.8-3.6	1.8-3.6		4	5.4	
	A	B	C_L = 100	1.2-3.6	1.2-3.6		8.6	13.5	
	A	B	C_L = 100	1.8-3.6	1.8-3.6		4.5	6	
	B	A	C_L = 15	0.9-3.6	0.9-3.6		18.9	30	ns
	B	A	C_L = 15	1.2-3.6	1.2-3.6		7.5	11.5	
	B	A	C_L = 15	1.8-3.6	1.8-3.6		3.7	5	
	B	A	C_L = 30	0.9-3.6	0.9-3.6		19.5	34	
	B	A	C_L = 30	1.2-3.6	1.2-3.6		7.8	11.9	
	B	A	C_L = 30	1.8-3.6	1.8-3.6		3.8	5.2	
	B	A	C_L = 50	1.2-3.6	1.2-3.6		8	12.3	
	B	A	C_L = 50	1.8-3.6	1.8-3.6		4	5.4	
	B	A	C_L = 100	1.2-3.6	1.2-3.6		8.6	13.5	
	B	A	C_L = 100	1.8-3.6	1.8-3.6		4.5	6	
t_{en}	OE	A	C_L = 15	0.9-3.6	0.9-3.6			262	ns
				1.2-3.6	1.2-3.6			64	
				1.8-3.6	1.8-3.6			37	
		B	C_L = 15	0.9-3.6	0.9-3.6			332	
				1.2-3.6	1.2-3.6			76	
				1.8-3.6	1.8-3.6			41	
t_{dis}	OE	A	C_L = 15	0.9-3.6	0.9-3.6			172	ns
		B	C_L = 15	0.9-3.6	0.9-3.6			169	ns
t_{rB}, t_{fB}	B-port rise and fall times		C_L = 15	0.9-3.6	0.9-3.6		2.95		ns
t_{sA}, t_{sA}	A-port rise and fall times		C_L = 15	0.9-3.6	0.9-3.6		3.1		ns
$t_{SK(O)}$	Channel-to-channel skew		C_L = 15	0.9-3.6	0.9-3.6			0.15	ns

(1) T_A = 25°C

6.8 Operating Characteristics

C_{pd} - power dissipation capacitance measured at T_A = 25°C.

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = V_{CCA} (outputs enabled)	34	pF
	B-port input, A-port output		34	
C_{pdB}	A-port input, B-port output		34	pF
	B-port input, A-port output		34	
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = GND (outputs disabled)	0.01	pF
	B-port input, A-port output		0.01	
C_{pdB}	A-port input, B-port output		0.01	pF
	B-port input, A-port output		0.01	

(1) V_{CCA}, V_{CCB} 0.9 V to 3.6 V

6.9 Typical Characteristics

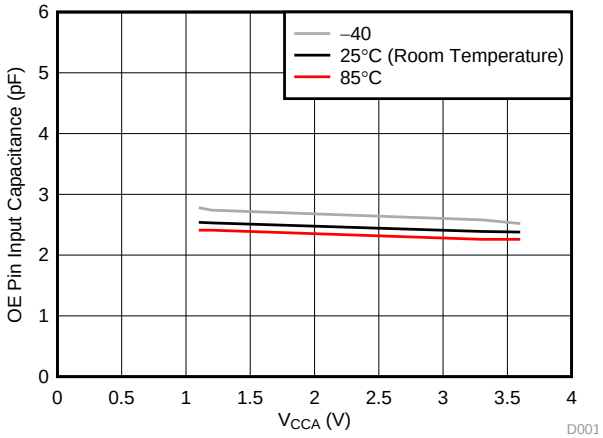
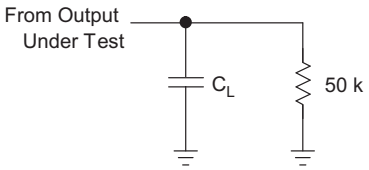
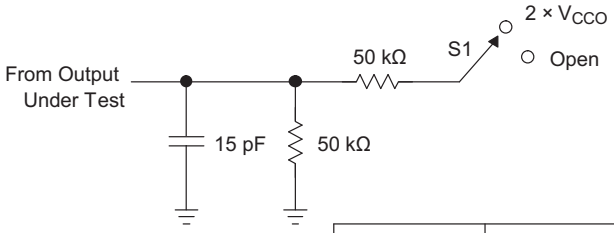


Figure 1. Input Capacitors for OE Pin (C_i) vs Power Supply (V_{CCA})

7 Parameter Measurement Information

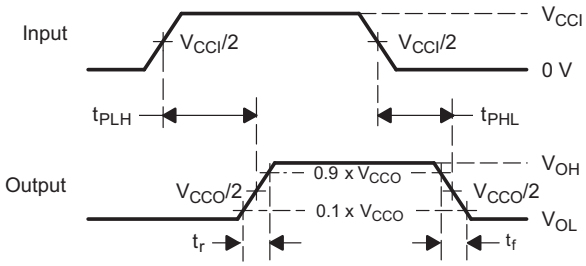


LOAD CIRCUIT FOR MAX DATA RATE, PULSE DURATION PROPAGATION DELAY OUTPUT RISE AND FALL TIME MEASUREMENT

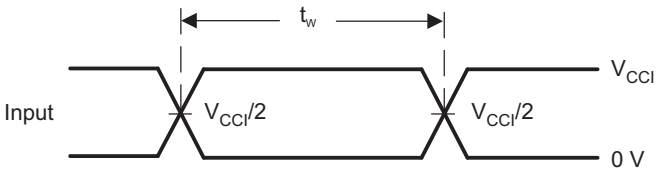


LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT

TEST	S1
t_{PZL}/t_{PLZ}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS PULSE DURATION

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.

C. The outputs are measured one at a time, with one transition per measurement.

D. t_{PLH} and t_{PHL} are the same as t_{pd}.

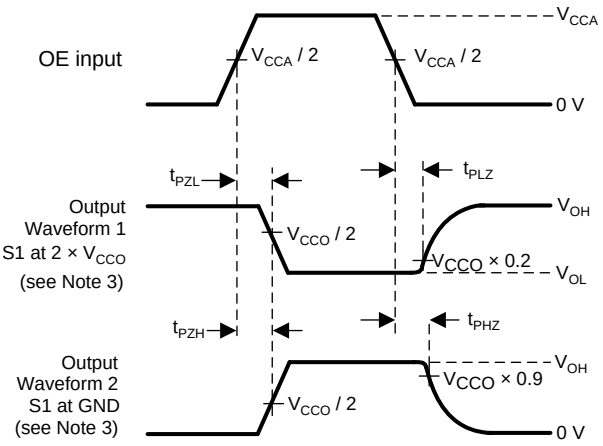
E. V_{CCI} is the V_{CC} associated with the input port.

F. V_{CCO} is the V_{CC} associated with output port.

G. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuits and Voltage Waveforms

Parameter Measurement Information (continued)



(1) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

(2) t_{PZL} and t_{PZH} are the same as t_{en}.

(3) Waveform 1 is for an output with internal such that the output is high, except when OE is high. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

Figure 3. Enable and Disable Times

8 Detailed Description

8.1 Overview

The TXB0304 and TXBN0304 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

8.1.1 Architecture

The TXB0304 and TXBN0304 architecture (see Figure 4) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0304 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 30 Ω at V_{CCO} = 0.9 V to 1 V, 10 Ω at V_{CCO} = 1.1 V to 1.7 V, and 5 Ω at V_{CCO} = 1.8 V to 3.3 V.

8.2 Functional Block Diagram

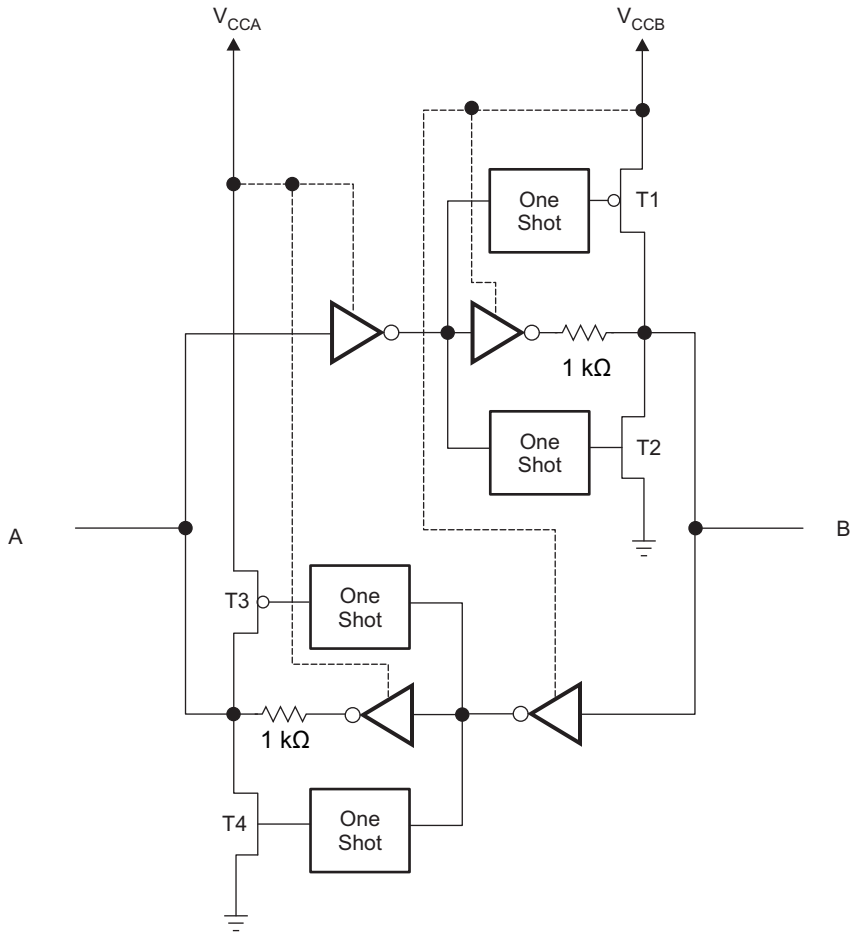
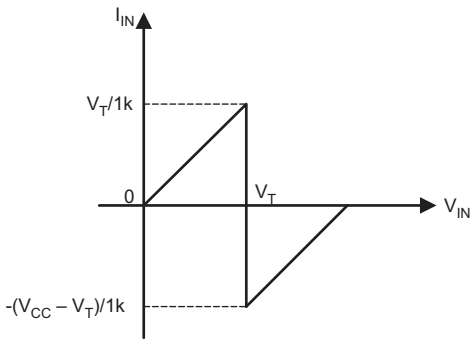


Figure 4. Architecture of TXB0304 I/O Cell

8.3 Feature Description

8.3.1 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0304//TXBN0304 are shown in Figure 5. For proper operation, the device driving the data I/Os of the TXB0304 must have drive strength of at least ±3 mA.



(1) V_{CC} is power supply of TXB0304.

(2) V_T is the input threshold voltage of TXB0304 (typically it is $V_{CC}/2$).

Figure 5. Typical I_{IN} vs V_{IN} Curve

8.4 Device Functional Modes

8.4.1 Enable and Disable

The TXB0304 has an OE input that is used to disable the device by setting OE = low ($\overline{OE}$ = high for TXBN0304), which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is high.

8.4.2 Pullup or Pulldown Resistor on I/O Lines

The TXB0304/TXBN0304 is designed to drive capacitive loads of up to 100 pF. The output drivers of the TXB0304 have low dc drive strength. If pull-up or pull-down resistors are connected externally to the data I/Os, their values must be kept higher than 20 kΩ to ensure that they do not contend with the output drivers of the TXB0304. but if the receiver is integrated with the smaller pull down or pull up resistor, below formula can be used for estimation to evaluate the V_{OH} and V_{OL} .

$$V_{ol} = V_{CCout} \times \frac{1.5k\Omega}{1.5k\Omega + R_{pu}} \quad (1)$$

$$V_{oh} = V_{CCout} \times \frac{R_{pd}}{1.5k\Omega + R_{pd}}$$

where

- V_{CCOUT} is the output port supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pull down resistor
- R_{PU} is the value of the external pull up resistor
- 1.5 kΩ is the counting the variation of the serial resistor 1kΩ in the I/O line. (2)

Because of this restriction on external resistors, the TXB0304 should not be used in applications such as I^2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS010X series of level translators.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TXB0304 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI TXS010X products. Any external pull-down or pull-up resistors are recommended larger than 20 kΩ.

9.2 Typical Application

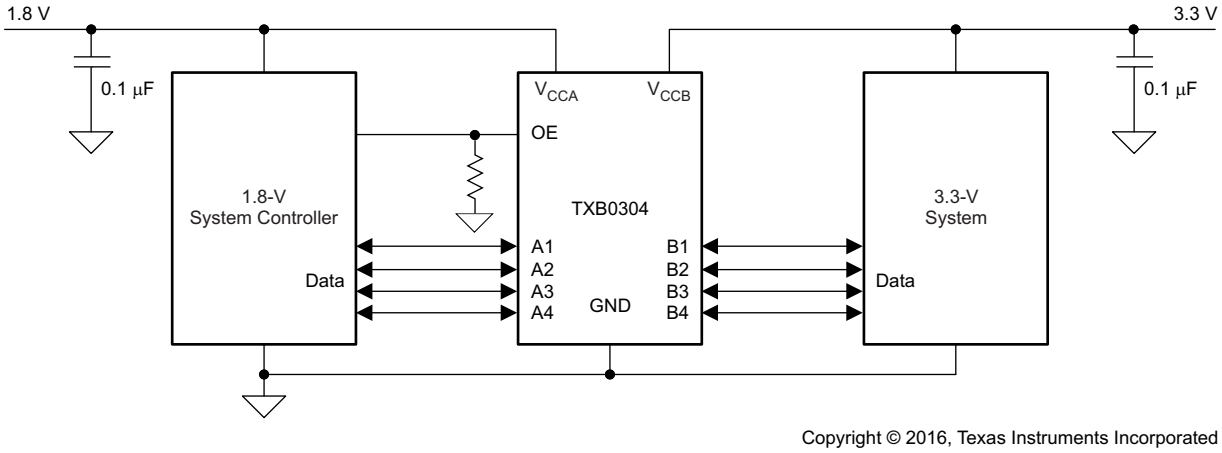


Figure 6. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	0.9 V to 3.6 V
Output voltage range	0.9 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXB0304 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXB0304 device is driving to determine the output voltage range.
  - Don't recommend to have the external pull-up or pull-down resistors. If mandatory, it is recommended the value should be larger than 20 kΩ.

• An external pull-down or pull-up resistor decreases the output V_{OH} and V_{OL}. Use the below equations in section 8.5.2 to draft estimate the V_{OH} and V_{OL} as a result of an external pull-down and pull-up resistor.

9.2.3 Application Curve

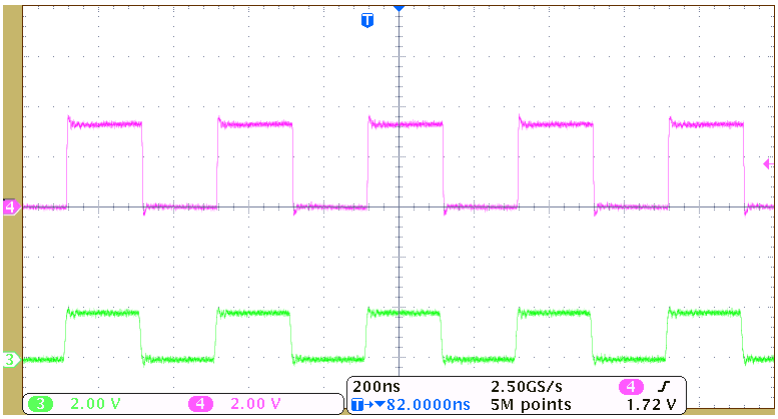


Figure 7. Level-Translation of a 2.5-MHz Signal

10 Power Supply Recommendations

There is no requirement for the power sequence. During operation, TXB0304 can work at both $V_{CCA} \leq V_{CCB}$ and $V_{CCA} \geq V_{CCB}$, During power-up sequencing, any power supply can be ramped up first. The TXB0304 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B}$ = 0 V).

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies. And should be placed as close as possible to the V_{CCA}, V_{CCB} pin and GND pin
- Short trace-lengths should be used to avoid excessive loading.
- For long transmission lines, place a series resistor equivalent to the impedance of the transmission lines to avoid signal integrity issues
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 10 ns, ensuring that any reflection encounters low impedance at the source driver.
- Pullup resistors are not required on both sides for Logic I/O.
- If pullup or pulldown resistors are needed, the resistor value must be over 20 kΩ.
- 20 kΩ is a safe recommended value, if the customer can accept higher Vol or lower Voh, smaller pull up or pull down resistor is allowed, the draft estimation is Vol = Vccout × 1.5k/(1.5k + Rpu) and Voh = Vccout × Rpd/(1.5k + Rpd).
- If pullup resistors are needed, please refer to the TXS0104 or contact TI.
- For detailed information, refer to application note SCEA043.

11.2 Layout Example

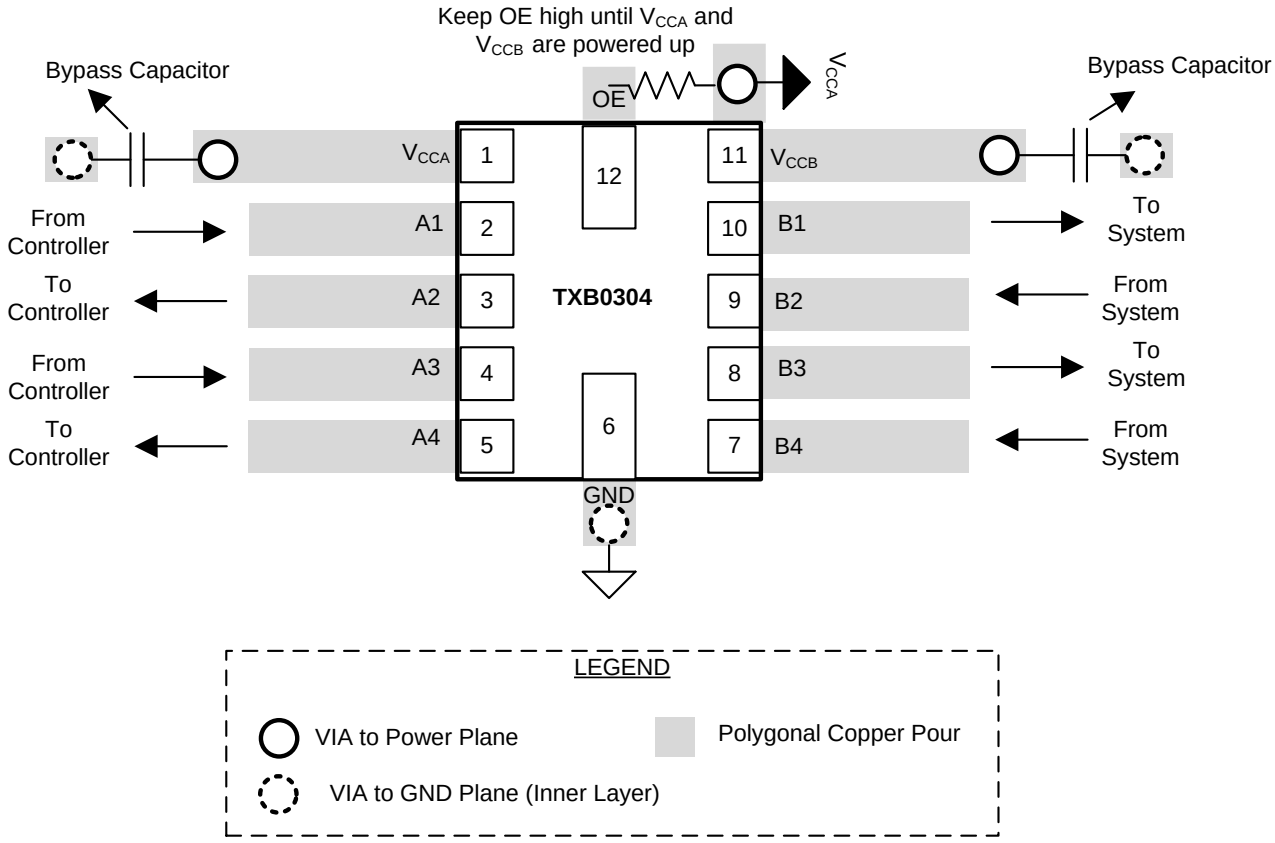


Figure 8. TXB0304 PCB Layout

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

关于 TI TXS010X 产品，请访问 www.ti.com.cn/product/cn/txs0101。

关于 TXB0304 IBIS 模型，请参见 SCEM544。

12.2 文档支持

12.2.1 相关文档

相关文档请参见以下部分：

- 应用报告，*《使用 TXB 型转换器进行电压转换的相关指南》*，SCEA043
- 用户指南，*《TXB0304 评估模块》*,SCEU003

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或"增强型塑料"的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0304RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZTJ	Samples
TXB0304RUTR	ACTIVE	UQFN	RUT	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(737 ~ 73R ~ 73V)	Samples
TXBN0304RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZTK	Samples
TXBN0304RUTR	ACTIVE	UQFN	RUT	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	74R	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

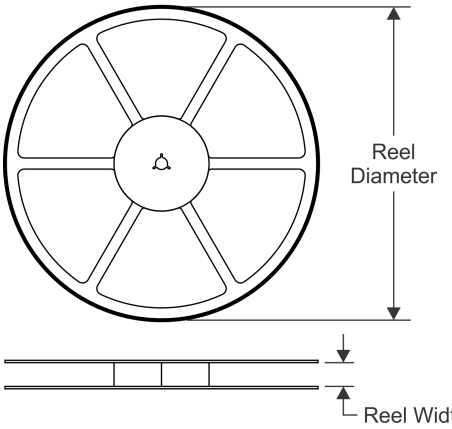
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

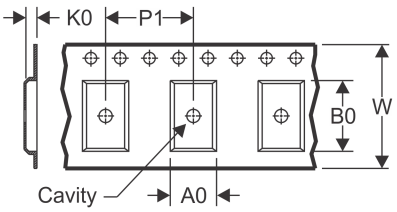
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

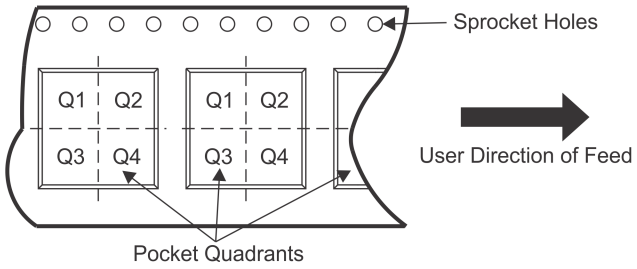


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

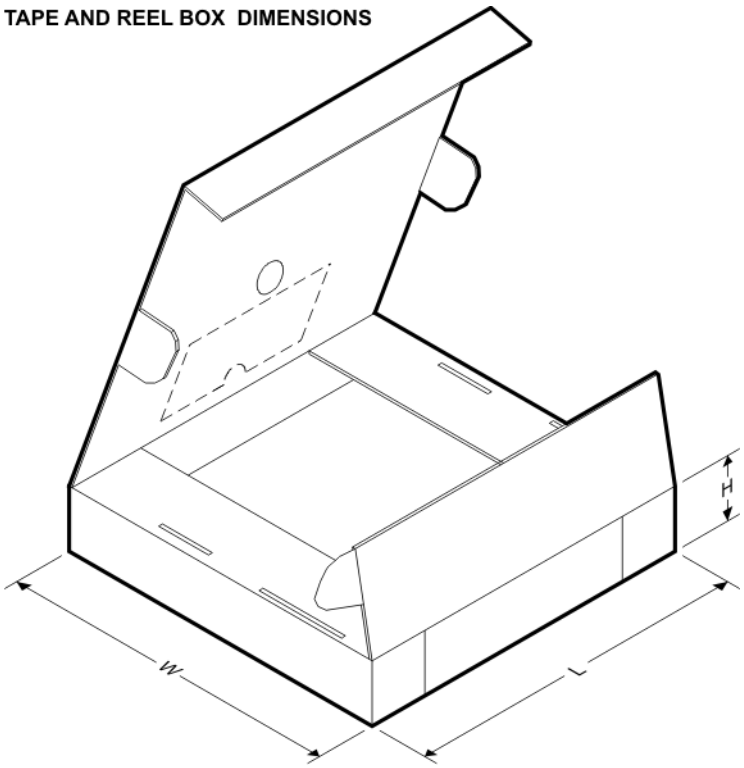
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0304RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1
TXB0304RUTR	UQFN	RUT	12	3000	180.0	9.5	1.9	2.3	0.75	4.0	8.0	Q1
TXBN0304RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1
TXBN0304RUTR	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1

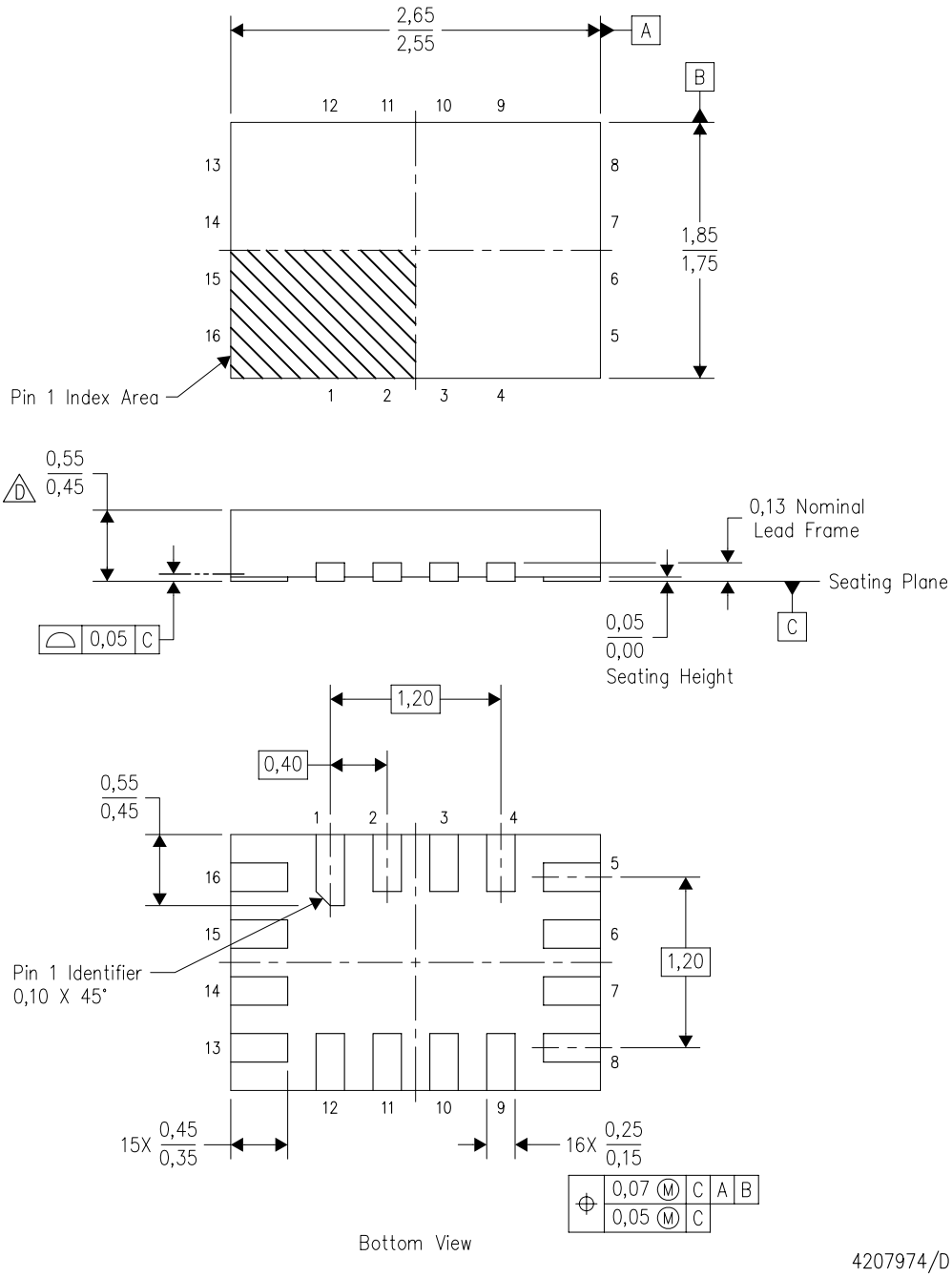
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

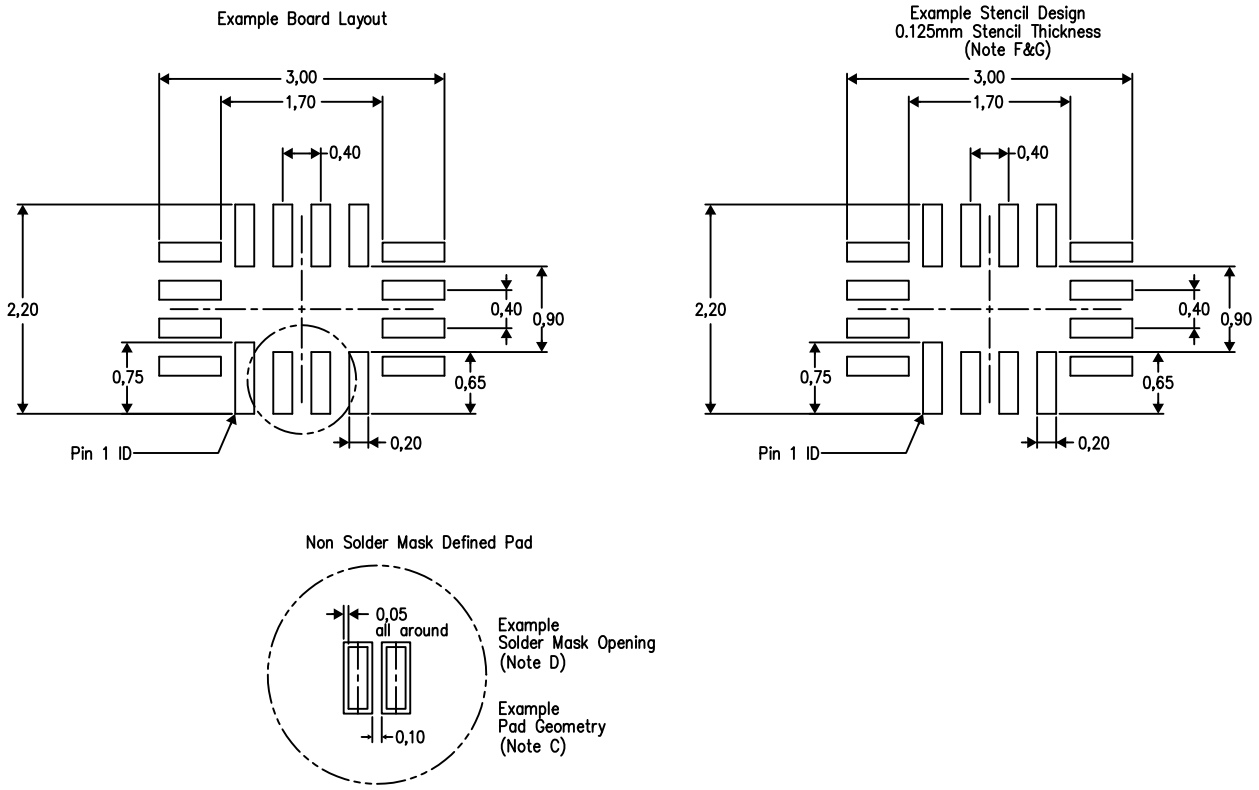
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0304RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0
TXB0304RUTR	UQFN	RUT	12	3000	184.0	184.0	19.0
TXBN0304RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0
TXBN0304RUTR	UQFN	RUT	12	3000	202.0	201.0	28.0

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UFHE, except minimum package thickness.

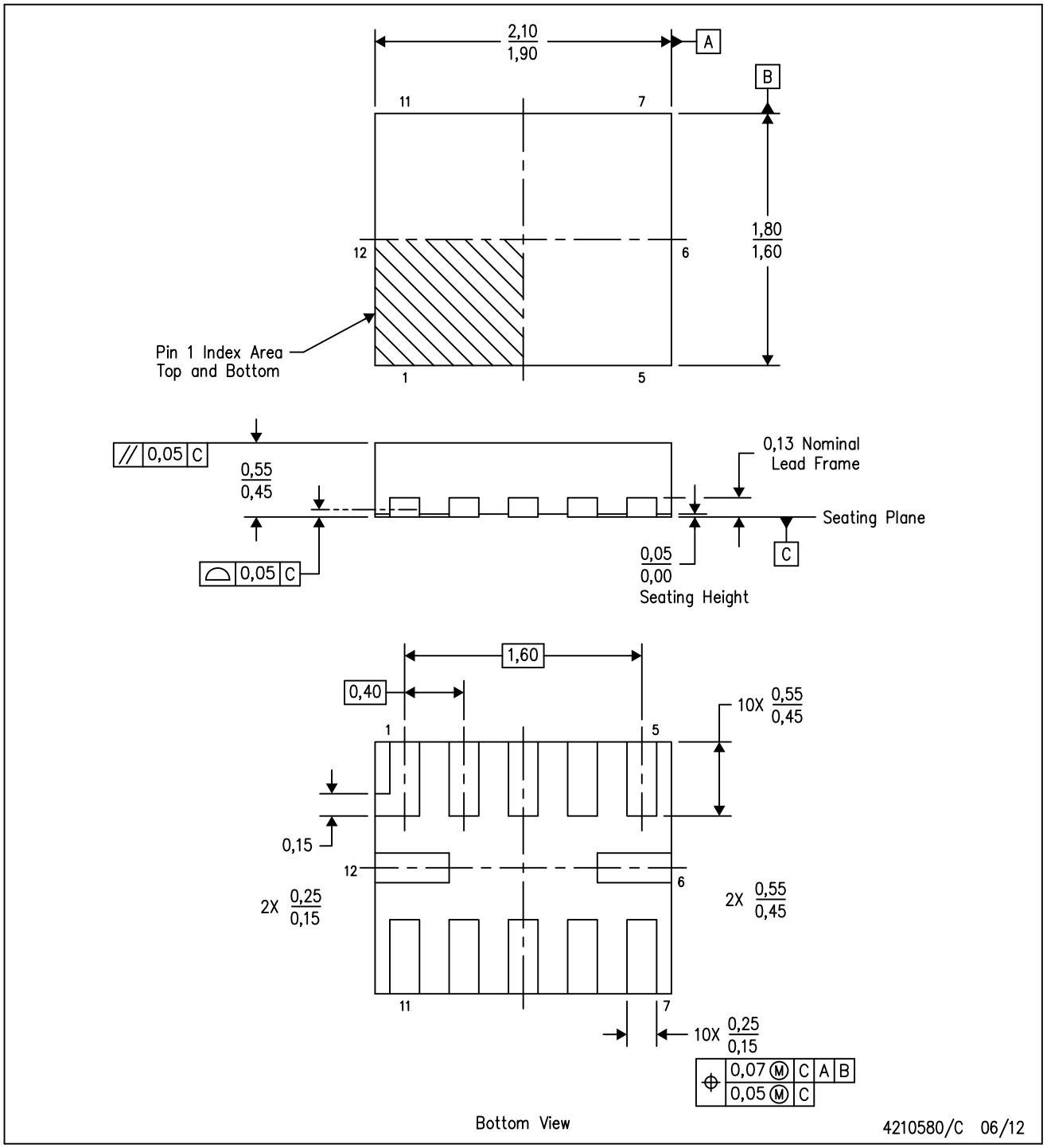
RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



4208244/C 02/13

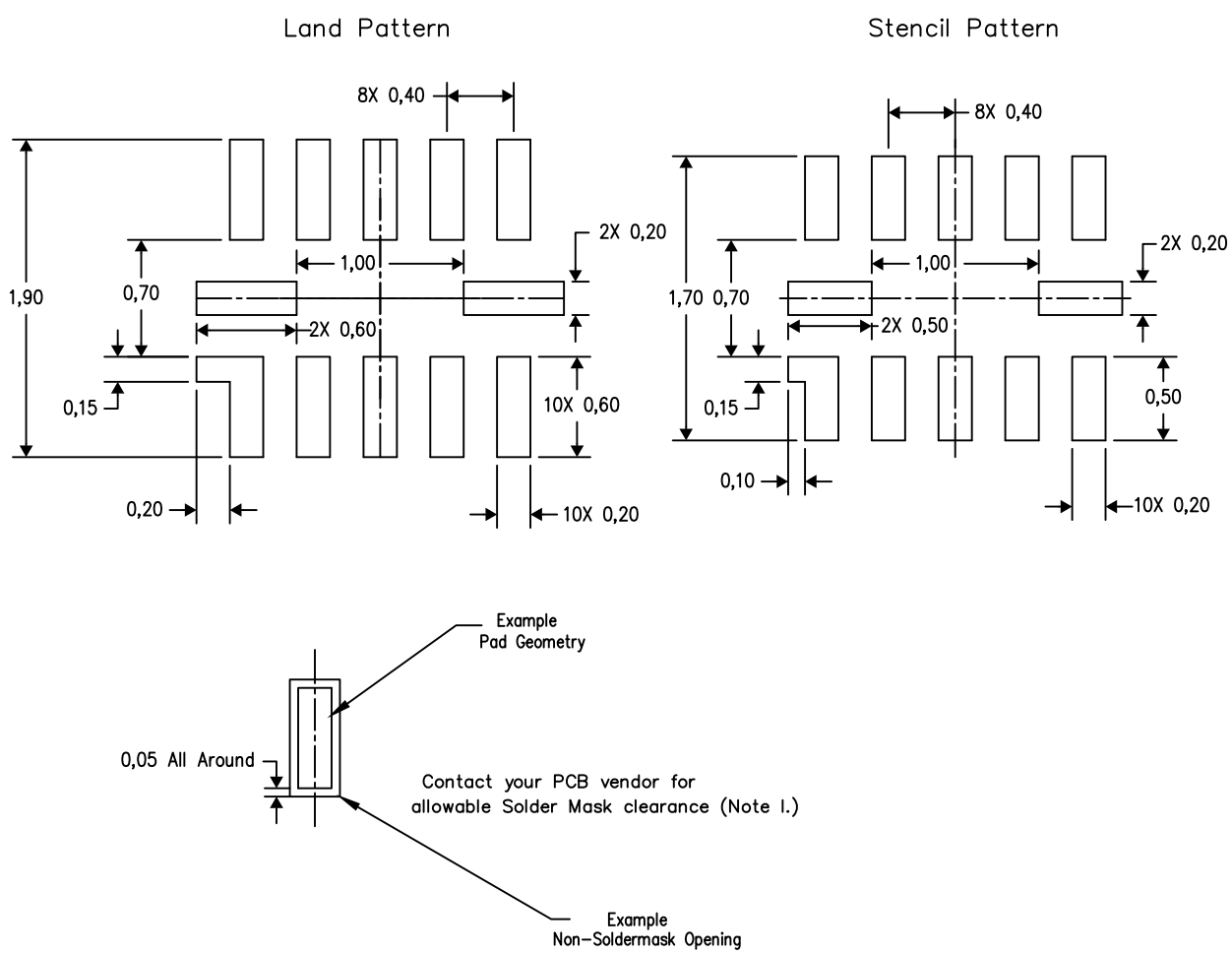
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

RUT (R–PUQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.

RUT (R–PUQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Over–printing land for larger area ratio is not advised due to land width and bridging potential. Exersize extreme caution.
H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
I. Component placement force should be minimized to prevent excessive paste block deformation.

重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (http://www.ti.com/sc/docs/stdterms.htm) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权 负责并确保 应用的安全性， 及设计人员的 应用 （包括应用中使用的所有 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的 应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何 应用前， 将彻底测试该等 应用和 该等应用中所用 TI 产品的 功能。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的 应用， 如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的 应用时， 才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法理授予您任何TI知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等产权包括但不限于任何专利权、版权、屏蔽作品权或与使用TI产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默认的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的 符合 相关功能安全标准和要求的应用。在应用内使用产品的行为本身不会 配有 任何安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和 标准。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的 产品， 并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122