TPS7A41 50V 输入电压、50mA 超高电压线性稳压器

1 特性

- 宽输入电压范围：7V 至 50V
- 准确度：
  - 标称：1%
  - 整个线路、负载和温度范围内：2.5%
- 低静态电流：25μA
- 关断时的静态电流：4.1μA
- 最大输出电流：50mA
- CMOS 逻辑电平兼容的使能引脚
- 可调节输出电压范围：约为 1.175V 至 48V
- 与陶瓷电容搭配工作时保持稳定:
  - 输入电容：≥ 1μF
  - 输出电容：≥ 4.7μF
- 压降电压：290mV
- 内置限流和热关断保护
- 封装方式：高散热性能的微型小外形尺寸封装 (MSOP)-8 PowerPAD™
- 工作温度范围：-40°C 至 125°C

2 应用

- 由工业用总线（具有高电压瞬态）供电的微处理器、微控制器
- 工业自动化
- 电信基础设施
- 车用
- 发光二级管 (LED) 照明
- 偏置电源

3 说明

TPS7A41 器件是一款能够耐受超高电压的线性稳压器，不仅融合了耐热增强型封装 (MSOP-8) 的优势，还能够承受持续直流电压或最高达 50V 的瞬态输入电压。

TPS7A41 与任何高于 4.7μF 的输出电容以及高于 1μF 的输入电容搭配使用时均可保持稳定（过热和浪涌保护）。鉴于这款器件的封装 (MSOP-8) 小巧且可能使用的输出电容也较小，因此实现起来只需占用非常小的电路板空间。此外，TPS7A41 还提供了一个与标准 CMOS 逻辑兼容的使能引脚 (EN)，用于使能低电流关断模式。

TPS7A41 具有热关断和电流限制功能，以便在故障情况下保护系统。MSOP-8 封装的工作温度范围为 T_J = -40°C 至 125°C。

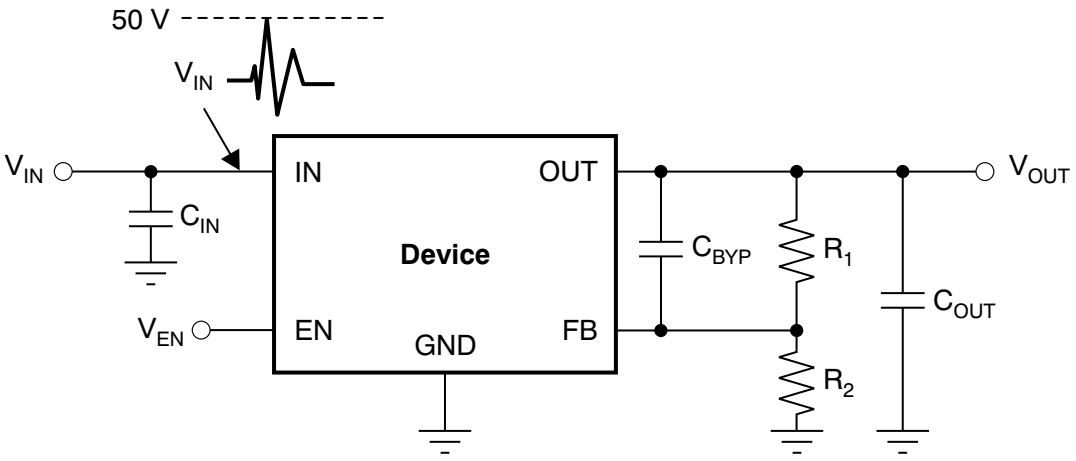
此外，TPS7A41 器件非常适合在电信和工业 应用中利用中间电压轨生成低压电源；该器件不但能够提供一个充分稳压的电压轨，而且能够承受超高的快速电压瞬变并在其间保持稳压状态。这些 功能 相当于一套更为简单且经济高效的电气浪涌保护电路，因此受到各类应用的 使用。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7A41	HVSSOP (8)	3.00mm x 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用图



目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 3
6.1 Absolute Maximum Ratings ... 3
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Dissipation Ratings ... 5
6.7 Typical Characteristics ... 6
7 **Detailed Description** ... 8
7.1 Overview ... 8
7.2 Functional Block Diagram ... 8
7.3 Feature Description ... 8
7.4 Device Functional Modes ... 9
8 **Application and Implementation** ... 10
8.1 Application Information ... 10
8.2 Typical Application ... 11
9 **Power Supply Recommendations** ... 12
10 **Layout** ... 13
10.1 Layout Guidelines ... 13
10.2 Layout Example ... 13
10.3 Thermal Considerations ... 13
10.4 Power Dissipation ... 14
10.5 Package Mounting ... 14
11 器件和文档支持 ... 15
11.1 社区资源 ... 15
11.2 商标 ... 15
11.3 静电放电警告 ... 15
11.4 Glossary ... 15
12 机械、封装和可订购信息 ... 15

4 修订历史记录

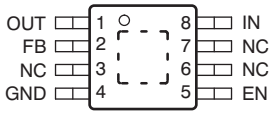
注：之前版本的页码可能与当前版本有所不同。

Changes from Original (December 2011) to Revision A **Page**

- 已添加 *ESD 额定值表*，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分。 ... 1
- Changed maximum *Recommended Operation Conditions* values for VIN, VOUT, and VEN. ... 4

5 Pin Configuration and Functions

DGN Package
8-Pin HVSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Regulator output. A capacitor greater than 4.7 µF must be tied from this pin to ground to assure stability.
FB	2	I	This pin is the input to the control-loop error amplifier. It is used to set the output voltage of the device.
NC	3	—	Not internally connected. This pin must either be left open or tied to GND.
	6		
	7		
GND	4	—	Ground
EN	5	I	This pin turns the regulator on or off. If $V_{EN} \geq V_{EN\_HI}$ the regulator is enabled. If $V_{EN} \leq V_{EN\_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
IN	8	I	Input supply
PowerPAD	—	—	Solder to printed-circuit-board (PCB) to enhance thermal performance. **NOTE: The PowerPAD is internally connected to GND.** Although it can be left floating, it is highly recommended to connect the PowerPAD to the GND plane.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–0.3	55	V
	OUT pin to GND pin	–0.3	55	V
	OUT pin to IN pin	–55	0.3	V
	FB pin to GND pin	–0.3	2	V
	FB pin to IN pin	–55	0.3	V
	EN pin to IN pin	–55	0.3	V
	EN pin to GND pin	–0.3	55	V
Current	Peak output	Internally limited		
Temperature	Operating junction temperature, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
VIN	7		50	V
VOUT	1.161		48	V
VEN	0		50	V
IOUT	0		50	mA

6.4 Thermal Information

THERMAL METRIC (1)		TPS7A41 DGN (HVSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 2 V or V_{IN} = 7 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, and FB tied to OUT, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		7		50	V
V_{REF}	Internal reference	T_J = 25°C, V_{FB} = V_{REF}, V_{IN} = 9 V, I_{OUT} = 25 mA	1.161	1.173	1.185	V
V_{OUT}	Output voltage range(1)	V_{IN} ≥ $V_{OUT(NOM)}$ + 2 V	V_{REF}		48	V
	Nominal accuracy	T_J = 25°C, V_{IN} = 9 V, I_{OUT} = 25 mA	–1		1	$\%V_{OUT}$
	Overall accuracy	$V_{OUT(NOM)}$ + 2 V ≤ V_{IN} ≤ 24 V(2) 100 µA ≤ I_{OUT} ≤ 50 mA	–2.5		2.5	$\%V_{OUT}$
$\Delta V_{O(\Delta VI)}$	Line regulation	7 V ≤ V_{IN} ≤ 50 V		0.03		$\%V_{OUT}$
$\Delta V_{O(\Delta VL)}$	Load regulation	100 µA ≤ I_{OUT} ≤ 50 mA		0.31		$\%V_{OUT}$
V_{DO}	Dropout voltage	V_{IN} = 17 V, $V_{OUT(NOM)}$ = 18 V, I_{OUT} = 20 mA		290		mV
		V_{IN} = 17 V, $V_{OUT(NOM)}$ = 18 V, I_{OUT} = 50 mA		0.78	1.3	V
I_{LIM}	Current limit	V_{OUT} = 90% $V_{OUT(NOM)}$, V_{IN} = 7 V, T_J ≤ 85°C	51	117	200	mA
		V_{OUT} = 90% $V_{OUT(NOM)}$, V_{IN} = 9 V	51	128	200	mA
I_{GND}	Ground current	7 V ≤ V_{IN} ≤ 50 V, I_{OUT} = 0 mA		25	65	µA
		I_{OUT} = 50 mA		25		µA
I_{SHDN}	Shutdown supply current	V_{EN} = 0.4 V		4.1	20	µA
I_{FB}	Feedback current(3)		–0.1	0.01	0.1	µA
I_{EN}	Enable current	7 V ≤ V_{IN} ≤ 50 V, V_{IN} = V_{EN}		0.02	1	µA
V_{EN_HI}	Enable high-level voltage		1.5		V_{IN}	V
V_{EN_LO}	Enable low- level voltage		0		0.4	V
V_{NOISE}	Output noise voltage	V_{IN} = 12 V, $V_{OUT(NOM)}$ = V_{REF}, C_{OUT} = 10 µF, BW = 10 Hz to 100 kHz		58		μV_{RMS}
		V_{IN} = 12 V, $V_{OUT(NOM)}$ = 5 V, C_{OUT} = 10 µF, C_{BYP}(4) = 10 nF, BW = 10 Hz to 100 kHz		73		μV_{RMS}
PSRR	Power-supply rejection ratio	V_{IN} = 12 V, $V_{OUT(NOM)}$ = 5 V, C_{OUT} = 10 µF, C_{BYP}(4) = 10 nF, f = 100 Hz		65		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		170		°C
		Reset, temperature decreasing		150		°C
T_J	Operating junction temperature range		–40		125	°C

(1) To ensure stability at no-load conditions, a current from the feedback resistive network greater than or equal to 10 µA is required.
(2) Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load ($P \approx (V_{IN} - V_{OUT}) \times I_{OUT}$ = (24 V – V_{REF}) × 50 mA ≈ 1.14 W). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heatsinking.
(3) I_{FB} > 0 flows out of the device.
(4) C_{BYP} refers to a bypass capacitor connected to the FB and OUT pins.

6.6 Dissipation Ratings

BOARD	PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$	DERATING FACTOR ABOVE T_A = 25°C	T_A ≤ 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
High-K(1)	DGN	55.9°C/W	8.47°C/W	16.6 mW/°C	1.83 W	1.08 W	0.833 W

(1) The JEDEC High-K (2s2p) board design used to derive this data was a 3-inch x 3-inch multilayer board with 2-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

6.7 Typical Characteristics

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 2 V or V_{IN} = 9 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, and FB tied to OUT, unless otherwise noted.

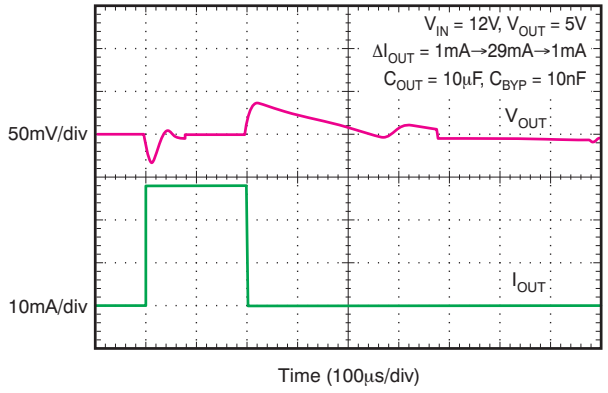


Figure 1. Load Transient Response

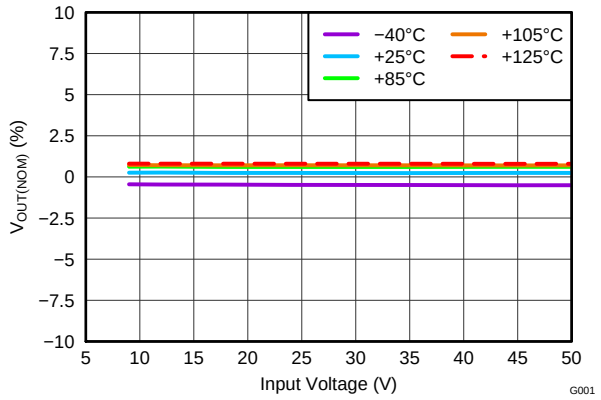


Figure 2. Line Regulation

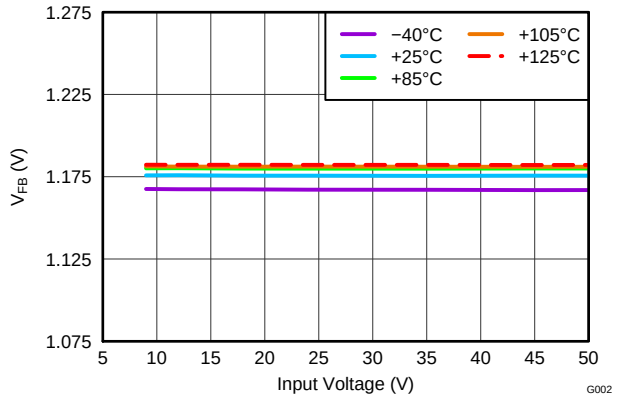


Figure 3. Feedback Voltage

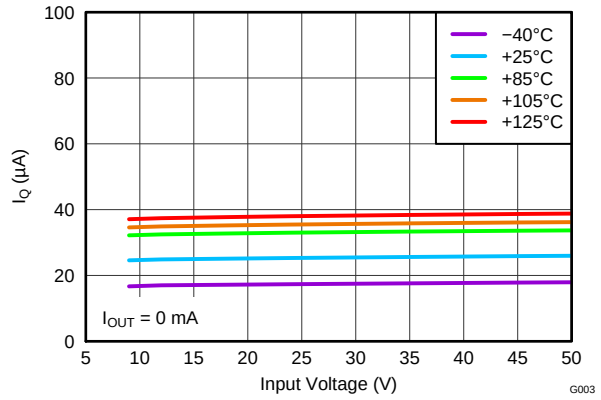


Figure 4. Quiescent Current vs Input Voltage

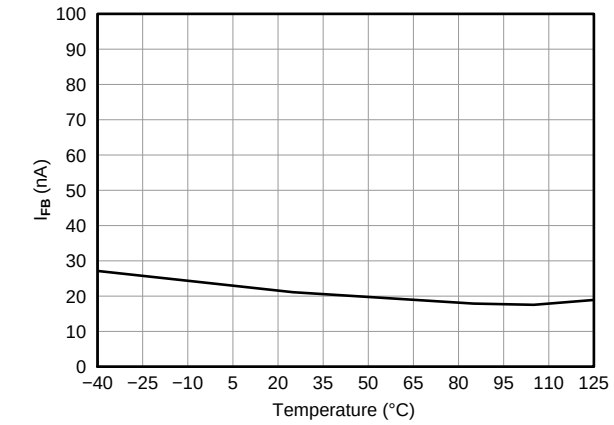


Figure 5. Feedback Current

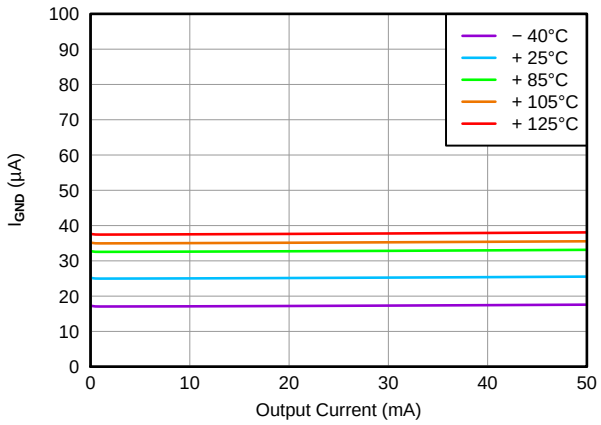


Figure 6. Ground Current

Typical Characteristics (continued)

At T_J = –40°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 2 V or V_{IN} = 9 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, and FB tied to OUT, unless otherwise noted.

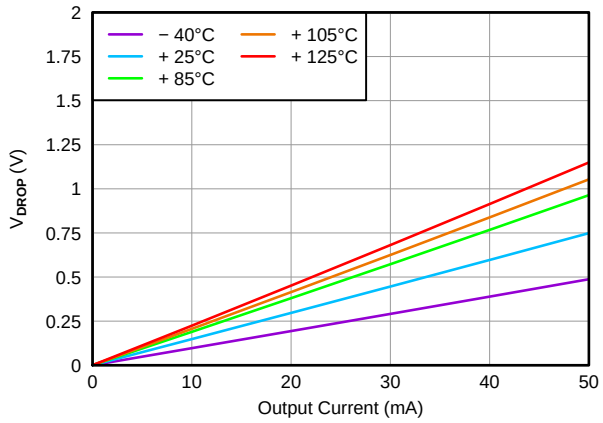


Figure 7. Dropout Voltage

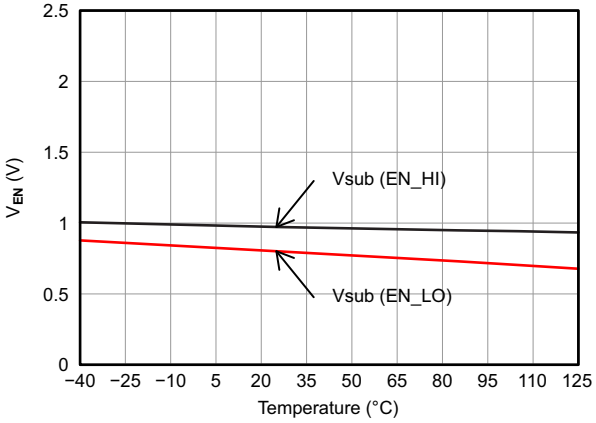


Figure 8. Enable Threshold Voltage

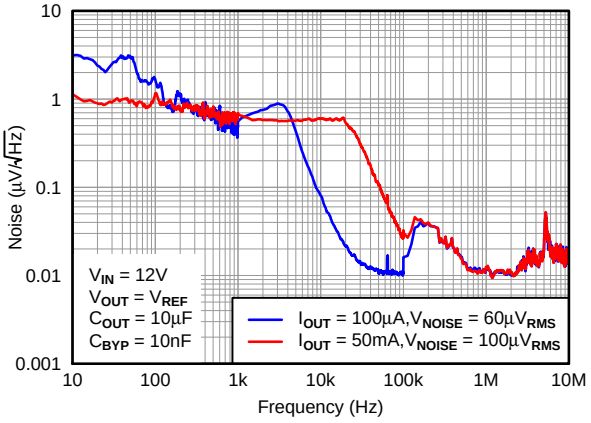


Figure 9. Output Spectral Noise Density

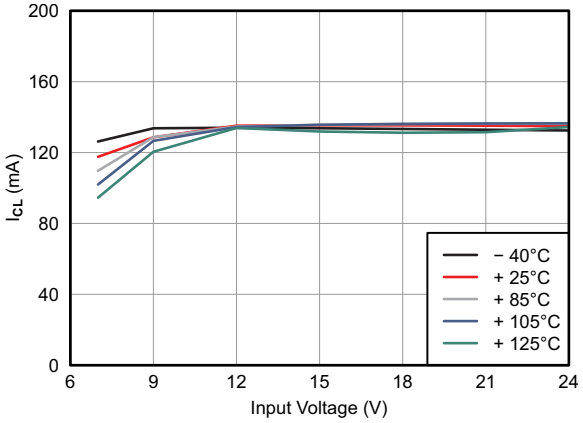


Figure 10. Current Limit

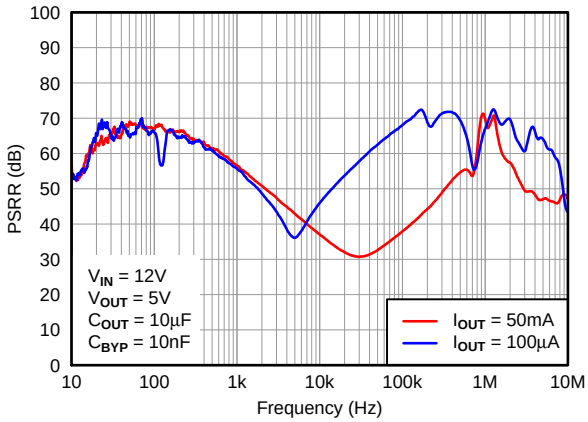


Figure 11. Power-Supply Rejection Ratio

7 Detailed Description

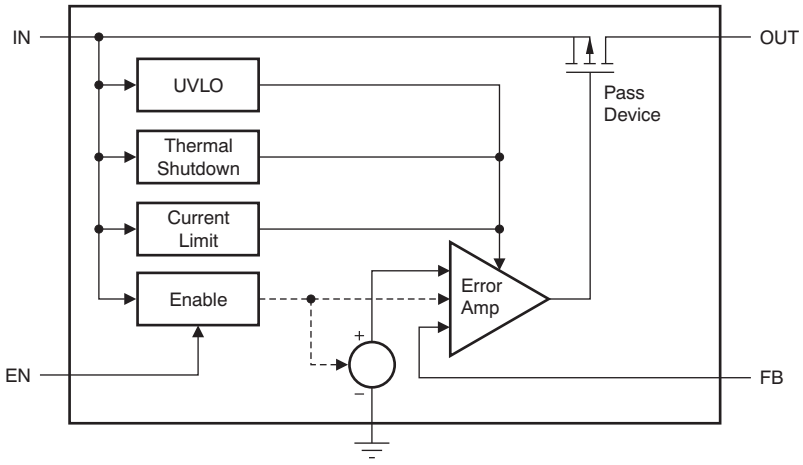
7.1 Overview

The TPS7A4101 belongs to a new generation of linear regulators that use an innovative BiCMOS process technology to achieve very high maximum input and output voltages.

This process not only allows the TPS7A4101 to maintain regulation during very fast high-voltage transients up to 50 V, but it also allows the TPS7A4101 to regulate from a continuous high-voltage input rail. Unlike other regulators created using bipolar technology, the TPS7A4101 ground current is also constant over its output current range, resulting in increased efficiency and lower power consumption.

These features, combined with a high thermal performance MSOP-8 PowerPAD package, make this device ideal for industrial and telecom applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable Pin Operation

The TPS7A4101 provides an enable pin (EN) feature that turns on the regulator when V_{EN} > 1.5 V.

7.3.2 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to a maximum of 125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A41 device has been designed to protect against overload conditions. The protection circuitry was not intended to replace proper heatsinking. Continuously running the TPS7A4001 device into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device (as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN\_HI}$	$I_{OUT} < I_{LIM}$	$T_J < 125°C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN\_HI}$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{EN\_LO}$	—	$T_J > 170°C$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Adjustable Operation

The TPS7A4101 has an output voltage range of approximately 1.175 V to 48 V. The nominal output voltage of the device is set by two external resistors, as shown in Figure 12.

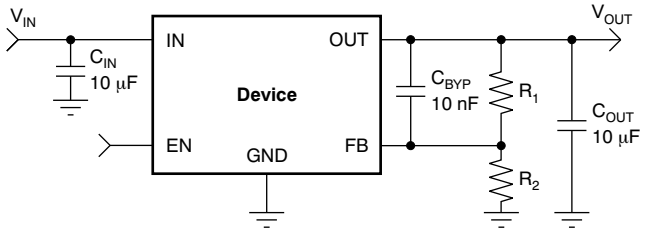


Figure 12. Adjustable Operation for Maximum AC Performance

R_1 and R_2 can be calculated for any output voltage range using the formula shown in Equation 1. To ensure stability under no-load conditions, this resistive network must provide a current greater than or equal to 10 µA.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right), \quad \text{where } \frac{V_{OUT}}{R_1 + R_2} \geq 10\ \mu A \tag{1}$$

If greater voltage accuracy is required, take into account the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

8.1.2 Transient Voltage Protection

One of the primary applications of the TPS7A4101 is to provide transient voltage protection to sensitive circuitry that may be damaged in the presence of high-voltage spikes.

This transient voltage protection can be more cost-effective and compact compared to topologies that use a transient voltage suppression (TVS) block.

8.2 Typical Application

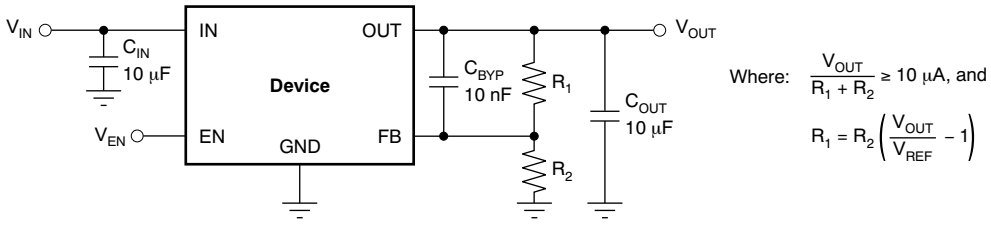


Figure 13. Example Circuit to Maximize Transient Performance

8.2.1 Design Requirements

For this design example, use the following parameters listed in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
V_{IN}	12 V, with 50 V surge tolerance
V_{OUT}	5 V (ideal), 4.981 V (actual)
I_{OUT}	28 mA
Accuracy	5 %
R1, R2	162 kΩ, 49.9 kΩ

8.2.2 Detailed Design Procedure

The maximum value of total feedback resistance can be calculated to be 500 kΩ. Equation 1 was used to calculate R1 and R2, and standard 1% resistors were selected to keep the accuracy within the 5% allocation. 10-uF ceramic input and output capacitors were selected, along with a 10-nF bypass capacitor for optimal AC performance.

8.2.2.1 Capacitor Recommendations

Low equivalent series resistance (ESR) capacitors should be used for the input, output, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved over-temperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

High ESR capacitors may degrade PSRR.

8.2.2.2 Input and Output Capacitor Requirements

The TPS7A4101 high voltage linear regulator achieves stability with a minimum output capacitance of 4.7 µF and input capacitance of 1 µF; however, TI highly recommends using 10-µF output and input capacitors to maximize AC performance.

8.2.2.3 Bypass Capacitor Requirements

Although a bypass capacitor (C_{BYP}) is not needed to achieve stability, TI highly recommends using a 10-nF bypass capacitor to maximize AC performance (including line transient, noise and PSRR).

8.2.2.4 Maximum AC Performance

To maximize line transient, noise, and PSRR performance, TI recommends including 10-µF (or higher) input and output capacitors, and a 10-nF bypass capacitor; see Figure 12. The solution shown delivers minimum noise levels of 58 μV_{RMS} and power-supply rejection levels above 36 dB from 10 Hz to 10 MHz.

8.2.2.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

The presence of the C_{BYP} capacitor may greatly improve the TPS7A4101 line transient response, as noted in Figure 1.

8.2.3 Application Curve

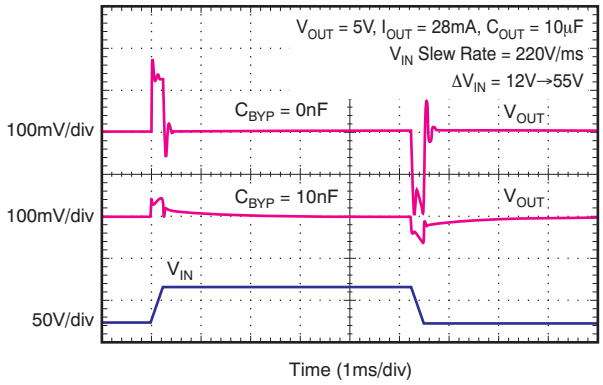


Figure 14. Line Transient Response vs C_{BYP}

9 Power Supply Recommendations

The input supply for the LDO should not exceed its recommended operating conditions (7 V to 50 V). The input voltage should provide adequate headroom for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance. The input and output supplies should also be bypassed with 10-µF capacitors located near the input and output pins. There should be no other components located between these capacitors and the pins.

10 Layout

10.1 Layout Guidelines

To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, C_{BYP}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for TPS7A41 evaluation board, available at www.ti.com.

10.2 Layout Example

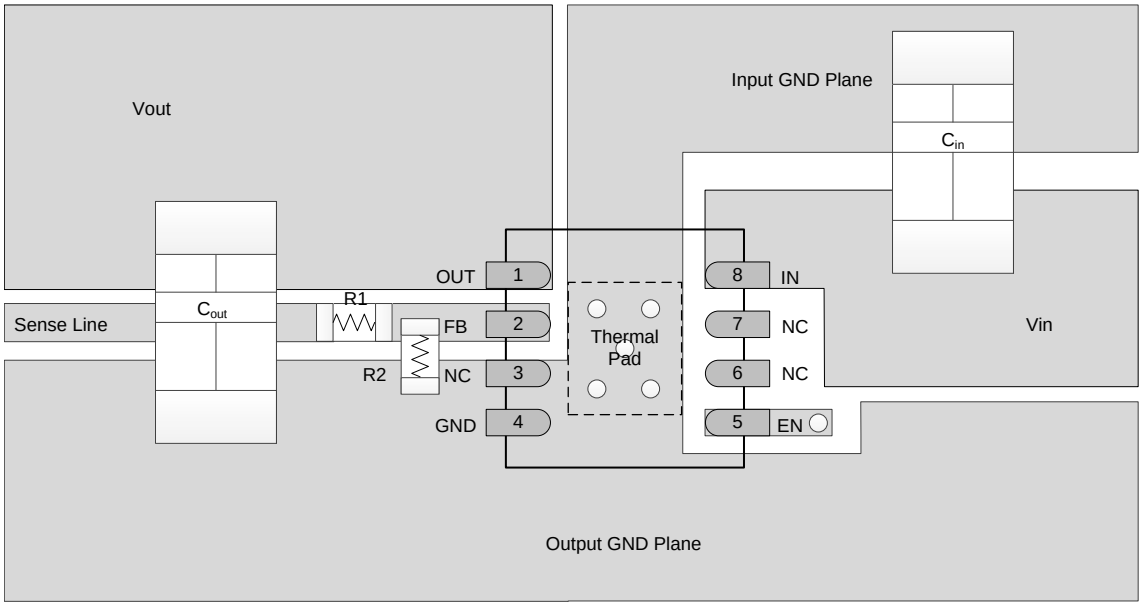


Figure 15. Recommended Layout Example

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to a maximum of 125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

Thermal Considerations (continued)

The internal protection circuitry of the TPS7A4101 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A4101 into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Dissipation Ratings*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} \quad (2)$$

10.5 Package Mounting

Solder pad footprint recommendations for the TPS7A4101 are available at *机械、封装和可订购信息* and at www.ti.com.

11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或"增强型塑料"的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A4101DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBB	Samples
TPS7A4101DGNT	ACTIVE	MSOP-PowerPAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

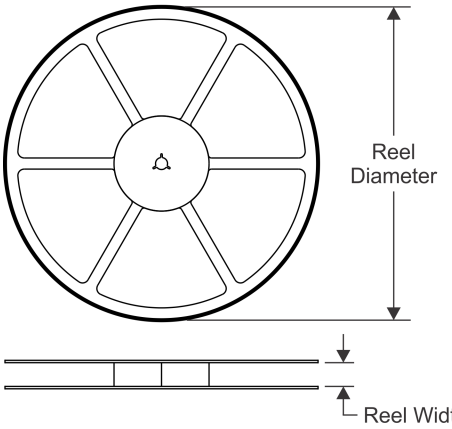
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

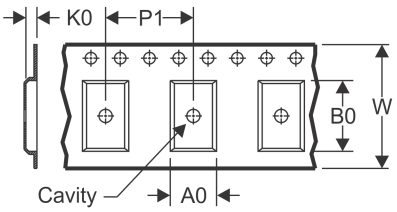
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

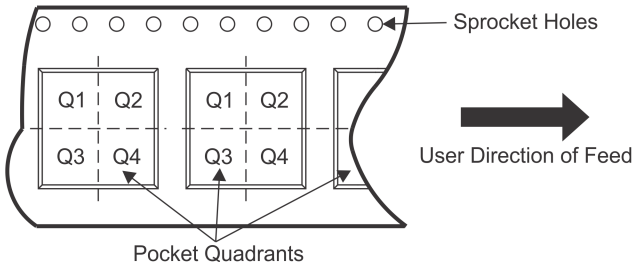


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

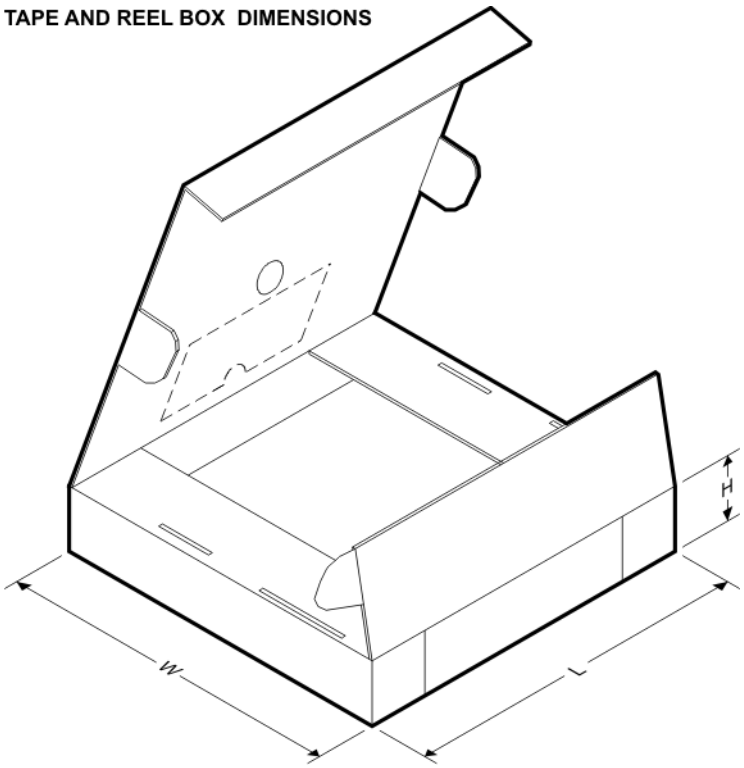
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A4101DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A4101DGNT	MSOP-Power PAD	DGN	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

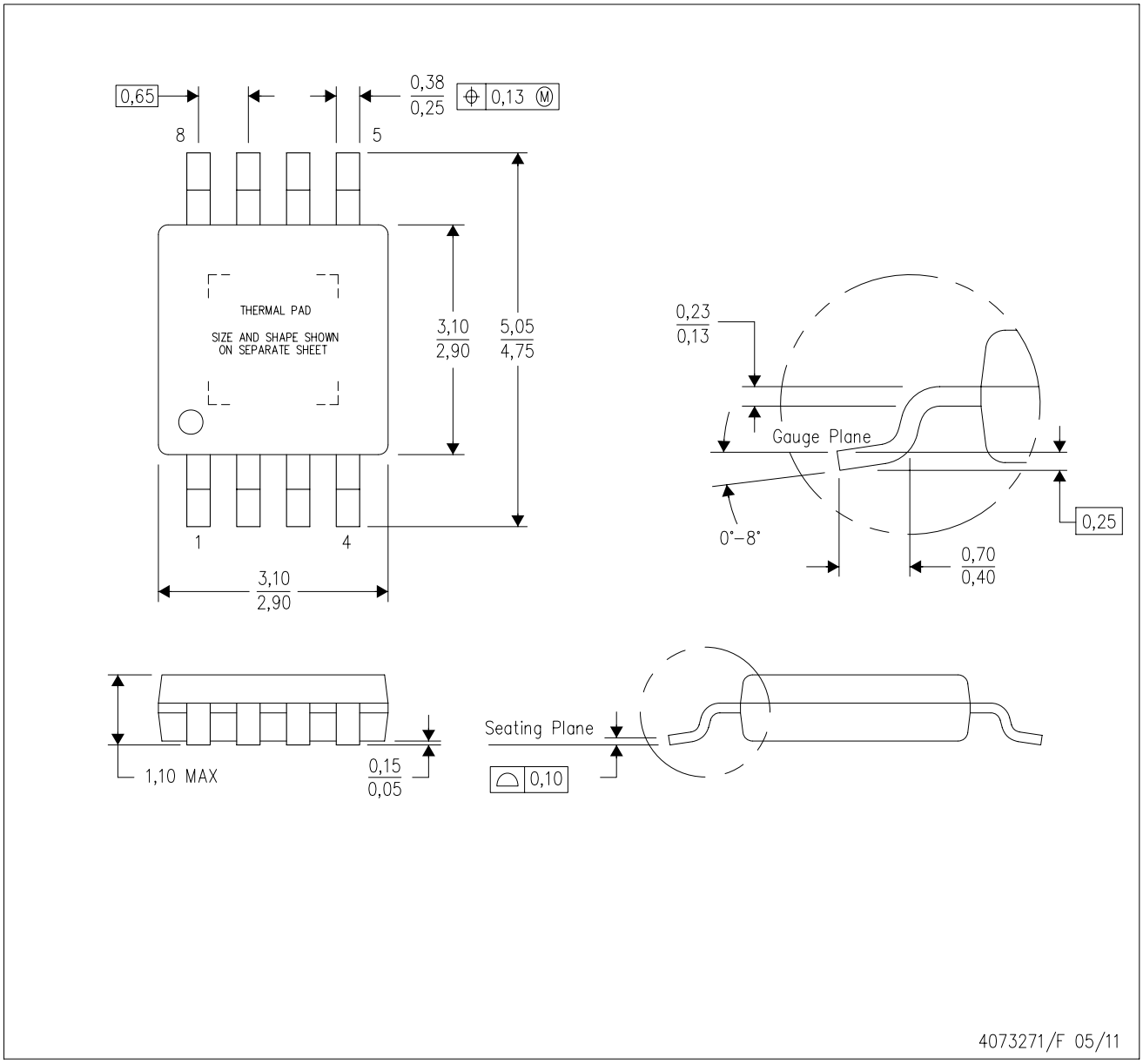
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A4101DGNR	MSOP-PowerPAD	DGN	8	2500	346.0	346.0	35.0
TPS7A4101DGNT	MSOP-PowerPAD	DGN	8	250	203.0	203.0	35.0

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

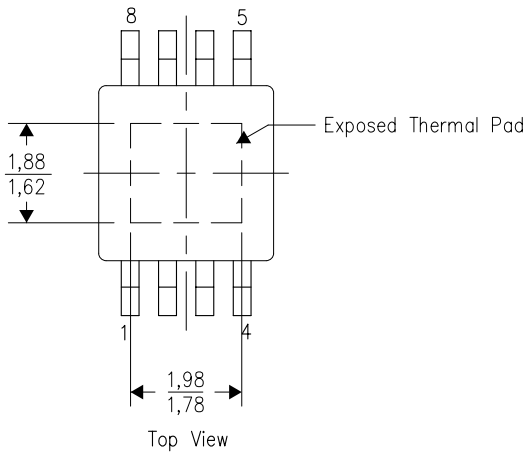
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



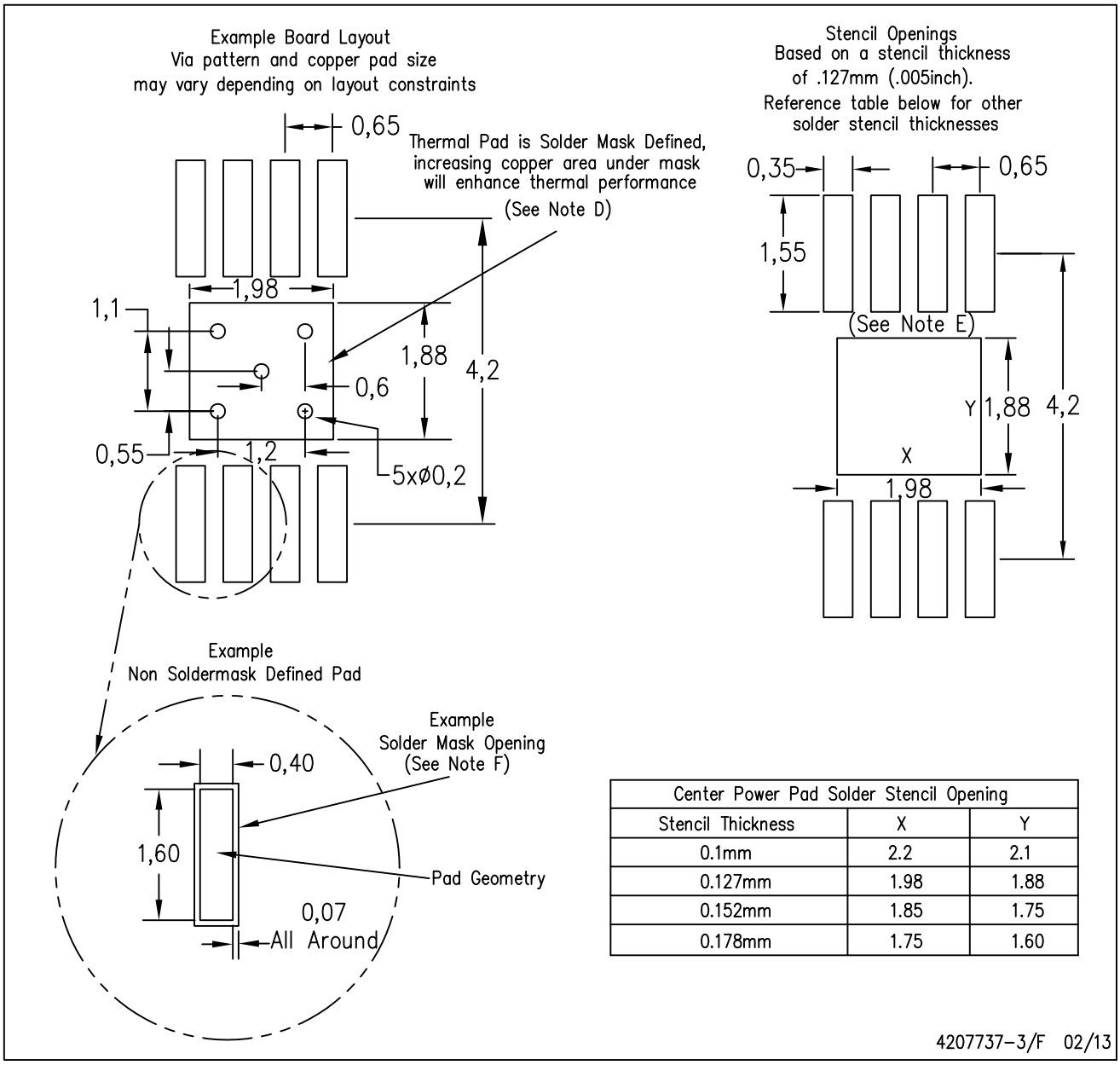
Exposed Thermal Pad Dimensions

4206323–3/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.2	2.1
0.127mm	1.98	1.88
0.152mm	1.85	1.75
0.178mm	1.75	1.60

4207737–3/F 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (http://www.ti.com/sc/docs/stdterms.htm) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权 负责并确保 应用的安全性， 及设计人员的 应用 （包括应用中使用的所有 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的 应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何 应用前， 将彻底测试该等 应用和 该等应用中所用 TI 产品的 功能。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的 应用， 如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的 应用时， 才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法理授予您任何TI知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等产权包括但不限于任何专利权、版权、屏蔽作品权或与使用TI产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默认的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的 符合 相关功能安全标准和要求的应用。在应用内使用产品的行为本身不会 配有 任何安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和 标准。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的 产品， 并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122