INA826 具有轨到轨输出的高精度、200μA 电源电流、3V 至 36V 电源仪表放大器

1 特性

- 输入共模范围：包括 V–
- 共模抑制：
  - 最小值为 104dB (G = 10)
  - 5kHz 时的最小值为 100dB (G = 10)
- 电源抑制：最小值为 100dB (G = 1)
- 低偏移电压：最大值为 150μV
- 增益漂移：1ppm/°C (G = 1)，35ppm/°C (G > 1)
- 噪声：18nV/√Hz，G ≥ 100
- 带宽：1MHz (G = 1)，60kHz (G = 100)
- 输入保护电压高达 ±40 V
- 轨到轨输出
- 电源电流：200μA
- 电源范围：
  - 单电源：3V 至 36V
  - 双电源：±1.5V 至 ±18V
- 特定温度范围：
  –40°C 至 +125°C
- 封装：8 引脚 VSSOP、SOIC 和 WSON

2 应用

- 工业过程控制
- 断路器
- 电池检测仪
- 心电图 (ECG) 放大器
- 电力自动化
- 医疗仪表
- 便携式仪表

3 说明

INA826 为低成本仪表放大器，功耗极低且能够在极宽的单电源或双电源范围内工作。可通过单个外部电阻在 1 到 1000 范围内设置增益。该器件在过热条件下具有很好的稳定性，即使在 G > 1 时，也可实现只有 35ppm/°C（最大值）的低增益漂移。

INA826 经优化可在频率高达 5kHz 时提供超过 100dB 的出色共模抑制比 (G = 10)。G = 1 时，在从负电源直至 1V 正电源的整个输入共模范围内共模抑制比将超过 84dB。INA826 采用轨到轨输出，非常适合通过 3V 单电源和高达 ±18V 的双电源供电的低电压操作。

附加电路可通过将输入电流限制在 8mA 以下来防止输入出现超出电源电压的过压情况（高达 ±40V）。

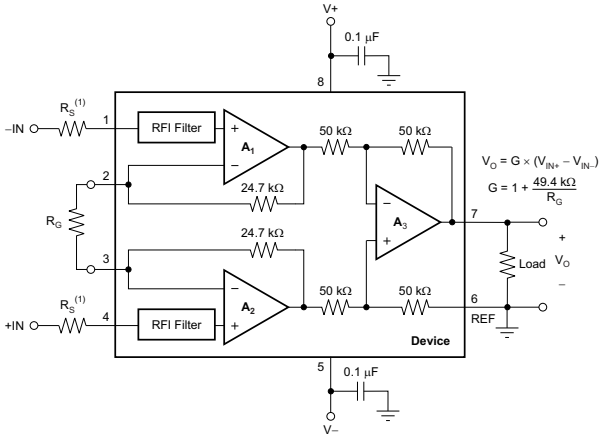
INA826 采用 8 引脚 SOIC、VSSOP 以及微型 3mm × 3mm WSON 表面贴装封装。所有版本的额定工作温度范围均为 -40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
INA826	SOIC (8)	4.90mm x 3.91mm
	WSON (8)	3.00mm × 3.00mm
	VSSOP (8)	3.00mm x 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

通用仪表放大器



(1) 如果输入电压始终高于 [(V–) – 2V] 或将单电源电流驱动能力限制在 3.5mA 以下，则此电阻可选；更多详细信息，请参见*Input Protection*部分。

目录

4 修订历史记录

Changes from Revision E (April 2013) to Revision F **Page**

- 已增加*器件信息表*、*ESD 额定值表*、*建议运行条件表*、*特性 说明*部分、*器件功能模式*部分、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- 已增加 TI 设计 ... 1
- 已将文档标题中的 2.7V 更改为 3V ... 1
- 已通篇将微型小外形尺寸 (MSOP) 更改为超薄小外形尺寸 (VSSOP)，将小外形尺寸 (SO) 更改为小外形尺寸集成电路 (SOIC)，将 DRG 更改为晶圆级小外形无引线 (WSON) ... 1
- 已更改*电源范围* 特性 分项的最小电压 ... 1
- 已更改*封装* 特性 要点 ... 1
- 已更改第 1 页的图 ... 1
- 已更改 描述 部分，其中包括对少量内容进行重新编写、对封装进行重命名以及将单电源电压值从 2.7V 更改为 3V ... 1
- Changed title of *Device Comparison Table* ... 4
- Deleted DGK Package*Package/Ordering Information* table ... 4
- Changed *Temperature* parameter symbols in *Absolute Maximum Ratings* table ... 5
- Changed Input, *Differential impedance* and *Common-mode impedance* parameter symbols in *Electrical Characteristics* table ... 6
- Changed Input, V_{CM} parameter test conditions in *Electrical Characteristics* table ... 6
- Deleted Gain, *Range of gain parameter* symbol from *Electrical Characteristics* table ... 7
- Changed Power Supply, V_S parameter test conditions and minimum specifications in *Electrical Characteristics* table ... 7
- Changed V_S voltage to 3.0 V and red V_{REF} trace to 1.5 V in Figure 9 and Figure 10 ... 9
- Changed V_S voltage level to 3.0 V in Figure 29 ... 12
- Changed blue V_S trace value to 3.0 V in Figure 36 ... 13
- Changed conditions of Figure 47 and Figure 48 ... 15
- Changed 2.7 V to 3 V and 1.35 V to 1.5 V in *Operating Voltage* section ... 24
- Changed TINA-TI simulation circuit links in *Using TINA-TI SPICE-Based Analog Simulation Program with the INA826* section ... 29

Changes from Revision D (March 2013) to Revision E **Page**

- Deleted package marking column from Package/Ordering Information table 4

Changes from Revision C (March 2012) to Revision D **Page**

- Changed Input voltage range parameter specification value in *Absolute Maximum Ratings* table 5

Changes from Revision B (December 2011) to Revision C **Page**

- 已更改 产品状态，从混合状态更改为量产数据..... 1
- Deleted gray shading and footnote 2 from Package/Ordering Information table 4
- Changed DFN-8 package to production data 4

Changes from Revision A (September 2011) to Revision B **Page**

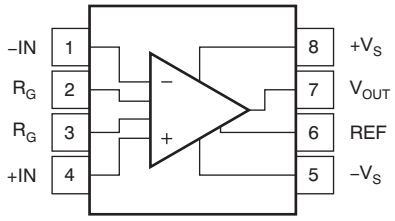
- Deleted gray from SO-8 row in Package/Ordering Information 4

5 Device Comparison Table

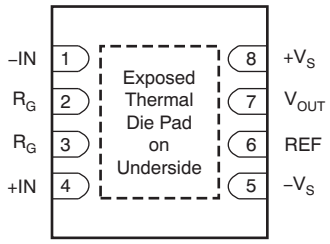
DEVICE	DESCRIPTION
INA333	25-μV V_{OS}, 0.1 μV/°C V_{OS} drift, 1.8-V to 5-V, RRO, 50-μA I_Q, chopper-stabilized INA
PGA280	20-mV to ±10-V programmable gain IA with 3-V or 5-V differential output; analog supply up to ±18 V
INA159	G = 0.2 V differential amplifier for ±10-V to 3-V and 5-V conversion
PGA112	Precision programmable gain op amp with SPI™ interface

6 Pin Configuration and Functions

DGK and D Package
8-Pin SOIC, VSSOP
Top View



DRG Package
8-Pin WSON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	SOIC, VSSOP	WSON		
–IN	1	1	I	Negative (inverting) input
+IN	4	4	I	Positive (noninverting) input
REF	6	6	I	Reference input. This pin must be driven by low impedance.
R_G	2	2	—	Gain setting pin. Place a gain resistor between pin 2 and pin 3.
	3	3		
V_{OUT}	7	7	O	Output
$–V_S$	5	5	—	Negative supply
$+V_S$	8	8	—	Positive supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage		–20	20	V
Signal input pins	Voltage	$(-V_S) - 40$	$(+V_S) + 40$	V
	REF pin	–20	+20	
Output short-circuit(2)		Continuous		
Temperature	Operating, T_A	–50	150	°C
	Junction, T_J		175	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to V_S / 2.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
		Machine model (MM)	±150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	Single supply	3		36	V
	Dual supply	±1.5		±18	
Specified temperature		–40		+125	°C
Operating temperature		–50		+150	°C

7.4 Thermal Information

THERMAL METRIC(1)		INA826			UNIT
		D (SOIC)	DGK (VSSOP)	DRG (WSON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	141.4	215.4	50.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.4	66.3	60.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.6	97.8	25.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.4	10.5	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.1	96.1	25.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	7.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{OSI}	Input stage offset voltage(1)	RTI			40	150	µV
		vs temperature, T_A = –40°C to +125°C			0.4	2	µV/°C
V_{OSO}	Output stage offset voltage(1)	RTI			200	700	µV
		vs temperature, T_A = –40°C to +125°C			2	10	µV/°C
PSRR	Power-supply rejection ratio	G = 1, RTI		100	124		dB
		G = 10, RTI		115	130		
		G = 100, RTI		120	140		
		G = 1000, RTI		120	140		
z_{id}	Differential impedance				20 || 1		GΩ || pF
z_{ic}	Common-mode impedance				10 || 5		GΩ || pF
	RFI filter, –3-dB frequency				20		MHz
V_{CM}	Operating input range(2)			V–		(V+) – 1	V
		V_S = ±1.5 V to ±18 V, T_A = –40°C to +125°C		See Figure 41 to Figure 44			
	Input overvoltage range	T_A = –40°C to 125°C				±40	V
CMRR	Common-mode rejection ratio	At dc to 60 Hz, RTI	G = 1, V_{CM} = (V–) to (V+) – 1 V	84	95		dB
			G = 10, V_{CM} = (V–) to (V+) – 1 V	104	115		
			G = 100, V_{CM} = (V–) to (V+) – 1 V	120	130		
			G = 1000, V_{CM} = (V–) to (V+) – 1 V	120	130		
			G = 1, V_{CM} = (V–) to (V+) – 1 V, T_A = –40°C to +125°C	80			
		At 5 kHz, RTI	G = 1, V_{CM} = (V–) to (V+) – 1 V	84			
			G = 10, V_{CM} = (V–) to (V+) – 1 V	100			
			G = 100, V_{CM} = (V–) to (V+) – 1 V	105			
			G = 1000, V_{CM} = (V–) to (V+) – 1 V	105			
BIAS CURRENT							
I_B	Input bias current	V_{CM} = V_S / 2			35	65	nA
		T_A = –40°C to +125°C				95	
I_{OS}	Input offset current	V_{CM} = V_S / 2			0.7	5	nA
		T_A = –40°C to +125°C				10	
NOISE VOLTAGE							
e_{NI}	Input stage voltage noise(3)	f = 1 kHz, G = 100, R_S = 0 Ω			18	20	nV/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 100, R_S = 0 Ω			0.52		$µV_{PP}$
e_{NO}	Output stage voltage noise(3)	f = 1 kHz, G = 1, R_S = 0 Ω			110	115	nV/√Hz
		f_B = 0.1 Hz to 10 Hz, G = 1, R_S = 0 Ω			3.3		$µV_{PP}$
I_n	Noise current	f = 1 kHz			100		fA/√Hz
		f_B = 0.1 Hz to 10 Hz			5		pA_{PP}

(1) Total offset, referred-to-input (RTI): $V_{OS} = (V_{OSI}) + (V_{OSO} / G)$.
(2) Input voltage range of the INA826 input stage. The input range depends on the common-mode voltage, differential voltage, gain, and reference voltage. See *Typical Characteristic* curves Figure 9 through Figure 16 and Figure 41 through Figure 44 for more information.
(3)

$$\text{Total RTI voltage noise} = \sqrt{(e_{NI})^2 + \left(\frac{e_{NO}}{G}\right)^2}.$$

Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GAIN							
G	Gain equation				$1 + \left(\frac{49.4\ k\Omega}{R_G}\right)$		V/V
	Range of gain			1		1000	V/V
GE	Gain error	G = 1, V_O = ±10 V			±0.003%	±0.015%	
		G = 10, V_O = ±10 V			±0.03%	±0.15%	
		G = 100, V_O = ±10 V			±0.04%	±0.15%	
		G = 1000, V_O = ±10 V			±0.04%	±0.15%	
	Gain vs temperature(4)	G = 1, T_A = –40°C to +125°C			±0.1	±1	ppm/°C
		G > 1, T_A = –40°C to +125°C			±10	±35	
	Gain nonlinearity	G = 1 to 100, V_O = –10 V to +10 V			1	5	ppm
		G = 1000, V_O = –10 V to +10 V			5	20	
OUTPUT							
	Voltage swing	R_L = 10 kΩ		(V–) + 0.1		(V+) – 0.15	V
	Load capacitance stability				1000		pF
Z_O	Open-loop output impedance				See Figure 56		
I_{SC}	Short-circuit current	Continuous to V_S / 2			±16		mA
FREQUENCY RESPONSE							
BW	Bandwidth, –3 dB	G = 1			1		MHz
		G = 10			500		kHz
		G = 100			60		
		G = 1000			6		
SR	Slew rate	G = 1, V_O = ±14.5 V			1		V/µs
		G = 100, V_O = ±14.5 V			1		
t_S	Settling time	0.01%	G = 1, V_{STEP} = 10 V		12		µs
			G = 10, V_{STEP} = 10 V		12		
			G = 100, V_{STEP} = 10 V		24		
			G = 1000, V_{STEP} = 10 V		224		
		0.001%	G = 1, V_{STEP} = 10 V		14		
			G = 10, V_{STEP} = 10 V		14		
			G = 100, V_{STEP} = 10 V		31		
			G = 1000, V_{STEP} = 10 V		278		
REFERENCE INPUT							
R_{IN}	Input impedance				100		kΩ
	Voltage range			(V–)		(V+)	V
	Gain to output				1		V/V
	Reference gain error				0.01%		
POWER SUPPLY							
V_S	Power-supply voltage	Single supply		3		36	V
		Dual supply		±1.5		±18	
I_Q	Quiescent current	V_{IN} = 0 V			200	250	µA
		vs temperature, T_A = –40°C to +125°C			250	300	
TEMPERATURE RANGE							
	Specified			–40		125	°C
	Operating			–50		150	°C

(4) The values specified for G > 1 do not include the effects of the external gain-setting resistor, R_G.

7.6 Typical Characteristics

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

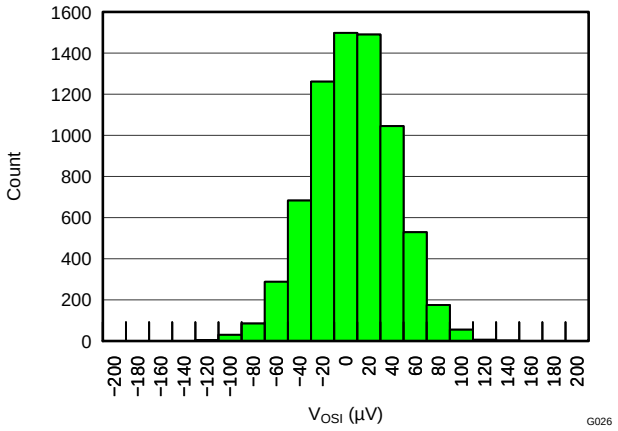


Figure 1. Typical Distribution of Input Offset Voltage

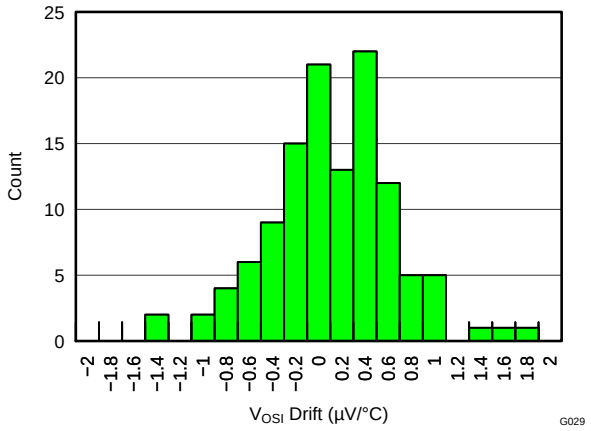


Figure 2. Typical Distribution of Input Offset Voltage Drift

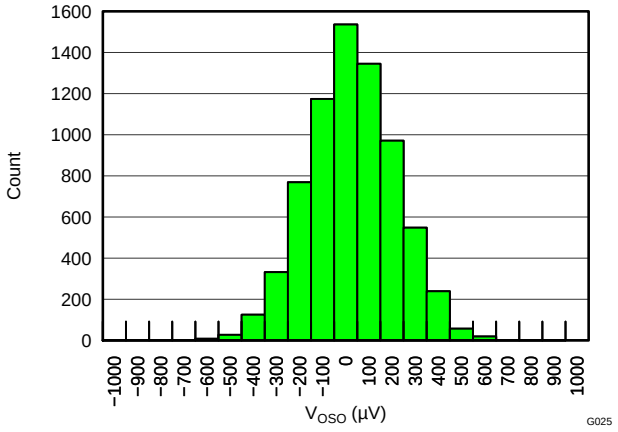


Figure 3. Typical Distribution of Output Offset Voltage

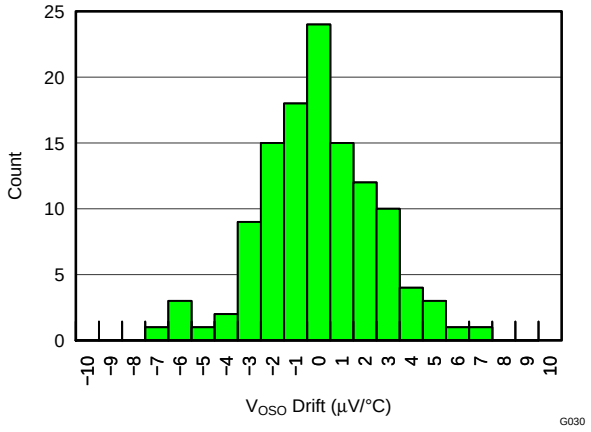


Figure 4. Typical Distribution of Output Offset Voltage Drift

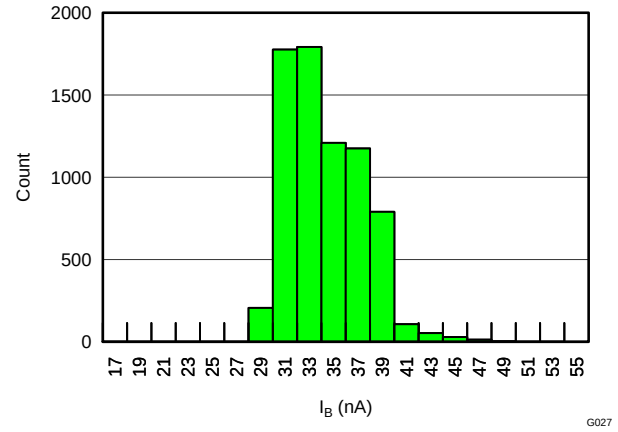


Figure 5. Typical Distribution of Input Bias Current

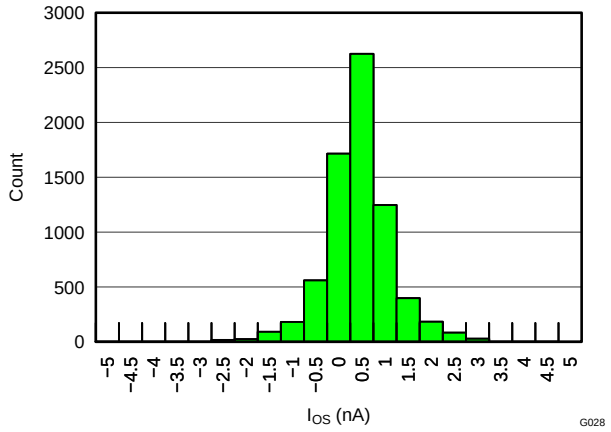


Figure 6. Typical Distribution of Input Offset Current

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

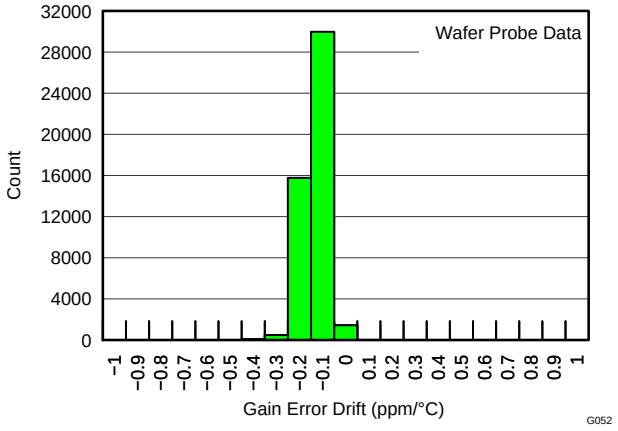


Figure 7. Typical Gain Error Drift Distribution (G = 1)

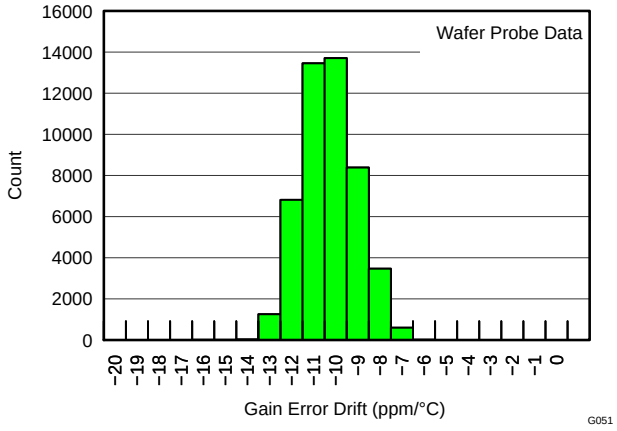


Figure 8. Typical Gain Error Drift Distribution (G > 1)

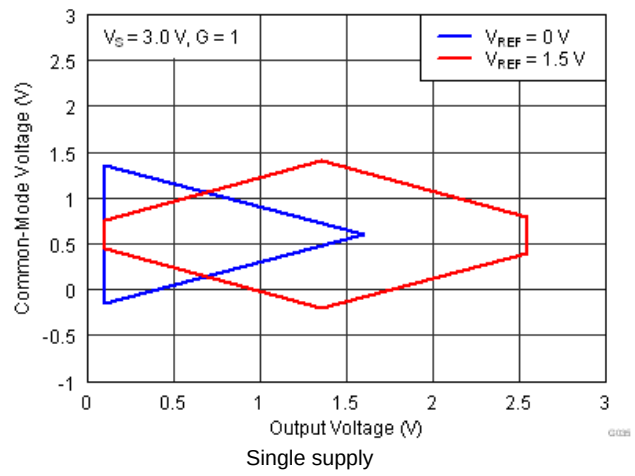


Figure 9. Input Common-Mode Voltage vs Output Voltage

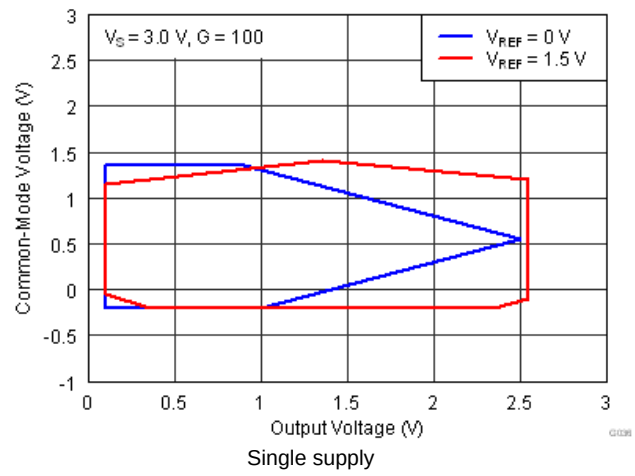


Figure 10. Input Common-Mode Voltage vs Output Voltage

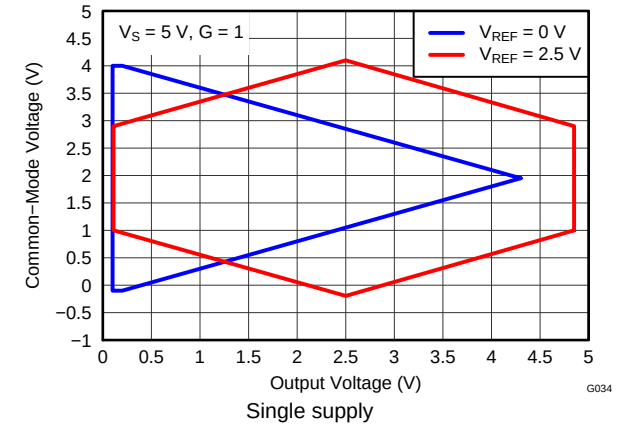


Figure 11. Input Common-Mode Voltage vs Output Voltage

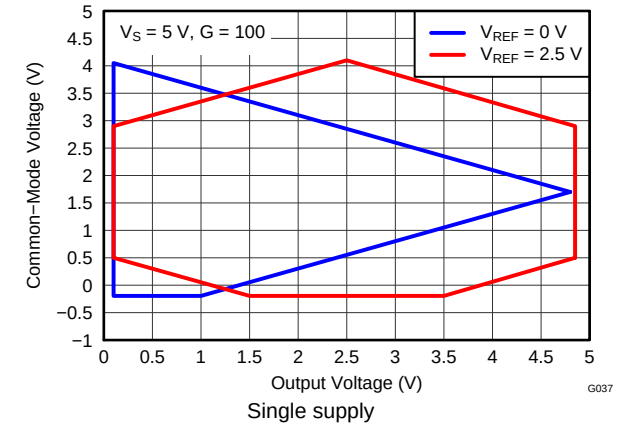


Figure 12. Input Common-Mode Voltage vs Output Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

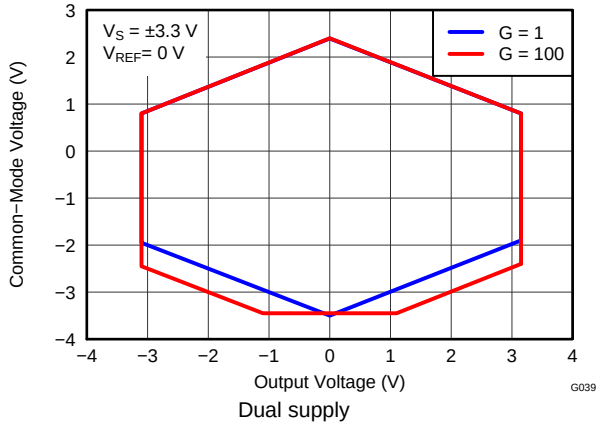


Figure 13. Input Common-Mode Voltage vs Output Voltage

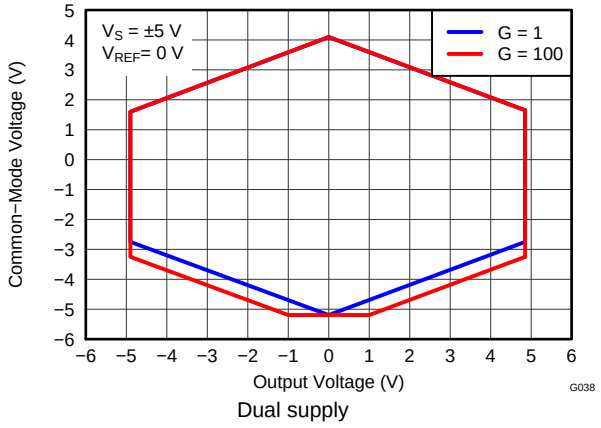


Figure 14. Input Common-Mode Voltage vs Output Voltage

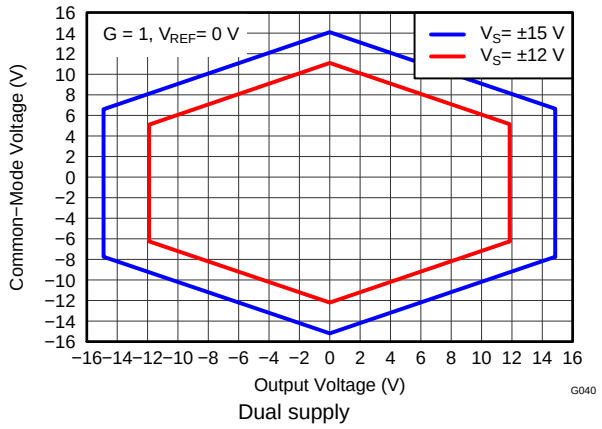


Figure 15. Input Common-Mode Voltage vs Output Voltage

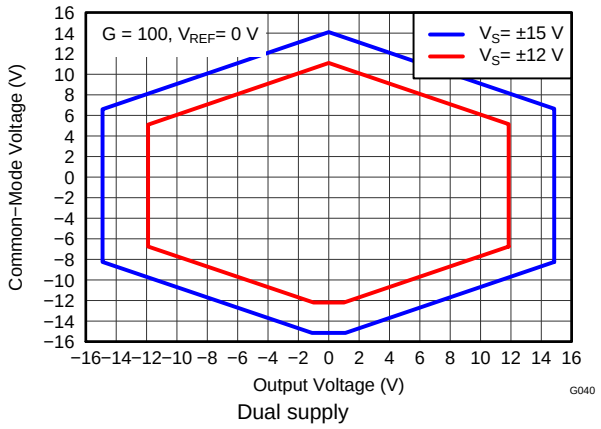


Figure 16. Input Common-Mode Voltage vs Output Voltage

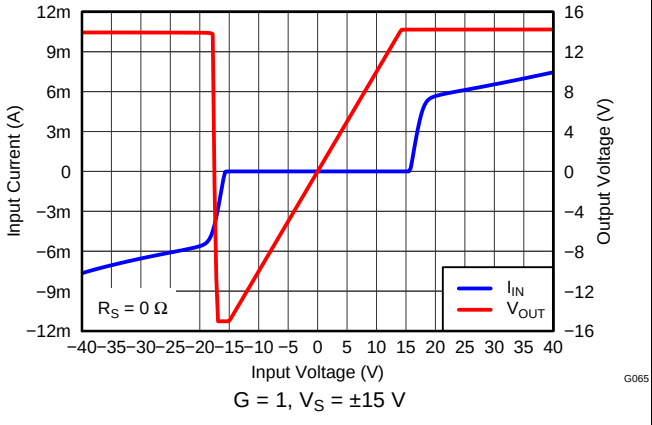


Figure 17. Input Overvoltage vs Input Current

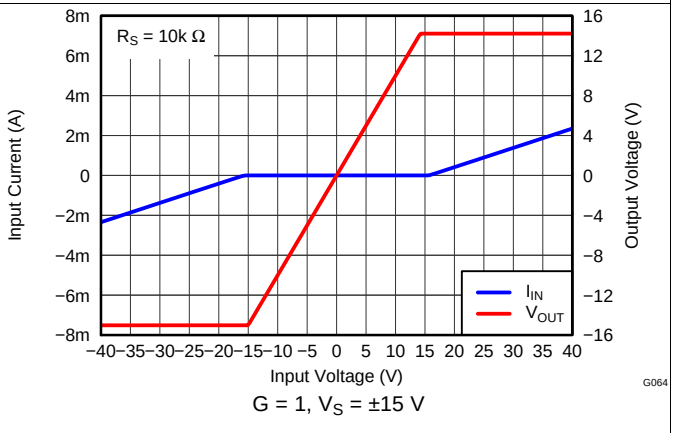


Figure 18. Input Overvoltage vs Input Current with 10-kΩ Resistance

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

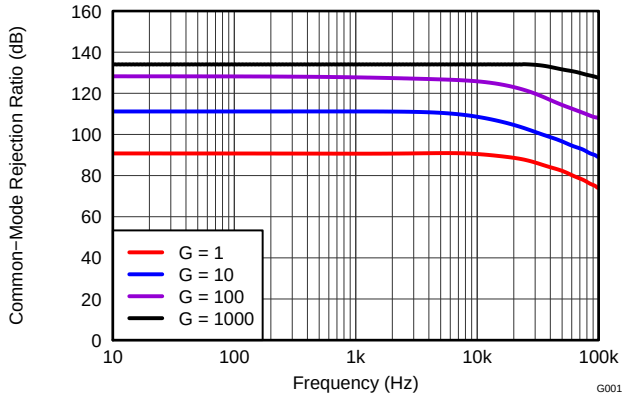


Figure 19. CMRR vs Frequency (RTI)

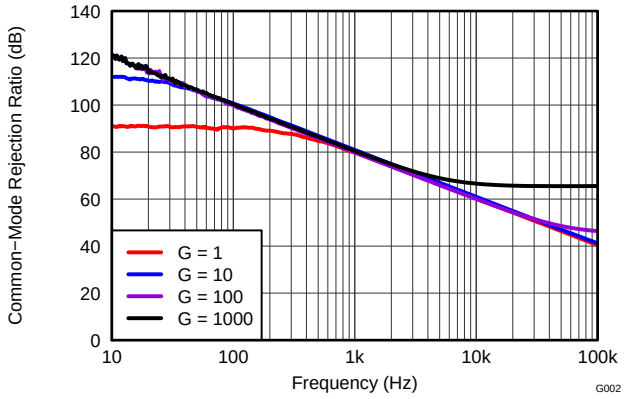


Figure 20. CMRR vs Frequency (RTI, 1-kΩ Source Imbalance)

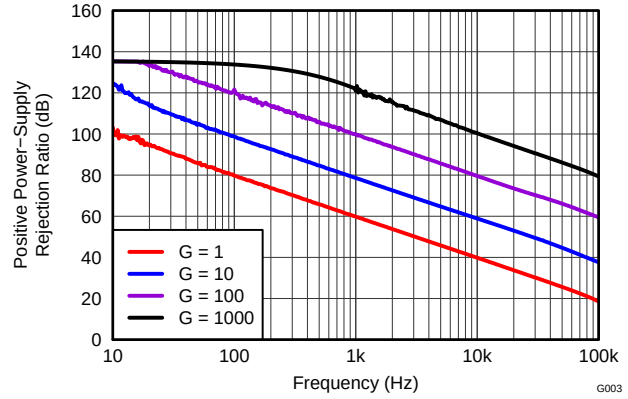


Figure 21. Positive PSRR vs Frequency (RTI)

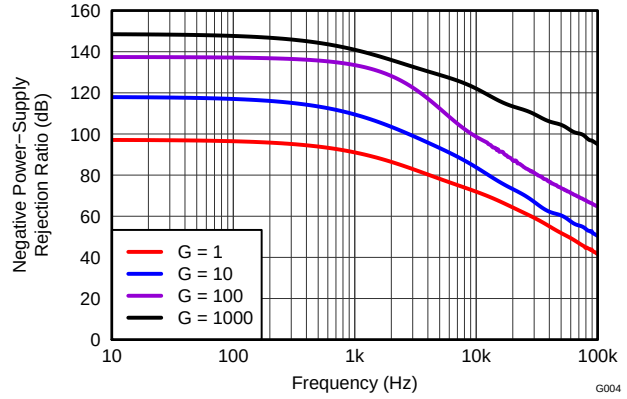


Figure 22. Negative PSRR vs Frequency (RTI)

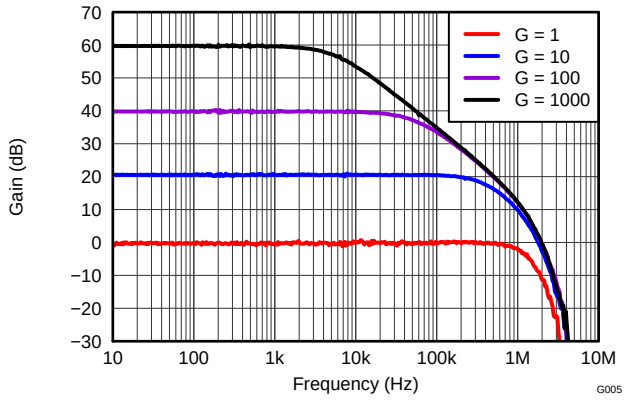


Figure 23. Gain vs Frequency

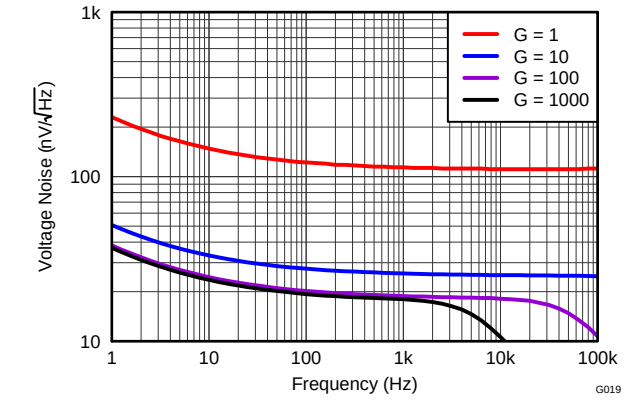


Figure 24. Voltage Noise Spectral Density vs Frequency (RTI)

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

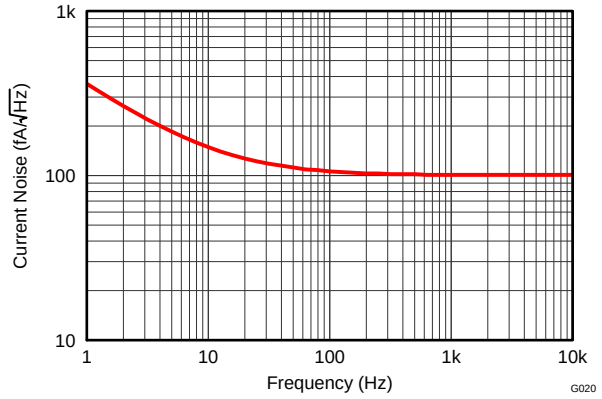


Figure 25. Current Noise Spectral Density vs Frequency (RTI)

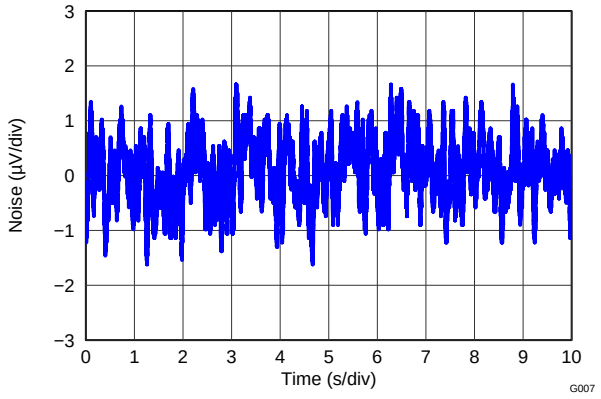


Figure 26. 0.1-Hz to 10-Hz RTI Voltage Noise (G = 1)

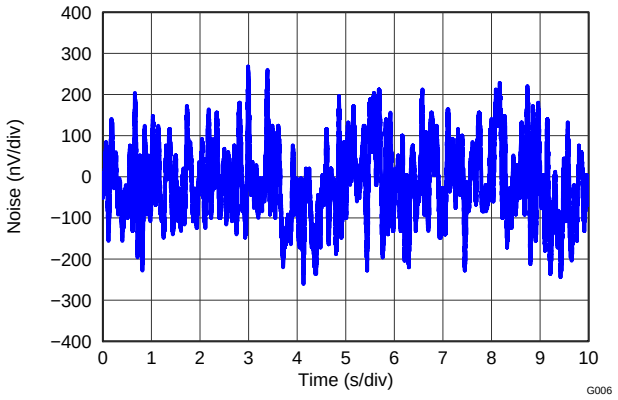


Figure 27. 0.1-Hz to 10-Hz RTI Voltage Noise (G = 1000)

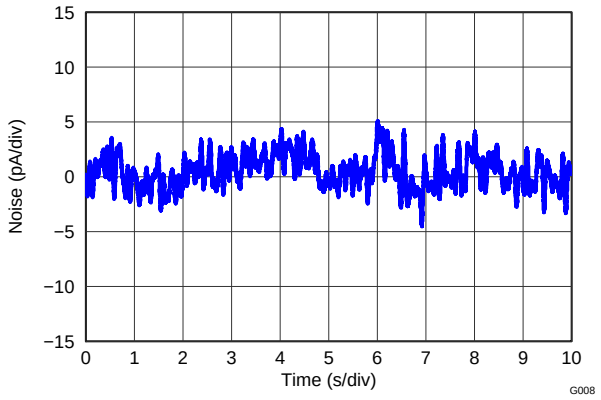
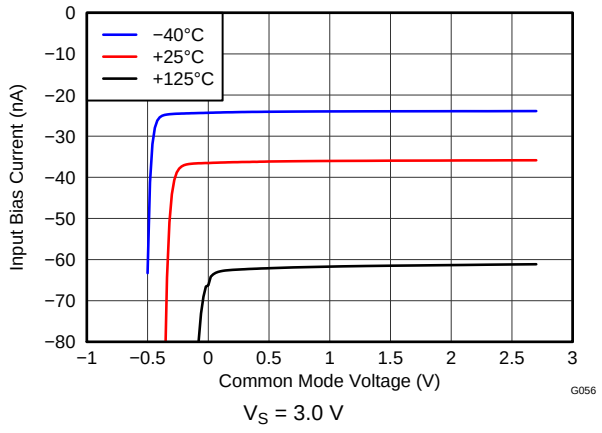
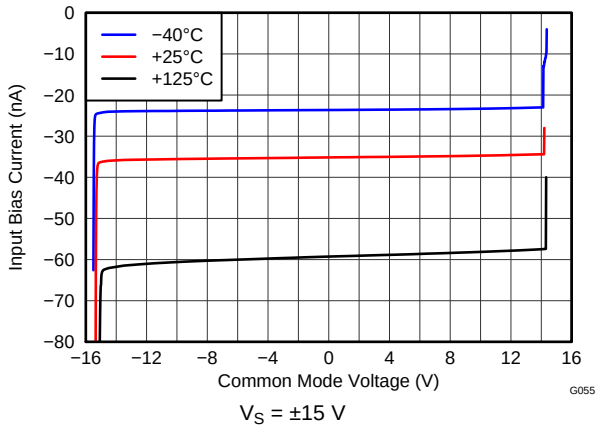


Figure 28. 0.1-Hz to 10-Hz RTI Current Noise



V_S = 3.0 V

Figure 29. Input Bias Current vs Common-Mode Voltage



V_S = ±15 V

Figure 30. Input Bias Current vs Common-Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

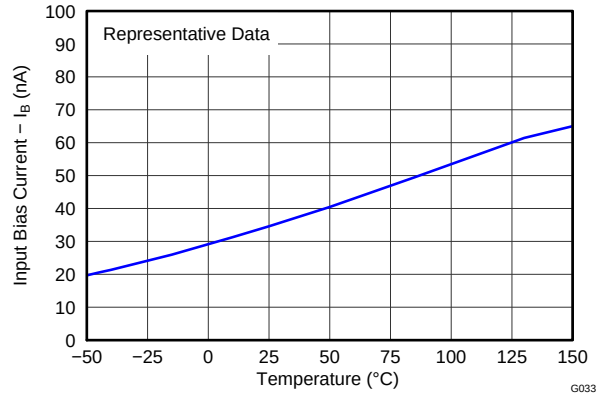


Figure 31. Input Bias Current vs Temperature

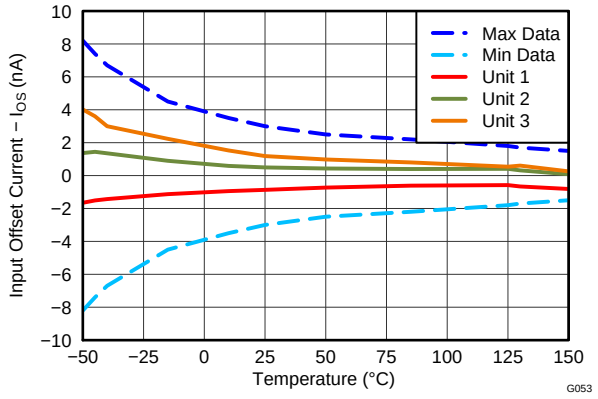


Figure 32. Input Offset Current vs Temperature

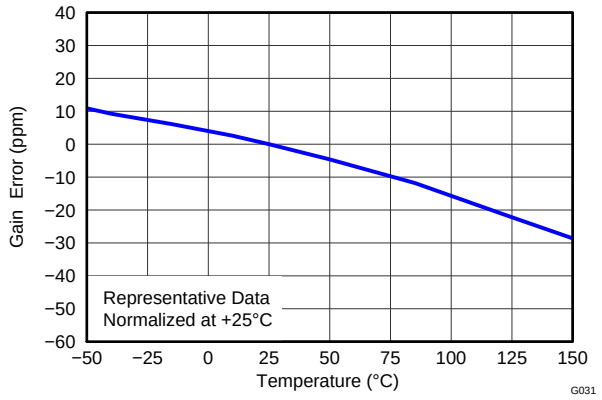


Figure 33. Gain Error vs Temperature (G = 1)

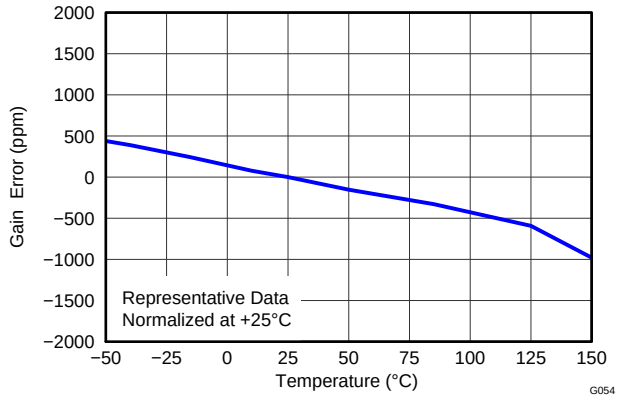


Figure 34. Gain Error vs Temperature (G > 1)

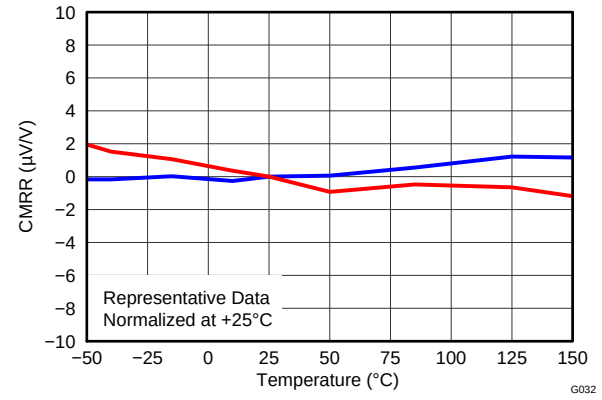


Figure 35. CMRR vs Temperature (G = 1)

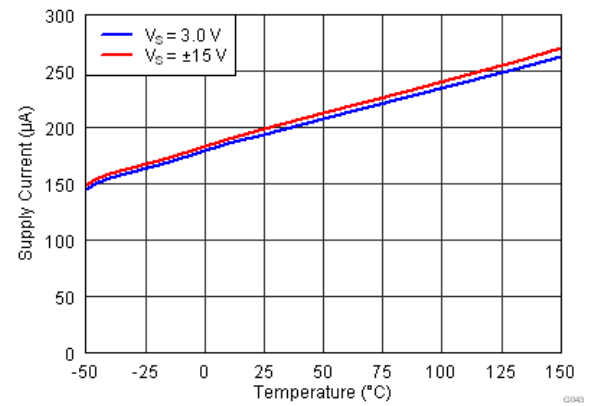


Figure 36. Supply Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

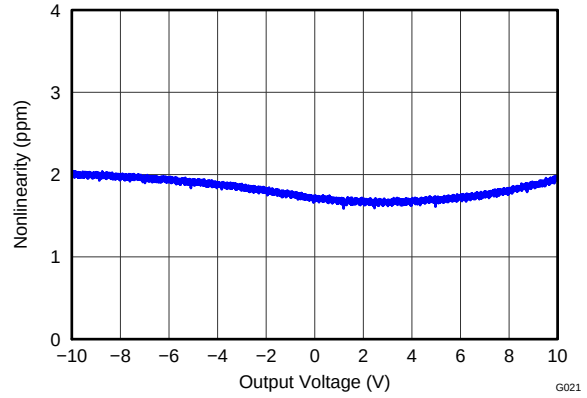


Figure 37. Gain Nonlinearity (G = 1)

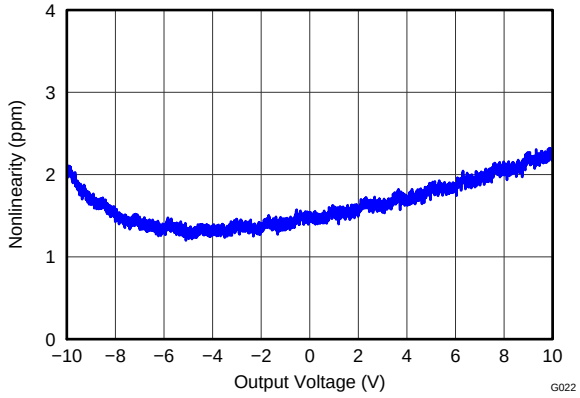


Figure 38. Gain Nonlinearity (G = 10)

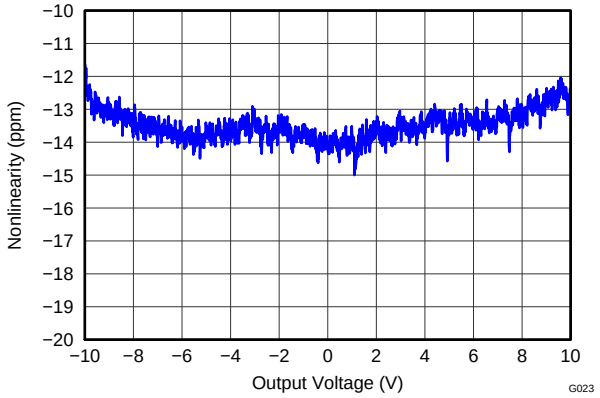


Figure 39. Gain Nonlinearity (G = 100)

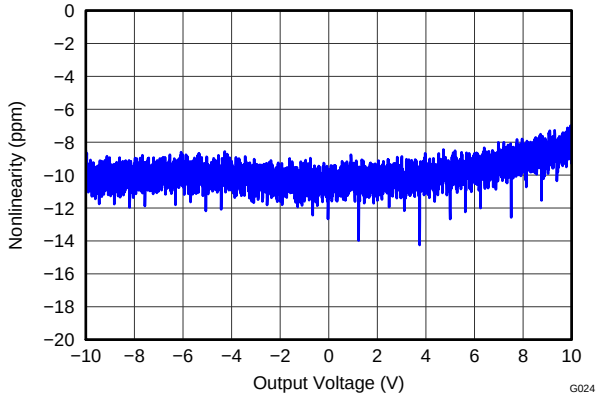


Figure 40. Gain Nonlinearity (G = 1000)

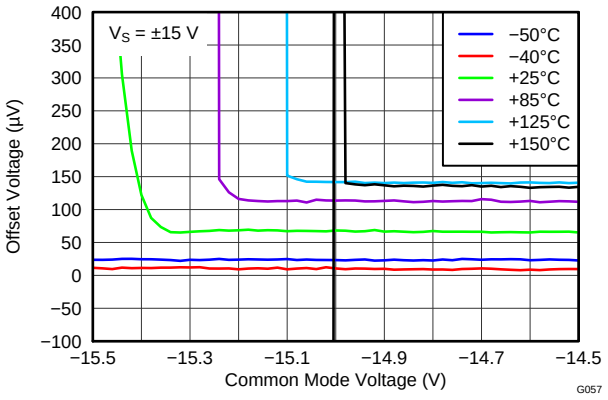


Figure 41. Offset Voltage vs Negative Common-Mode Voltage

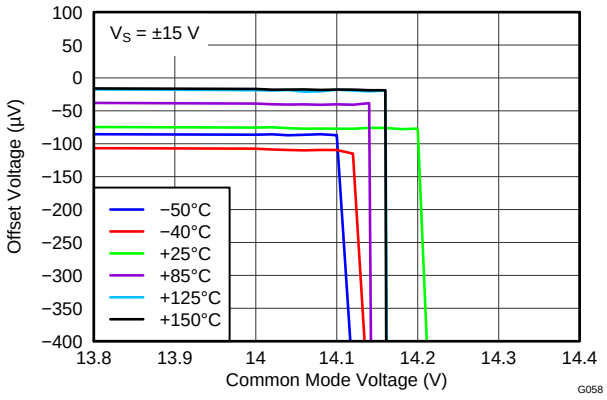


Figure 42. Offset Voltage vs Positive Common-Mode Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

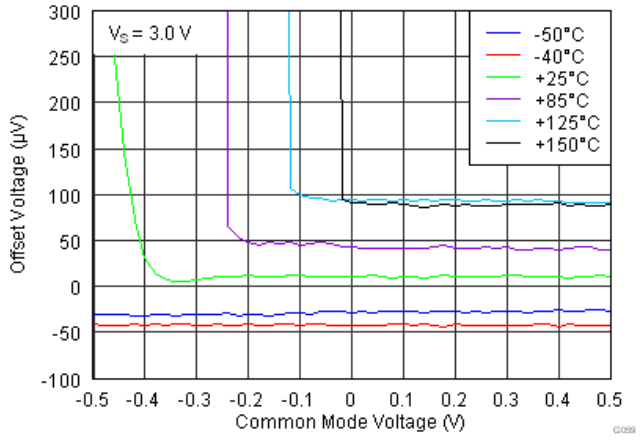


Figure 43. Offset Voltage vs Negative Common-Mode Voltage

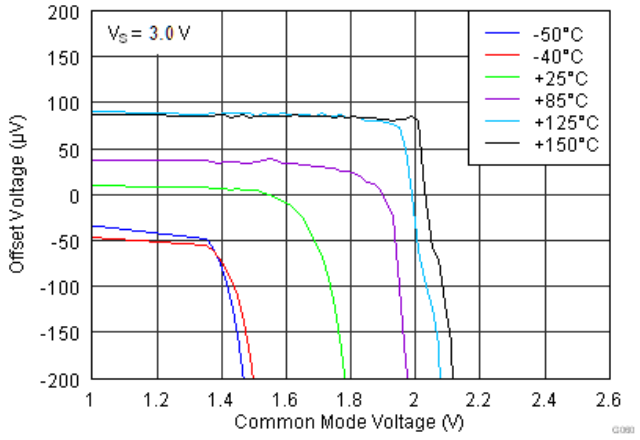


Figure 44. Offset Voltage vs Positive Common-Mode Voltage

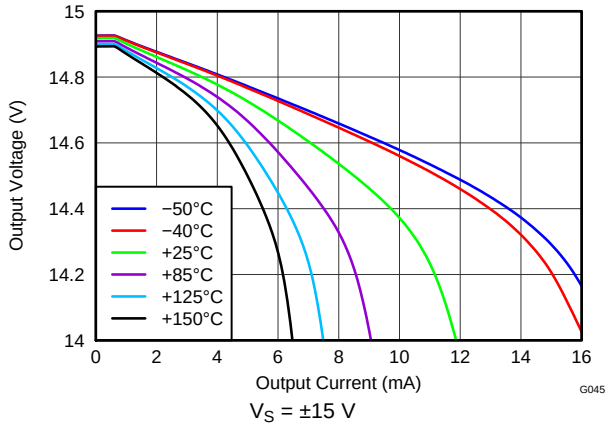


Figure 45. Positive Output Voltage Swing vs Output Current

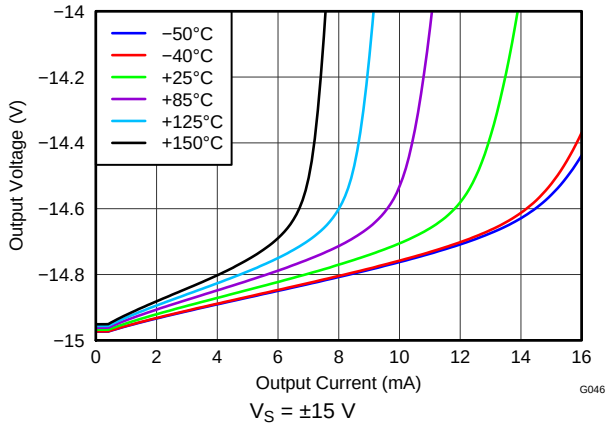


Figure 46. Negative Output Voltage Swing vs Output Current

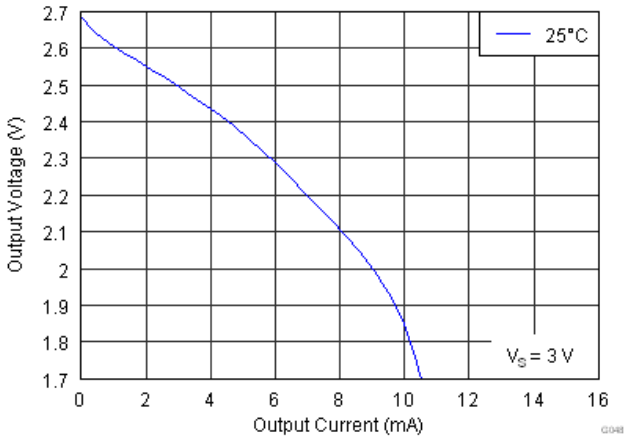


Figure 47. Positive Output Voltage Swing vs Output Current

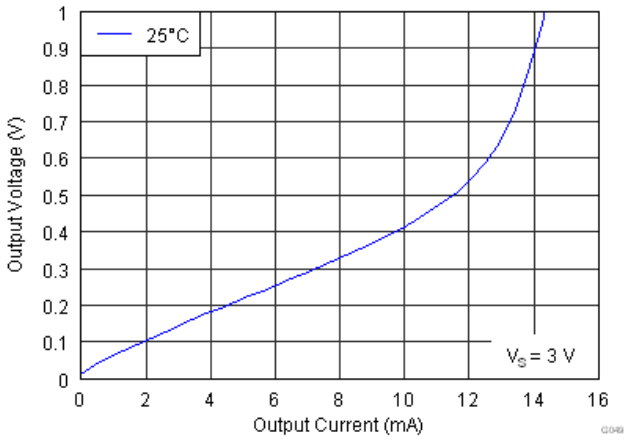


Figure 48. Negative Output Voltage Swing vs Output Current

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)

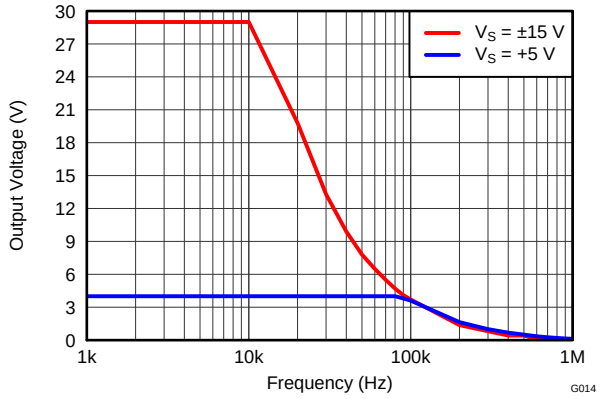
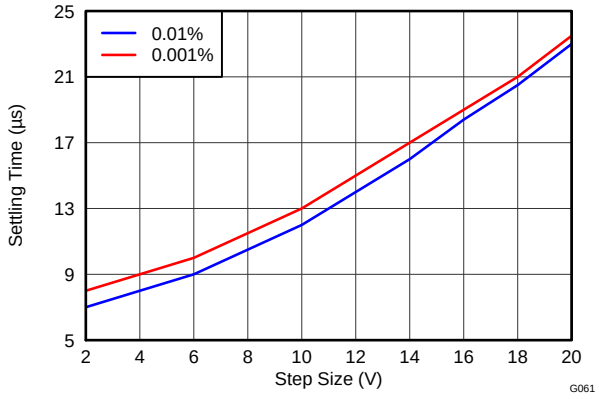


Figure 49. Large-Signal Frequency Response



V_S = ±15 V

Figure 50. Settling Time vs Step Size

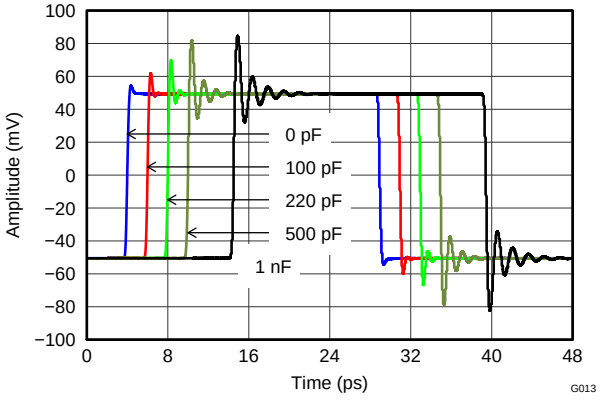
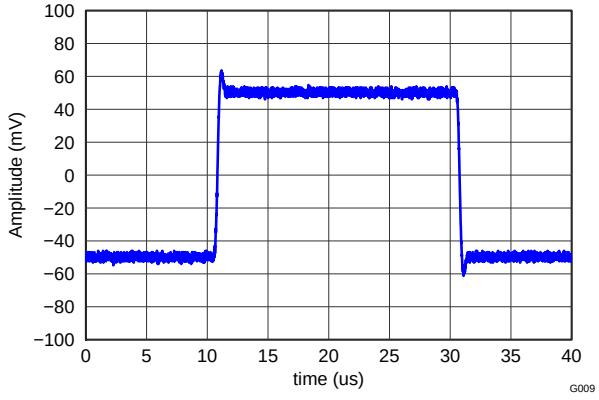
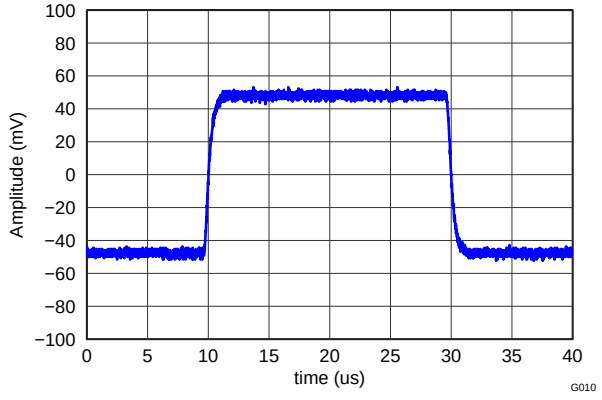


Figure 51. Small-Signal Response Over Capacitive Loads (G = 1)



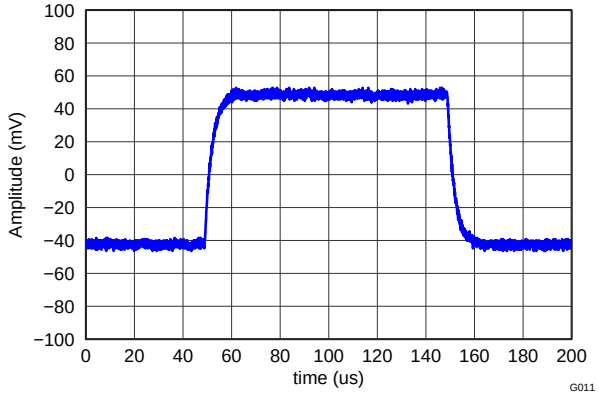
G = 1, R_L = 1 kΩ, C_L = 100 pF

Figure 52. Small-Signal Response



G = 10, R_L = 10 kΩ, C_L = 100 pF

Figure 53. Small-Signal Response

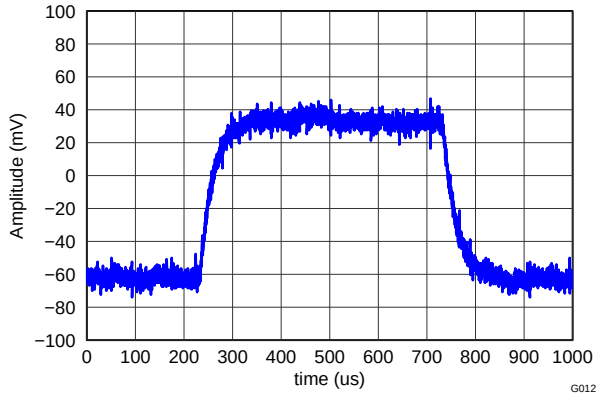


G = 100, R_L = 10 kΩ, C_L = 100 pF

Figure 54. Small-Signal Response

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15 V, R_L = 10 kΩ, V_{REF} = 0 V, and G = 1 (unless otherwise noted)



G = 1000, R_L = 10 kΩ, C_L = 100 pF

Figure 55. Small-Signal Response

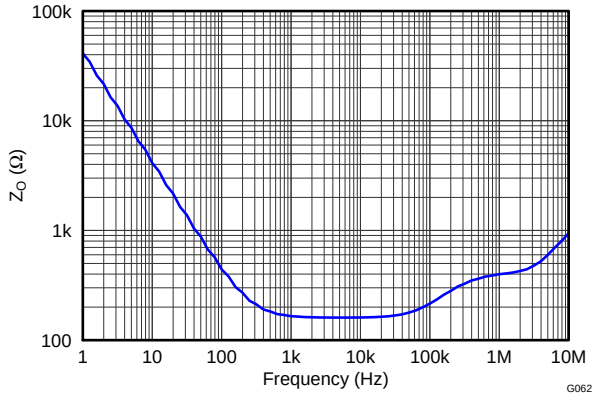


Figure 56. Open-Loop Output Impedance

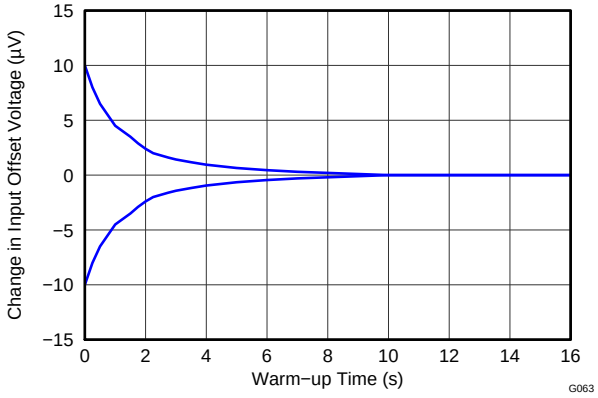


Figure 57. Change in Input Offset Voltage vs Warm-Up Time

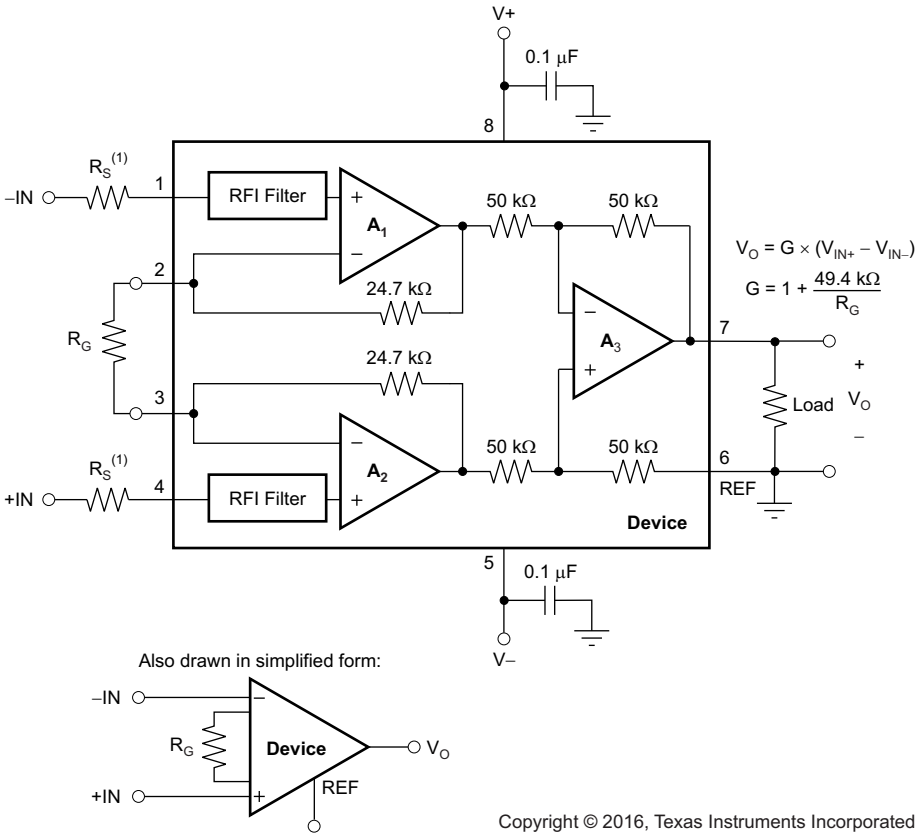
8 Detailed Description

8.1 Overview

The *Functional Block Diagram* section shows the basic connections required for operation of the INA826. Good layout practice mandates the use of bypass capacitors placed as close to the device pins as possible.

The output of the INA826 is referred to the output reference (REF) terminal, which is normally grounded. This connection must be low-impedance to assure good common-mode rejection. Although 5 Ω or less of stray resistance can be tolerated when maintaining specified CMRR, small stray resistances of tens of ohms in series with the REF pin can cause noticeable degradation in CMRR.

8.2 Functional Block Diagram



(1) This resistor is optional if the input voltage stays above [(V–) – 2 V] or if the signal source current drive capability is limited to less than 3.5 mA; see the *Input Protection* section for more details.

8.3 Feature Description

8.3.1 Inside the INA826

See the *Functional Block Diagram* section for a simplified representation of the INA826. A more detailed diagram (shown in Figure 58) provides additional insight into the INA826 operation.

Each input is protected by two field-effect transistors (FETs) that provide a low series resistance under normal signal conditions, and preserve excellent noise performance. When excessive voltage is applied, these transistors limit input current to approximately 8 mA.

The differential input voltage is buffered by Q_1 and Q_2 and is impressed across R_G, causing a signal current to flow through R_G, R_1, and R_2. The output difference amplifier, A_3, removes the common-mode component of the input signal and refers the output signal to the REF terminal.

The equations shown in Figure 58 describe the output voltages of A_1 and A_2. The V_{BE} and voltage drop across R_1 and R_2 produce output voltages on A_1 and A_2 that are approximately 0.8 V higher than the input voltages.

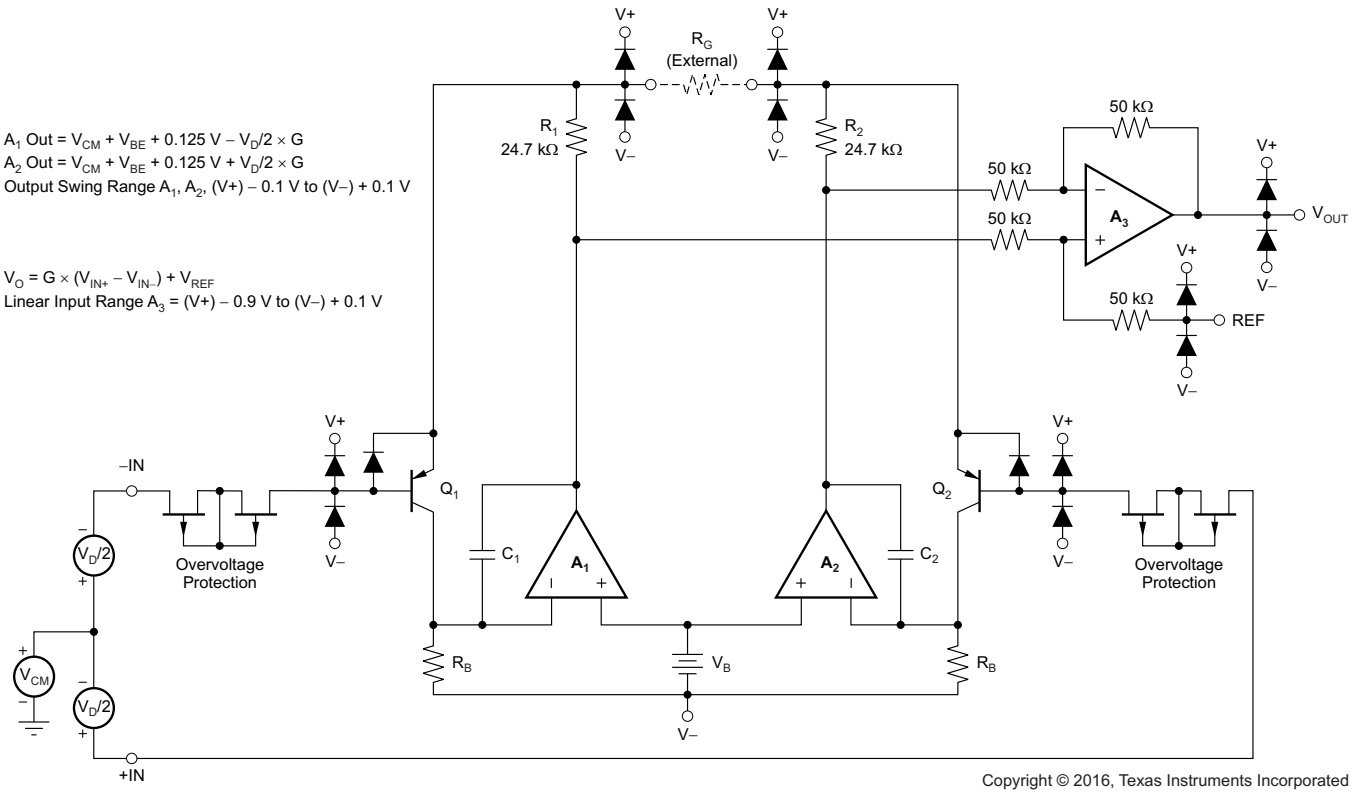


Figure 58. INA826 Simplified Circuit Diagram

Feature Description (continued)

8.3.2 Setting the Gain

Gain of the INA826 is set by a single external resistor, R_G, connected between pins 2 and 3. The value of R_G is selected according to Equation 1:

$$G = 1 + \left(\frac{49.4\ k\Omega}{R_G} \right) \quad (1)$$

Table 1 lists several commonly-used gains and resistor values. The 49.4-kΩ term in Equation 1 comes from the sum of the two internal 24.7-kΩ feedback resistors. These on-chip resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficients of these resistors are included in the gain accuracy and drift specifications of the INA826.

Table 1. Commonly-Used Gains and Resistor Values

DESIRED GAIN (V/V)	R_G (Ω)	NEAREST 1% R_G (Ω)
1	—	—
2	49.4 k	49.9 k
5	12.35 k	12.4 k
10	5.489 k	5.49 k
20	2.600 k	2.61 k
50	1.008 k	1 k
100	499	499
200	248	249
500	99	100
1000	49.5	49.9

8.3.2.1 Gain Drift

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift can be directly inferred from the gain of Equation 1.

The best gain drift of 1 ppm/°C can be achieved when the INA826 uses G = 1 without R_G connected. In this case, the gain drift is limited only by the slight mismatch of the temperature coefficient of the integrated 50-kΩ resistors in the differential amplifier (A_3). At G greater than 1, the gain drift increases as a result of the individual drift of the 24.7-kΩ resistors in the feedback of A_1 and A_2, relative to the drift of the external gain resistor R_G. Process improvements of the temperature coefficient of the feedback resistors now make possible specifying a maximum gain drift of the feedback resistors of 35 ppm/°C, thus significantly improving the overall temperature stability of applications using gains greater than 1.

Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (such as a possible unstable gain error) at gains of approximately 100 or greater. To ensure stability, avoid parasitic capacitance of more than a few picofarads at R_G connections. Careful matching of any parasitics on both R_G pins maintains optimal CMRR over frequency; see the *Typical Characteristics* curves (Figure 19 and Figure 20).

8.3.3 Offset Trimming

Most applications require no external offset adjustment; however, if necessary, adjustments can be made by applying a voltage to the REF terminal. Figure 59 shows an optional circuit for trimming the output offset voltage. The voltage applied to the REF terminal is summed at the output. The op amp buffer provides low impedance at the REF terminal to preserve good common-mode rejection.

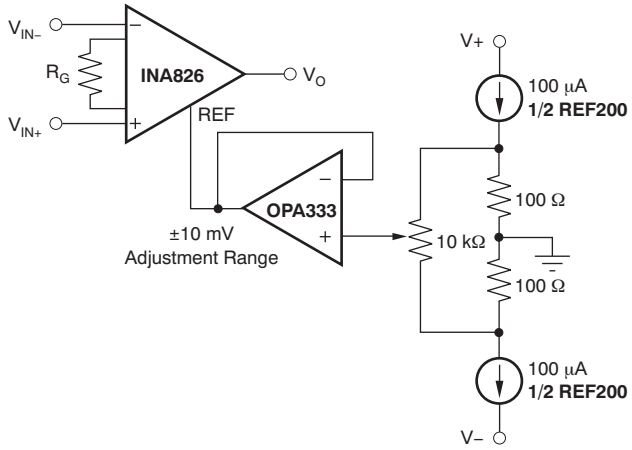


Figure 59. Optional Trimming of the Output Offset Voltage

8.3.4 Input Common-Mode Range

The linear input voltage range of the INA826 input circuitry extends from the negative supply voltage to 1 V below the positive supply and maintains 84-dB (minimum) common-mode rejection throughout this range. The common-mode range for most common operating conditions is described in the input common-mode voltage versus output voltage *Typical Characteristics* curves (Figure 9 through Figure 15) and the offset voltage versus common-mode voltage curves (Figure 41 through Figure 43). The INA826 can operate over a wide range of power supplies and V_{REF} configurations, thus providing a comprehensive guide to common-mode range limits for all possible conditions is impractical.

The most commonly overlooked overload condition occurs when a circuit exceeds the output swing of A_1 and A_2, which are internal circuit nodes that cannot be measured. Calculating the expected voltages at the output of A_1 and A_2 (see Figure 58) provides a check for the most common overload conditions. The designs of A_1 and A_2 are identical and the outputs can swing to within approximately 100 mV of the power-supply rails. For example, when the A_2 output is saturated, A_1 can still be in linear operation, responding to changes in the noninverting input voltage. This difference can give the appearance of linear operation but the output voltage is invalid.

A single-supply instrumentation amplifier has special design considerations. To achieve a common-mode range that extends to single-supply ground, the INA826 employs a current-feedback topology with PNP input transistors; see Figure 58. The matched PNP transistors Q_1 and Q_2 shift the input voltages of both inputs up by a diode drop, and (through the feedback network) shift the output of A_1 and A_2 by approximately 0.8 V. With both inputs and V_{REF} at single-supply ground (negative power supply), the output of A_1 and A_2 is well within the linear range, allowing differential measurements to be made at the GND level. As a result of this input level-shifting, the voltages at pin 2 and pin 3 are not equal to the respective input terminal voltages (pin 1 and pin 4). For most applications, this inequality is not important because only the gain-setting resistor connects to these pins.

8.3.5 Input Protection

The inputs of the INA826 are individually protected for voltages up to ±40 V. For example, a condition of –40 V on one input and 40 V on the other input does not cause damage. However, if the input voltage exceeds (V–) – 2 V and the signal source current drive capability exceeds 3.5 mA, the output voltage switches to the opposite polarity; see Figure 17. This polarity reversal can easily be avoided by adding resistance of 10 kΩ in series with both inputs.

Internal circuitry on each input provides low series impedance under normal signal conditions. If the input is overloaded, the protection circuitry limits the input current to a safe value of approximately 8 mA. Figure 17 and Figure 18 illustrate this input current limit behavior. The inputs are protected even if the power supplies are disconnected or turned off.

8.3.6 Input Bias Current Return Path

The input impedance of the INA826 is extremely high—approximately 20 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically 35 nA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 60 shows various provisions for an input bias current path. Without a bias current path, the inputs float to a potential that exceeds the common-mode range of the INA826 and the input amplifiers saturate. If the differential source resistance is low, the bias current return path can be connected to one input (as shown in the thermocouple example in Figure 60). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

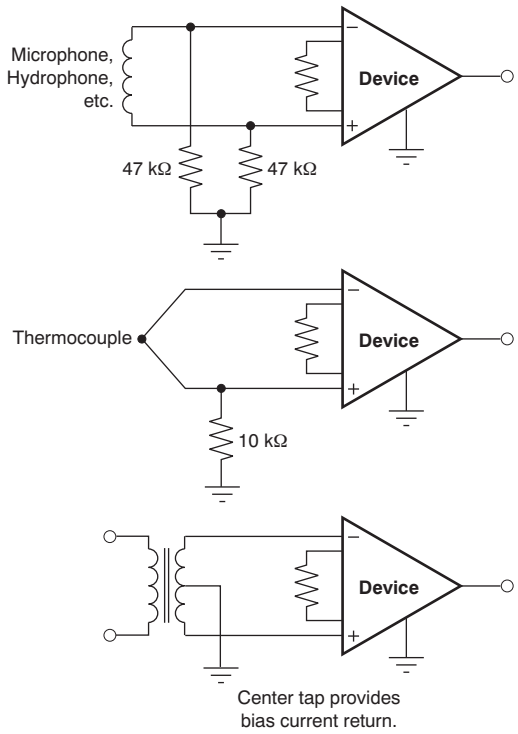


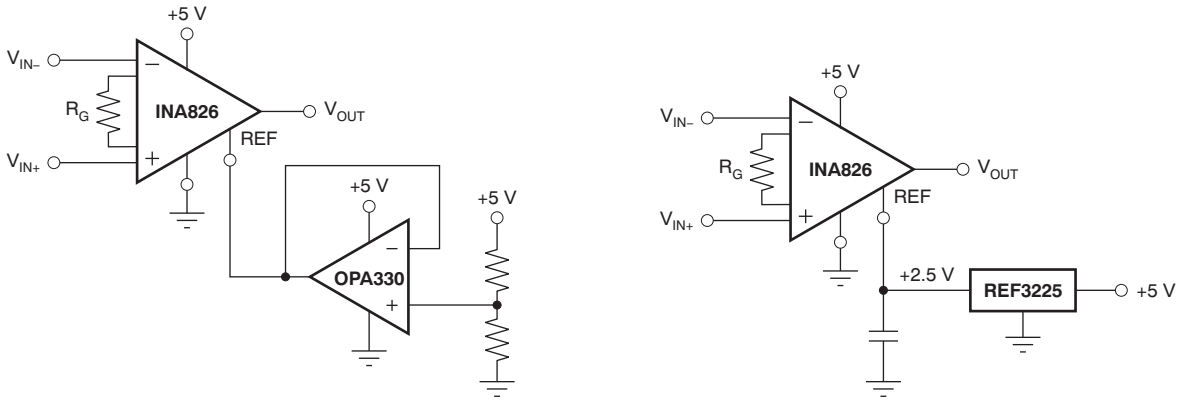
Figure 60. Providing an Input Common-Mode Current Path

8.3.7 Reference Terminal

The output voltage of the INA826 is developed with respect to the voltage on the reference terminal. Often, in dual-supply operation, the reference pin (pin 6) is connected to the low-impedance system ground. In single-supply operation, offsetting the output signal to a precise mid-supply level can be useful (for example, 2.5 V in a 5-V supply environment). To accomplish this level shift, a voltage source can be tied to the REF pin to level-shift the output so that the INA826 can drive a single-supply ADC, for example.

For the best performance, keep the source impedance to the REF terminal below 5 Ω. As illustrated in the *Functional Block Diagram* section, the reference resistor is at one end of a 50-kΩ resistor. Additional impedance at the REF pin adds to this 50-kΩ resistor. The imbalance in the resistor ratios results in degraded common-mode rejection ratio (CMRR).

Figure 61 shows two different methods of driving the reference pin with low impedance. The OPA330 is a low-power, chopper-stabilized amplifier and therefore offers excellent stability over temperature. The OPA330 is available in the space-saving SC70 and even smaller chip-scale package. The REF3225 is a precision reference in the small SOT23-6 package.



a) Level shifting using the OPA330 as a low-impedance buffer

b) Level shifting using the low-impedance output of the REF3225

Figure 61. Options for Low-Impedance Level Shifting

8.3.8 Dynamic Performance

Figure 23 illustrates that, despite its low quiescent current of only 200 µA, the INA826 achieves much wider bandwidth than other INAs in its class. This achievement is a result of using TI's proprietary high-speed precision bipolar process technology. The current-feedback topology provides the INA826 with wide bandwidth even at high gains. Settling time also remains excellent at high gain because of a high slew rate of 1 V/µs.

8.3.9 Operating Voltage

The INA826 operates over a power-supply range of 3 V to 36 V (±1.5 V to ±18 V). Supply voltages higher than 40 V (±20 V) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section of this data sheet.

8.3.9.1 Low-Voltage Operation

The INA826 can operate on power supplies as low as ±1.5 V. Most parameters vary only slightly throughout this supply voltage range; see the *Typical Characteristics* section. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. The *Typical Characteristics* curves Figure 9 through Figure 15 and Figure 41 through Figure 43 describe the range of linear operation for various supply voltages, reference connections, and gains.

8.3.10 Error Sources

Most modern signal-conditioning systems calibrate errors at room temperature. However, calibration of errors that result from a change in temperature is normally difficult and costly. Therefore, minimizing these errors is important by choosing high-precision components such as the INA826 that have improved specifications in critical areas that impact the precision of the overall system. Figure 62 shows an example application.

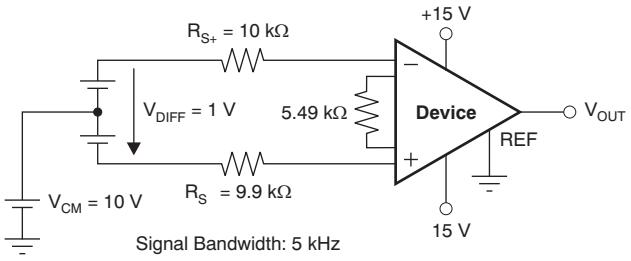


Figure 62. Example Application with G = 10 V/V and 1-V Differential Voltage

Resistor-adjustable INAs such as the INA826 show the lowest gain error in G = 1 because of the inherently well-matched drift of the internal resistors of the differential amplifier. At gains greater than 1 (for instance, G = 10 V/V or G = 100 V/V) the gain error becomes a significant error source because of the contribution of the resistor drift of the 24.7-kΩ feedback resistors in conjunction with the external gain resistor. Except for very high gain applications, the gain drift is by far the largest error contributor compared to other drift errors, such as offset drift.

The INA826 offers excellent gain error over temperature for both G > 1 and G = 1 (no external gain resistor). Table 2 summarizes the major error sources in common INA applications and compares the two cases of G = 1 (no external resistor) and G = 10 (5.49-kΩ external resistor). As can be seen in Table 2, although the static errors (absolute accuracy errors) in G = 1 are almost twice as great as compared to G = 10, there are much fewer drift errors because of the much lower gain error drift. In most applications, these static errors can readily be removed during calibration in production. All calculations refer the error to the input for easy comparison and system evaluation.

Table 2. Error Calculation

ERROR SOURCE	ERROR CALCULATION	INA826		
		SPECIFICATION	G = 10 ERROR (ppm)	G = 1 ERROR (ppm)
ABSOLUTE ACCURACY AT 25°C				
Input offset voltage (μV)	V_{OSI} / V_{DIFF}	150	150	150
Output offset voltage (μV)	V_{OSO} / (G × V_{DIFF})	700	70	700
Input offset current (nA)	I_{OS} × maximum (R_{S+}, $R_{S–}$) / V_{DIFF}	5	50	50
CMRR (dB)	V_{CM} / ($10^{CMRR/20}$ × V_{DIFF})	104 (G = 10), 84 (G = 1)	63	631
Total absolute accuracy error (ppm)			333	1531
DRIFT TO 105°C				
Gain drift (ppm/°C)	GTC × (T_A – 25)	35 (G = 10), 1 (G = 1)	2800	80
Input offset voltage drift (μV/°C)	(V_{OSI_TC} / V_{DIFF}) × (T_A – 25)	2	160	160
Output offset voltage drift (μV/°C)	[V_{OSO_TC} / (G × V_{DIFF})] × (T_A – 25)	10	80	800
Offset current drift (pA/°C)	I_{OS_TC} × maximum (R_{S+}, $R_{S–}$) × (T_A – 25) / V_{DIFF}	60	48	48
Total drift error (ppm)			3088	1088
RESOLUTION				
Gain nonlinearity (ppm of FS)		5	5	5
Voltage noise (1 kHz)	$\sqrt{BW} \times \sqrt{(e_{NI}^2 + \left(\frac{e_{NO}}{G}\right)^2 \times \frac{6}{V_{DIFF}}}$	e_{NI} = 18, e_{NO} = 110	10	10
Total resolution error (ppm)			15	15
TOTAL ERROR				
Total error	Total error = sum of all error sources		3436	2634

8.4 Device Functional Modes

The INA826 has a single functional mode and is operational when the power-supply voltage is greater than 3 V (±1.5 V). The maximum power-supply voltage for the INA826 is 36 V (±18 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The low power consumption, high performance, and low cost of the INA826 make the device an excellent instrumentation amplifier for many applications. The INA826 can be used in many low-power, portable applications because the device has a low quiescent current (200 µA, typ) and comes in a small 8-pin WSON package. The input protection circuitry, low maximum gain drift, low offset voltage, and 36-V maximum supply voltage also make the INA826 an ideal choice for industrial applications as well.

9.2 Typical Application

Figure 63 shows a three-terminal programmable-logic controller (PLC) design for the INA826. This PLC reference design accepts inputs of ±10 V or ±20 mA. The output is a single-ended voltage of 2.5 V ±2.3 V (or 200 mV to 4.8 V). Many PLCs typically have these input and output ranges.

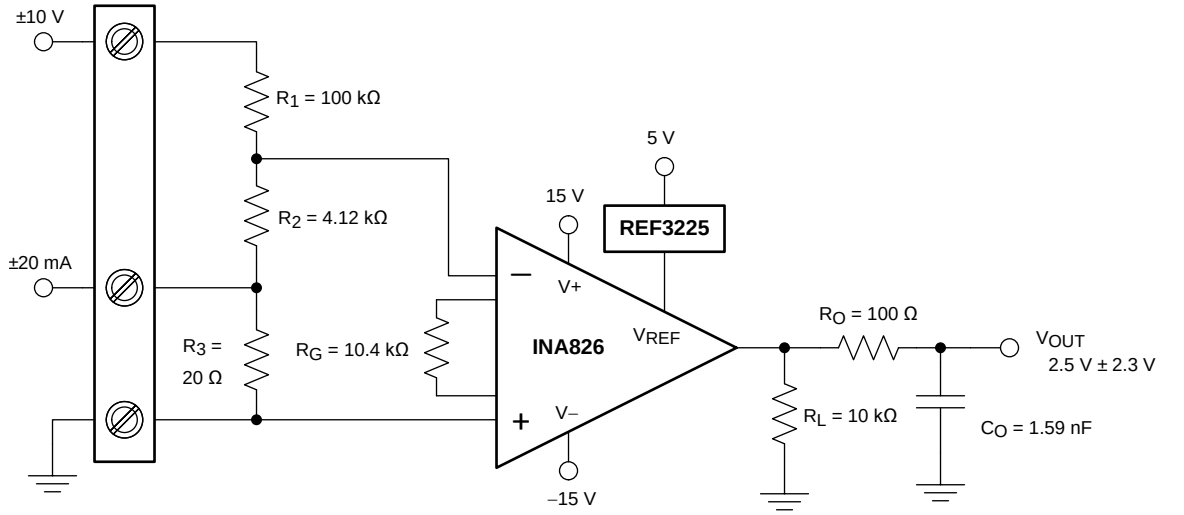


Figure 63. Three-Terminal PLC Design

9.2.1 Design Requirements

This design has these requirements:

- Supply voltage: ±15 V, 5 V
- Inputs: ±10 V, ±20 mA
- Output: 2.5 V, ±2.3 V

9.2.2 Detailed Design Procedure

There are two modes of operation for the circuit shown in Figure 63: current input and voltage input. This design requires $R_1 >> R_2 >> R_3$. Given this relationship, the current input mode transfer function is given by Equation 2.

$$V_{OUT-I} = V_D \times G + V_{REF} = -(I_{IN} \times R_3) \times G + V_{REF} \quad (2)$$

where

- G represents the gain of the instrumentation amplifier

Typical Application (continued)

The transfer function for the voltage input mode is shown by Equation 3.

$$V_{OUT-V} = V_D \times G + V_{REF} = -\left(V_{IN} \times \frac{R_2}{R_1 + R_2}\right) \times G + V_{REF} \quad (3)$$

R_1 sets the input impedance of the voltage input mode. The minimum typical input impedance is 100 kΩ. 100 kΩ is selected for R_1 because increasing the R_1 value also increases noise. The value of R_3 must be extremely small compared to R_1 and R_2. 20 Ω for R_3 is selected because that resistance value is much smaller than R_1 and yields an input voltage of ±400 mV when operated in current mode (±20 mA).

Equation 4 can be used to calculate R_2 given V_D = ±400 mV, V_{IN} = ±10 V, and R_1 = 100 kΩ.

$$V_D = V_{IN} \times \frac{R_2}{R_1 + R_2} \rightarrow R_2 = \frac{R_1 \times V_D}{V_{IN} - V_D} = 4.167\ k\Omega \quad (4)$$

The value obtained from Equation 4 is not a standard 0.1% value, so 4.12 kΩ is selected. R_1 and R_2 also use 0.1% tolerance resistors to minimize error.

The ideal gain of the instrumentation amplifier is calculated with Equation 5.

$$G = \frac{V_{OUT} - V_{REF}}{V_D} = \frac{4.8\ V - 2.5\ V}{400\ mV} = 5.75\ \frac{V}{V} \quad (5)$$

Using the INA826 gain equation, the gain-setting resistor value is calculated as shown by Equation 6.

$$G_{INA826} = 1 + \frac{49.4\ k\Omega}{R_G} \rightarrow R_G = \frac{49.4\ k\Omega}{G_{INA826} - 1} = \frac{49.4\ k\Omega}{5.75 - 1} = 10.4\ k\Omega \quad (6)$$

10.4 kΩ is a standard 0.1% resistor value that can be used in this design. Finally, the output RC filter components are selected to have a –3-dB cutoff frequency of 1 MHz.

9.2.3 Application Curves

Figure 64 and Figure 65 illustrate typical characteristic curves for Figure 63.

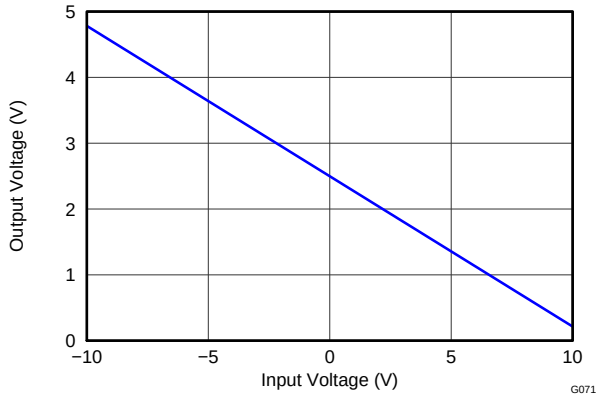


Figure 64. PLC Output Voltage vs Input Voltage

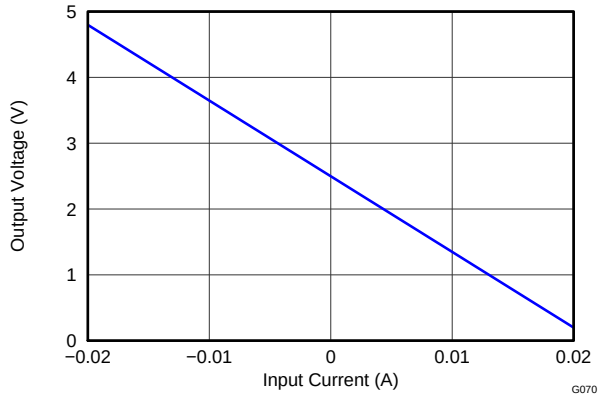


Figure 65. PLC Output Voltage vs Input Current

9.3 System Examples

9.3.1 Circuit Breaker

Figure 66 shows the INA826 used in a circuit breaker application.

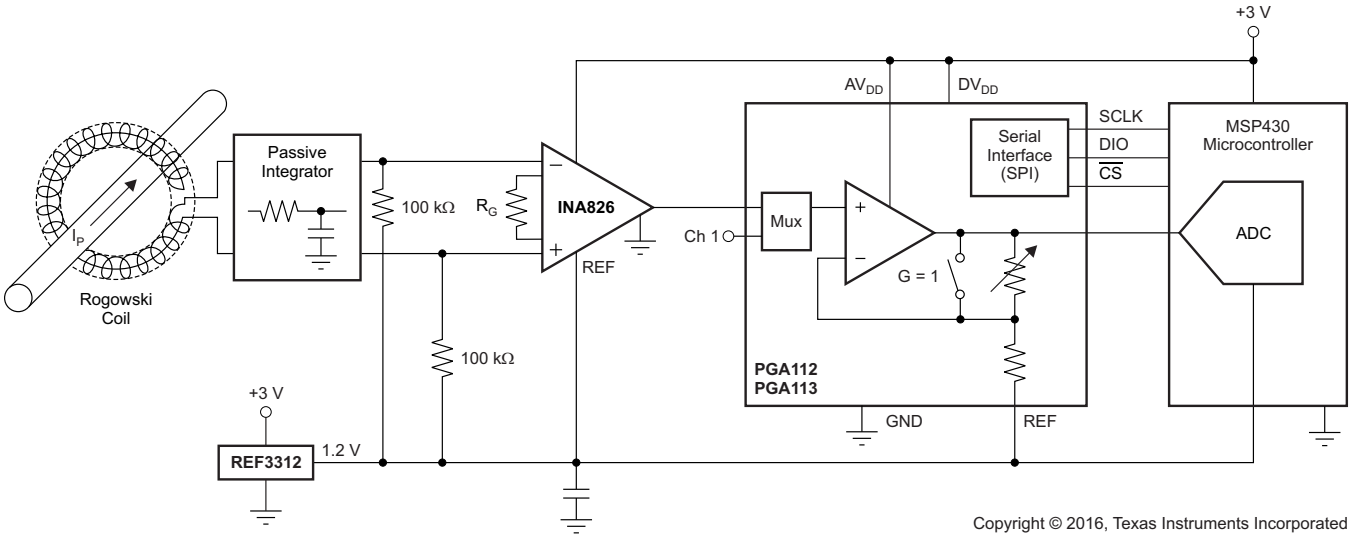


Figure 66. Circuit Breaker Example

9.3.2 Programmable Logic Controller (PLC) Input

The INA826 used in an example programmable logic controller (PLC) input application is shown in Figure 67.

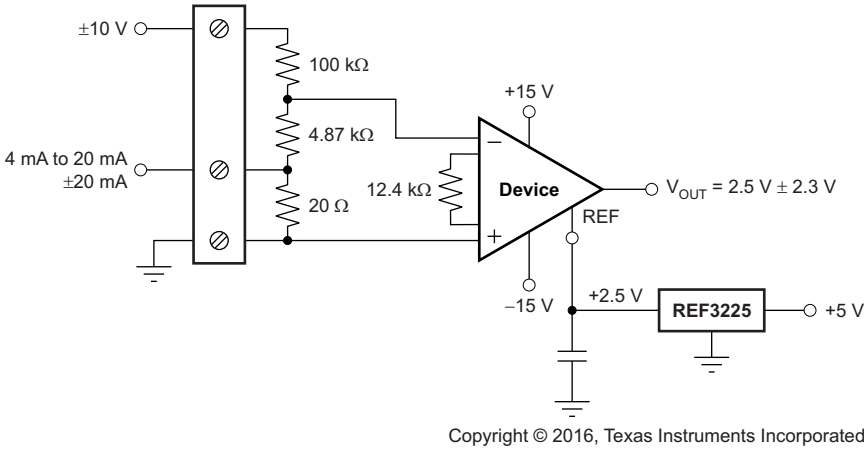


Figure 67. ±10-V, 4-mA to 20-mA PLC Input

Additional application ideas are illustrated in Figure 68 to Figure 72.

System Examples (continued)

9.3.3 Using TINA-TI SPICE-Based Analog Simulation Program with the INA826

TINA is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. TINA provides all the conventional dc, transient, and frequency domain analysis of SPICE as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer users the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Figure 68 and Figure 70 illustrate example TINA-TI circuits for the INA826 that can be used to develop, modify, and assess the circuit design for specific applications. Links to download these simulation files are provided in this section.

NOTE

These files require that either the TINA software (from DesignSoft) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

The circuit in Figure 68 is used to convert inputs of ±10 V, ±5 V, or ±20 mA to an output voltage range from 0.5 V to 4.5 V. The input selection depends on the settings of SW_1 and SW_2. Further explanation as well as the TINA-TI simulation circuit is provided in the compressed file that can be downloaded at the following link: *PLC Circuit*.

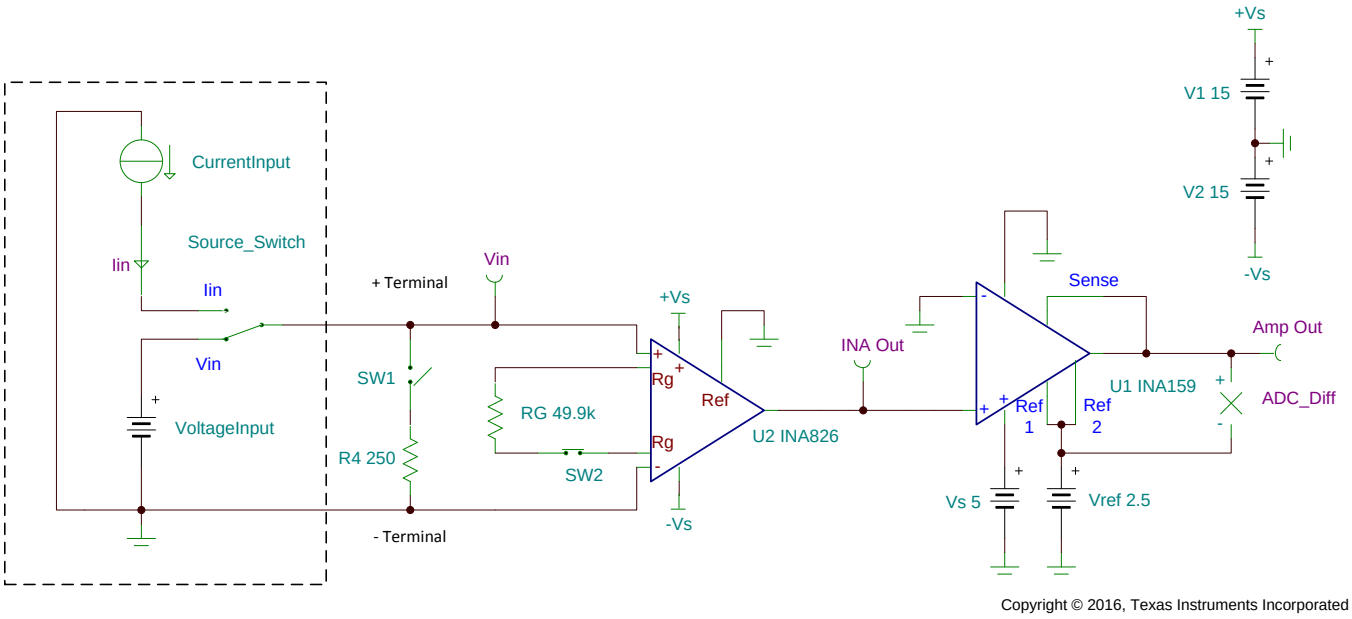


Figure 68. Two-Terminal Programmable Logic Controller (PLC) Input

System Examples (continued)

Figure 69 is an example of a LEAD I ECG circuit. The input signals come from leads attached to the right arm (RA) and left arm (LA). These signals are simulated with the circuitry in the corresponding boxes. Protection resistors (R_{PROT1} and R_{PROT2}) and filtering are also provided. The OPA333 is used as an integrator to remove the gained-up dc offsets and servo the INA826 outputs to V_{REF}. Finally, the right leg drive is biased to a potential ($+V_S$ / 2) and inverts and amplifies the average common-mode signal back into the patient's right leg. This architecture reduces the 50- and 60-Hz noise pickup.

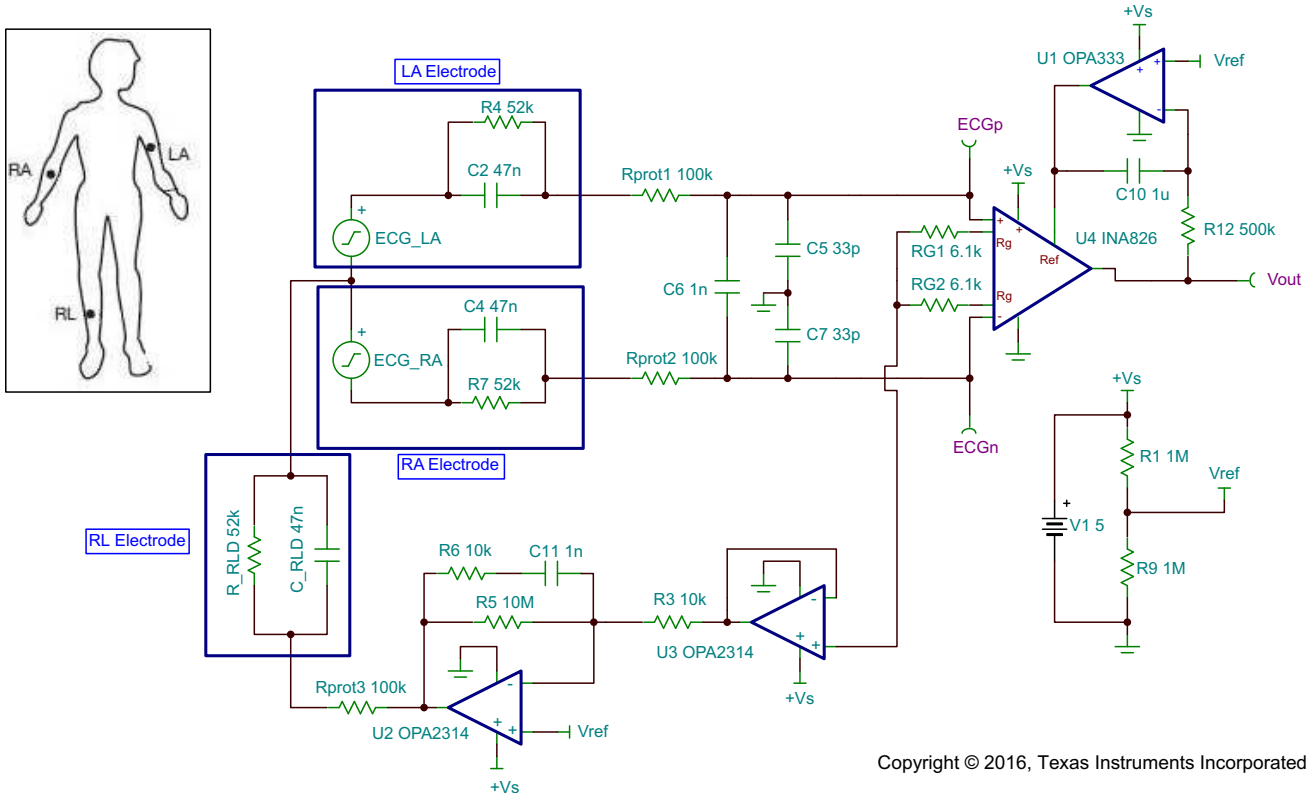


Figure 69. ECG Circuit

System Examples (continued)

Figure 70 shows an example of how the INA826 can be used for low-side current sensing. The load current (I_{LOAD}) creates a voltage drop across the shunt resistor (R_{SHUNT}). This voltage is amplified by the INA826 with gain set to 100. The output swing of the INA826 is set by the common-mode voltage (which is 0 V in low-side current sensing) and power supplies. Therefore, a dual-supply circuit is implemented. The load current is set from 1 A to 10 A, corresponding to an output voltage range from 350 mV to 3.5 V. The output range can be adjusted by changing the shunt resistor and the gain of the INA826. Click the following link to download the TINA-TI file: *Current Sensing Circuit*.

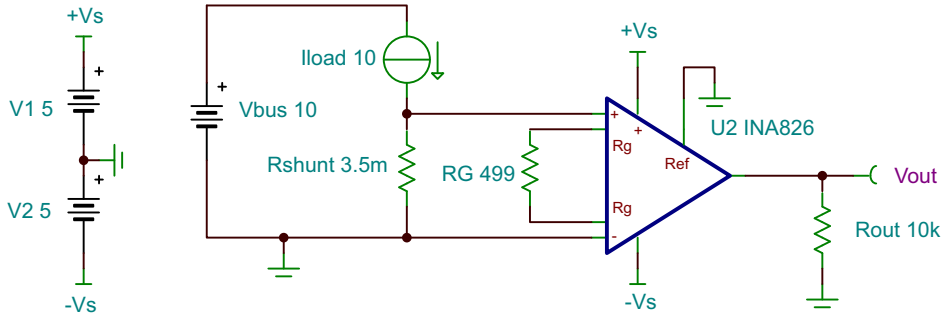


Figure 70. Low-Side Current Sensing

System Examples (continued)

Figure 71 shows an example of how the INA826 can be used for RTD signal conditioning. This circuit creates an excitation current (I_{SET}) by forcing 2.5 V from the REF5025 across R_{SET}. The zero-drift, low-noise OPA188 creates the virtual ground that maintains a constant differential voltage across R_{SET} with changing common-mode voltage. This voltage is necessary because the voltage on the positive input of the INA826 fluctuates over temperature as a result of the changing RTD resistance. Click the following link to download the TINA-TI file: *RTD Circuit*.

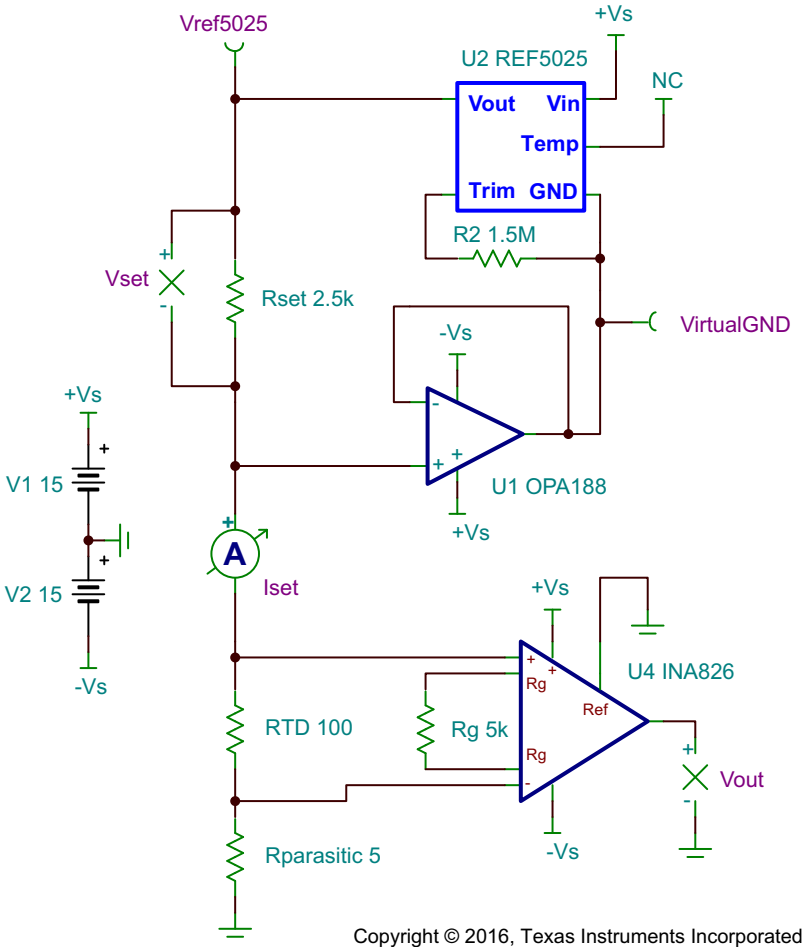


Figure 71. RTD Signal Conditioning

System Examples (continued)

The circuit in Figure 72 creates a precision current I_{SET} by forcing the INA826 V_{DIFF} across R_{SET}. The input voltage V_{IN} is amplified to the output of the INA826 and then divided down by the gain of the INA826 to create V_{DIFF}. I_{SET} can be controlled either by changing the value of the gain-set resistor R_G, the set resistor R_{SET}, or by changing V_{OUT} through the gain of the composite loop. Care must be taken to ensure that the changing load resistance R_L does not create a voltage on the negative input of the INA826 that violates the compliance of the common-mode input range. Likewise, the voltage on the output of the OPA170 must remain compliant throughout the changing load resistance for this circuit to function properly.

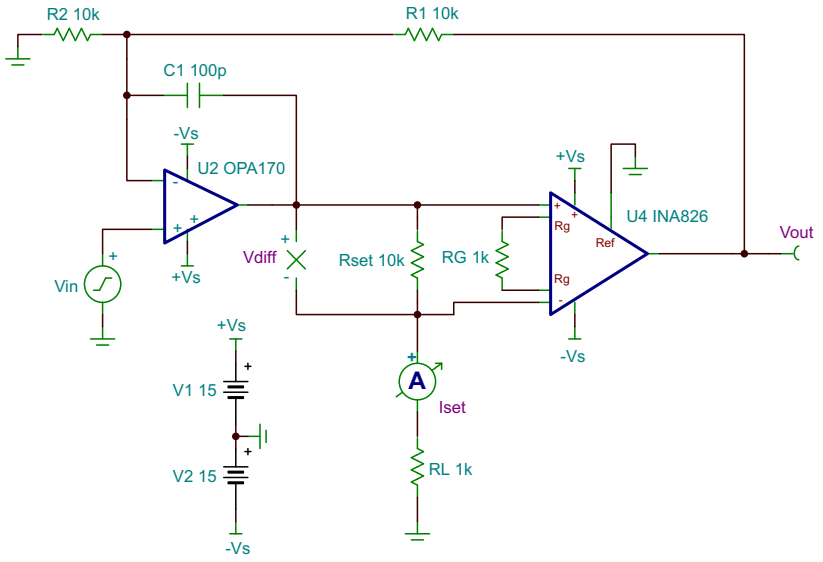


Figure 72. Precision Current Source

10 Power Supply Recommendations

The nominal performance of the INA826 is specified with a supply voltage of ±15 V and mid-supply reference voltage. The device can also be operated using power supplies from ±1.5 V (3 V) to ±18 V (36 V) and non mid-supply reference voltages with excellent performance. Parameters that can vary significantly with operating voltage and reference voltage are illustrated in the *Typical Characteristics* section.

11 Layout

11.1 Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place 0.1-μF bypass capacitors close to the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

The INA826EVM is intended to provide basic functional evaluation of the INA826. An image of the INA826EVM is provided in Figure 73. The INA826EVM is also available for purchase through the TI eStore.

11.1.1 CMRR vs Frequency

The INA826 pinout is optimized for achieving maximum CMRR performance over a wide range of frequencies. However, care must be taken to ensure that both input paths are well-matched for source impedance and capacitance to avoid converting common-mode signals into differential signals. In addition, parasitic capacitance at the gain-setting pins can also affect CMRR over frequency. For example, in applications that implement gain switching using switches or PhotoMOS® relays to change the value of R_G, choose the component so that the switch capacitance is as small as possible.

11.2 Layout Example

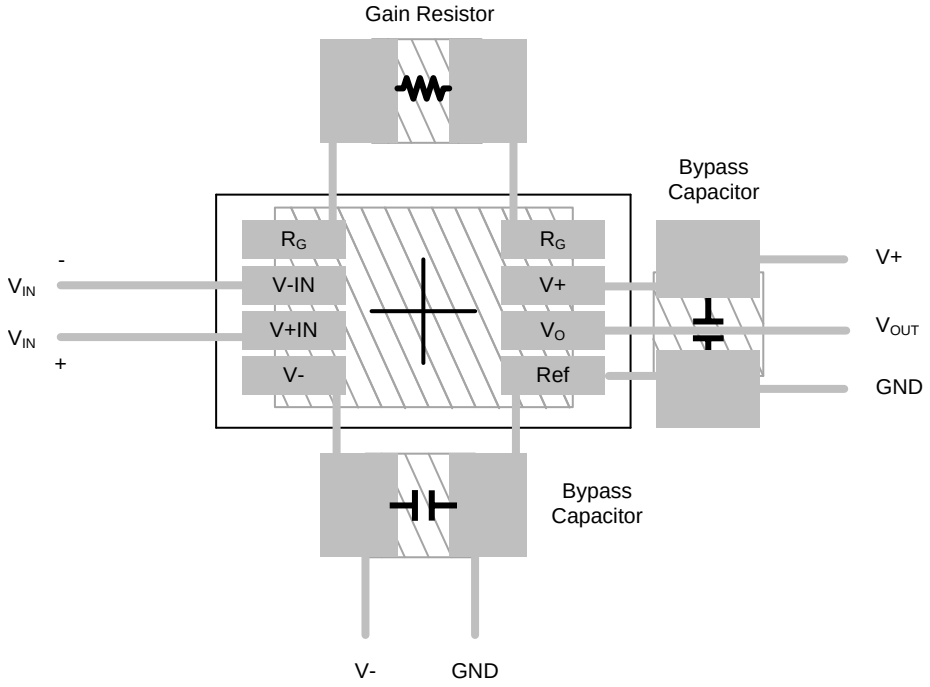


Figure 73. INA826 Example Layout

The INA826EVM provides the following features:

- Intuitive evaluation with silkscreen schematic
- Easy access to nodes with surface-mount test points
- Advanced evaluation with two prototype areas
- Reference voltage source flexibility
- Convenient input and output filtering

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

《OPAx330 50μV VOS、0.25μV/°C、35μA CMOS 运算放大器零漂移系列》（文献编号：SBOS432）

《REF32xx 4ppm/°C、100μA、SOT23-6 系列电压基准》（文献编号：SBVS058）

《REF50xx 低噪声、极低漂移、高精度电压基准》（文献编号：SBOS410）

《INA333 微功耗 (50μA)、零漂移、轨到轨输出仪表放大器》（文献编号：SBOS445）

《PGA280 零漂移高压可编程增益仪表放大器》（文献编号：SBOS487）

《INA159 高精度、0.2 级增益转换差分放大器》（文献编号：SBOS333）

《PGA11x 带多路复用器的零漂移可编程增益放大器》（文献编号：SBOS424）

《INA826EVM 用户指南》（文献编号：SBOU115）

TINA-TI 软件文件夹

12.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

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12.5 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA826AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA826	Samples
INA826AIDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPDI	Samples
INA826AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPDI	Samples
INA826AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA826	Samples
INA826AIDRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPEI	Samples
INA826AIDRGT	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	IPEI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

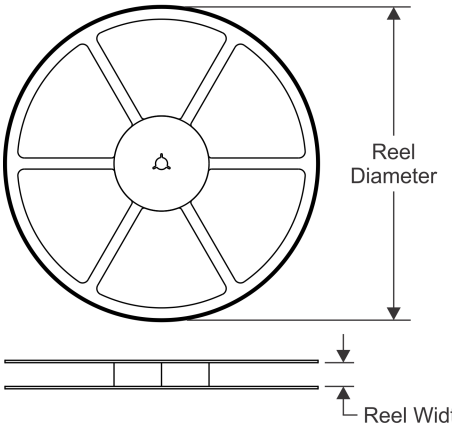
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

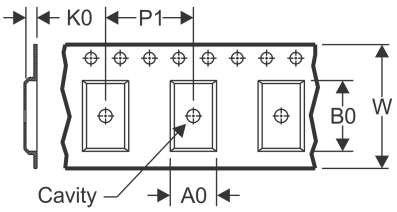
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

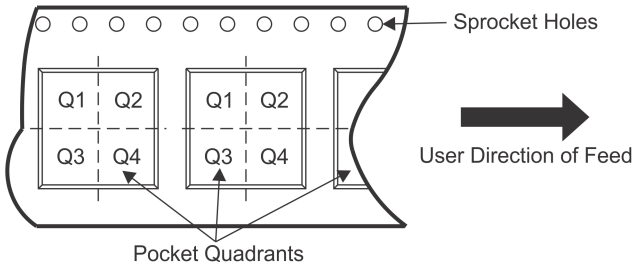


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

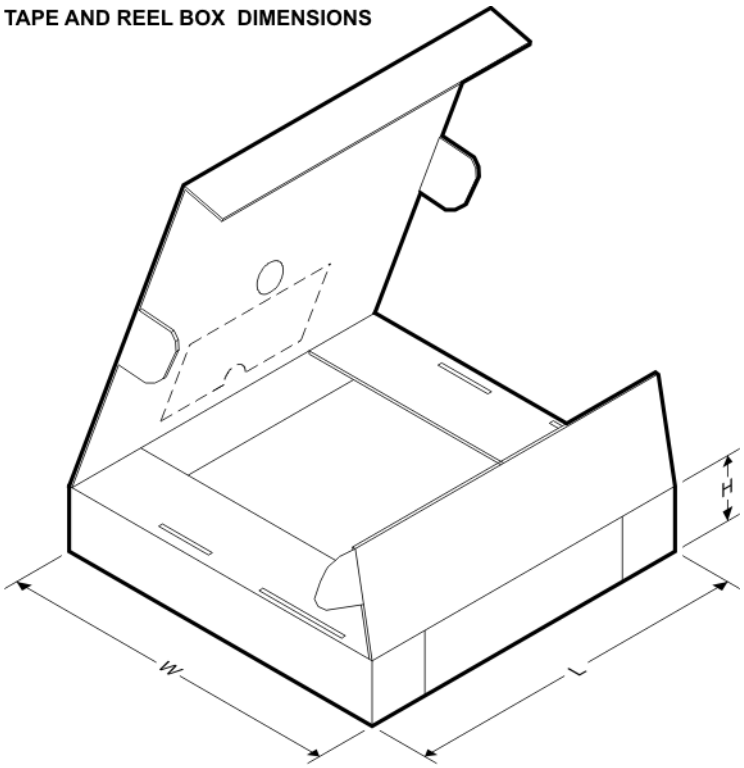
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA826AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA826AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA826AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
INA826AIDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

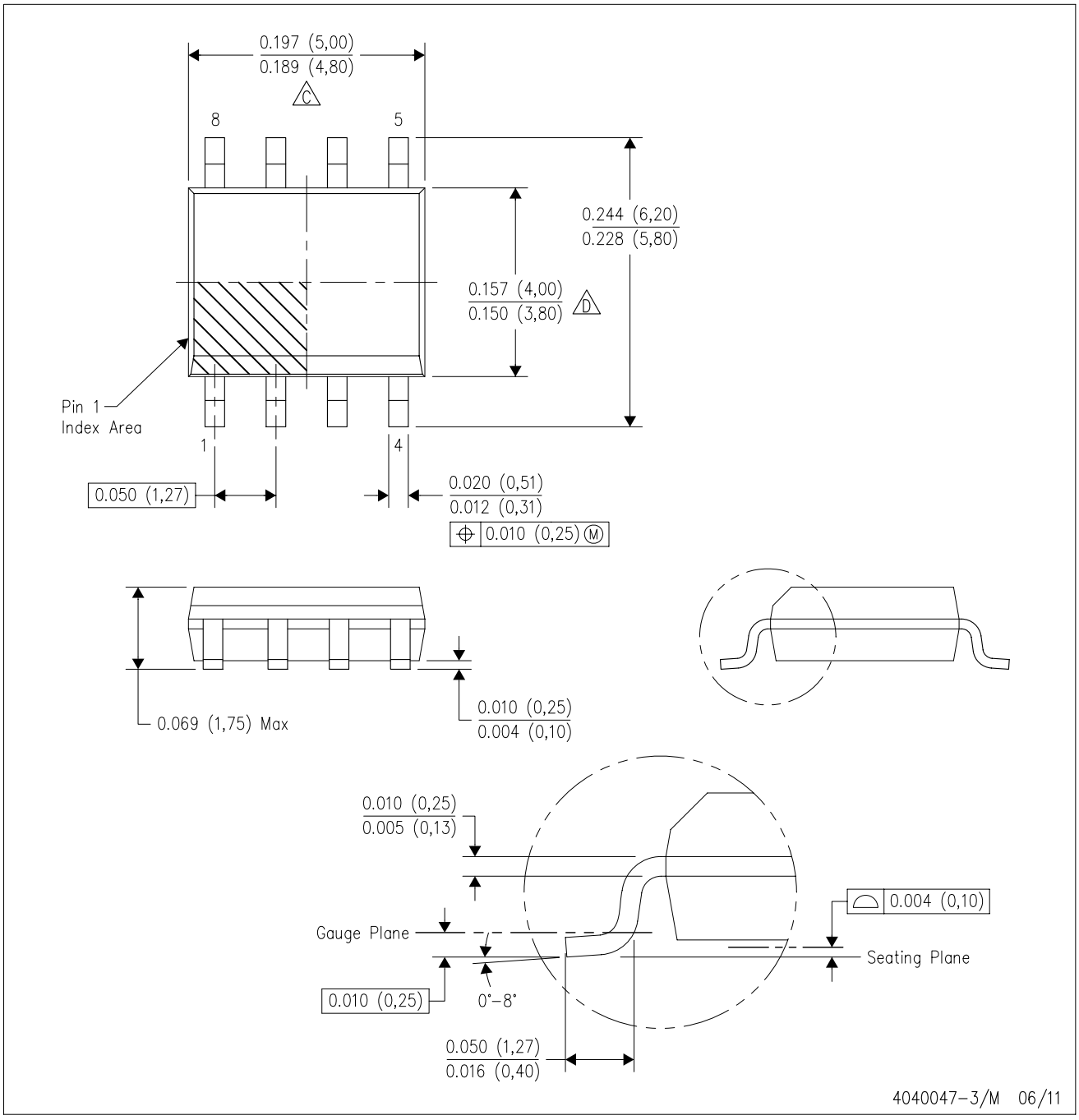
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

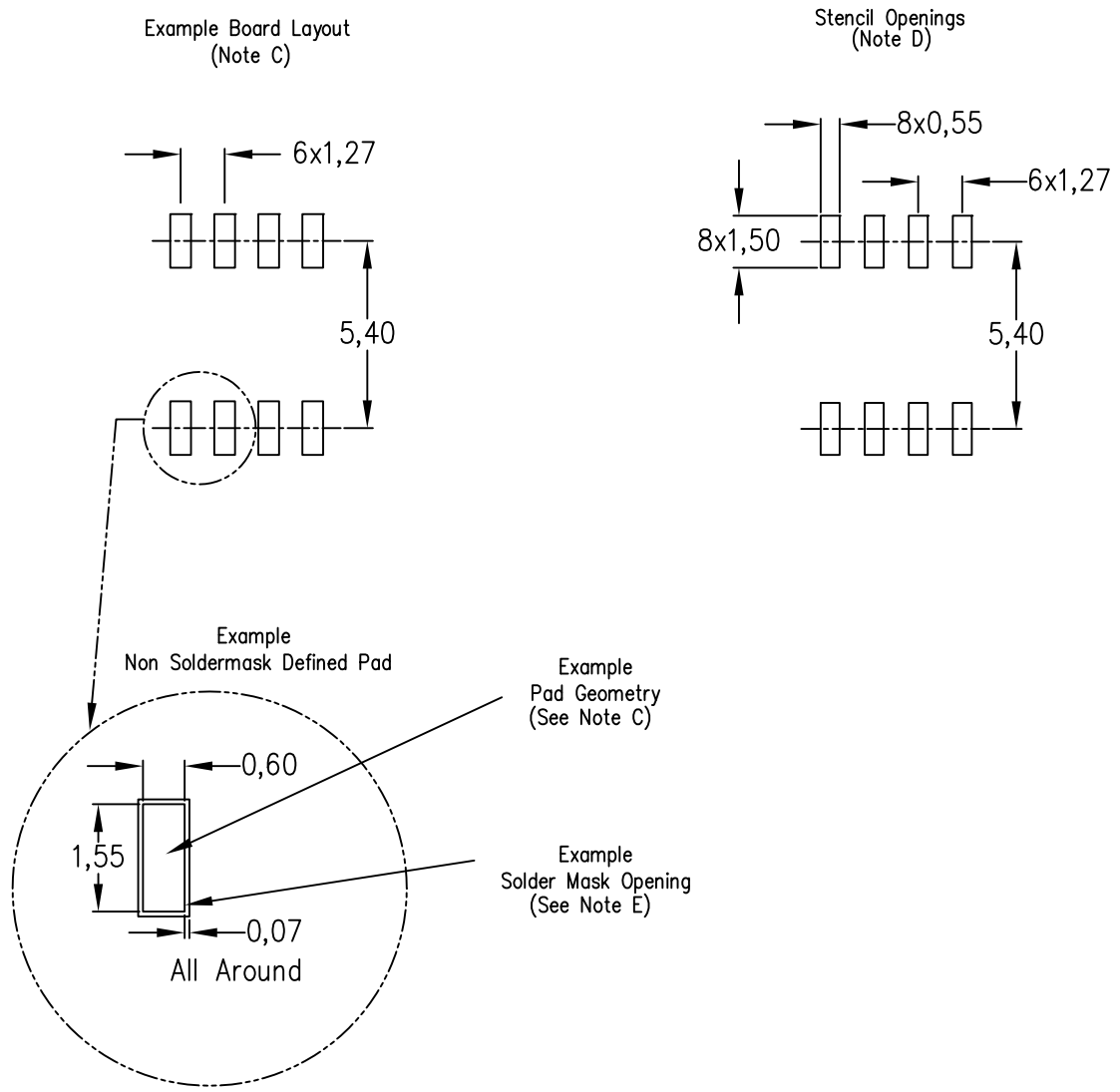
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA826AIDGKR	VSSOP	DGK	8	2500	346.0	346.0	41.0
INA826AIDR	SOIC	D	8	2500	367.0	367.0	35.0
INA826AIDRGR	SON	DRG	8	3000	367.0	367.0	35.0
INA826AIDRGT	SON	DRG	8	250	210.0	185.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



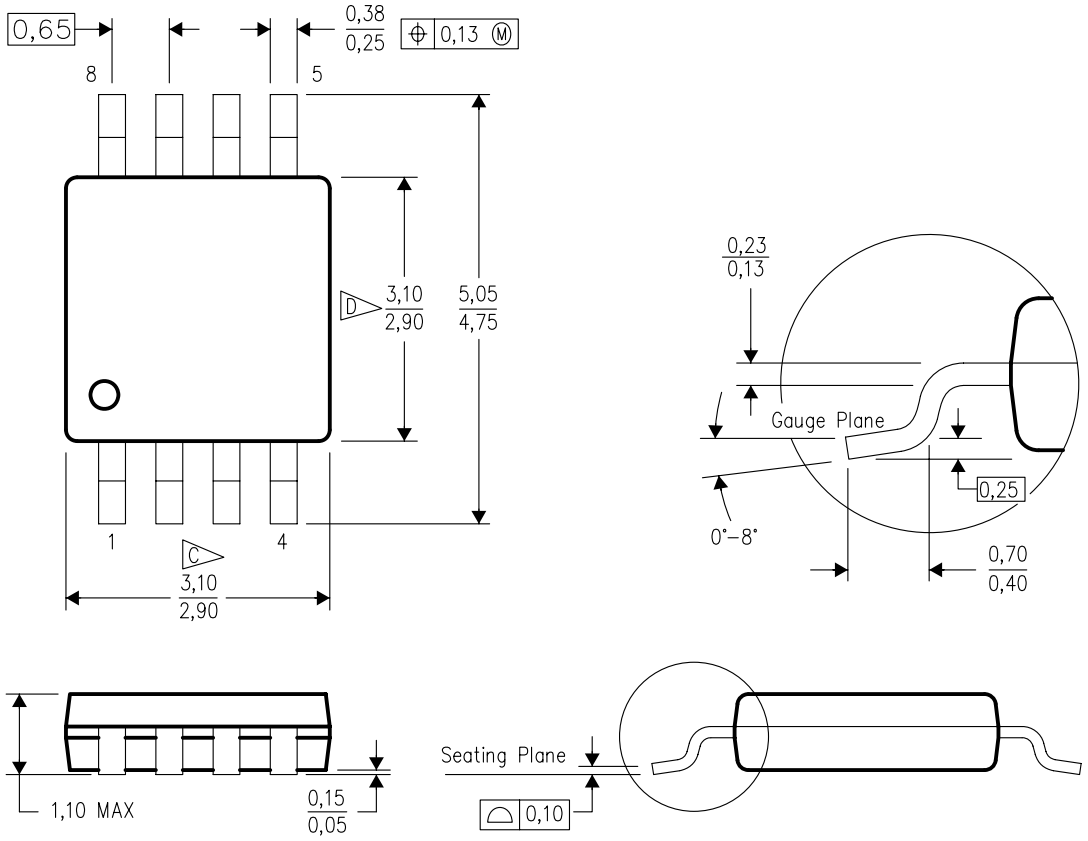
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

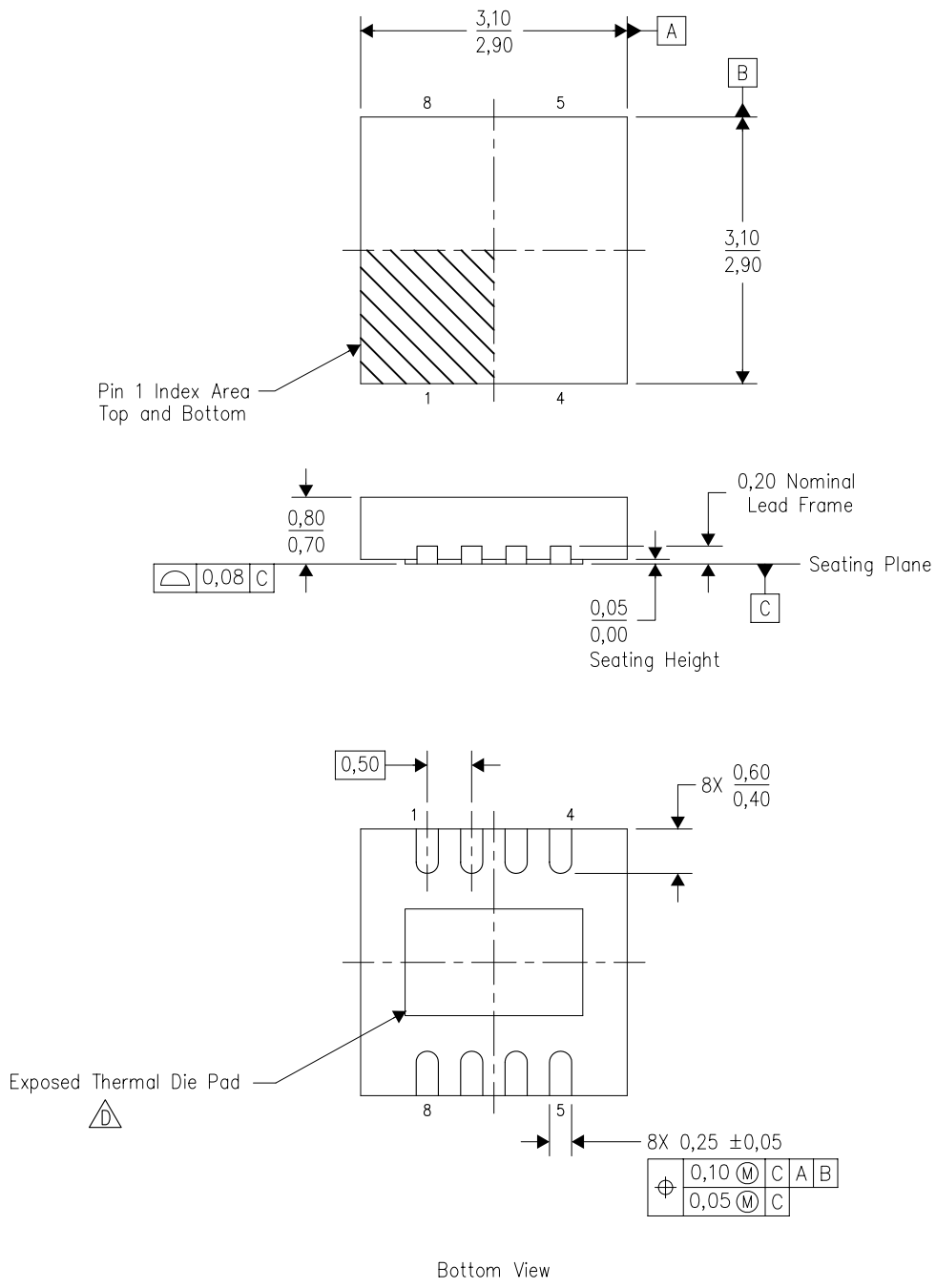
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

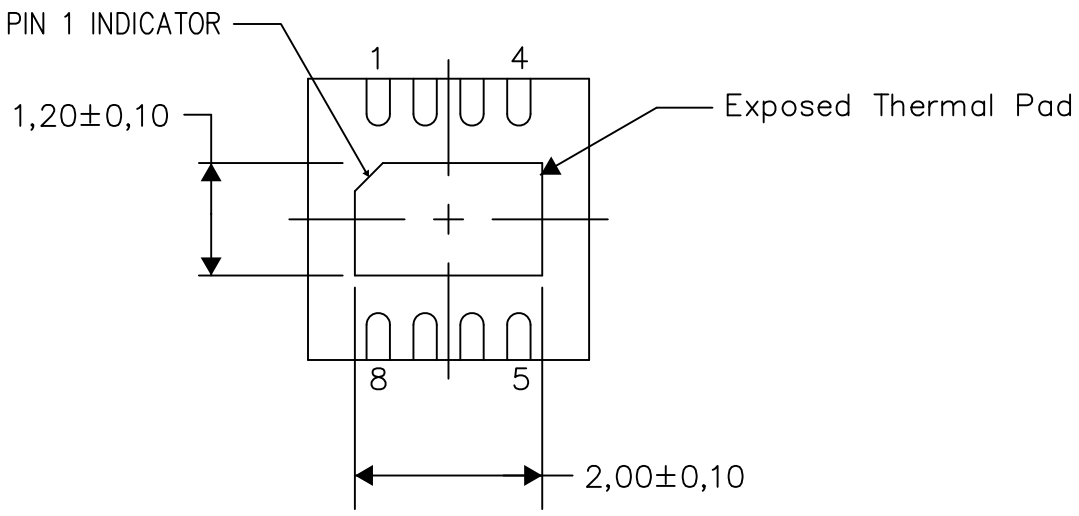
DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



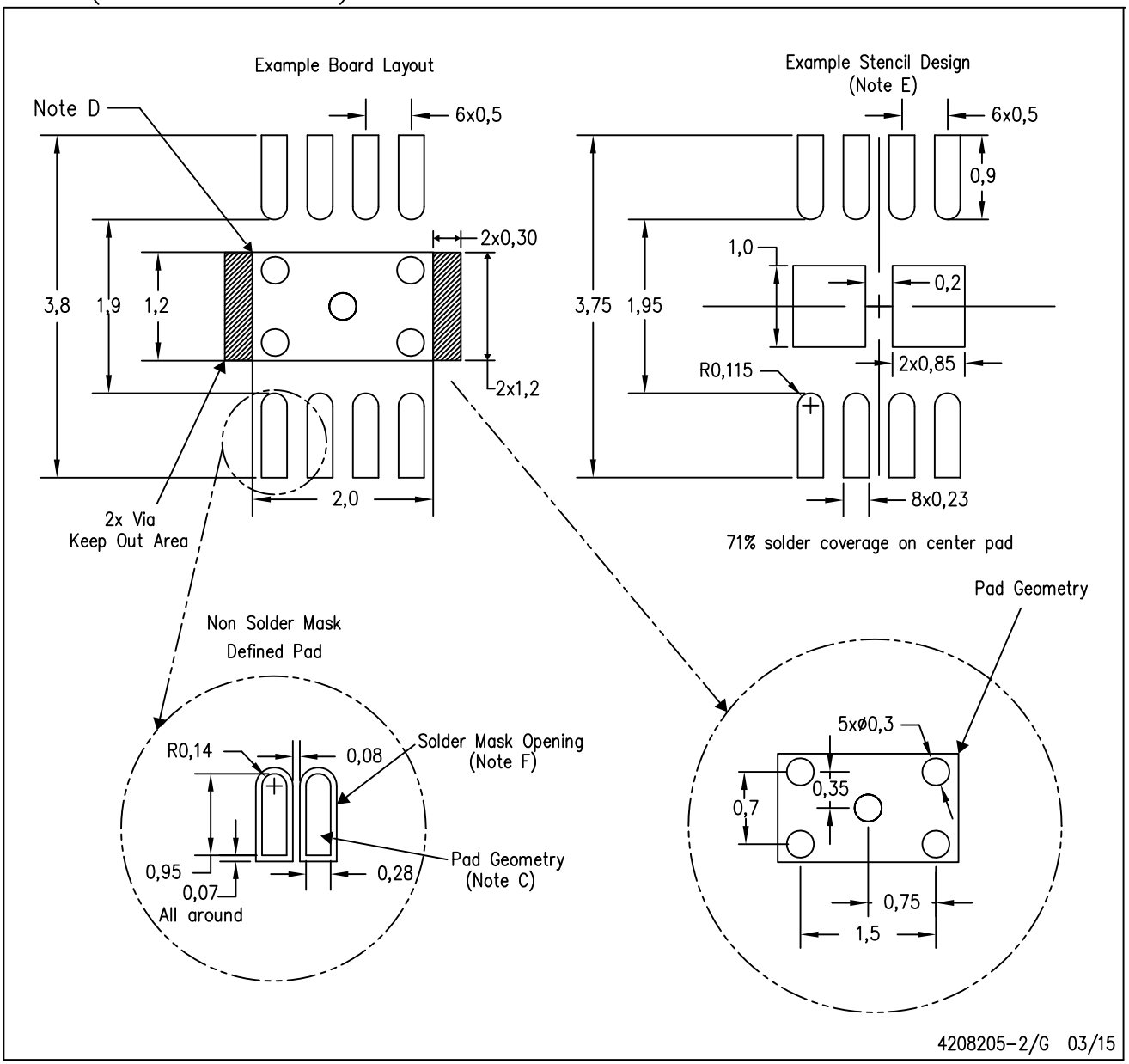
Bottom View

Exposed Thermal Pad Dimensions

4206881–2/I 03/15

NOTE: All linear dimensions are in millimeters

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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