Application Notes: AN_SY8204

High Efficiency Fast Response, 4A, 30V Input Synchronous Step Down Regulator

General Description

SY8204 develops a high efficiency synchronous step-down DC-DC converter capable of delivering 4A output current. SY8204 operates over a wide input voltage range from 4.5V to 30V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

SY8204 adopts the proprietary instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. In addition, it operates at pseudo-constant frequency of 500kHz under continous conduction mode to minimize the size of inductor and capacitor.

Ordering Information

SY8204 ( )

- Temperature Code
- Package Code
- Optional Spec Code

Temperature Range: -40°C to 85°C

Ordering Number	Package type	Note
SY8204FCC	SO8E	--

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom): 80/50 mΩ
- 4.5-30V input voltage range
- Instant PWM architecture to achieve fast transient responses
- External softstart limits the inrush curre t
- Pseudo-constant frequency: 500kHz at heavy loads
- 4A continuous, 5A peak load current capability
- 1.5% 0.6V reference
- Output over current limit
- Output short circuit p otection with current fold back
- Thermal shut own and auto recovery
- RoHS Compliant and Halogen Free
- Compact package: SO8E

Applications

- LCD-TV
- SetTop Box
- Notebook
- High power AP router
- LCD Monitor
- DVR/NVR
- NAS

Typical Applications

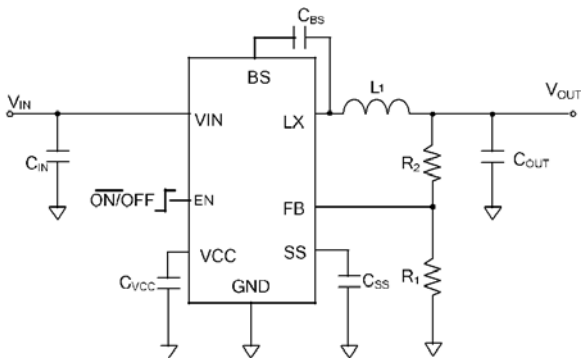


Figure 1. Schematic Diagram

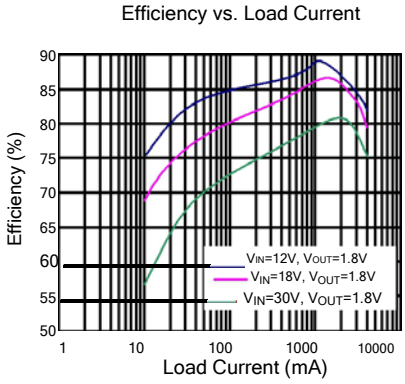
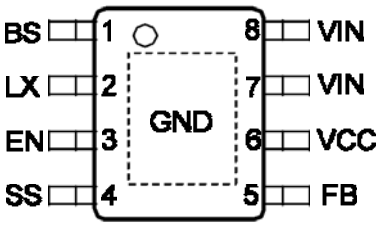


Figure 2. Efficiency vs. Load Current

Pinout (top view)



Top Mark: AHI*xyz* (device code: AHI, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
EN	3	Enable control.
BS	1	Boot-Strap Pin. Supply high side gate driver. Decouple his pin to LX pin with 0.1uF ceramic cap.
LX	2	Inductor pin. Connect this pin to the switching node of inductor
VCC	6	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Add a 1uF bypass capacitor between this pin and GND.
VIN	7,8	Voltage Supply Pin. Decouple this pin to GND pin with at least 4.7uF ceramic cap.
FB	5	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: Vout=0.6*(1+R1/R2)
GND	Exposed Paddle	Ground pin.
SS	4	Softstart programming pin. Connect a capacitor from this pin to ground to program the softst rt time. Tss=Css*0.6V/10uA

Absolute Maximum Ratings (Note 1)

VIN, LX, BS, EN---------- 33V
VCC, FB, SS, BS-LX ---------- 4V
Power Dissipation, P_D @ T_A = 25°C SO8E---------- ---------- 3.3W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 30°C/W
θ_{JC} ---------- 10°C/W
Junction Temperature Range ---------- - 40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- - 65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4.5V to 30V
Junction Temperature Range ---------- - 40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(VIN = 12V, VOUT = 5V, COUT = 47uF, TA = 25°C, IOUT = 1A unless otherwise specified)

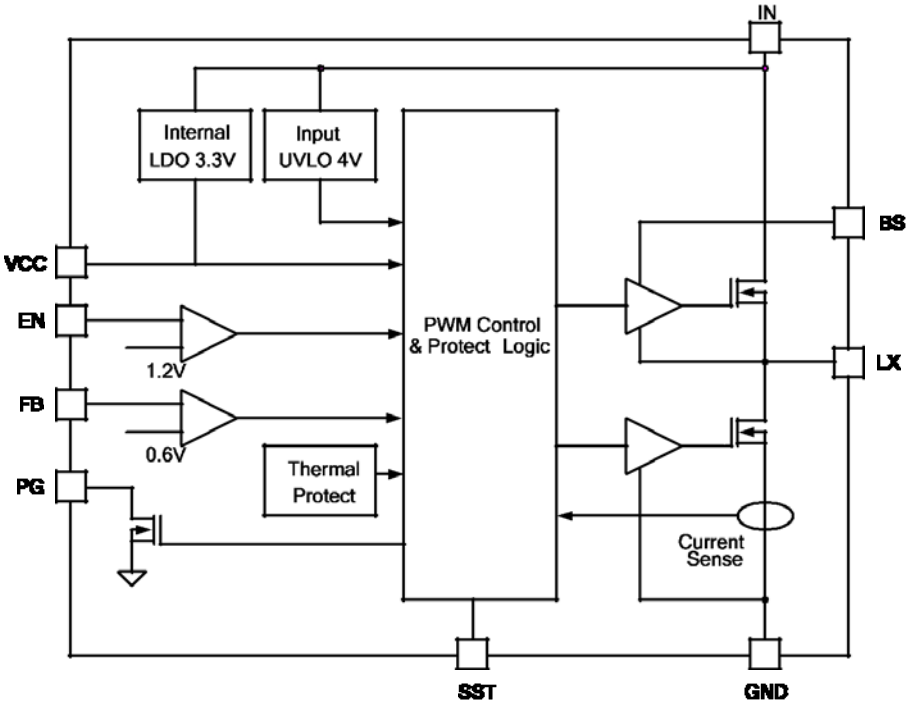
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		30	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}*105%		200		μA
Shutdown Current	I_{SHDN}	EN=0		5	10	μA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
FB Input Current	I_{FB}	V_{FB}=V_{CC}	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			80		mΩ
Bottom FET RON	$R_{DS(ON)2}$			50		mΩ
Bottom FET Current Limit	I_{LIM}		5			A
EN falling threshold	V_{ENL}		1.1	1.2	1.3	V
EN threshold hysteresis	$V_{EN,HYS}$			0.1		V
Input UVLO threshold	V_{UVLO}				4	V
UVLO hysteresis	V_{HYS}			0.2		V
Oscillator Frequency	F_{OSC}	I_{OUT}=200mA		0.5		MHz
Min ON Time				80		ns
Min OFF Time				120		ns
Internal LDO Output	V_{VCC}	V_{IN}=4V	3.2	3.3	3.4	V
Thermal Shutdown Temperature	T_{SD}			160		°C
Thermal Shutdown Hysteresis	$T_{SD,HYS}$			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" ma y cause permanent damage to the device. These are stress ratings only. Functional operation of the evice at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θJA is measured in the natural convection at T_A = 25°C on a low effective single layer thermal con ductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of SO8E packages is the case position for θJC measurement.

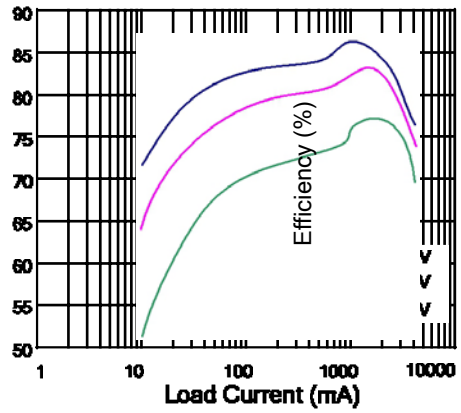
Note 3: The device is not guaranteed to function outside its operating conditions.

Function Block

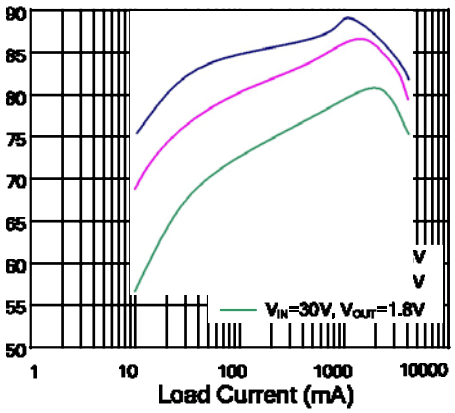


Typical Performance Characteristics

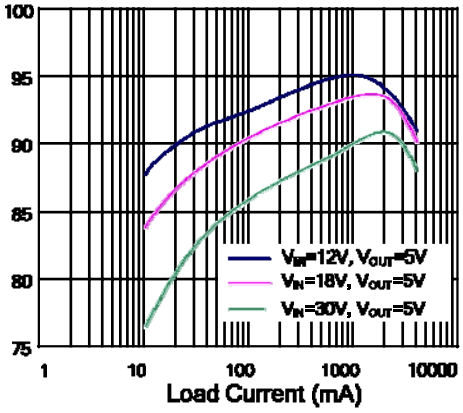
Efficiency vs. Load Current



Efficiency vs. Load Current



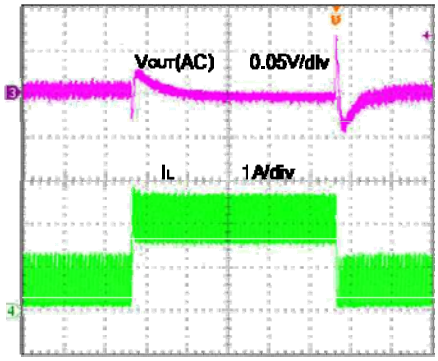
Efficiency vs. Load Current



Efficiency (%)

Load Transient

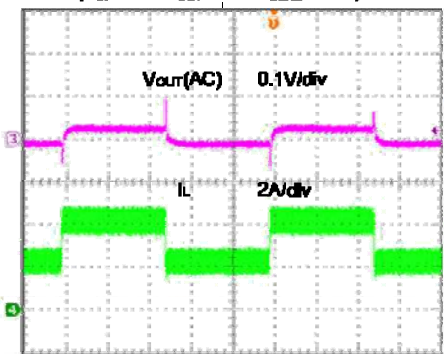
(V_{IN}=12V, V_{OUT}=1.8V, I_{LOAD}=0.4-2A)



Time (100µs/div)

Load Transient

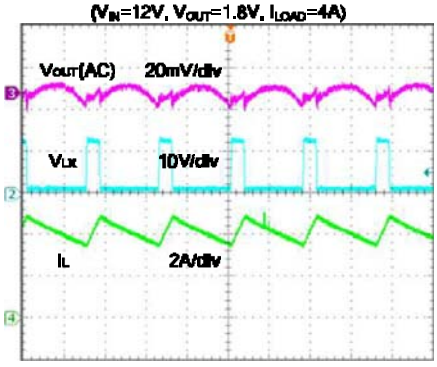
(V_{IN}=12V, V_{OUT}=1.8V, I_{LOAD}=2-4A)



Time (100µs/div)

Output Ripple

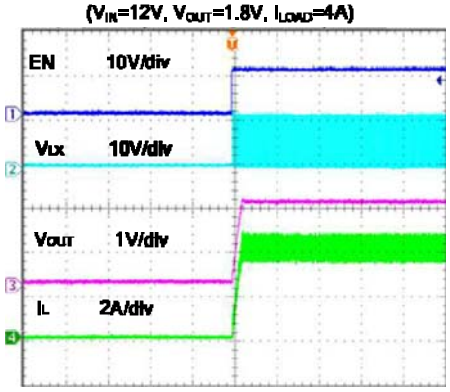
(V_{IN}=12V, V_{OUT}=1.8V, I_{LOAD}=4A)



Time (1µs/div)

Startup

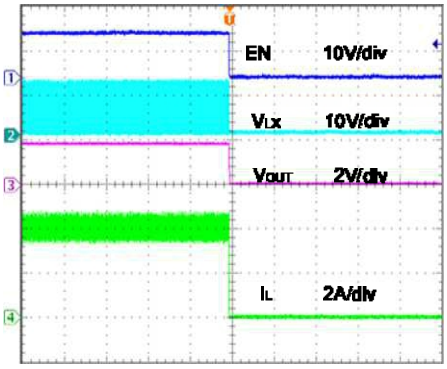
(V_{IN}=12V, V_{OUT}=1.8V, I_{LOAD}=4A)



Time (10ms/div)

Shutdown

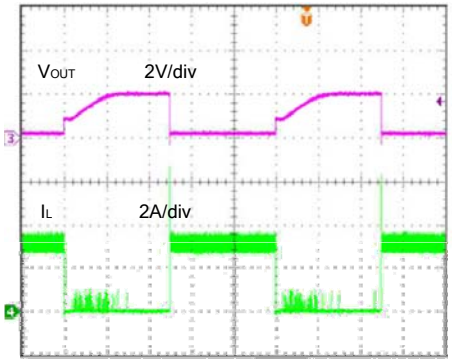
(V_{IN}=12V, V_{OUT}=1.8V, I_{LOAD}=4A)



Time (10ms/div)

Short Circuit Protection

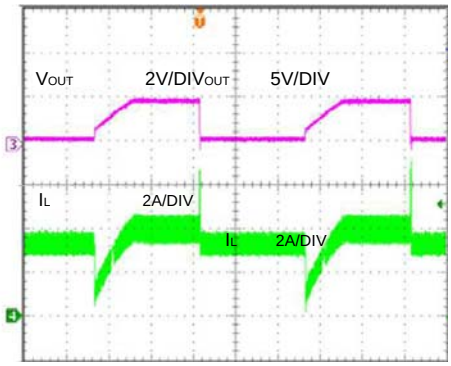
(V_{IN}=12V, V_{OUT}=1.8V, Open to Short)



Time (2ms/div)

SH RT CIRCUIT PROTECTION

(V_{IN}=12V, V_{OUT}=1.8V, 4A TO SHORT)



TIME (2MS/DIV)

Operation

SY8204 is a synchronous buck regulator IC that integrates the PWM control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low Rds(on) power switches and proprietary PWM control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

SY8204 provides protection functions such as cycle by cycle current limiting and thermal shutdown protection. SY8204 will sense the output voltage conditions for the fault protection.

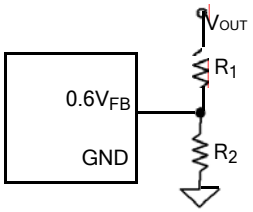
Applications Information

Because of the high integration in the SY8204 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If Vout is 3.3V, R_1=100k is chosen, then using following equation, R_2 can be calculated to be 22.1k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 .$$



Input capacitor C_{IN}:

The ripple cu ent through input capacitor is calculated as：

$$I_{CIN\_RMS} = I_{OUT} \cdot \sqrt{D(1-D)} .$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 10uF low ESR ceramic capacitor is recommended.

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor greater than 47uF capacitance.

Output inductor L:

There are several considerations in choos ng this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.
The SY8204 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mΩ to achieve a good overall efficiency.

Soft-start

Connect a capacitor from softstart programming pin to ground to program the softstart time.

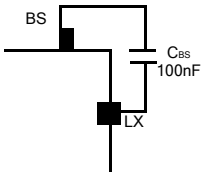
Tss=Css*0.6V/10uA

Enable Operation

Pulling the EN pin low (<1.2V) will shut down the device. During shutdown mode, the SY8204 shutdown current drops to lower than 5uA, Driving the EN pin high (>1.3V) will turn on the IC again.

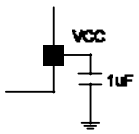
External Boostrap Cap

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.



VCC LDO

The 3.3V internal reference. This pin should be bypassed to ground with a 1uf ceramic capacitor. This pin may be used with an external DC load of 20mA or less



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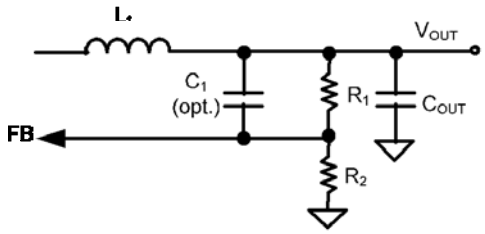
Load Transient Considerations:

The SY8204 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 100pF ceramic cap in parallel with R1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.



Layout Design:

The layout design of SY8204 regulator is relatively simple. For the best efficiency and minimum noise promblem, we should place the follow g components close to the IC: C_{IN}, C_{VCC} L, R1 and R2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desi able.

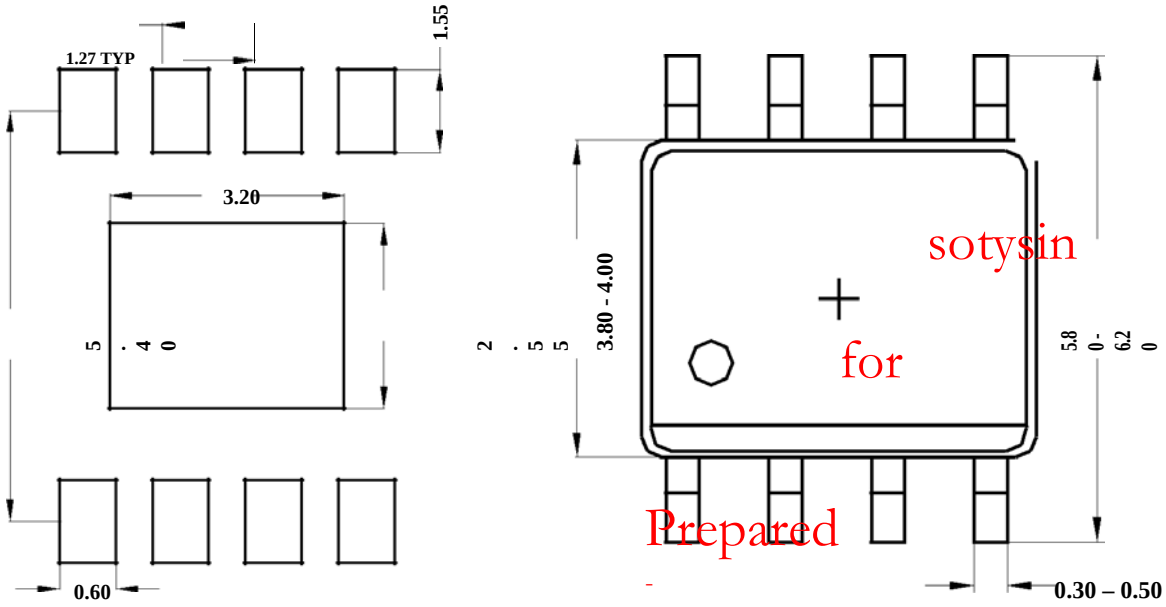
2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

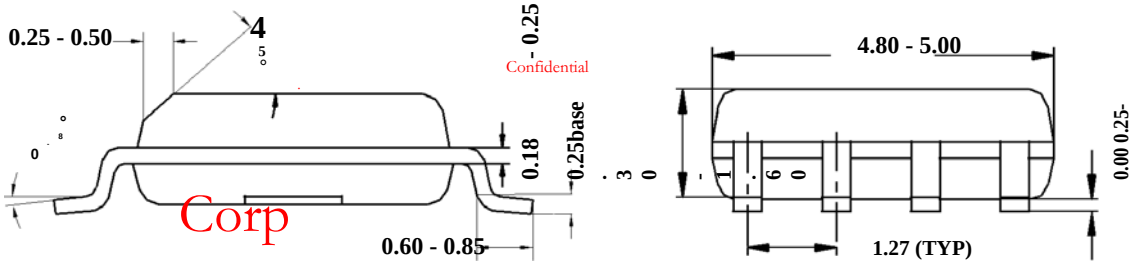
4) The components R_1 and R_2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

SO8E Package outline & PCB layout design



Recommended Pad Layout



Notes: All dimensions are in millimeters.

Silergy

All dimensions don't include mold flash & metal burr.