TLV8x3 具有低电平有效的开漏复位功能的 3 引脚电压监控器

1 特性

- 3 引脚 SOT23 封装
- 电源电流：9μA（典型值）
- 精密电源电压监视器：
  2.5V、3V、3.3V 和 5V
- 具有 200ms 固定延迟时间的
  上电复位发生器
- 与 MAX803 引脚兼容
- 温度范围：-40°C 至 +125°C
- 开漏、$\overline{\text{RESET}}$ 输出

2 应用

- 数字信号处理器 (DSP)、微控制器和微处理器
- 便携式和电池供电类设备
- 机顶盒
- 服务器
- 电器
- 可编程控制元件
- 智能仪表
- 工业设备
- 车载系统

3 说明

TLV8x3 系列监控电路主要为数字信号处理器 (DSP) 以及基于处理器的系统提供电路初始化和时序监控。

TLV803、TLV853 和 TLV863 在功能上是等效的。TLV853 和 TLV863 分别提供了与 TLV803 不同的替代引脚分配。

上电期间，$\overline{\text{RESET}}$ 会在电源电压 (V_{DD}) 超出 1.1V 时置为有效。因此只要满足以下条件，监控电路就会监视 V_{DD} 并将 $\overline{\text{RESET}}$ 保持为有效状态：V_{DD} 保持在阈值电压 V_{IT} 以下。内部定时器将使输出延迟恢复至待机状态（高电平），以确保系统正常复位。延迟时间 ($t_{d(typ)}$ = 200ms) 从 V_{DD} 超过阈值电压 V_{IT} 后开始。当电源电压降至阈值电压 V_{IT} 以下时，输出再次变为激活状态（低电平）。该系列中的所有器件均具有一个通过内部分压器设定的固定感测阈值电压 (V_{IT})。

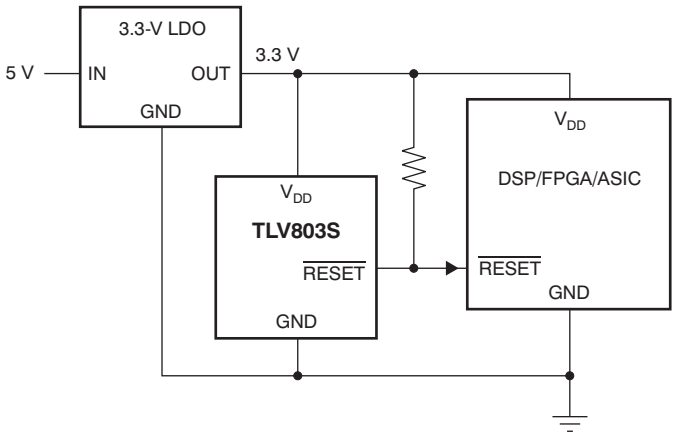
该产品系列专为 2.5V、3V、 3.3 以及 5V 电源电压而设计。这些器件采用 3 引脚小外形尺寸晶体管 (SOT)-23 封装。TLV803 器件的额定工作温度范围为 -40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLV8x3	SOT-23 (3)	2.92mm × 1.30mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。

典型应用



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (August 2011) to Revision C **Page**

- 已将 TLV853 器件添加至数据表 ... 1
- 已将页眉上显示的器件部件编号从标有字母的器件版本更改为显示单个 TLV803 器件 ... 1
- 已添加*器件信息*和 *ESD 额定值*表 ... 1
- 已添加*详细 说明*，*应用和实施*，*电源相关建议*，*布局*，*器件和文档支持*以及*机械、封装和可订购信息*部分 ... 1
- 已更改*应用*部分要点 ... 1
- 已从首页中删除引脚分配并将其移动至*引脚配置和功能*部分 ... 1
- Deleted Package/Ordering Information table; for package and ordering information, see the package option addendum at the end of the data sheet. ... 3
- Changed all "free-air" to "junction" and all "T_A" to "T_J" for all temperature ranges throughout data sheet ... 4
- Changed "free-air temperature" to "junction temperature" in *Absolute Maximum Ratings* condition statement ... 4
- Deleted *Soldering temperature* from *Absolute Maximum Ratings* table ... 4
- Changed *Thermal Information* table; updated thermal resistance values for all parameters ... 4
- Changed "free-air temperature" to "junction temperature" in *Electrical Characteristics* condition statement ... 5
- Changed temperature noted in *Switching Characteristics* condition statement ... 5

Changes from Revision A (June 2011) to Revision B **Page**

- 已将关于 TLV863 的新段落添加至*说明*部分 ... 1
- 已在首页中添加 TLV863 引脚分配 ... 1
- Added TLV863M to Package/Ordering Information ... 3
- Added TLV863 to Thermal Information ... 4
- Added TLV863M to Negative-Going Input Threshold Voltage parameter ... 5
- Added TLV863M to Hysteresis parameter ... 5
- Added TLV863 to Functional Block Diagram ... 7

5 Device Comparison

Table 1. Device Threshold Options

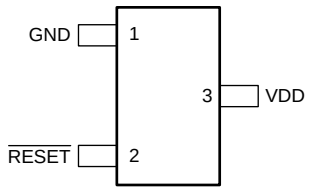
DEVICE	THRESHOLD VOLTAGE
TLV803Z	2.25 V
TLV803R	2.64 V
TLV803S	2.93 V
TLV803M	4.38 V
TLV853M	4.38 V
TLV863M	4.38 V

Table 2. Device Family Comparison

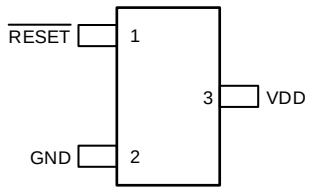
DEVICE	FUNCTION
TLV803	Open-Drain, $\overline{\text{RESET}}$ Output
TLV809	Push-Pull, $\overline{\text{RESET}}$ Output
TLV810	Push-Pull, RESET Output

6 Pin Configuration and Functions

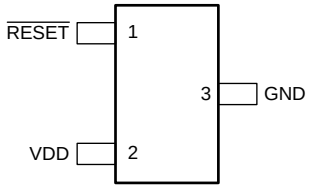
TLV803: DBZ Package
3-Pin SOT-23
Top View



TLV853: DBZ Package
3-Pin SOT-23
Top View



TLV863: DBZ Package
3-Pin SOT-23
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	TLV803	TLV853	TLV863		
GND	1	2	3	—	Ground pin.
$\overline{\text{RESET}}$	2	1	1	O	$\overline{\text{RESET}}$ is an open-drain output that is driven to a low impedance state when $\overline{\text{RESET}}$ is asserted. $\overline{\text{RESET}}$ remains low (asserted) for the delay time (t_d) after V_{DD} exceeds V_{IT-}. Use a 10-kΩ to 1-MΩ pullup resistor on this pin. The pullup voltage is not limited by V_{DD}.
VDD	3	3	2	I	Supply voltage pin. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	VDD(2)	0	7	V
	All other pins(2)	–0.3	+7	
Current	Maximum low output current, I_{OL}		5	mA
	Maximum high output current, I_{OH}		–5	
	Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})		±20	
	Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})		±20	
Temperature	Operating junction temperature range, T_J	–40	125	°C
	Storage temperature range, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation the device should not be operated at 7 V for more than t = 1000h continuously

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Thermal Information

THERMAL METRIC(1)		TLV8x3 DBZ (SOT-23) 3 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	328.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	135.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	59.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.4 Recommended Operating Conditions

at specified temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	1.1	6	V
T_J	Operating junction temperature	–40	125	°C

7.5 Electrical Characteristics

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage		V_{DD} = 2 V to 6 V, I_{OL} = 500 µA			0.2	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA			0.4	
			V_{DD} = 6 V, I_{OL} = 4 mA			0.4	
	Power-up reset voltage(1)		I_{OL} = 50 µA, V_{OL} < 0.2 V	1.1			V
V_{IT-}	Negative-going input threshold voltage(2)	TLV803Z	T_J = – 40°C to +125°C	2.20	2.25	2.30	V
		TLV803R		2.58	2.64	2.70	
		TLV803S		2.87	2.93	2.99	
		TLV8x3M		4.28	4.38	4.48	
V_{hys}	Hysteresis	TLV803Z	T_J = 25°C, I_{OL} = 50 µA		30		mV
		TLV803R			35		
		TLV803S			40		
		TLV8x3M			60		
I_{DD}	Supply current		V_{DD} = 2 V, output unconnected		9	15	µA
			V_{DD} = 6 V, output unconnected		20	30	
I_{OH}	Output leakage current		V_{DD} = 6 V			100	nA

(1) The lowest supply voltage at which $\overline{\text{RESET}}$ becomes valid. $t_{r,VDD} \leq 66.7$ V/ms.
(2) To ensure best stability of the threshold voltage, place a bypass capacitor (0.1-µF ceramic) near the supply terminals.

7.6 Switching Characteristics

over operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse duration at V_{DD}	V_{DD} = 1.08 V_{IT-} to 0.92 V_{IT-}		1		µs
t_d	Delay time	$V_{DD} \geq V_{IT-}$ + 0.2 V; see Timing Diagram	120	200	280	ms

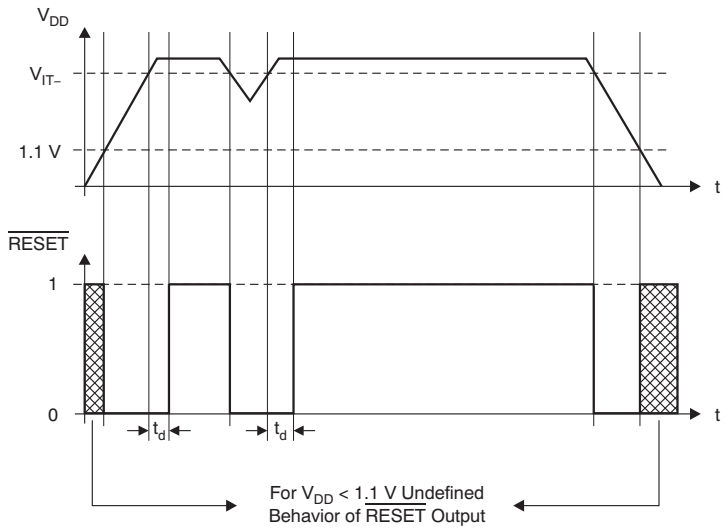


Figure 1. Timing Diagram

7.7 Typical Characteristics

at T_J = 25°C, V_{IT-} = 4.38 V, and V_{DD} = 5.0 V (unless otherwise noted)

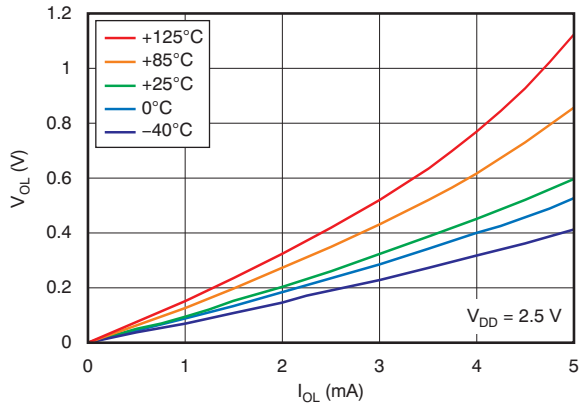


Figure 2. Low-Level Output Voltage vs Low-Level Output Current

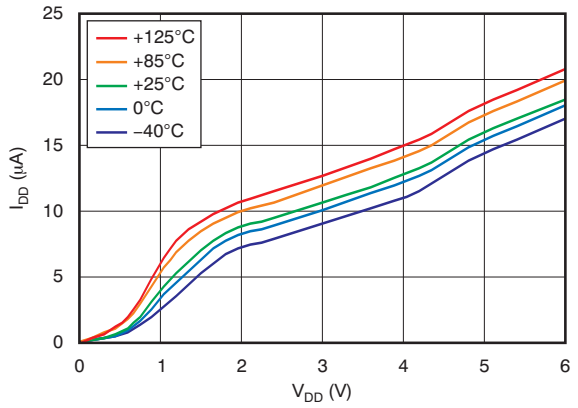


Figure 3. Supply Current vs Supply Voltage

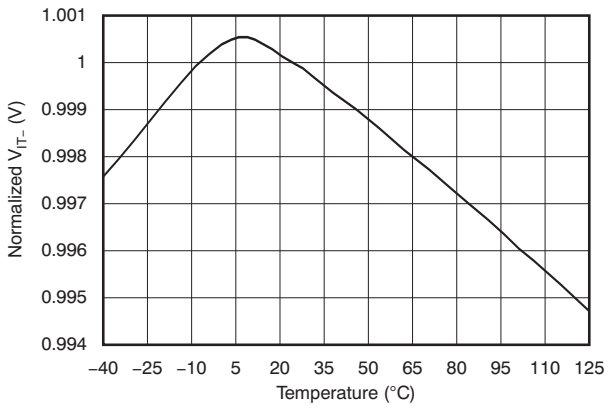


Figure 4. Normalized to 25°C Negative-Going Input Threshold Voltage vs Temperature

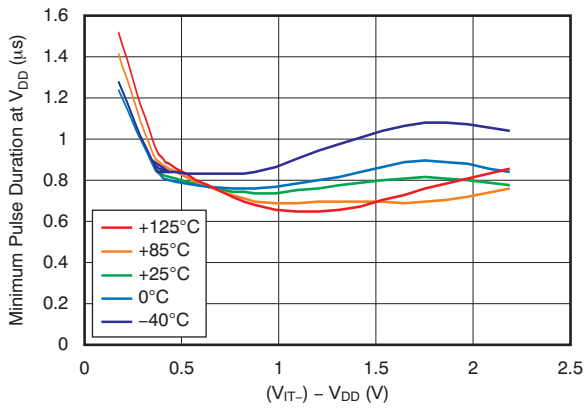


Figure 5. Minimum Pulse Duration At V_{DD} vs Overdrive Voltage

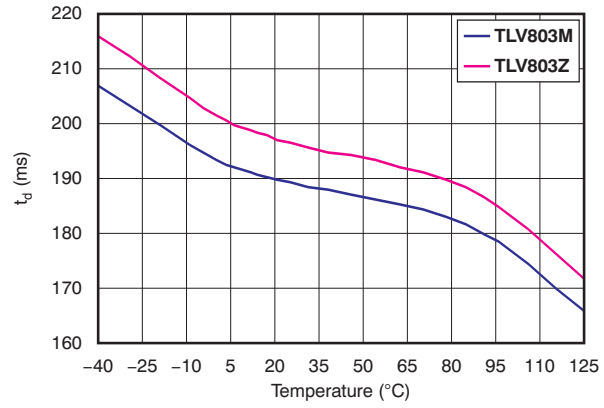


Figure 6. Delay Time vs Temperature

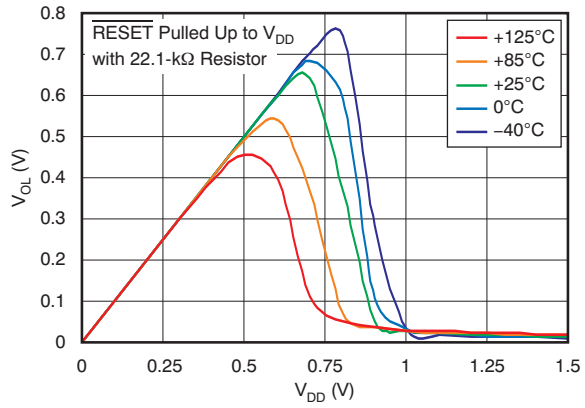


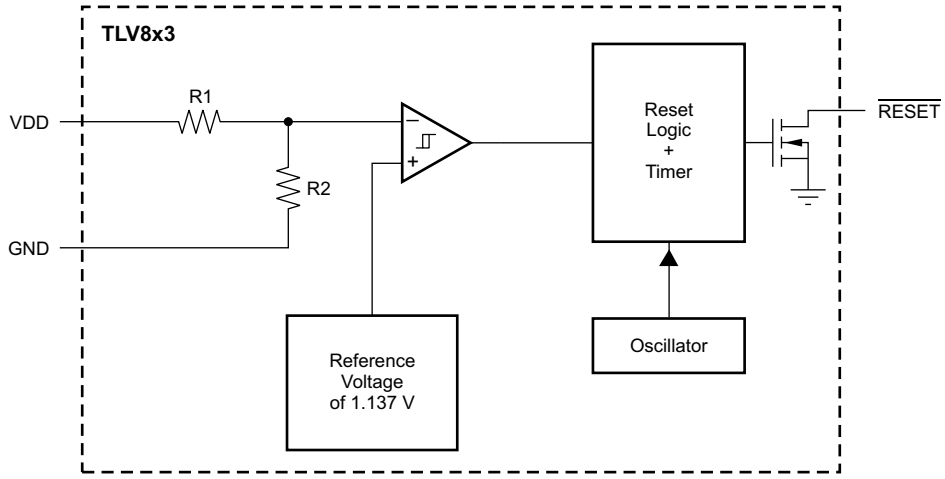
Figure 7. Power-Up Low-Level Output Voltage vs Supply Voltage

8 Detailed Description

8.1 Overview

The TLV803 family of supervisory circuits provides circuit initialization and timing supervision. The TLV853 and TLV863 are both functionally equivalent to the TLV803. These devices output a logic low whenever V_{DD} drops below the negative-going threshold voltage (V_{IT-}). The output, $\overline{\text{RESET}}$, remains low for approximately 200 ms after the V_{DD} voltage exceeds the positive-going threshold voltage ($V_{IT-} + V_{hys}$). These devices are designed to ignore fast transients on the V_{DD} pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 V_{DD} Transient Rejection

The TLV803 has built-in rejection of fast transients on the V_{DD} pin. The rejection of transients depends on both the duration and the amplitude of the transient. The amplitude of the transient is measured from the bottom of the transient to the negative threshold voltage of the TLV803, as shown in Figure 8.

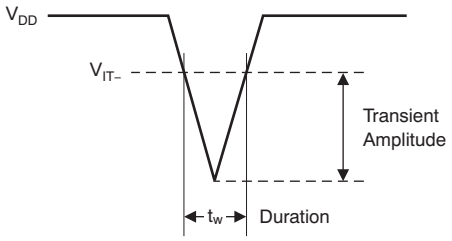


Figure 8. Voltage Transient Measurement

The TLV803 does not respond to transients that are fast duration/low amplitude or long duration/small amplitude. Figure 5 shows the relationship between the transient amplitude and duration needed to trigger a reset. Any combination of duration and amplitude above the curve generates a reset signal.

Feature Description (continued)

8.3.2 Reset During Power Up and Power Down

The TLV803 output is valid when V_{DD} is greater than 1.1 V. When V_{DD} is less than 1.1 V, the output transistor turns off and becomes high impedance. The voltage on the $\overline{\text{RESET}}$ pin rises to the voltage level connected to the pull-up resistor. Figure 9 shows a typical waveform for power-up, assuming the $\overline{\text{RESET}}$ pin has a pull-up resistor connected to the V_{DD} pin.

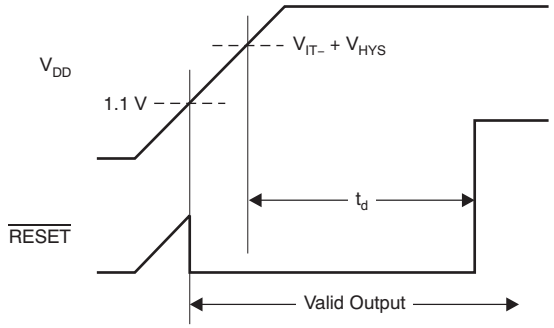


Figure 9. Power-Up Response

8.3.3 Bidirectional Reset Pins

Some microcontrollers have bidirectional reset pins that act as both inputs and outputs. In a situation where the TLV803 is pulling the $\overline{\text{RESET}}$ line low while the microcontroller is trying the force the $\overline{\text{RESET}}$ line high, a series resistor should be placed between the output of the TLV803 and the $\overline{\text{RESET}}$ pin of the microcontroller to protect against excessive current flow. Figure 10 shows the connection of the TLV803 to a microcontroller using a series resistor to drive a bidirectional $\overline{\text{RESET}}$ line.

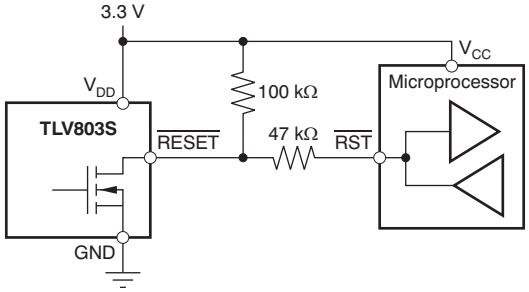


Figure 10. Connection To Bidirectional Reset Pin

8.4 Device Functional Modes

8.4.1 Normal Operation (VDD > Power-Up Reset Voltage)

When the voltage on VDD is greater than 1.1 V, the $\overline{\text{RESET}}$ signal asserts when V_{DD} is less than V_{IT-} and deasserts when V_{DD} is greater thanV_{IT-}.

8.4.2 Power On Reset (VDD < Power-Up Reset Voltage)

When the voltage on VDD is lower than the required voltage to internally pull the asserted output to GND (power-up reset voltage), both outputs are in a high-impedance state.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Monitoring Multiple Supplies

Because the TLV803 has an open-drain output, multiple TLV803 outputs can be directly tied together to form a logical OR-ing function for the $\overline{\text{RESET}}$ line. Only one pull-up resistor is required for this configuration. Figure 11 shows two TLV803s connected together to provide monitoring of a 3.3-V power rail and a 5.0-V power rail. A reset is generated if either power rail falls below the threshold voltage of its corresponding TLV803.

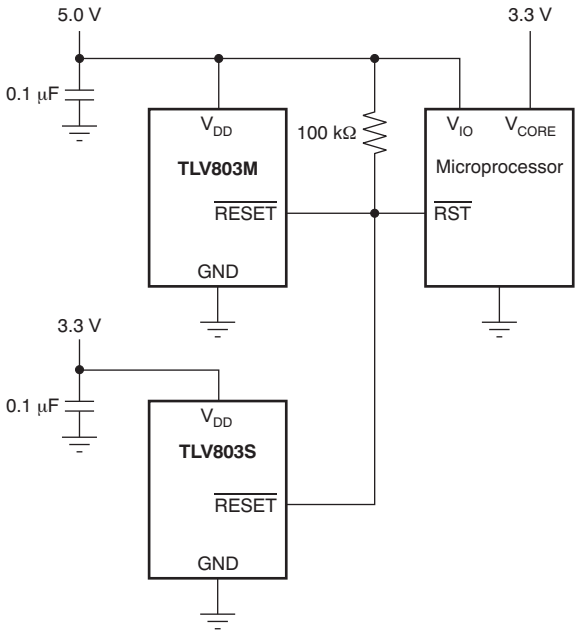


Figure 11. Multiple Voltage Rail Monitoring

9.1.2 Output Level Shifting

The $\overline{\text{RESET}}$ output of the TLV803 can be pulled to a maximum voltage of 6 V and can be pulled higher in voltage than V_{DD}. It is useful to provide level shifting of the output for cases where the monitored voltage is less than the useful logic levels of the load. Figure 12 shows the TLV803Z used to monitor a 2.5-V power rail, with a logic $\overline{\text{RESET}}$ input to a microprocessor that is connected to 5.0 V and has 5.0-V logic levels.

Application Information (continued)

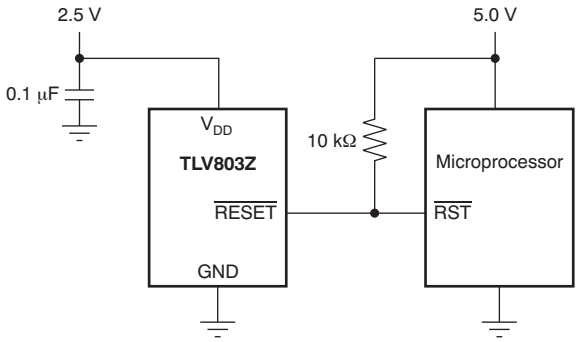


Figure 12. Output Voltage Level Shifting

9.2 Typical Application

Figure 13 shows TLV803S being used to monitor the supply rail for a DSP, FPGA, or ASIC.

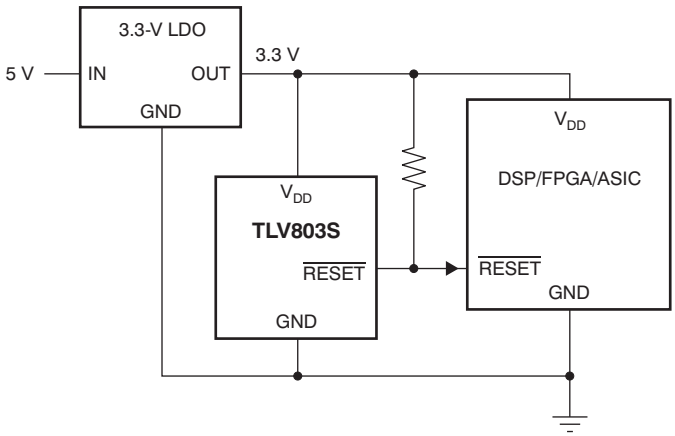


Figure 13. Typical Application

9.2.1 Design Requirements

This design calls for a 3.3-V rail to be monitored. The design resets if the supply rail falls below 2.93 V. The output must satisfy 3.3-V CMOS logic.

9.2.2 Detailed Design Procedure

Select the TLV803S to satisfy the voltage threshold requirement.

Place a pullup resistor on $\overline{\text{RESET}}$ to VDD in order to satisfy the output logic requirement.

Typical Application (continued)

9.2.3 Application Curves

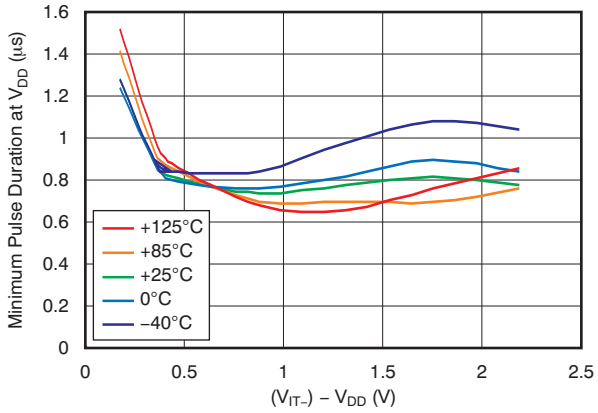


Figure 14. Minimum Pulse Duration At V_{DD} vs Overdrive Threshold Voltage vs Temperature Voltage

10 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 1.1 V and 6 V.

11 Layout

11.1 Layout Guidelines

Place the C_{IN} decoupling capacitor close to the device.

11.2 Layout Example

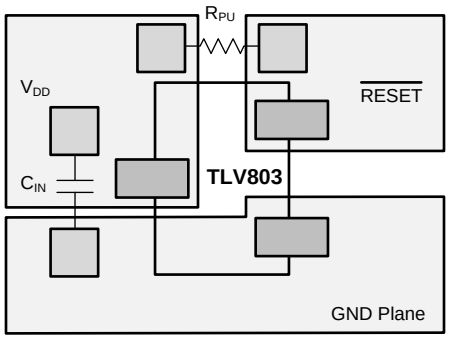


Figure 15. Layout Example (DBZ Package)

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 评估模块

评估模块 (EVM) 可与 TLV803 配套使用，帮助评估初始电路性能。TLV803SEVM-019 评估模块（和相关用户指南）可在德州仪器 (TI) 网站上的产品文件夹中获取，也可直接从 TI 网上商店购买。

12.1.1.2 Spice 模型

分析模拟电路和系统的性能时，使用 SPICE 模型对电路性能进行计算机仿真非常有用。您可以从相应产品文件夹中的*工具和软件*下获取 TLV803、TLV853 和 TLV863 的 SPICE 模型。

12.2 文档支持

12.2.1 相关文档

- 《TLV803SEVM-019 用户指南》。文献编号：SLVU461。

12.3 相关链接

表 3 列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，以及样片与购买的快速访问。

表 3. 相关链接

部件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TLV803	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV853	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV863	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商标

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12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
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数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
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微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV803MDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOUQ	Samples
TLV803MDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOUQ	Samples
TLV803RDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOSQ	Samples
TLV803RDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOSQ	Samples
TLV803SDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOTQ	Samples
TLV803SDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VOTQ	Samples
TLV803ZDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VORQ	Samples
TLV803ZDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VORQ	Samples
TLV853MDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZGM4	Samples
TLV853MDBZT	ACTIVE	SOT-23	DBZ	3	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZGM4	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

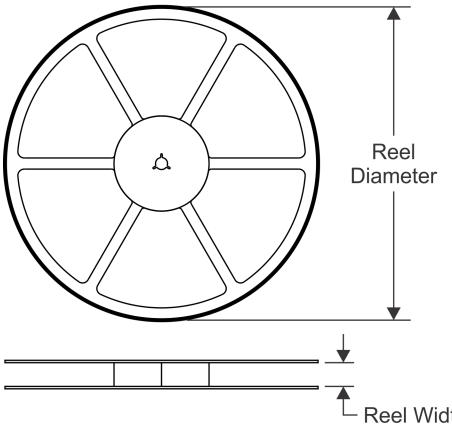
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

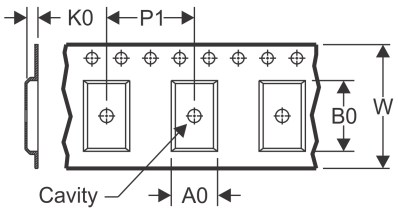
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

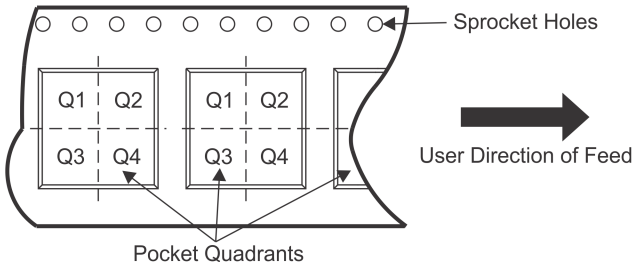


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

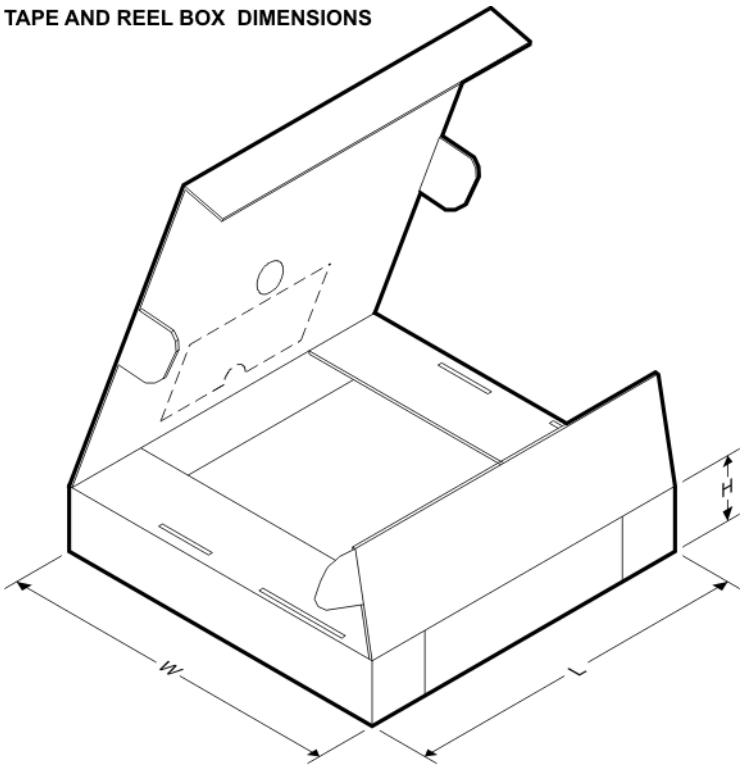
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV803MDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV803MDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV803RDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV803RDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV803SDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV803SDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV803ZDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV803ZDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV853MDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TLV853MDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



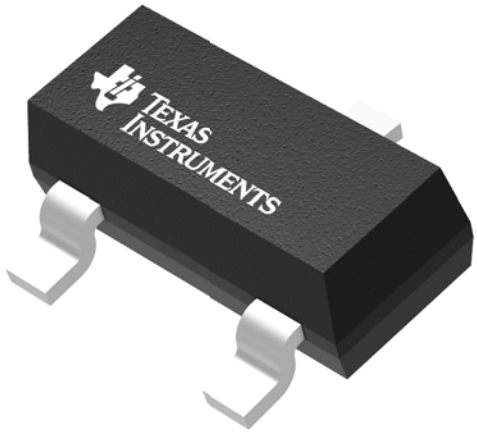
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV803MDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV803MDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
TLV803RDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV803RDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
TLV803SDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV803SDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
TLV803ZDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV803ZDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0
TLV853MDBZR	SOT-23	DBZ	3	3000	203.0	203.0	35.0
TLV853MDBZT	SOT-23	DBZ	3	250	203.0	203.0	35.0

GENERIC PACKAGE VIEW

DBZ 3 SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



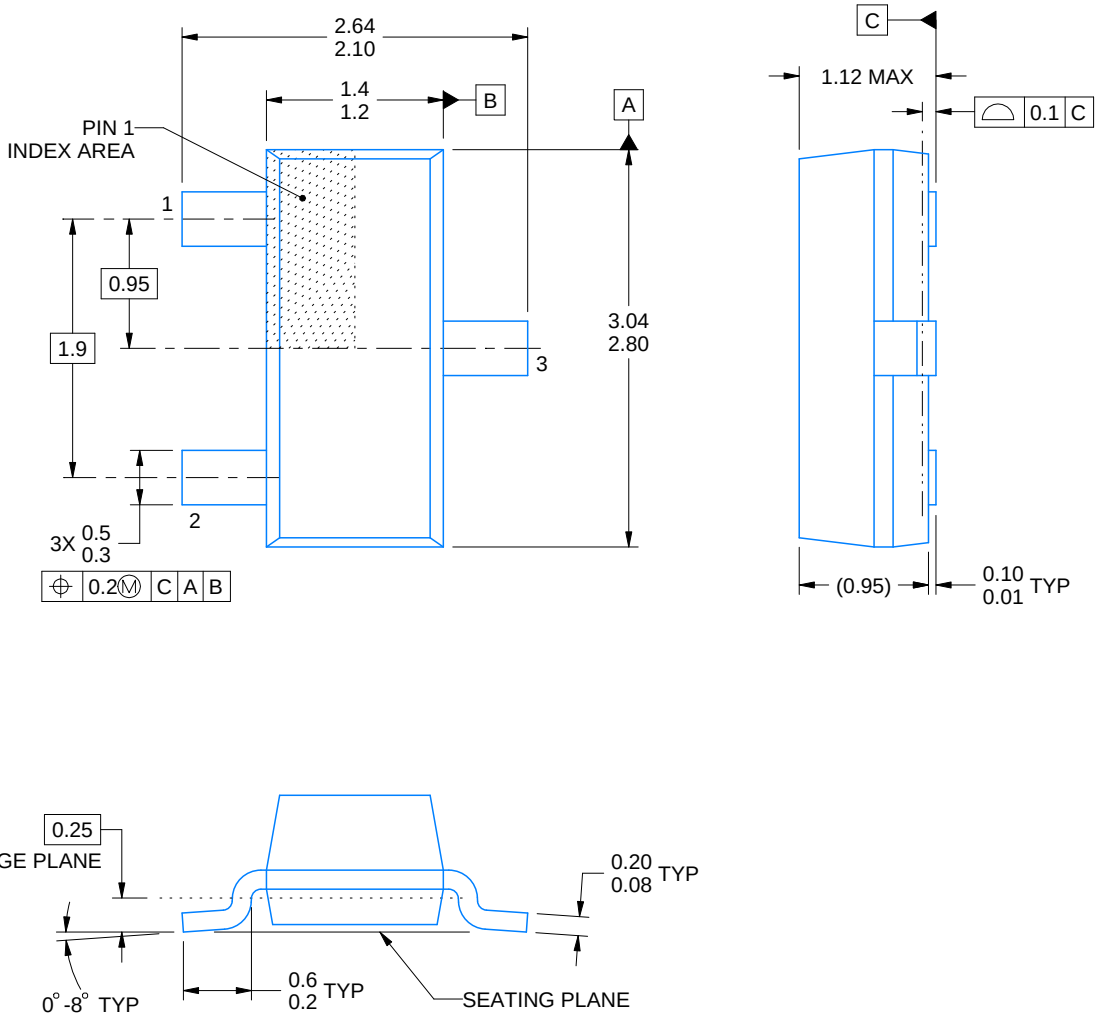
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

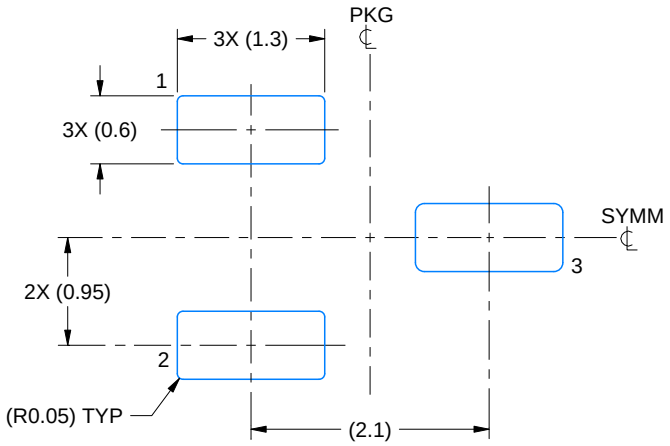
SMALL OUTLINE TRANSISTOR



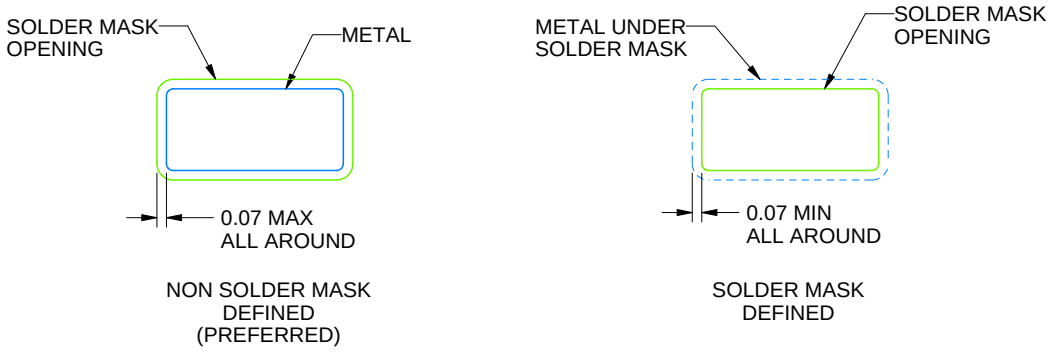
4214838/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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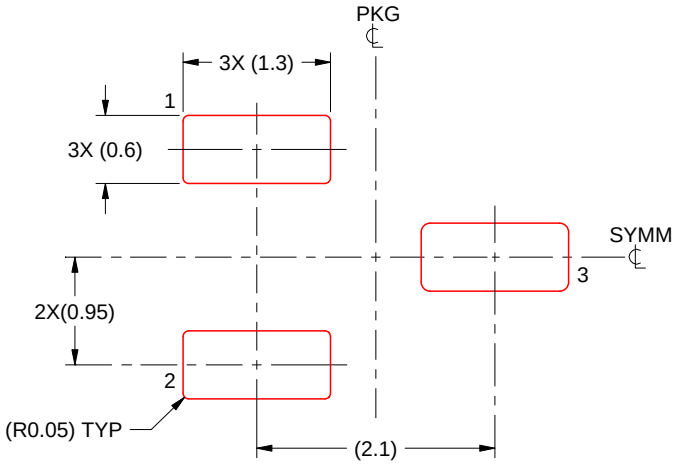
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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