TUSB319-Q1 USB Type-C DFP Port Controller

1 Features

- Meets USB Type-C™ Specifications
- Supports DFP (Host/Source) Applications with up to 15W Power
- Supports Type-C Current Mode Advertisement up to 3 A (Default, 1.5 A, 3 A)
- Provides Type-C Plug Orientation
- Channel Configuration (CC)
  - Attach of USB Port Detection
  - Cable Orientation Detection
- V_{BUS} Detection
- Supply Voltage: 3.8 V to 5.5 V
- Low Current Consumption
- 2 x 2 mm WSON Package with 0.5 mm Pitch
- Industrial Temperature Range of –40°C to 85°C

2 Applications

- Wall-charger
- Automotive Car Charger, USB Port
- DFP Port for Desktop, Notebooks, All-in-One

3 Description

The TUSB319-Q1 is a USB Type-C Downstream Facing Port (DFP) controller. The TUSB319-Q1 monitors the USB Type-C Configuration Channel (CC) lines to determine when an USB device is attached. If an Upstream Facing Port (UFP) device is attached, the TUSB319-Q1 drives an open drain output ID that can be used in the system to apply VBUS power. The device also communicates the selectable VBUS current sourcing capability to the UFP via the CC lines.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB319-Q1	WSON (8)	2.00 mm x 2.00 mm 0.5 mm pitch

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

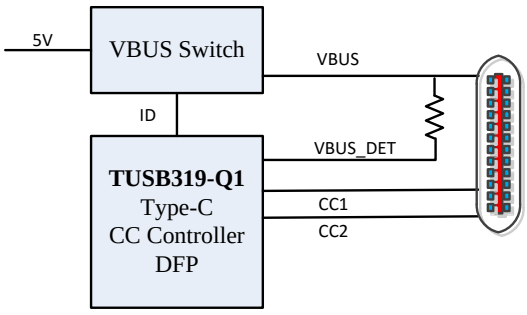


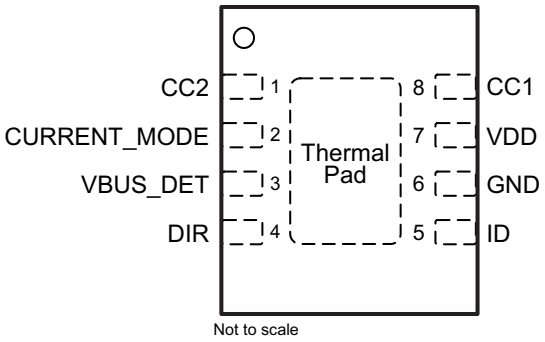
Table of Contents

4 Revision History

DATE	REVISION	NOTES
February 2017	*	Initial release.

5 Pin Configuration and Functions

DRF Package
8-Pin WSON
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CC2 (1)	1	I/O	Type-C configuration channel signal 2
CURRENT_MODE	2	I	Advertise VBUS current. This 3-level input is used to control Type-C current advertisement. The pin can be dynamically set. L - Default Current is 500 mA for USB 2.0 and 900 mA for USB 3.1. Pull-down to GND or leave unconnected. M - Medium current is 1.5 A. Pull-up to TUSB319-Q1 V_{DD} with 500-kΩ resistor. H - High current is 3 A. Pull-up to TUSB319-Q1 V_{DD} with 10-kΩ resistor.
VBUS_DET	3	I	5-V to 28-V system V_{BUS} input voltage. One 900-kΩ external resistor required between system V_{BUS} and VBUS_DET pin.
DIR	4	O	Type-C plug orientation. This open drain output indicates the detected plug orientation: Type-C plug position 2 (H); Type-C plug position 1 (L).
ID (1)	5	O	Open drain output; asserted low when the CC pins detect device attachment.
GND	6	G	Ground
VDD	7	P	3.8-V to 5-V power
CC1 (1)	8	I/O	Type-C configuration channel signal 1

(1) CC1, CC2 and ID pins are failsafe with leakage current defined in the *Electrical Characteristics*.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{DD}	–0.3	6	V
Control pins	CC1, CC2, CURRENT_MODE, ID, DIR	–0.3	6	V
	VBUS_DET	–0.3	4	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±3000	V
		Charged-device model (CDM), per AEC Q100-0111	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage range	3.8		5.5	V
$V_{DD(transient)}$	Transient voltage (with maximum width of 5 ms)	3.5		6	V
$V_{DD(ramp)}$	V_{DD} ramp time			40	mS
V_{BUS}	System V_{BUS} voltage	0	5	28	V
VBUS_DET	VBUS_DET threshold voltage on the pin			3.8	V
T_A	Operating free air temperature range	–40	25	85	°C
T_J	Junction temperature	–40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		TUSB319-Q1 DRF (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bot) thermal resistance	43.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and C Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device average power consumption		Active		105	140	µA
		Unattached		105	140	µA
CC1 and CC2 Pins						
$I_{CC(DEFAULT\_P)}$	Default mode pullup current source.		64	80	96	µA
$I_{CC(MED\_P)}$	Medium (1.5 A) mode pullup current source.		166	180	194	µA
$I_{CC(HIGH\_P)}$	High (3 A) mode pullup current source.		304	330	356	µA
$I_{(FS,CC)}$	Fail safe current (CC1, CC2)	VDD = 0 V, CC1, CC2 = 5 V			1	µA
Control Pins: CURRENT_MODE, DIR, ID						
V_{IL}	Low-level control signal input voltage, (CURRENT_MODE)				0.4	V
V_{IM}	Mid-level control signal input voltage (CURRENT_MODE)		0.28 × V_{DD}		0.56 × V_{DD}	V
V_{IH}	High-level control signal input voltage (CURRENT_MODE)		V_{DD} - 0.3			V
I_{IH}	High-level input current		–1		1	µA
I_{IL}	Low-level input current		–1		1	µA
$I_{(FS,ID)}$	Fail safe current (ID)	VDD = 0 V, ID = 5 V			1	µA
$R_{PD(CUR)}$	Internal pulldown resistance for CURRENT_MODE pin			275		kΩ
V_{OL}	Low-level signal output voltage (open-drain) (ID and DIR)	I_{OL} = –1.6 mA			0.4	V
$R_{p(ODext)}$	External pullup resistor on open drain IOs (ID and DIR)			200		kΩ
$R_{p(cm\_med)}$	External pull-up resistor on CURRENT_MODE pin to advertise 1.5-A current			500		kΩ
$R_{p(cm\_high)}$	External pull-up resistor on CURRENT_MODE pin to advertise 3-A current			10		kΩ
VBUS_DET IO Pins (Connected to System V_{BUS} signal through external resistor)						
$V_{BUS(THR)}$	V_{BUS} threshold range		2.4	3.3	4.2	V
$V_{BUS\_DET(THR)}$	V_{BUS_DET} pin threshold		236	315	394	mV
R_{VBUS}	External resistor between V_{BUS} and VBUS_DET pin		850	900(1)	910	KΩ
$R_{VBUS(PD)}$	Internal pulldown resistance for VBUS_DET			95		KΩ

(1) If smaller R_{VBUS} is desired add an additional resistor from VBUS_DET pin to GND in parallel to internal 95K resistor keeping the same ratio of pull-up and pull-down resistors.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{CCCB\_DEFAULT}$	Port attachment debounce time		168		ms
t_{VBUS_DB}	Debounce of VBUS_DET pin after valid V_{BUS_THR} (See Figure 1.)		2		ms

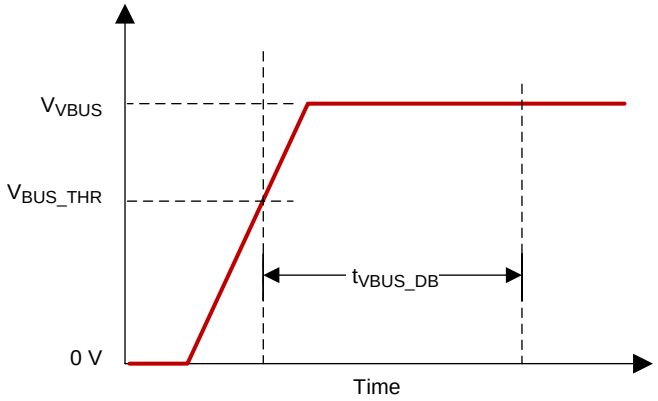


Figure 1. VBUS Detect and Debounce

7 Detailed Description

7.1 Overview

The USB Type-C ecosystem operates around a small form factor connector and cable that is flippable and reversible. Because of the nature of the connector, a scheme is needed to determine the connector orientation. Additional schemes are needed to determine when a USB port is attached and the acting role of the USB port (DFP, UFP), as well as to communicate Type-C current capabilities. These schemes are implemented over the CC pins according to the USB Type-C specifications. The TUSB319-Q1 device provides Configuration Channel (CC) logic for determining USB port attach and detach, cable orientation, and Type-C current mode for DFP applications.

7.1.1 Cables, Adapters, and Direct Connect Devices

Type-C Specifications defines several cables, plugs and receptacles to be used to attach ports. The TUSB319-Q1 device supports all cables, receptacles, and plugs. The device does not support e-marking.

7.1.1.1 USB Type-C Receptacles and Plugs

Below is list of Type-C receptacles and plugs supported by the device:

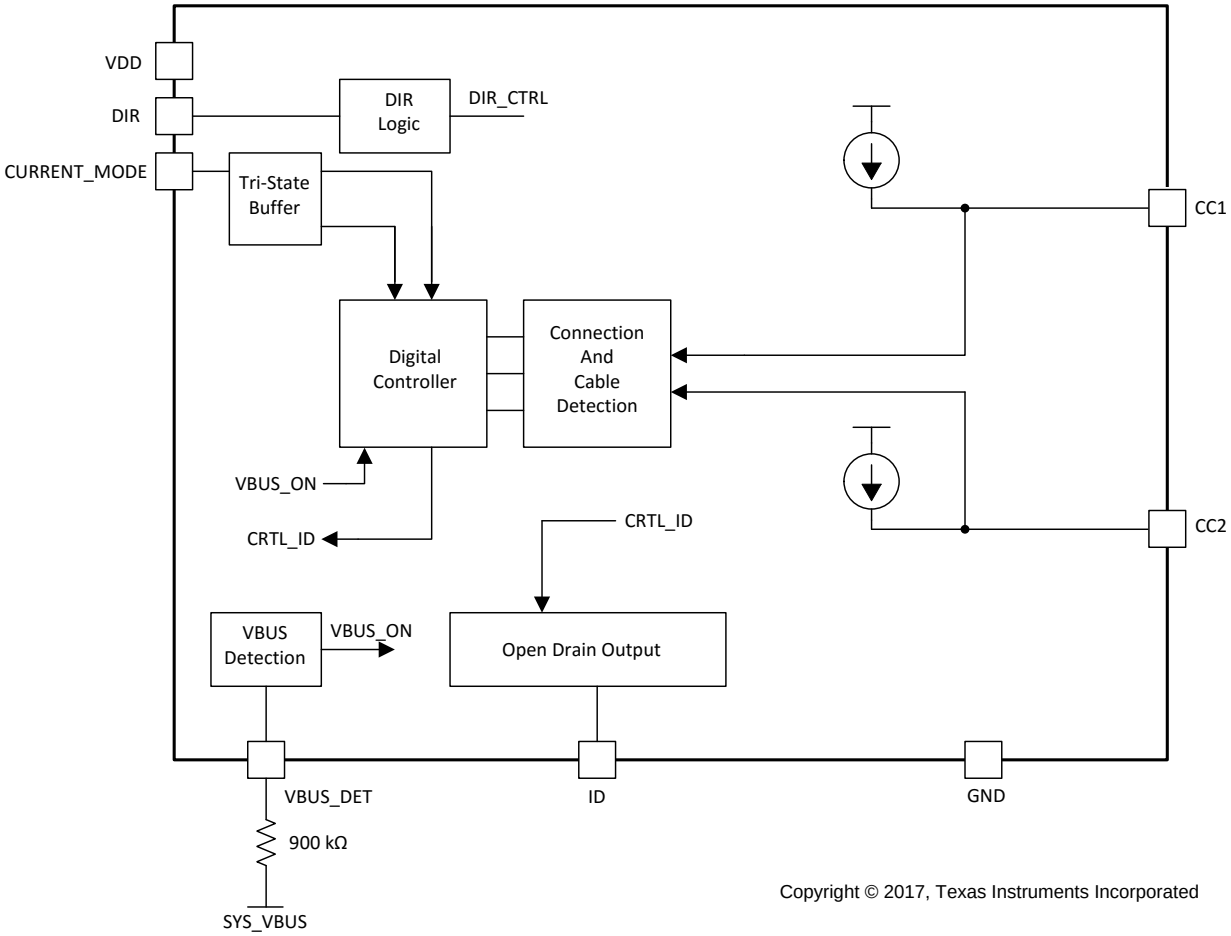
- USB Type-C receptacle for USB2.0 and USB3.1 and full-featured platforms and devices
- USB full-featured Type-C plug
- USB2.0 Type-C plug

7.1.1.2 USB Type-C Cables

Below is a list of Type-C cables types supported by the device:

- USB full-featured Type-C cable with USB3.1 full-featured plug
- USB2.0 Type-C cable with USB2.0 plug
- Captive cable with either a USB full-featured plug or USB2.0 plug

7.2 Functional Block Diagram



7.3 Feature Description

Table 1. Supported Features for the TUSB319-Q1 Device by Mode

SUPPORTED FEATURES	DFP
Port attach and detach	Yes
Cable orientation	Yes
Current advertisement	Yes
Legacy cables	Yes

7.3.1 Downstream Facing Port (DFP) - Source

The TUSB319-Q1 is a DFP device; it presents the appropriate Rp resistors on both CC pins, based on the state of the CURRENT_MODE pin to advertise the desired current level (USB-standard, 1.5 A and 3 A).

The TUSB319-Q1 can operate with older USB Type-C 1.0 devices except for a USB Type-C 1.0 DRP device. This limitation is a result of backwards compatibility problem between USB Type-C 1.1 DFP and a USB Type-C 1.0 DRP.

7.3.2 Type-C Current Mode

The TUSB319-Q1 device supports both advertising Type-C current by means of the CURRENT_MODE pin, which allows the CC controller to advertise 500 mA (for USB2.0) or 900 mA (for USB3.1) if CURRENT_MODE pin is left unconnected or pulled to GND. If a higher level of current is required, the CURRENT_MODE can be pulled up to VDD through a 500-kΩ resistor to advertise medium current at 1.5 A or pulled up to V_{DD} through a 10-kΩ resistor to advertise high current at 3 A. Table 2 lists the Type-C current advertisements and detection.

Table 2. Type-C Current Advertisement and Detection

TYPE-C CURRENT		CURRENT ADVERTISEMENT
Default	500 mA (USB2.0) 900 mA (USB3.1)	CURRENT_MODE = L
Medium - 1.5 A		CURRENT_MODE = M
High - 3 A		CURRENT_MODE = H

7.3.3 V_{BUS} Detection

The TUSB319-Q1 device supports VBUS detection according to the Type-C Specification. The system VBUS voltage must be routed through a 900-kΩ resistor to the VBUS_DET pin on the TUSB319-Q1. When voltage on VBUS_DET pin is below the $V_{BUS(THR)}$ and R_d is detected on either CC1 or CC2, the TUSB319 assumes system V_{BUS} is at vSafe0V (V_{BUS} < 800 mV) and will assert ID low.

If VBUS_DET pin is left unconnected system needs to ensure that the VBUS level is below vSafe0V before VBUS is enabled.

7.3.4 Cable Orientation

The TUSB319-Q1 detects the cable orientation by monitoring the voltage on the CC pins. When a voltage level within the proper threshold is detected on CC1, the DIR pin is pulled low. When a voltage level within the proper threshold is detected on CC2, the DIR is pulled high. The DIR pin is an open drain output.

7.4 Device Functional Modes

The TUSB319-Q1 device has two functional modes. Table 3 lists these modes:

Table 3. USB Type-C States According to TUSB319-Q1 Functional Modes

MODES	GENERAL BEHAVIOR	STATES(1)
Unattached	USB port unattached.	Unattached.SRC
		AttachWait.SRC
Active	USB port attached.	Attached.SRC

(1) Required; not in sequential order.

7.4.1 Unattached Mode

Unattached mode is the primary mode of operation for the TUSB319-Q1 device, because a USB port can be unattached for a lengthy period of time. In unattached mode, all IOs are operational. After the TUSB319-Q1 device is powered up, the part enters unattached mode until a successful attach has been determined.

7.4.2 Active Mode

Active mode is defined as the port being attached. When in active mode, the TUSB319-Q1 device communicates to the system that the USB port is attached. This happens through the ID pin. The TUSB319-Q1 device exits active mode when the cable is unplugged.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TUSB319-Q1 device is a Type-C configuration channel logic and port controller. The TUSB319-Q1 device can detect when a Type-C device is attached, what type of device is attached, the orientation of the cable, and power capabilities, this power capabilities are sourcing only since the TUSB319-Q1 device can be used in a source application (DFP) only.

8.2 Typical Application

8.2.1 DFP Mode

Figure 2 shows the TUSB319-Q1 on a DFP port with USB3 functionality.

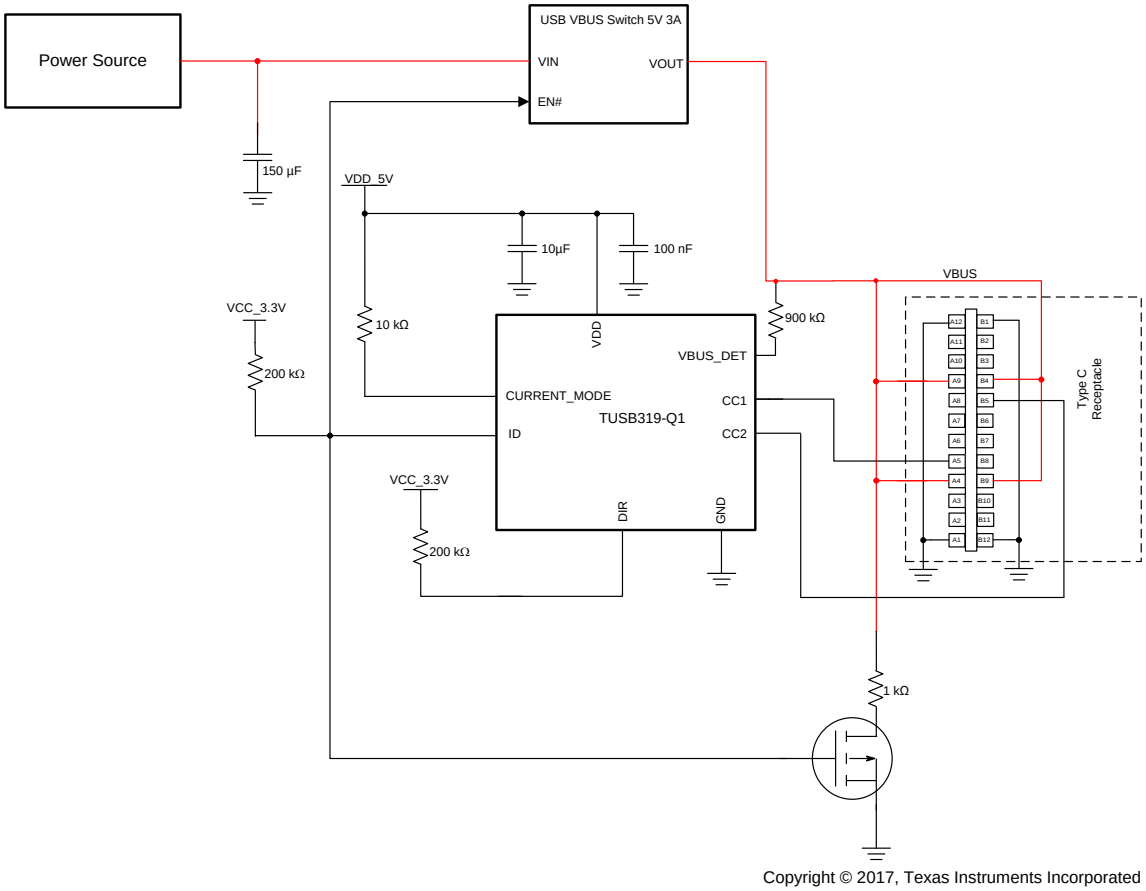


Figure 2. DFP Mode Schematic

Typical Application (continued)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 4:

Table 4. Design Requirements for DFP Mode

DESIGN PARAMETER	VALUE
V_{DD} (3.8 V to 5.5 V)	5 V
Advertised Type-C Current (Default, 1.5 A, 3 A)	3 A

8.2.1.2 Detailed Design Procedure

The TUSB319-Q1 device supports a V_{DD} in the range of 3.8 V to 5.5 V. In this particular case, V_{DD} is set to 5 V. A 100-nF capacitor is placed near V_{DD}.

The TUSB319-Q1 current advertisement is determined by the state of the CURRENT_MODE pin. In this particular example, 3 A advertisement is desired so the CURRENT_MODE pin is pulled high to V_{DD} through 10-kΩ resistor.

The VBUS_DET pin must be connected through a 900-kΩ resistor to V_{BUS} on the Type-C that is connected. This large resistor is required to protect the TUSB319-Q1 device from large V_{BUS} voltage that is possible in present day systems. This resistor along with internal pulldown keeps the voltage observed by the TUSB319-Q1 device in the recommended range.

The USB2 specification requires the bulk capacitance on V_{BUS} of at least 120 µF. In this particular case, a 150-µF capacitor was chosen.

TUSB319-Q1 does not provide VBUS discharge and requires an external solution either through switched resistor pull-down as shown in Figure 2 or elsewhere in the system.

8.2.1.3 Application Curve

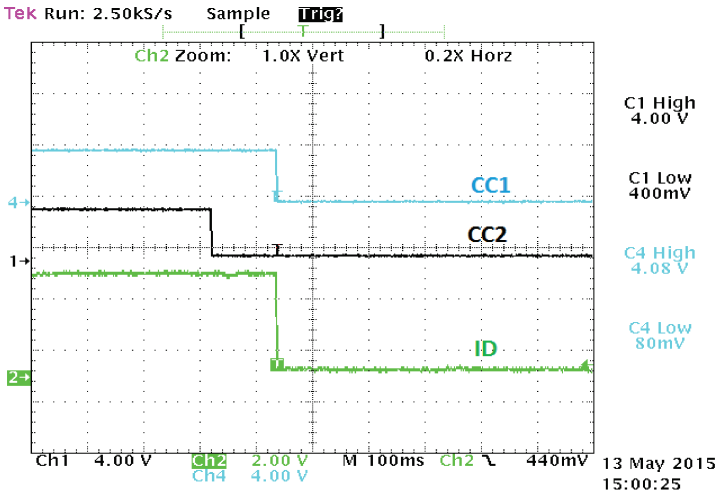


Figure 3. CC Detection

8.3 Initialization Set Up

The general power-up sequence for the TUSB319-Q1 device is as follows:

1. System is powered off (device has no VDD).
2. V_{DD} ramps – POR circuit.
3. The TUSB319-Q1 device enters unattached mode.
4. The TUSB319-Q1 device monitors the CC pins.
5. The TUSB319-Q1 device enters active mode when attach has been successfully detected.

9 Power Supply Recommendations

The TUSB319-Q1 device has a wide power supply range from 3.8 V to 5.5 V.

10 Layout

10.1 Layout Guidelines

1. An extra trace (or stub) is created when connecting between more than two points. A trace connecting pin A6 to pin B6 will create a stub because the trace also has to go to the USB Host. Ensure that:
   – A stub created by short on pin A6 (DP) and pin B6 (DP) at Type-C receptacle does not exceed 3.5 mm.
   – A stub created by short on pin A7 (DM) and pin B7 (DM) at Type-C receptacle does not exceed 3.5 mm.
2. A 100-nF capacitor should be placed as close as possible to the VDD pin.

10.2 Layout Example

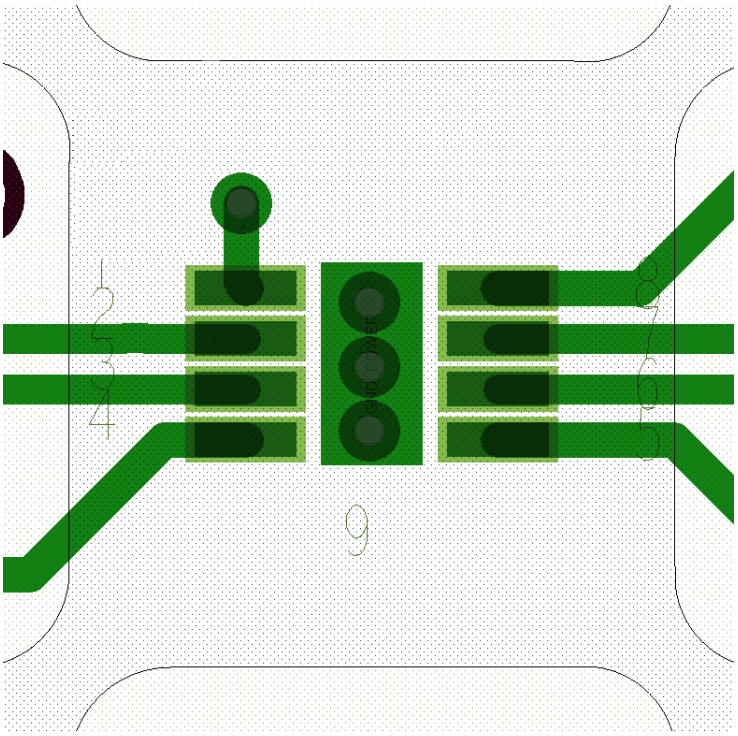


Figure 4. Example Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB319IDRFRQ1	ACTIVE	WSON	DRF	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	T319	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

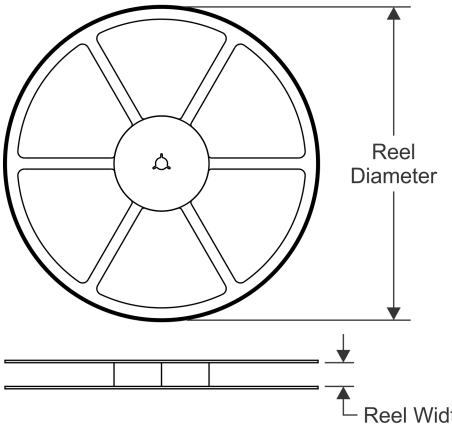
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

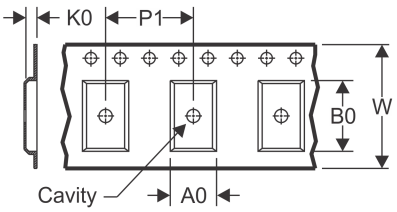
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

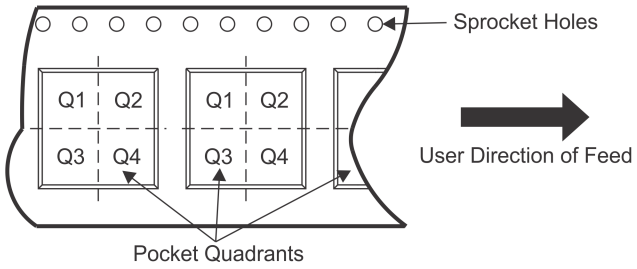


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

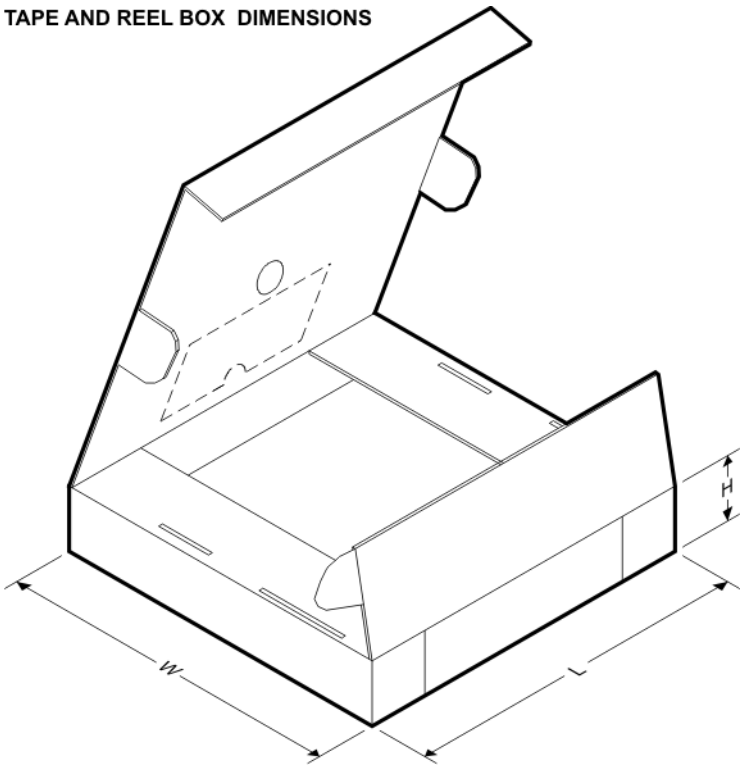
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB319IDRFRQ1	WSON	DRF	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

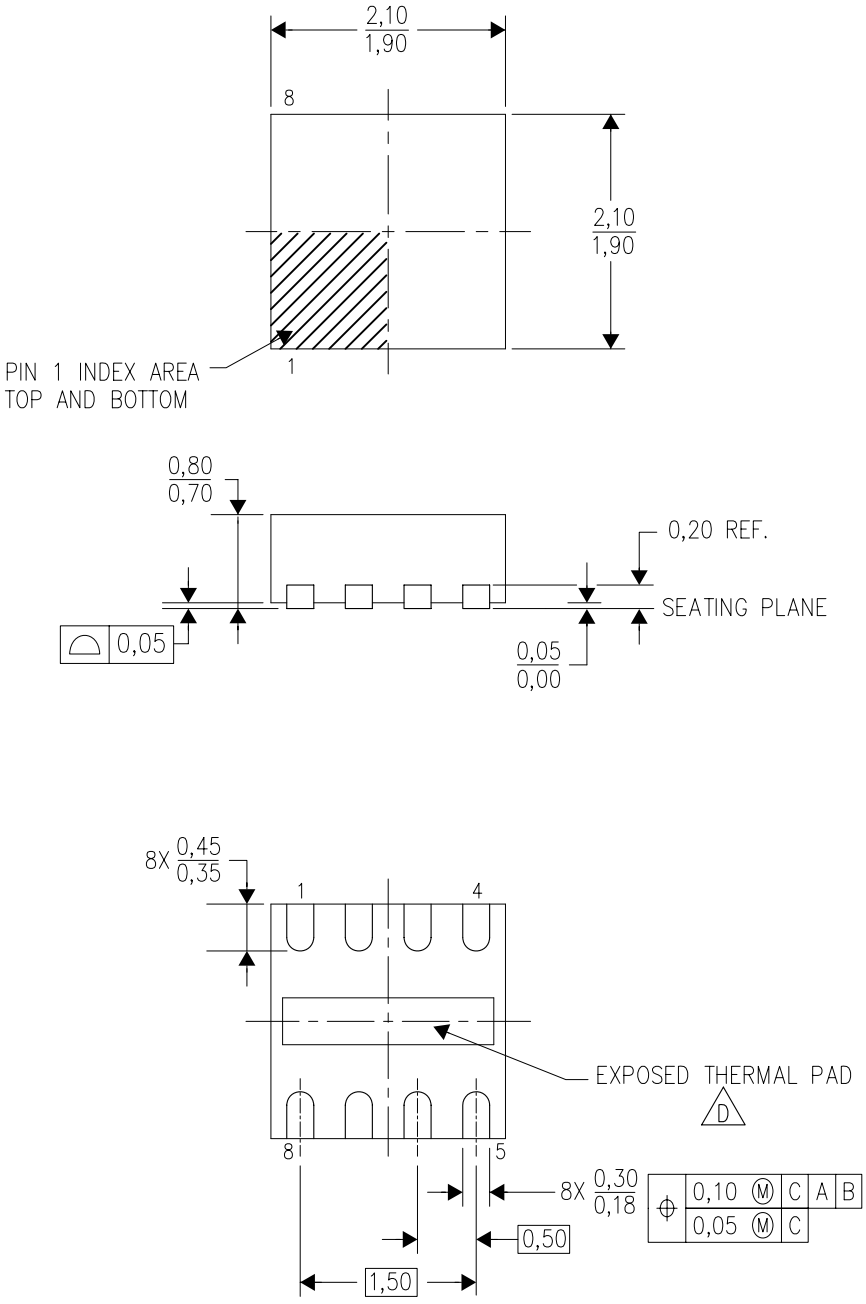
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB319IDRFRQ1	WSON	DRF	8	3000	210.0	185.0	35.0

DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4205287/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

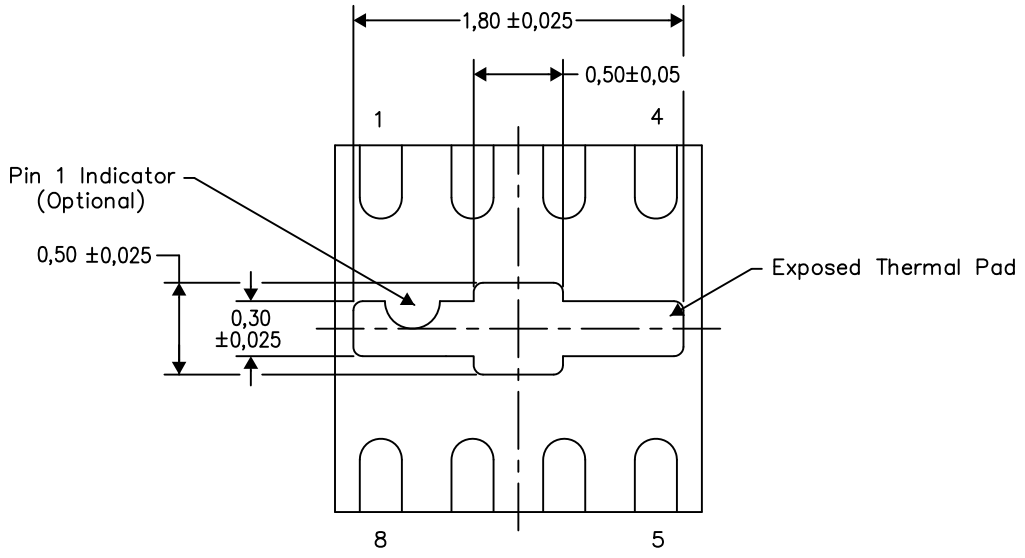
DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



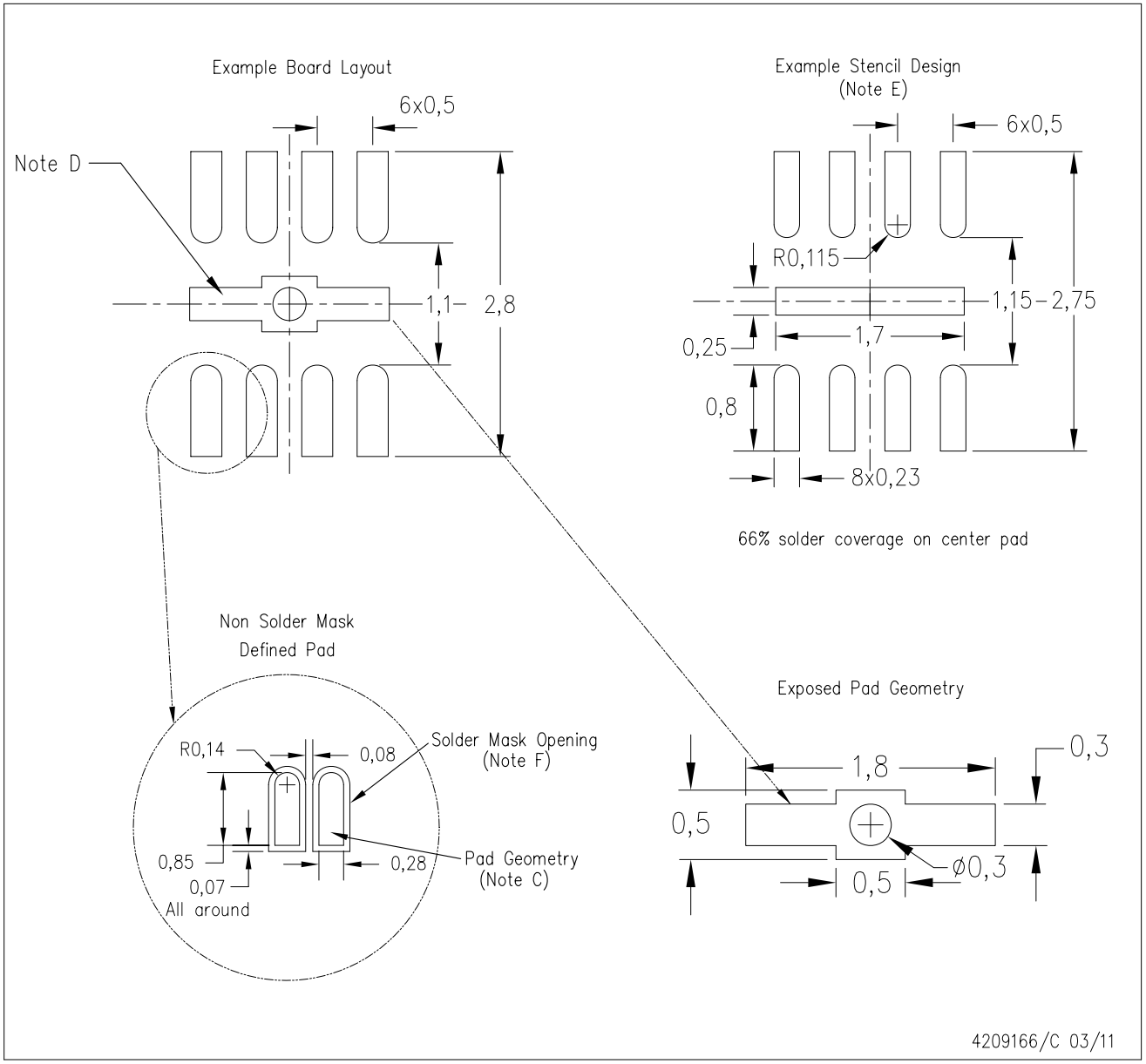
Bottom View

Exposed Thermal Pad Dimensions

4206840/H 12/14

NOTE: A. All linear dimensions are in millimeters

DRF (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265