

## SN74AUP1G04 Low-Power Single Inverter Gate

### 1 Features

- Available in the Ultra Small 0.64 mm<sup>2</sup> Package (DPW) with 0.5-mm Pitch
- Low Static-Power Consumption ( $I_{CC} = 0.9 \mu\text{A Max}$ )
- Low Dynamic-Power Consumption ( $C_{pd} = 4.1 \text{ pF Typ at } 3.3 \text{ V}$ )
- Low Input Capacitance ( $C_i = 1.5 \text{ pF Typ}$ )
- Low Noise – Overshoot and Undershoot <math><10\% \text{ of } V\_{CC}</math>
- $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input ( $V_{hys} = 250 \text{ mV Typ at } 3.3 \text{ V}$ )
- Wide Operating  $V_{CC}$  Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 3.9 \text{ ns Max at } 3.3 \text{ V}$
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- ATCA Solutions
- Active Noise Cancellation (ANC)
- Barcode Scanner
- Blood Pressure Monitor
- CPAP Machine
- Cable Solutions
- DLP 3D Machine Vision, Hyperspectral Imaging, Optical Networking, and Spectroscopy
- E-Book
- Embedded PC
- Field Transmitter: Temperature or Pressure Sensor
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- Network-Attached Storage (NAS)
- Server Motherboard and PSU
- Software Defined Radio (SDR)
- TV: High-Definition (HDTV), LCD, and Digital
- Video Communications System
- Wireless Data Access Card, Headset, Keyboard, Mouse, and LAN Card
- X-ray: Baggage Scanner, Medical, and Dental

### 3 Description

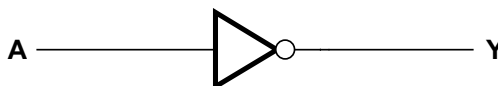
The SN74AUP1G04 device is a single inverter gate performs the Boolean function  $Y = A$ .

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUP1G04	SOT-23 (5)	2.90 mm × 1.60 mm
	SOT (5)	2.00 mm × 1.25 mm
	SOT (5)	1.60 mm × 1.20 mm
	USON (6)	1.45 mm × 1.00 mm
	X2SON (4)	0.80 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Simplified Schematic



## Table of Contents

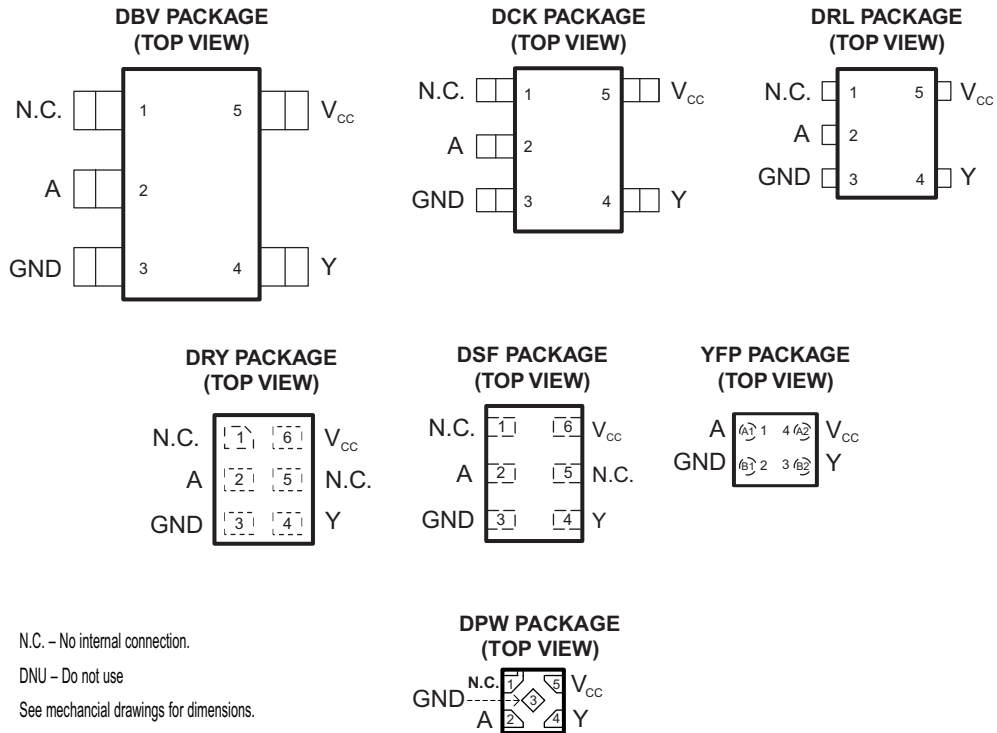
<b>1 Features</b> .....	<b>1</b>	Pulse Width .....	<b>9</b>
<b>2 Applications</b> .....	<b>1</b>	8.2 Enable and Disable Times .....	<b>10</b>
<b>3 Description</b> .....	<b>1</b>	<b>9 Detailed Description</b> .....	<b>11</b>
<b>4 Simplified Schematic</b> .....	<b>1</b>	9.1 Overview .....	<b>11</b>
<b>5 Revision History</b> .....	<b>2</b>	9.2 Functional Block Diagram .....	<b>11</b>
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	9.3 Feature Description .....	<b>11</b>
<b>7 Specifications</b> .....	<b>4</b>	9.4 Device Functional Modes .....	<b>11</b>
7.1 Absolute Maximum Ratings .....	<b>4</b>	<b>10 Application and Implementation</b> .....	<b>12</b>
7.2 Handling Ratings .....	<b>4</b>	10.1 Application Information .....	<b>12</b>
7.3 Recommended Operating Conditions .....	<b>5</b>	10.2 Typical Application .....	<b>12</b>
7.4 Thermal Information .....	<b>5</b>	<b>11 Power Supply Recommendations</b> .....	<b>14</b>
7.5 Electrical Characteristics .....	<b>6</b>	<b>12 Layout</b> .....	<b>14</b>
7.6 Switching Characteristics, $C_L = 5$ pF .....	<b>6</b>	12.1 Layout Guidelines .....	<b>14</b>
7.7 Switching Characteristics, $C_L = 10$ pF .....	<b>7</b>	12.2 Layout Example .....	<b>14</b>
7.8 Switching Characteristics, $C_L = 15$ pF .....	<b>7</b>	<b>13 Device and Documentation Support</b> .....	<b>15</b>
7.9 Switching Characteristics, $C_L = 30$ pF .....	<b>7</b>	13.1 Trademarks .....	<b>15</b>
7.10 Operating Characteristics .....	<b>7</b>	13.2 Electrostatic Discharge Caution .....	<b>15</b>
7.11 Typical Characteristics .....	<b>8</b>	13.3 Glossary .....	<b>15</b>
<b>8 Parameter Measurement Information</b> .....	<b>9</b>	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>15</b>
8.1 Propagation Delays, Setup and Hold Times, and			

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision J (May 2014) to Revision K</b>	<b>Page</b>
• Updated document to new TI data sheet format .....	<b>1</b>
• Updated $I_{off}$ in Features. ....	<b>1</b>
• Added Applications .....	<b>1</b>
• Added Handling Ratings table .....	<b>4</b>
• Added Thermal Information table .....	<b>5</b>
• Added Typical Characteristics .....	<b>8</b>

## 6 Pin Configuration and Functions



### Pin Functions

NAME	PIN				I/O	DESCRIPTION
	DBV, DCK, DRL	DSF, DRY	YFP	DPW		
NC	1	1, 5	—	1	—	No Connection
A	2	2	A1	2	I	Input A
GND	3	3	B1	3	—	Ground Pin
Y	4	4	B2	4	O	Output Y
VCC	5	6	A2	5	—	Power Pin

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	4.6	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	4.6	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	4.6	V
V <sub>O</sub>	Output voltage range in the high or low state <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50 mA
I <sub>O</sub>	Continuous output current			±20 mA
	Continuous current through V <sub>CC</sub> or GND			±50 mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 7.2 Handling Ratings

		MIN	MAX	UNIT
T <sub>stg</sub>	Storage temperature range	-65	150	°C
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>		V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>		

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	0.8	3.6	V	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub>	V	
		V <sub>CC</sub> = 1.1 V to 1.95 V	0.65 × V <sub>CC</sub>		
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.6		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 0.8 V	0	V	
		V <sub>CC</sub> = 1.1 V to 1.95 V	0.35 × V <sub>CC</sub>		
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	0.9		
V <sub>I</sub>	Input voltage	0	3.6	V	
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 0.8 V	–20	μA	
		V <sub>CC</sub> = 1.1 V	–1.1		
		V <sub>CC</sub> = 1.4 V	–1.7		
		V <sub>CC</sub> = 1.65 V	–1.9		
		V <sub>CC</sub> = 2.3 V	–3.1		
		V <sub>CC</sub> = 3 V	–4		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 0.8 V	20	μA	
		V <sub>CC</sub> = 1.1 V	1.1		
		V <sub>CC</sub> = 1.4 V	1.7		
		V <sub>CC</sub> = 1.65 V	1.9		
		V <sub>CC</sub> = 2.3 V	3.1		
		V <sub>CC</sub> = 3 V	4		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 0.8 V to 3.6 V		200	ns/V
T <sub>A</sub>	Operating free-air temperature	–40	85	°C	

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	DBV	DCK	DPW	DRL	DRY	DSF	UNIT	
	5 PINS	5 PINS	5 PINS	5 PINS	6 PINS	6 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	298.6	314.4	291.8	349.7	554.9	407.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	240.2	128.7	224.2	120.5	385.4	232.0	
R <sub>θJB</sub>	Junction-to-board thermal resistance	134.6	100.6	245.8	171.4	388.2	306.9	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	114.5	7.1	31.4	10.8	159.0	40.3	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	133.9	99.8	245.6	169.4	384.1	306.0	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	n/a	195.4	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –20 μA	0.8 V to 3.6 V	V <sub>CC</sub> – 0.1			V <sub>CC</sub> – 0.1		V
	I <sub>OH</sub> = –1.1 mA	1.1 V	0.75 × V <sub>CC</sub>			0.7 × V <sub>CC</sub>		
	I <sub>OH</sub> = –1.7 mA	1.4 V	1.11			1.03		
	I <sub>OH</sub> = –1.9 mA	1.65 V	1.32			1.3		
	I <sub>OH</sub> = –2.3 mA	2.3 V	2.05			1.97		
	I <sub>OH</sub> = –3.1 mA		1.9			1.85		
	I <sub>OH</sub> = –2.7 mA	3 V	2.72			2.67		
	I <sub>OH</sub> = –4 mA		2.6			2.55		
V <sub>OL</sub>	I <sub>OL</sub> = 20 μA	0.8 V to 3.6 V				0.1	0.1	V
	I <sub>OL</sub> = 1.1 mA	1.1 V	0.3 × V <sub>CC</sub>			0.3 × V <sub>CC</sub>		
	I <sub>OL</sub> = 1.7 mA	1.4 V	0.31			0.37		
	I <sub>OL</sub> = 1.9 mA	1.65 V	0.31			0.35		
	I <sub>OL</sub> = 2.3 mA	2.3 V	0.31			0.33		
	I <sub>OL</sub> = 3.1 mA		0.44			0.45		
	I <sub>OL</sub> = 2.7 mA	3 V	0.31			0.33		
	I <sub>OL</sub> = 4 mA		0.44			0.45		
I <sub>I</sub>	A input	V <sub>I</sub> = GND to 3.6 V	0 V to 3.6 V			0.1	0.5	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V			0.2	0.6	μA
ΔI <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V to 0.2 V			0.2	0.6	μA
I <sub>CC</sub>		V <sub>I</sub> = GND or I <sub>O</sub> = 0 (V <sub>CC</sub> to 3.6 V)	0.8 V to 3.6 V			0.5	0.9	μA
ΔI <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> – 0.6 V, I <sub>O</sub> = 0	3.3 V			40	50	μA
C <sub>I</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	0 V			1.5		pF
			3.6 V			1.5		
C <sub>O</sub>		V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			2.5		pF

## 7.6 Switching Characteristics, C<sub>L</sub> = 5 pF

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	0.8 V	15.6					ns
			1.2 V ± 0.1 V	3.3	5.9	10.8	2.1	13.5	
			1.5 V ± 0.1 V	2.5	4.2	7	1.6	8.8	
			1.8 V ± 0.15 V	2.2	3.4	5.9	1.4	7	
			2.5 V ± 0.2 V	1.7	2.5	4	1.3	4.9	
			3.3 V ± 0.3 V	1.4	2.1	3.2	1.2	3.9	

### 7.7 Switching Characteristics, $C_L = 10$ pF

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	0.8 V	17.7					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	3.9	6.9	12.2	3.1	15	
			$1.5\text{ V} \pm 0.1\text{ V}$	3	5	8.1	2.5	9.9	
			$1.8\text{ V} \pm 0.15\text{ V}$	2.6	4	6.9	2.1	7.9	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.1	3	4.6	1.7	5.6	
			$3.3\text{ V} \pm 0.3\text{ V}$	1.8	2.5	3.8	1.5	4.5	

### 7.8 Switching Characteristics, $C_L = 15$ pF

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	0.8 V	19.5					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	4.7	7.8	13	3.8	15.9	
			$1.5\text{ V} \pm 0.1\text{ V}$	3.7	5.6	8.6	3.1	10.6	
			$1.8\text{ V} \pm 0.15\text{ V}$	3.2	4.6	7.4	2.6	8.5	
			$2.5\text{ V} \pm 0.2\text{ V}$	2.5	3.5	5.1	2.1	6.1	
			$3.3\text{ V} \pm 0.3\text{ V}$	2.2	2.9	4.2	1.9	5	

### 7.9 Switching Characteristics, $C_L = 30$ pF

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

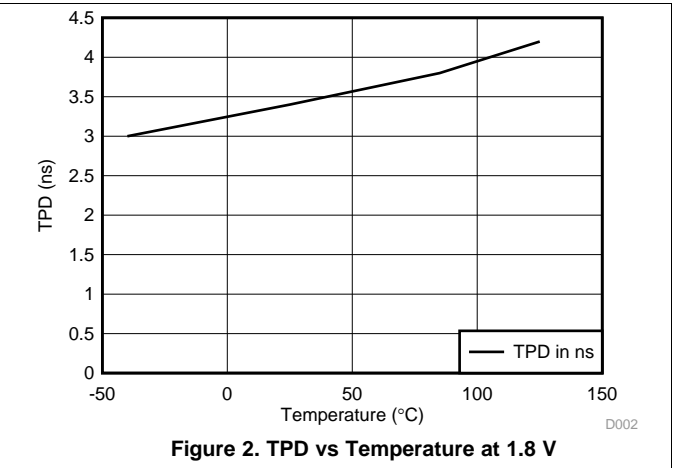
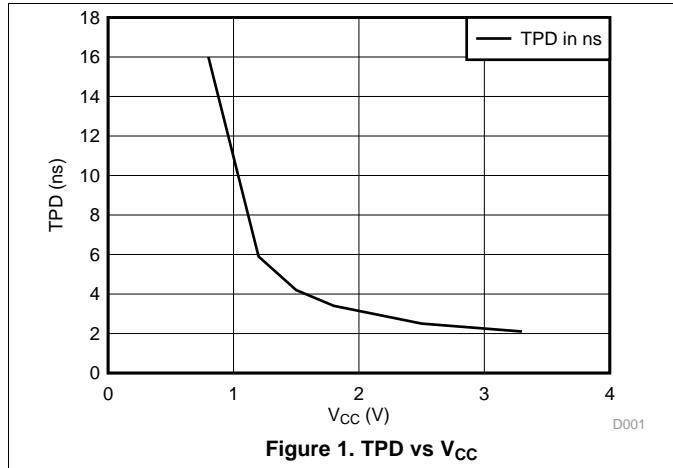
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A	Y	0.8 V	25.4					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	6.8	10.4	16	6.1	19	
			$1.5\text{ V} \pm 0.1\text{ V}$	5.3	7.6	10.8	4.8	12.9	
			$1.8\text{ V} \pm 0.15\text{ V}$	4.6	6.3	9.2	4.1	10.5	
			$2.5\text{ V} \pm 0.2\text{ V}$	3.6	4.8	6.5	3.3	7.6	
			$3.3\text{ V} \pm 0.3\text{ V}$	3.2	4	5.4	2.9	6.2	

### 7.10 Operating Characteristics

 $T_A = 25^\circ\text{C}$ 

PARAMETER	TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$f = 10\text{ MHz}$	0.8 V	3.9	pF
		$1.2\text{ V} \pm 0.1\text{ V}$	3.9	
		$1.5\text{ V} \pm 0.1\text{ V}$	3.9	
		$1.8\text{ V} \pm 0.15\text{ V}$	3.9	
		$2.5\text{ V} \pm 0.2\text{ V}$	3.9	
		$3.3\text{ V} \pm 0.3\text{ V}$	4.1	

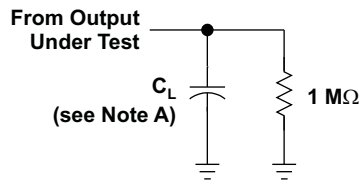
**7.11 Typical Characteristics**





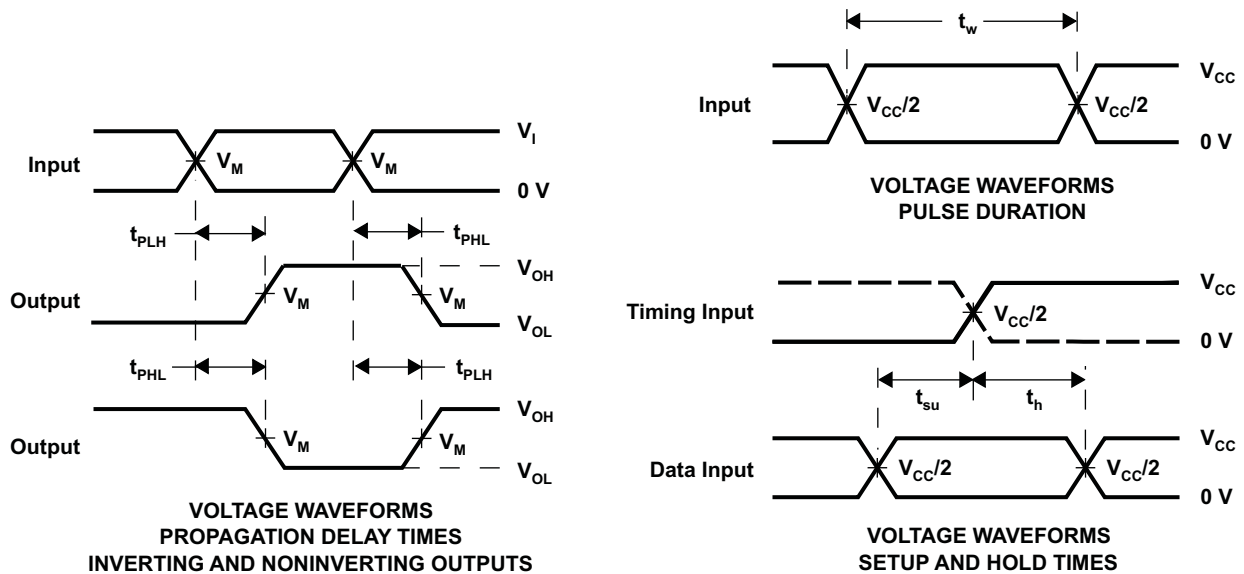
## 8 Parameter Measurement Information

### 8.1 Propagation Delays, Setup and Hold Times, and Pulse Width



LOAD CIRCUIT

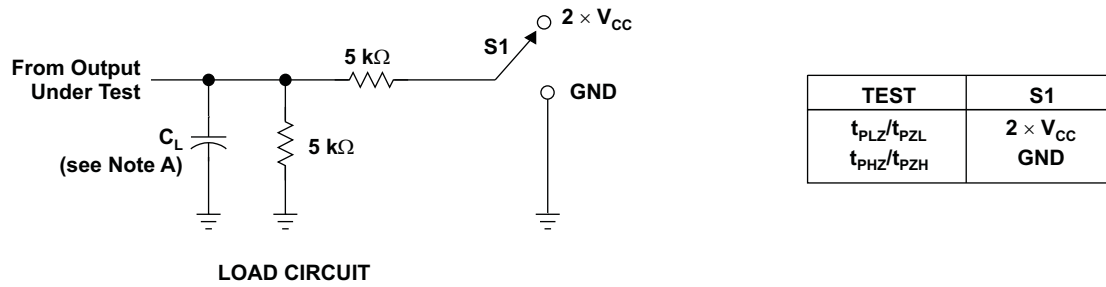
	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$



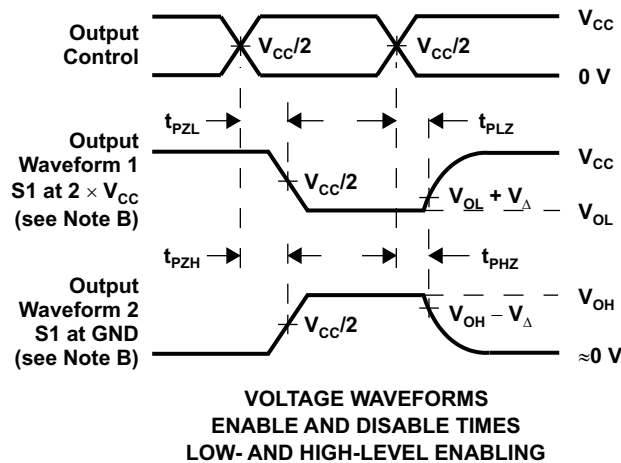
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r/t_f = 3 \text{ ns}$ .  
 C. The outputs are measured one at a time, with one transition per measurement.  
 D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

## 8.2 Enable and Disable Times



	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$
$V_{\Delta}$	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r/t_f = 3 \text{ ns}$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G. All parameters and waveforms are not applicable to all devices.

**Figure 4. Load Circuit and Voltage Waveforms**

## 9 Detailed Description

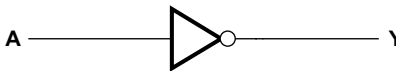
### 9.1 Overview

The SN74AUP1G04 device is a single inverter gate performs the Boolean function  $Y = \bar{A}$ .

The AUP family of devices has quiescent power consumption less than 1  $\mu\text{A}$  and comes in the ultra small DPW package. The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

This device is fully specified for partial-power-down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The  $I_{\text{off}}$  feature also allows for live insertion.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

- Wide operating  $V_{\text{CC}}$  range of 0.8 V to 3.6 V
- 3.6-V I/O tolerant to support down translation
- Input hysteresis allows slow input transition and better switching noise immunity at the input
- $I_{\text{off}}$  feature allows voltages on the inputs and outputs when  $V_{\text{CC}}$  is 0 V
- Low noise due to slower edge rates

### 9.4 Device Functional Modes

**Table 1. Function Table**

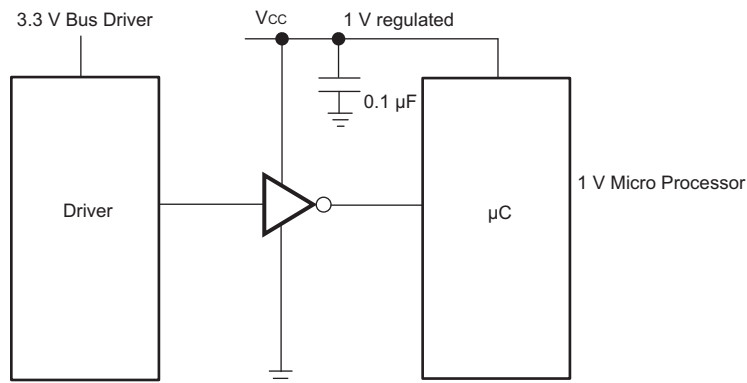
INPUT A	INPUT B
H	L
L	H

## 10 Application and Implementation

### 10.1 Application Information

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire  $V_{CC}$  range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

### 10.2 Typical Application



**Figure 5. Typical Application Schematic**

#### 10.2.1 Design Requirements

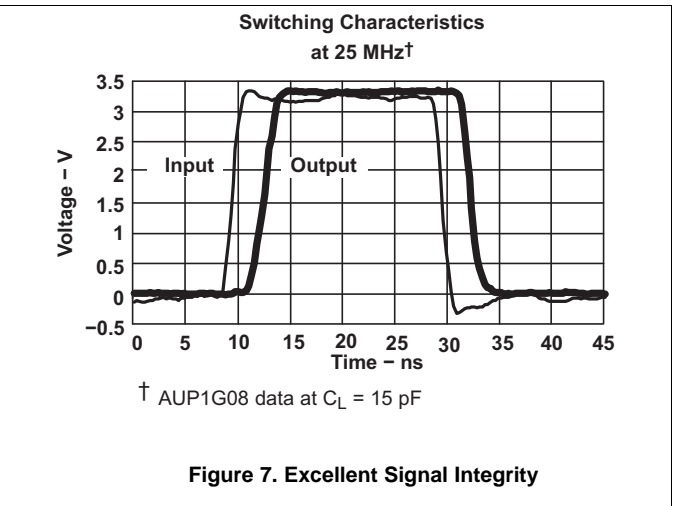
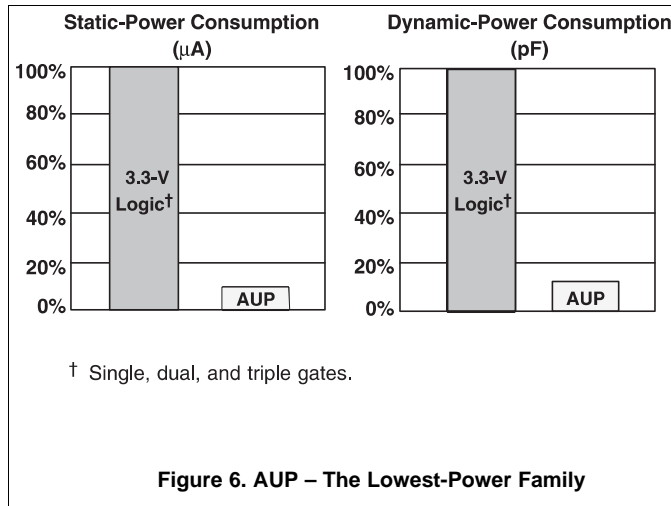
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits.

#### 10.2.2 Detailed Design Procedure

1. Recommended Input conditions
  - Rise time and fall time specs. See  $(\Delta t/\Delta V)$  in [Recommended Operating Conditions](#)
  - Specified high and low levels. See  $(V_{IH}$  and  $V_{IL})$  in [Recommended Operating Conditions](#)
  - Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid  $V_{CC}$
2. Recommend output conditions
  - Load currents should not exceed 20 mA on the output and 50 mA total for the part
  - Outputs should not be pulled above  $V_{CC}$

Typical Application (continued)

10.2.3 Application Curves



The AUP family of single gate logic makes excellent translators for the new lower voltage microprocessors that typically are powered from 0.8 V to 1.2 V. They can drop the voltage of peripheral drivers and accessories that are still powered by 3.3 V to the new uC power levels.

## 11 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the [Recommended Operating Conditions](#) table.

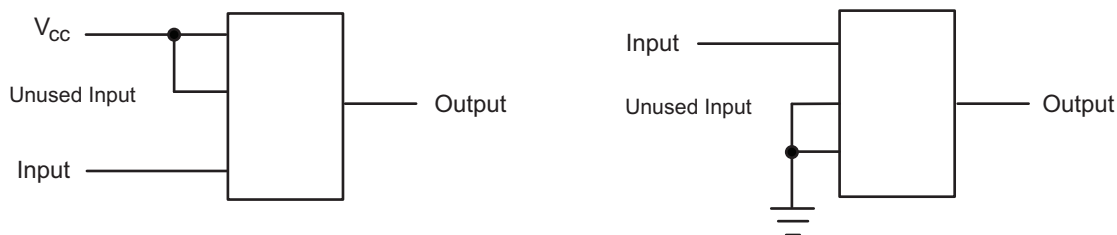
Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and a 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 8](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

### 12.2 Layout Example



**Figure 8. Layout Diagram**

## 13 Device and Documentation Support

### 13.1 Trademarks

The  $I_{off}$  feature also allows for live insertion. is a trademark of others. All other trademarks are the property of their respective owners.

### 13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1G04DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	(H04F ~ H04R)	<a href="#">Samples</a>
SN74AUP1G04DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	(H04F ~ H04R)	<a href="#">Samples</a>
SN74AUP1G04DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HC5 ~ HCF ~ HCK ~ HCR)	<a href="#">Samples</a>
SN74AUP1G04DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HC5 ~ HCF ~ HCK ~ HCR)	<a href="#">Samples</a>
SN74AUP1G04DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HC5 ~ HCF ~ HCK ~ HCR)	<a href="#">Samples</a>
SN74AUP1G04DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HC5 ~ HCF ~ HCR)	<a href="#">Samples</a>
SN74AUP1G04DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HC5 ~ HCF ~ HCR)	<a href="#">Samples</a>
SN74AUP1G04DPWR	ACTIVE	X2SON	DPW	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	C4	<a href="#">Samples</a>
SN74AUP1G04DRLR	ACTIVE	SOT-5X3	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HC7 ~ HCR)	<a href="#">Samples</a>
SN74AUP1G04DRLRG4	ACTIVE	SOT-5X3	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HC7 ~ HCR)	<a href="#">Samples</a>
SN74AUP1G04DRY2	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC	<a href="#">Samples</a>
SN74AUP1G04DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC	<a href="#">Samples</a>
SN74AUP1G04DSF2	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HC	<a href="#">Samples</a>
SN74AUP1G04DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HC	<a href="#">Samples</a>
SN74AUP1G04YFPR	ACTIVE	DSBGA	YFP	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HC N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.



---

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

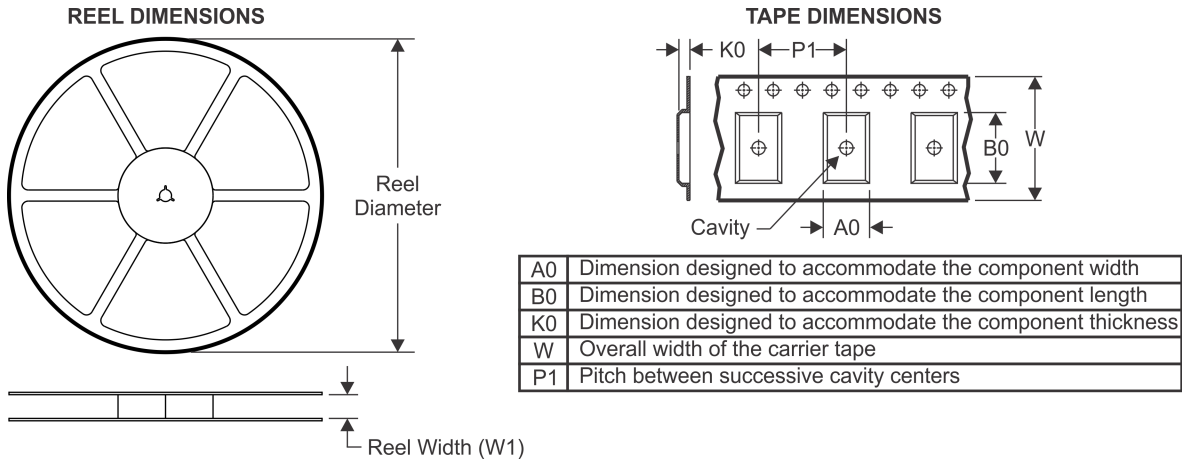
<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

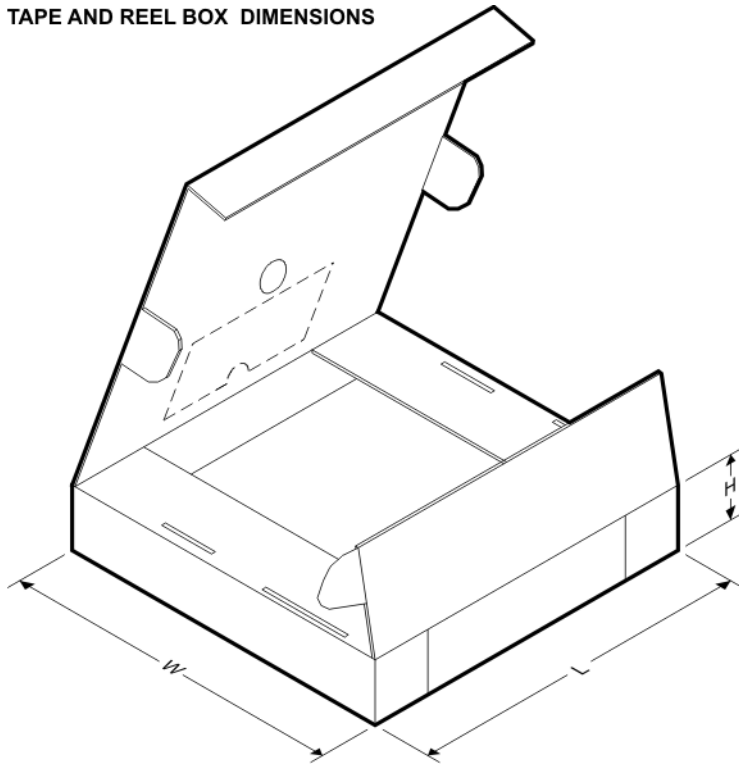
**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G04DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G04DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G04DBVT	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
SN74AUP1G04DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G04DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G04DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP1G04DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G04DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G04DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AUP1G04DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74AUP1G04DRLR	SOT-5X3	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AUP1G04DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G04DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74AUP1G04DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G04DSF2	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74AUP1G04DSF2	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q3
SN74AUP1G04DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
SN74AUP1G04YFPR	DSBGA	YFP	4	3000	178.0	9.2	0.89	0.89	0.58	4.0	8.0	Q1

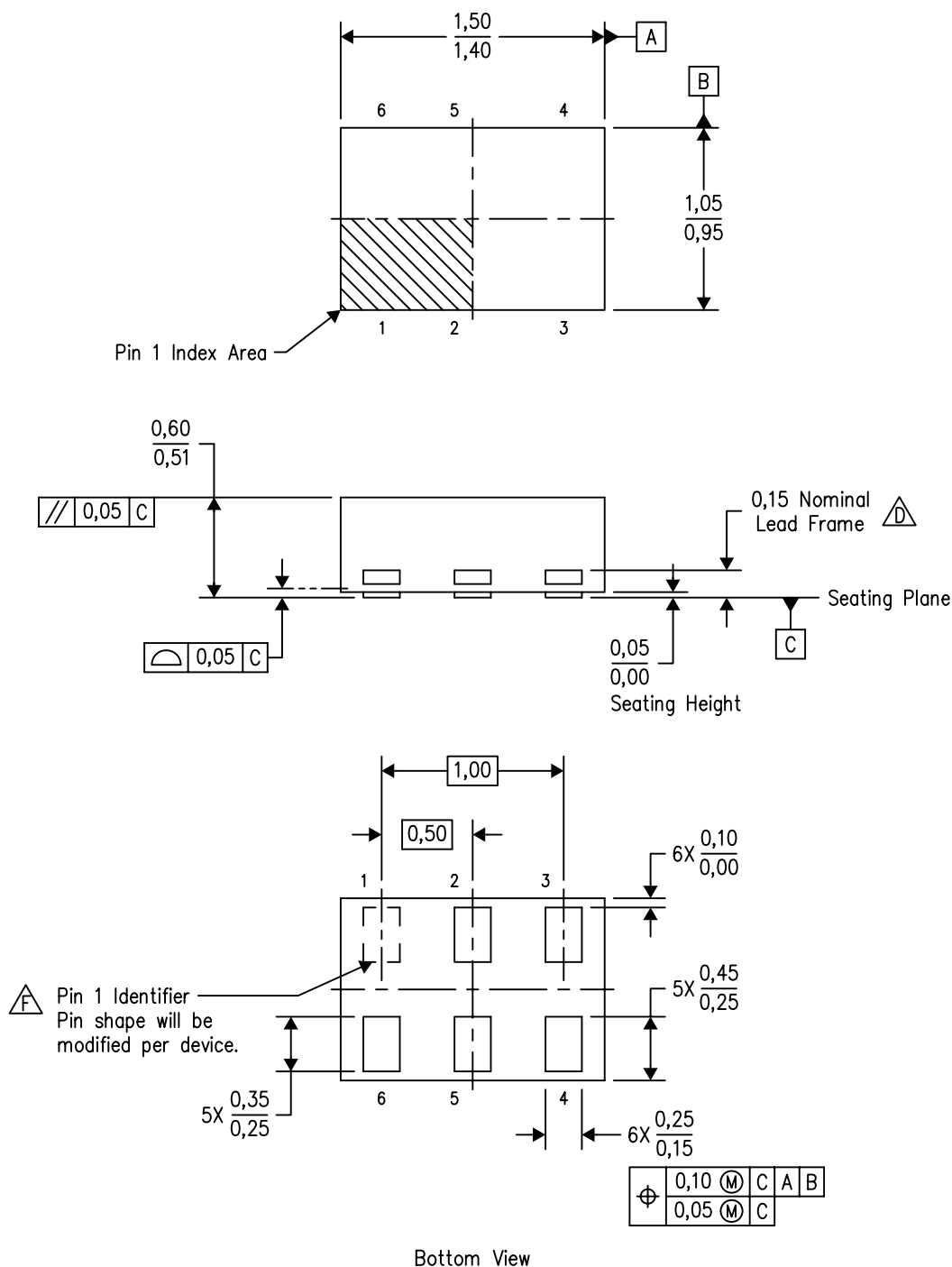
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G04DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G04DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AUP1G04DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AUP1G04DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G04DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G04DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AUP1G04DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUP1G04DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G04DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G04DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74AUP1G04DRLR	SOT-5X3	DRL	5	4000	184.0	184.0	19.0
SN74AUP1G04DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G04DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G04DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G04DSF2	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G04DSF2	SON	DSF	6	5000	202.0	201.0	28.0
SN74AUP1G04DSFR	SON	DSF	6	5000	202.0	201.0	28.0
SN74AUP1G04YFPR	DSBGA	YFP	4	3000	220.0	220.0	35.0

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

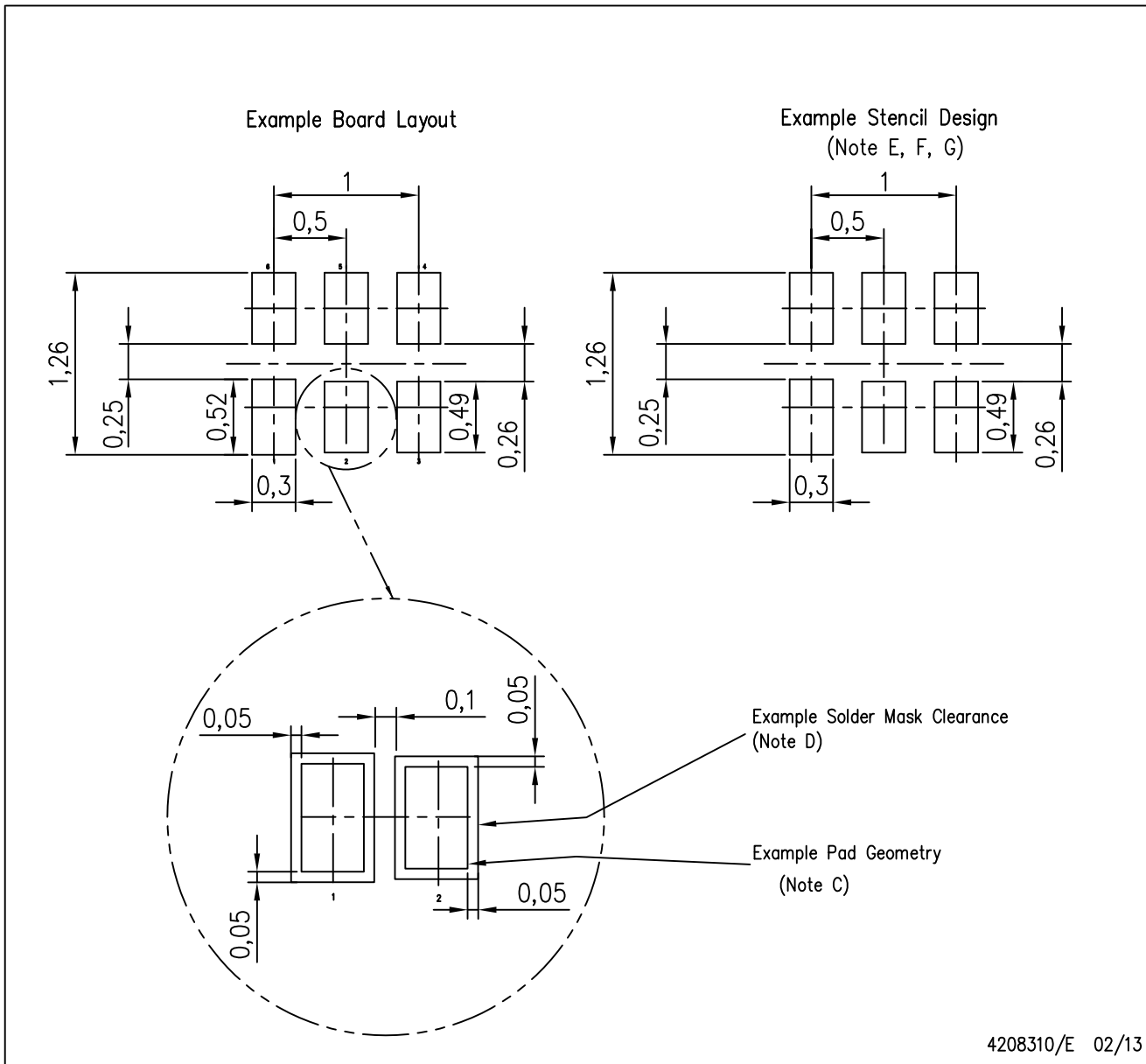


4207181/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. SON (Small Outline No-Lead) package configuration.
  - $\triangle D$  The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
  - E. This package complies to JEDEC MO-287 variation UFAD.
  - $\triangle F$  See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

## GENERIC PACKAGE VIEW

DPW 5

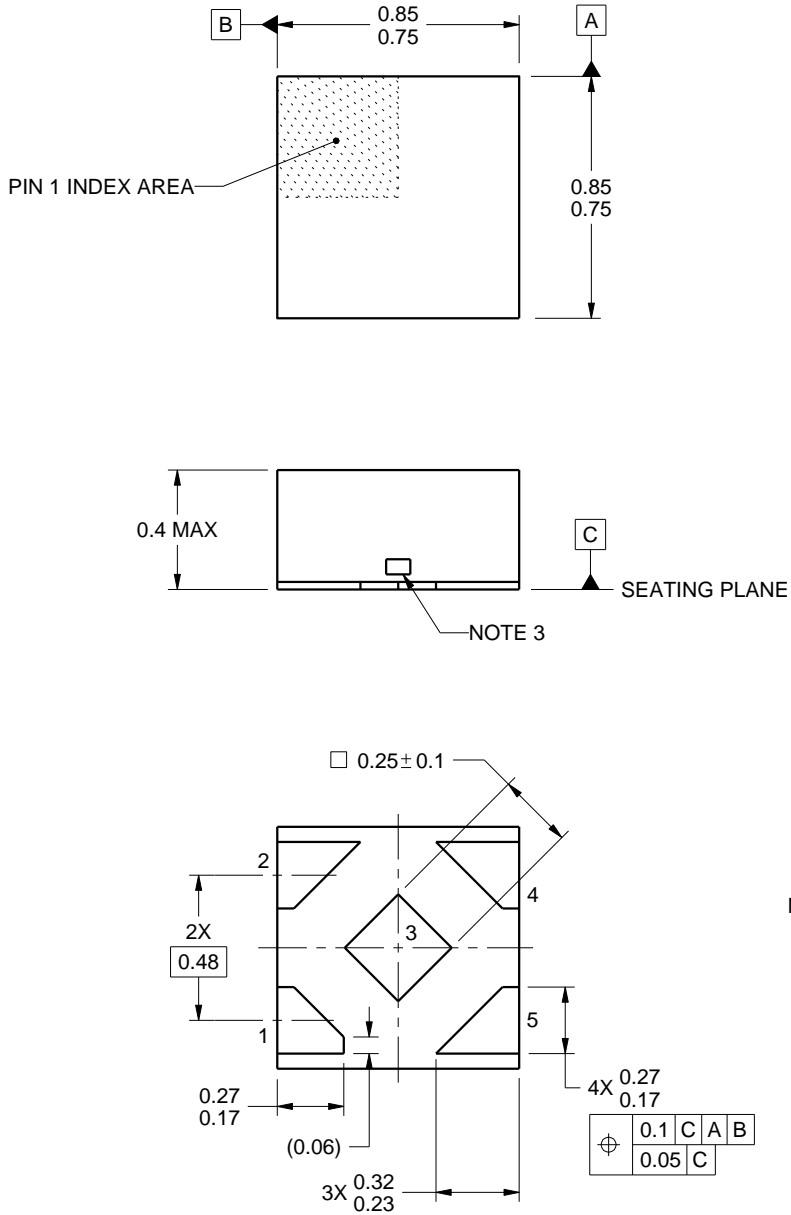
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4211218-3/D



4223102/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



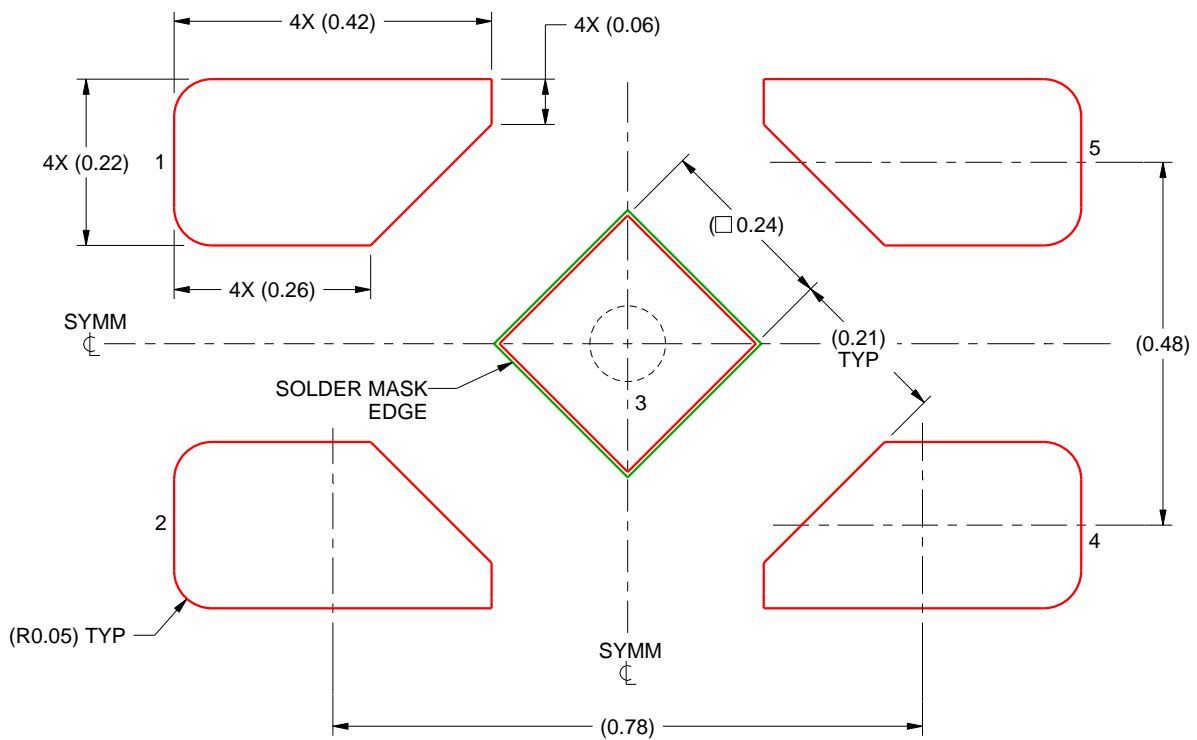


# EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



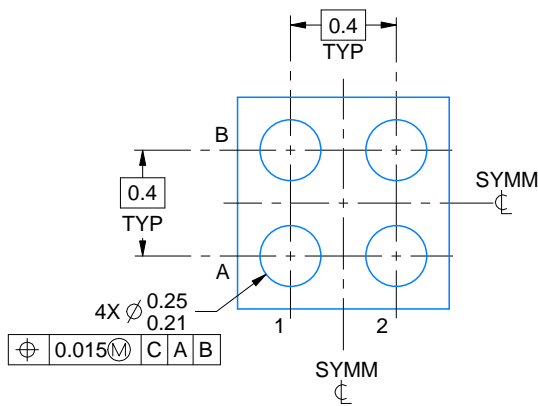
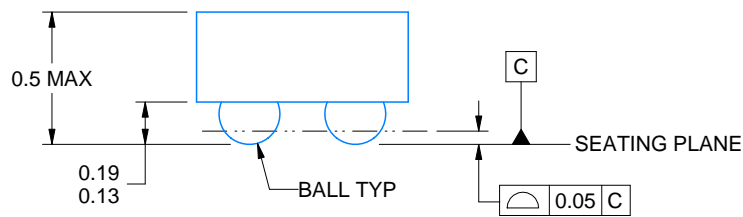
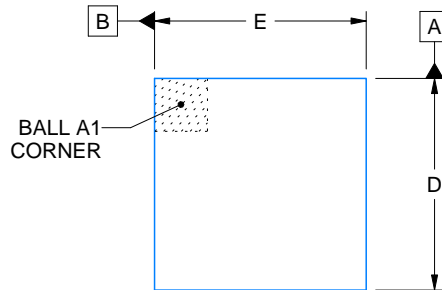
SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD  
92% PRINTED SOLDER COVERAGE BY AREA  
SCALE:100X

4223102/A 07/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



D: Max = 0.79 mm, Min = 0.73 mm  
 E: Max = 0.79 mm, Min = 0.73 mm

4223507/A 01/2017

NOTES:

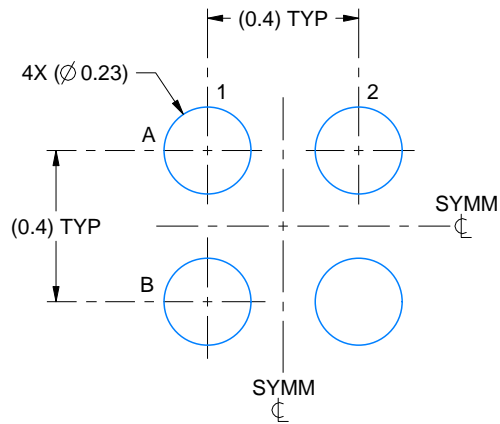
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

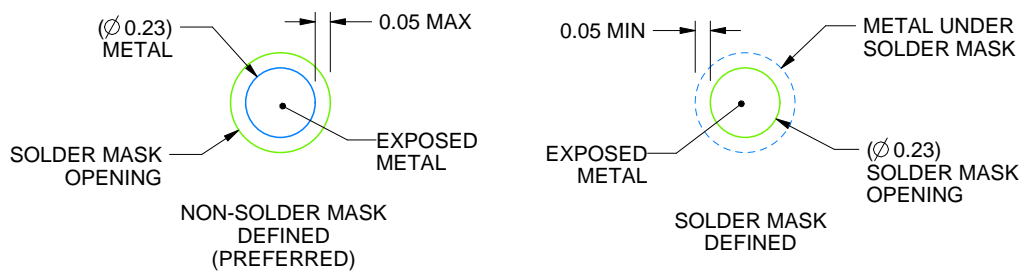
YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:50X



SOLDER MASK DETAILS  
NOT TO SCALE

4223507/A 01/2017

NOTES: (continued)

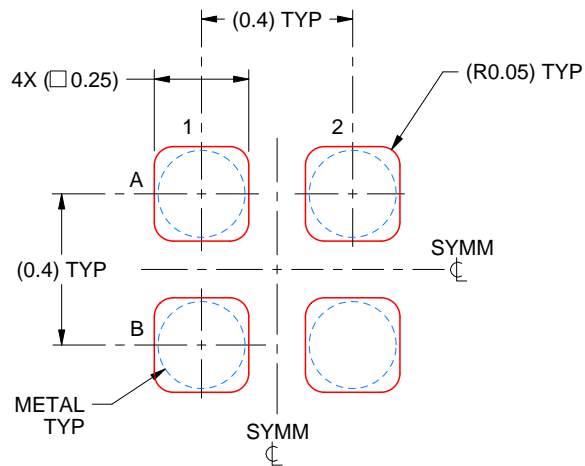
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

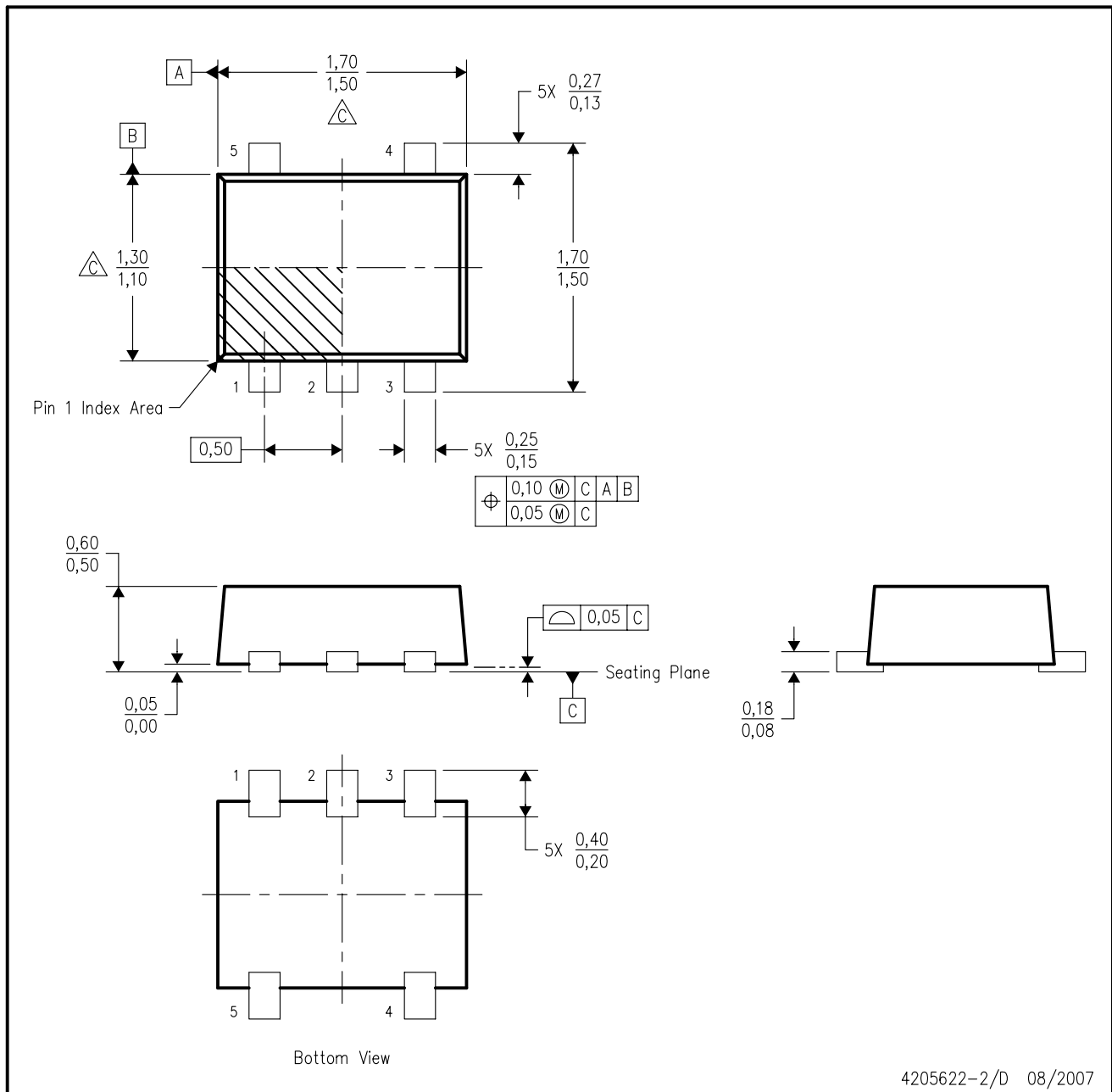


SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:50X

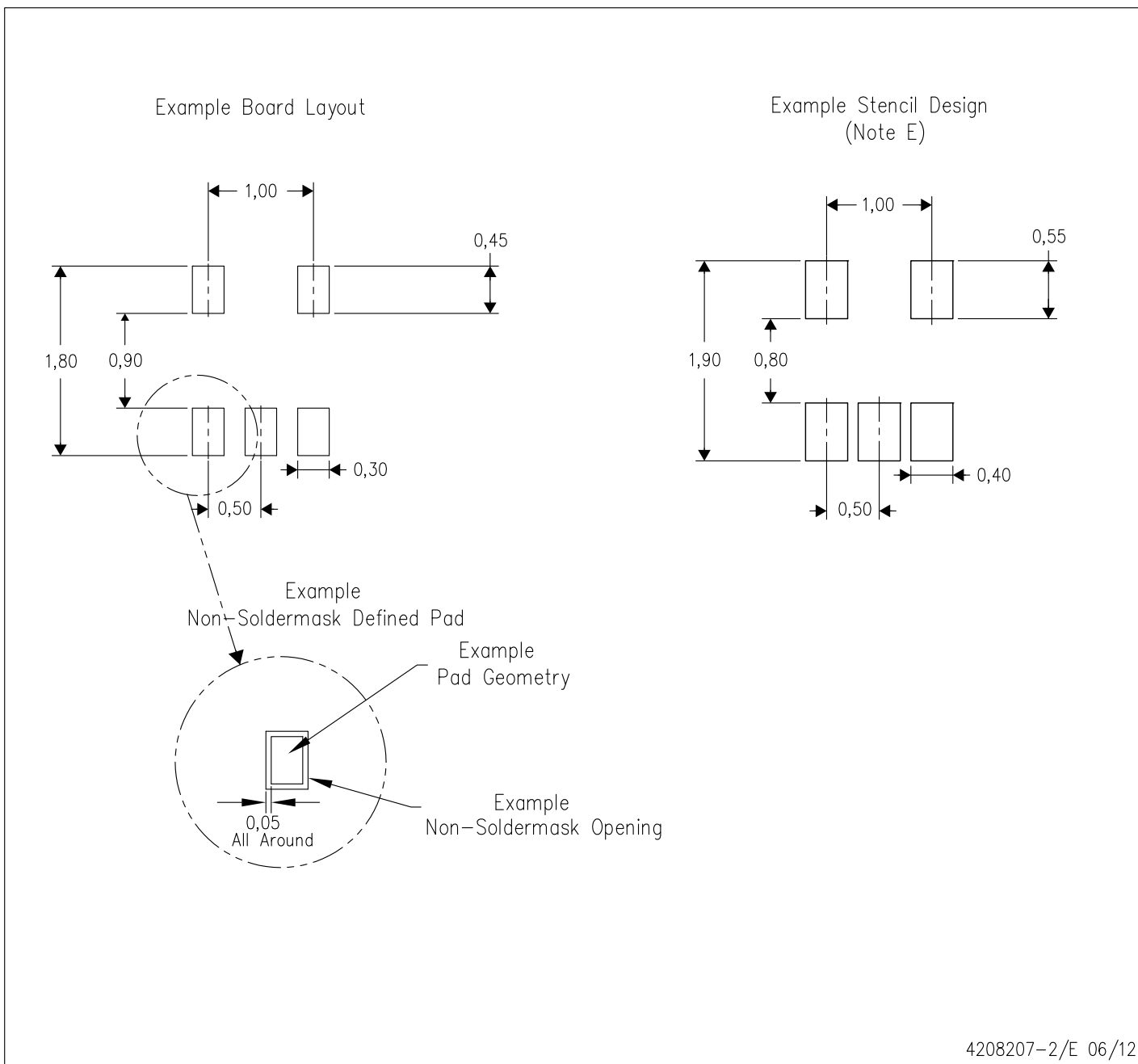
4223507/A 01/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
  - D. JEDEC package registration is pending.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
  - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



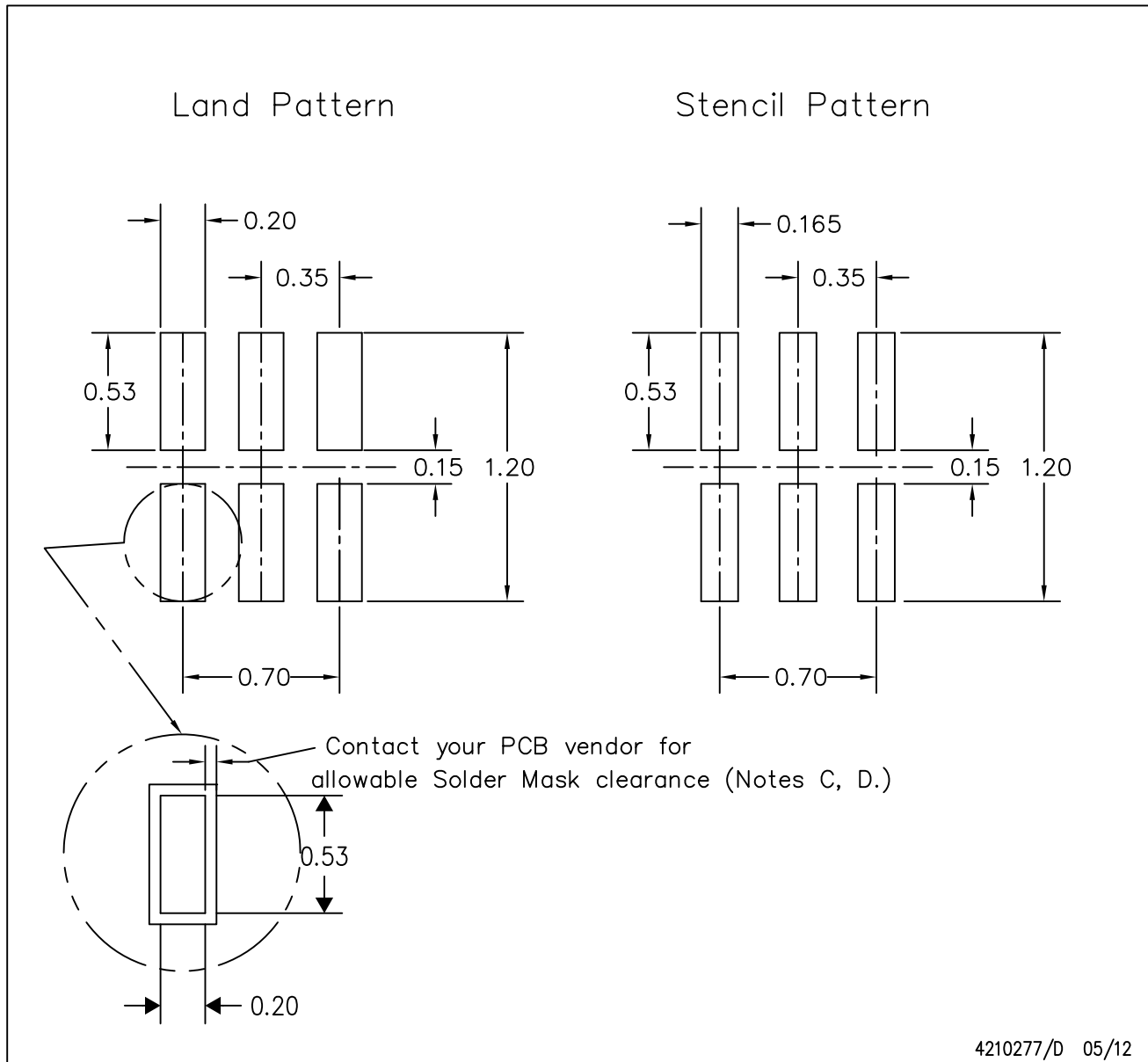
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.





DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



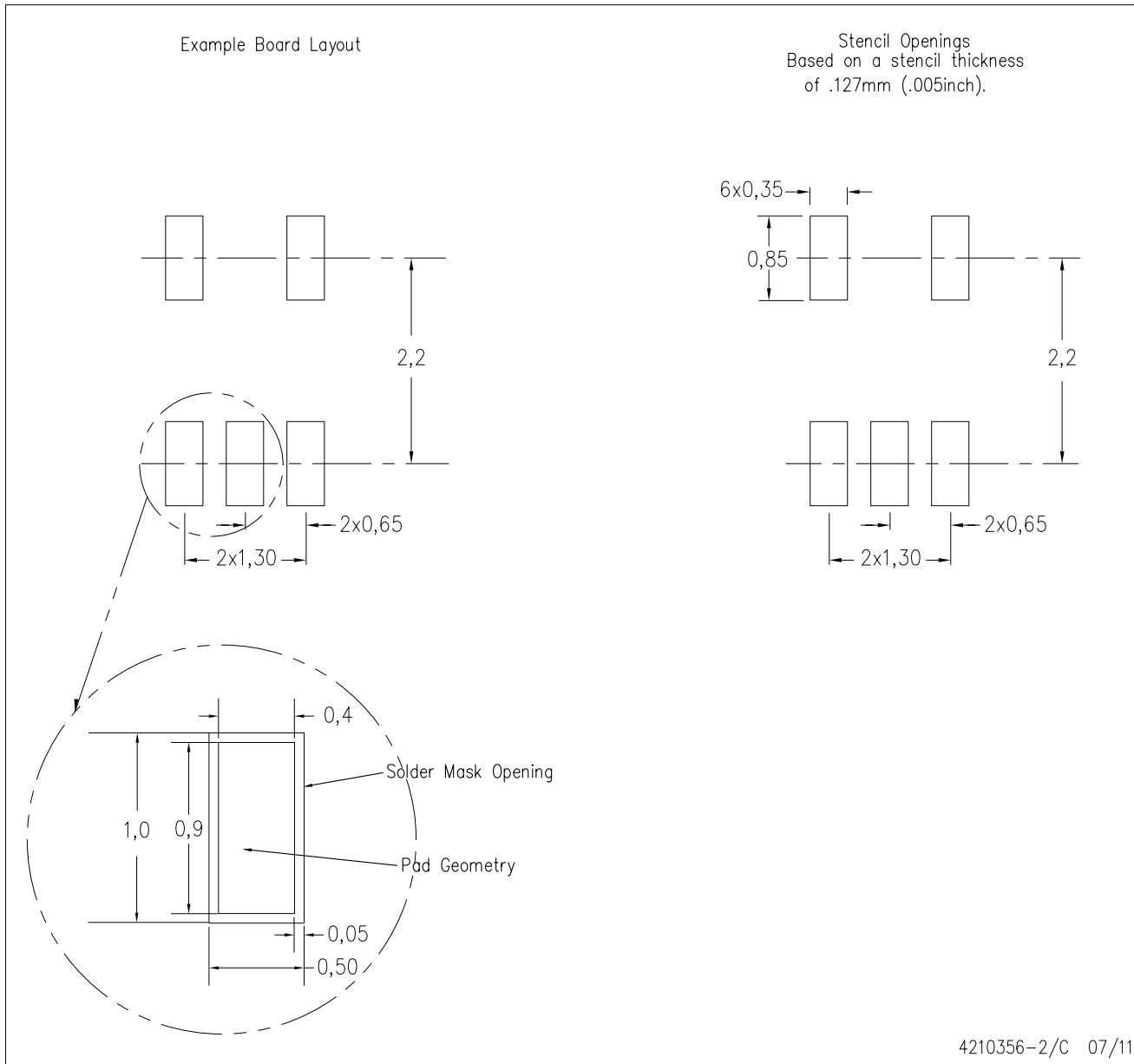
4210277/D 05/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
  - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
  - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
  - H. Component placement force should be minimized to prevent excessive paste block deformation.



DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.