# 250mA低瞬态电流，超低噪音，高电源抑制比(PSRR)低压降线性稳压器

查询样品: TPS73433-Q1, TPS73401-Q1

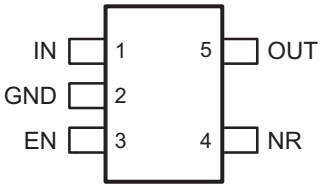
## 特性

- 符合汽车应用要求
- 具有使能功能**(EN)**的**250mA**低压降稳压器
- 低 $I_Q$： **44μA**
- 提供了多个输出电压版本：
  - 固定**3.3V**输出：
  - 从 **1.25V** 到 **6.2V** 的可调节输出
- 高 **PSRR**：频率 **1kHz** 时为 **60dB**
- 超低噪音：**28μ$V_{RMS}$**
- 快速启动时间：**45μs**
- 与一个典型输出电容值为**2.0μF**的低等效串联电阻一起工作时保持稳定
- 负载**/**线路瞬态响应优良
- **2%** 总体准确度（在负载**/**线路**/**温度上）
- 薄型小尺寸晶体管**(SOT)-23**封装

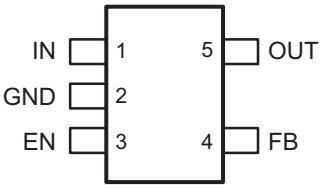
## 说明

TPS734xx-Q1低压降(LDO)，低功率线性稳压器系列产品在保证极低的接地电流的前提下提供出色的交流(ac)性能。 当消耗的接地电流非常低时（典型值44μA），提供高电源抑制比(PSRR)，低噪音，快速启动，和出色的线路和负载瞬态响应。 TPS734xx-Q1与陶瓷电容器一起工作时保持稳定并且使用先进的BiCOMS制造工艺来在输出电压为250mV时生成一个典型值为125mV的压降电压。 TPS734xx-Q1使用一个精度电压基准和反馈环路来实现全部负载，线路，变化，和温度变化范围上2%的总精度。 其额定温度范围$T_A$ = –40°C至+105°C并且采用薄型ThinSOT-23封装，此封装方式是无线耳机，打印机，和无线网路(WLAN)卡的理想选择。

TPS73433TDDCRQ1
TSOT23-5
(TOP VIEW)




TPS73401TDDCRQ1
TSOT23-5
(TOP VIEW)



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**Table 1. ORDERING INFORMATION(1)**

| PRODUCT | $V_{OUT}$ | PACKAGE MARKING |
|---|---|---|
| TPS73433TDDCRQ1 | 3.3V | PXTQ |
| TPS73401TDDCRQ1 | Adjustable | Preview |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating temperature range (unless otherwise noted).

| PARAMETER | TPS734xx-Q1 | UNIT |
|---|---|---|
| $V_{IN}$ range | –0.3 to +7.0 | V |
| $V_{EN}$ range | –0.3 to $V_{IN}$ +0.3 | V |
| $V_{OUT}$ range | –0.3 to $V_{IN}$ +0.3 | V |
| $V_{FB}$ range | –0.3 to $V_{FB}$ (TYP) +0.3 | V |
| Peak output current | Internally limited | |
| Continuous total power dissipation | See Dissipation Ratings Table | |
| Junction temperature range, $T_J$ | –55 to +150 | °C |
| Storage junction temperature range, $T_{STG}$ | –55 to +150 | °C |
| ESD rating, HBM | 2 | kV |
| ESD rating, CDM | 1 | kV |
| ESD rating, MM | 100 | V |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

## DISSIPATION RATINGS

| BOARD | PACKAGE | $R_{\theta JC}$ | $R_{\theta JA}$ | DERATING FACTOR ABOVE $T_A$ = +25°C | $T_A$ < +25°C | $T_A$ = +70°C | $T_A$ = +85°C |
|---|---|---|---|---|---|---|---|
| Low-K(1) | DDC | 90°C/W | 280°C/W | 3.6mW/°C | 360mW | 200mW | 145mW |
| High-K(2) | DDC | 90°C/W | 200°C/W | 5.0mW/°C | 500mW | 275mW | 200mW |

(1) The JEDEC low-K (1s) board used to derive this data was a 3in × 3in (7,62cm × 7,62cm), two-layer board with 2-ounce (56,699g) copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in × 3in (7,62cm × 7,62cm), multilayer board with 1-ounce (28,35g) internal power and ground planes and 2-ounce (56,699g) copper traces on top and bottom of the board

## ELECTRICAL CHARACTERISTICS

Over operating temperature range ($T_A$ = –40°C to +105°C), $V_{IN}$ = $V_{OUT(TYP)}$ + 0.3V or 2.7V, whichever is greater; $I_{OUT}$ = 1mA, $V_{EN}$ = $V_{IN}$, $C_{OUT}$ = 2.2µF, $C_{NR}$ = 0.01µF, unless otherwise noted. For TPS73401-Q1, $V_{OUT}$ = 3.0V.
Typical values are at $T_A$ = +25°C.

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range(1) | | | 2.7 | | 6.5 | V |
| $V_{FB}$ | Internal reference (TPS73401-Q1) | | | 1.184 | 1.208 | 1.232 | V |
| $V_{OUT}$ | Output voltage range (TPS73401-Q1) | | | $V_{FB}$ | | 6.3 | V |
| $V_{OUT}$ | Output accuracy | Nominal | $T_A$ = +25°C | –1.0 | | +1.0 | % |
| $V_{OUT}$ | Output accuracy(1) | Over $V_{IN}$, $I_{OUT}$, Temp | $V_{OUT}$ + 0.3V ≤ $V_{IN}$ ≤ 6.5V<br>1mA ≤ $I_{OUT}$ ≤ 250mA | –2.0 | ±1.0 | +2.0 | % |
| $\Delta V_{OUT}$%/ $\Delta V_{IN}$ | Line regulation(1) | | $V_{OUT(NOM)}$ + 0.3V ≤ $V_{IN}$ ≤ 6.5V | | 0.02 | | %/V |
| $\Delta V_{OUT}$%/ $\Delta I_{OUT}$ | Load regulation | | 500µA ≤ $I_{OUT}$ ≤ 250mA | | 0.005 | | %/mA |
| $V_{DO}$ | Dropout voltage ($V_{IN}$ = $V_{OUT(NOM)}$ – 0.1V) | | $I_{OUT}$ = 250mA | | 125 | 219 | mV |
| $I_{CL}$ | Output current limit | | $V_{OUT}$ = 0.9 × $V_{OUT(NOM)}$ | 300 | 580 | 900 | mA |
| $I_{GND}$ | Ground pin current | | 500µA ≤ $I_{OUT}$ ≤ 250mA | | 45 | 65 | µA |
| $I_{SHDN}$ | Shutdown current ($I_{GND}$) | | $V_{EN}$ ≤ 0.4V | | 0.15 | 1.0 | µA |
| $I_{FB}$ | Feedback pin current (TPS73401-Q1) | | | –0.5 | | 0.5 | µA |
| PSRR | Power-supply rejection ratio<br>$V_{IN}$ = 3.85V, $V_{OUT}$ = 2.85V,<br>$C_{NR}$ = 0.01µF, $I_{OUT}$ = 100mA | | f = 100Hz | | 60 | | dB |
| | | | f = 1kHz | | 56 | | dB |
| | | | f = 10kHz | | 41 | | dB |
| | | | f = 100kHz | | 28 | | dB |
| $V_N$ | Output noise voltage<br>BW = 10Hz to 100kHz, $V_{OUT}$ = 2.8V | | $C_{NR}$ = 0.01µF | | 11 x $V_{OUT}$ | | $\mu V_{RMS}$ |
| | | | $C_{NR}$ = none | | 95 x $V_{OUT}$ | | $\mu V_{RMS}$ |
| $T_{STR}$ | Startup time,<br>$V_{OUT}$ = 0 ~ 90%,<br>$V_{OUT}$ = 2.85V,<br>$R_L$ = 14Ω, $C_{OUT}$ = 2.2µF | | $C_{NR}$ = none | | 45 | | µs |
| | | | $C_{NR}$ = 0.001µF | | 45 | | µs |
| | | | $C_{NR}$ = 0.01µF | | 50 | | µs |
| | | | $C_{NR}$ = 0.047µF | | 50 | | µs |
| $V_{EN(HI)}$ | Enable high (enabled) | | | 1.2 | | $V_{IN}$ | V |
| $V_{EN(LO)}$ | Enable low (shutdown) | | | 0 | | 0.4 | V |
| $I_{EN(HI)}$ | Enable pin current, enabled | | $V_{EN}$ = $V_{IN}$ = 6.5V | | 0.03 | 1.0 | µA |
| $T_{SD}$ | Thermal shutdown temperature | | Shutdown, temperature increasing | | 165 | | °C |
| | | | Reset, temperature decreasing | | 145 | | °C |
| $T_A$ | Operating temperature | | | –40 | | +105 | °C |
| UVLO | Undervoltage lock-out | | $V_{IN}$ rising | 1.90 | 2.20 | 2.65 | V |
| | Hysteresis | | $V_{IN}$ falling | | 70 | | mV |

(1) Minimum $V_{IN}$ = $V_{OUT}$ + $V_{DO}$ or 2.7V, whichever is greater.

## DEVICE INFORMATION

### FUNCTIONAL BLOCK DIAGRAMS

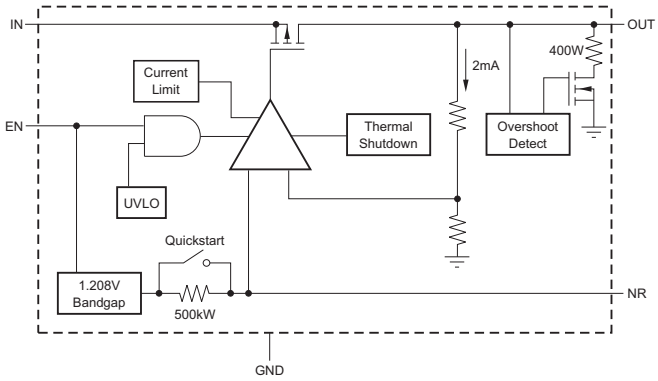



**Figure 1. Fixed Voltage Versions**

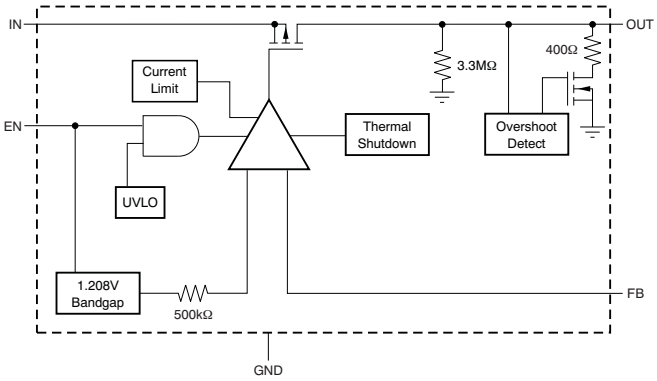
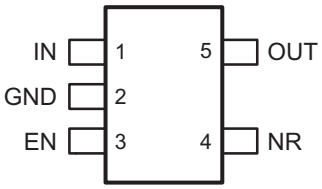


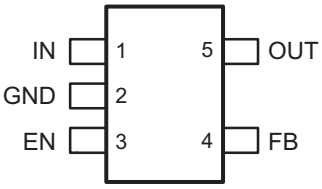

**Figure 2. Adjustable Voltage Versions**

### PIN CONFIGURATIONS

TPS73433TDDCRQ1
TSOT23-5
(TOP VIEW)




TPS73401TDDCRQ1
TSOT23-5
(TOP VIEW)




### PIN DESCRIPTIONS

| TPS734xx-Q1 | | DESCRIPTION |
|---|---|---|
| NAME | DDC | |
| IN | 1 | Input supply. |
| GND | 2 | Ground. The pad must be tied to GND. |
| EN | 3 | Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used. |
| NR | 4 | Fixed voltage versions only; connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This allows output noise to be reduced to very low levels. |
| FB | 4 | Adjustable version only; this is the input to the control loop error amplifier, and is used to set the output voltage of the device. |
| OUT | 5 | Output of the regulator. A small capacitor (total typical capacitance ≥ 2.0μF ceramic) is needed from this pin to ground to assure stability. |

## TYPICAL CHARACTERISTICS

Over operating temperature range ($T_A$ = –40°C to +105°C); $V_{IN}$ = $V_{OUT(TYP)}$ + 0.3V or 2.7V, whichever is greater; $I_{OUT}$ = 1mA, $V_{EN}$ = $V_{IN}$,$C_{OUT}$ = 2.2µF, $C_{NR}$ = 0.01µF, unless otherwise noted. For TPS73401-Q1, $V_{OUT}$ = 3.0V. Typical values are at $T_A$ = +25°C.

**TPS73401-Q1 LINE REGULATION**

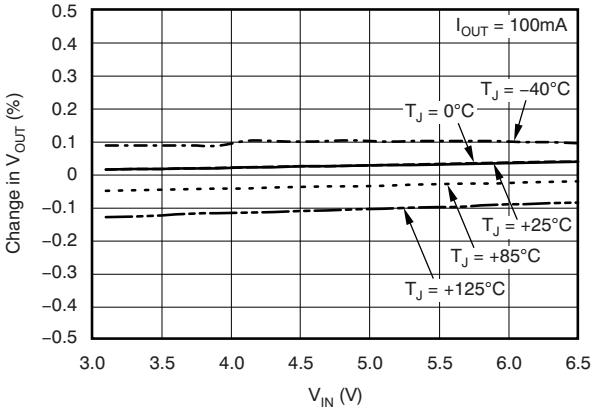



**Figure 3.**

**TPS73401-Q1 LOAD REGULATION**

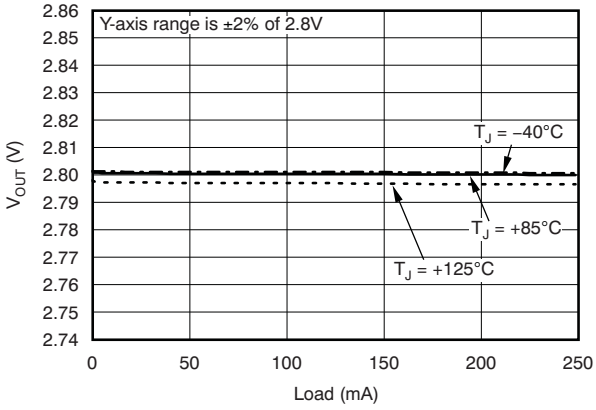



**Figure 4.**

**TPS73401-Q1 DROPOUT VOLTAGE vs OUTPUT CURRENT**

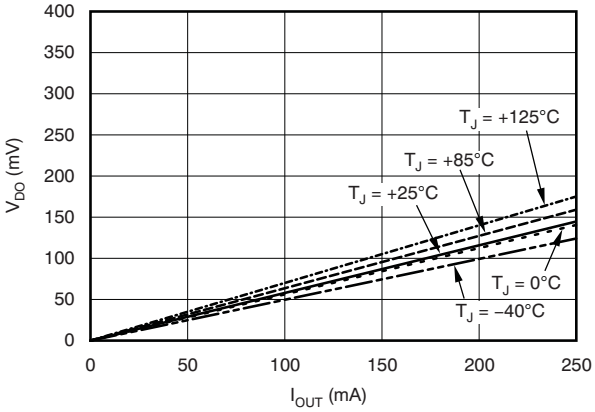



**Figure 5.**

**POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY ($V_{IN}$ – $V_{OUT}$ = 1.0V)**

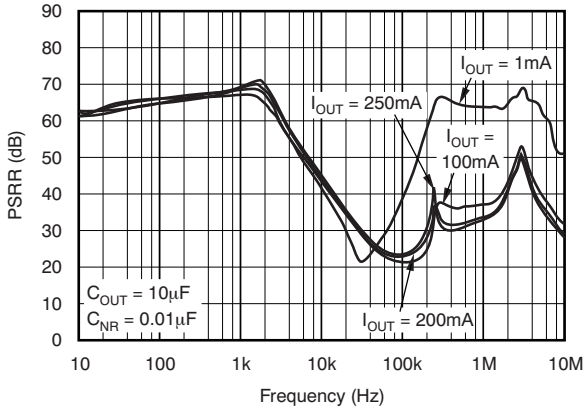



**Figure 6.**

**POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY ($V_{IN}$ – $V_{OUT}$ = 0.5V)**

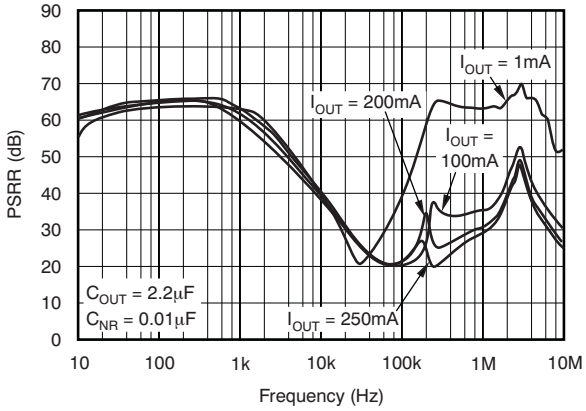



**Figure 7.**

**POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY ($V_{IN}$ – $V_{OUT}$ = 0.3V)**

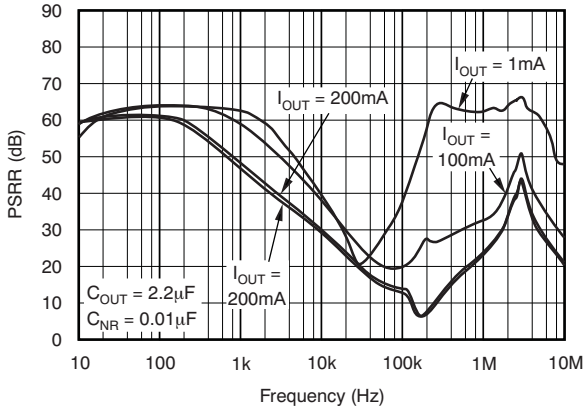



**Figure 8.**

## APPLICATION INFORMATION

The TPS734xx-Q1 family of LDO regulators combines the high performance required of many RF and precision analog applications with ultra-low current consumption. High PSRR is provided by a high gain, high bandwidth error loop with good supply rejection at very low headroom ($V_{IN}$ – $V_{OUT}$). Fixed voltage versions provide a noise reduction pin to bypass noise generated by the bandgap reference and to improve PSRR while a quick-start circuit fast-charges this capacitor at startup. The combination of high performance and low ground current also make the TPS734xx-Q1 an excellent choice for portable applications. All versions have thermal and over-current protection and are fully specified from –40°C to +105°C.

Figure 9 shows the basic circuit connections for fixed voltage models. Figure 10 gives the connections for the adjustable output version (TPS73401-Q1). $R_1$ and $R_2$ can be calculated for any output voltage using the formula in Figure 10.

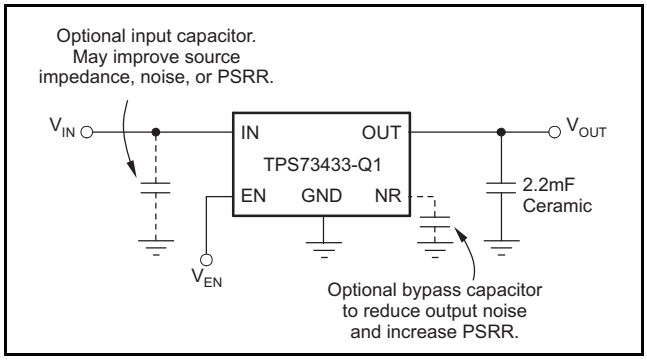



**Figure 9. Typical Application Circuit for FIxed Voltage Versions**

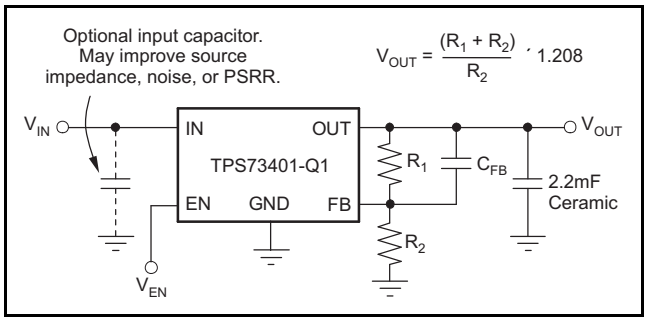



**Figure 10. Typical Application Circuit for Adjustable Voltage Versions**

### Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. The ground of this capacitor should be connected as close as the ground of output capacitor; a capacitor value of 0.1µF is enough in this condition. When it is difficult to place these two ground points close together, a 1µF capacitor is recommended. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1µF input capacitor may be necessary to ensure stability.

The TPS734xx-Q1 is designed to be stable with standard ceramic output capacitors of values 2.2µF or larger. X5R and X7R type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR of the output capacitor should be < 1.0Ω, so output capacitor type should be either ceramic or conductive polymer electrolytic.

### Feedback Capacitor Requirements (TPS73401-Q1 only)

The feedback capacitor, $C_{FB}$, shown in Figure 10 is required for stability. For a parallel combination of $R_1$ and $R_2$ equal to 250kΩ, any value from 3pF to 1nF can be used. Fixed voltage versions have an internal 30pF feedback capacitor that is quick-charged at start-up. The adjustable version does not have this quick-charge circuit, so values below 5pF should be used to ensure fast startup; values above 47pF can be used to implement an output voltage soft-start. Larger value capacitors also improve noise slightly. The TPS73401-Q1 is stable in unity-gain configuration (OUT tied to FB) without $C_{FB}$.

### Output Noise

In most LDOs, the bandgap is the dominant noise source. If a noise reduction capacitor ($C_{NR}$) is used with the TPS734xx-Q1, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01µF noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives 2µA of divider current has the same noise performance as a fixed voltage version.

To further optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2Ω. This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point (FB pin) such that with $C_{NR}$ = 0.01µF, total noise is given approximately by Equation 1:

$$V_N = \frac{11\mu V_{RMS}}{V} \times V_{OUT} \quad (1)$$

The TPS73401-Q1 adjustable version does not have the noise-reduction pin available, so ultra-low noise operation is not possible. Noise can be minimized according to the above recommendations.

## Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for $V_{IN}$ and $V_{OUT}$, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

## Internal Current Limit

The TPS734xx-Q1 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in current limit for extended periods of time.

The PMOS pass element in the TPS734xx-Q1 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

## Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

## Dropout Voltage

The TPS734xx-Q1 uses a PMOS pass transistor to achieve low dropout. When ($V_{IN}$ – $V_{OUT}$) is less than the dropout voltage ($V_{DO}$), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS,\ ON}$ of the PMOS pass element. Because the PMOS device behaves like a resistor in dropout, $V_{DO}$ approximately scales with output current.

As with any linear regulator, PSRR and transient response are degraded as ($V_{IN}$ – $V_{OUT}$) approaches dropout. This effect is shown in the Typical Characteristics section.

## Startup and Noise Reduction Capacitor

Fixed voltage versions of the TPS734xx-Q1 use a quick-start circuit to fast-charge the noise reduction capacitor, $C_{NR}$, if present (see the Functional Block Diagrams). This architecture allows the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage $C_{NR}$ capacitor must be used; most ceramic capacitors are appropriate in this configuration.

Note that for fastest startup, $V_{IN}$ should be applied first, then the enable pin (EN) driven high. If EN is tied to IN, startup is somewhat slower. Refer to the Typical Characteristics section. The quick-start switch is closed for approximately 135µs. To ensure that $C_{NR}$ is fully charged during the quick-start time, a 0.01µF or smaller capacitor should be used.

## Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response. In the adjustable version, adding $C_{FB}$ between OUT and FB improves stability and transient response. The transient response of the TPS734xx-Q1 is enhanced by an active pull-down that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pull-down device behaves like a 400Ω resistor to ground.

## Undervoltage Lock-Out (UVLO)

The TPS734xx-Q1 utilizes an undervoltage lock-out circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a de-glitch feature so that it typically ignores undershoot transients on the input if they are less than 50µs duration.

## Minimum Load

The TPS734xx-Q1 is stable and well-behaved with no output load. To meet the specified accuracy, a minimum load of 1mA is required. Below 1mA at junction temperatures near +125°C, the output can drift up enough to cause the output pull-down to turn on. The output pull-down limits voltage drift to 5% typically but ground current could increase by approximately 50µA. In typical applications, the junction cannot reach high temperatures at light loads because there is no appreciable dissipated power. The specified ground current would then be valid at no load conditions in most applications.

## Thermal Information

### Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS734xx-Q1 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS734xx-Q1 into thermal shutdown degrades device reliability.

### Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Dissipation Ratings* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current time the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT} \quad (2)$$

### Package Mounting

Solder pad footprint recommendations for the TPS734xx-Q1 are available from the Texas Instruments web site at www.ti.com.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS73401DDCR | ACTIVE | SOT-23-THIN | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OCW | Samples |
| TPS73401DDCT | ACTIVE | SOT-23-THIN | DDC | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OCW | Samples |
| TPS73401DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CBG | Samples |
| TPS73401DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CBG | Samples |
| TPS73418DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CBI | Samples |
| TPS73418DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CBI | Samples |
| TPS73430DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CVW | Samples |
| TPS73430DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CVW | Samples |
| TPS73433DDCR | ACTIVE | SOT-23-THIN | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OEV | Samples |
| TPS73433DDCT | ACTIVE | SOT-23-THIN | DDC | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | OEV | Samples |
| TPS73433DRVR | ACTIVE | WSON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CVX | Samples |
| TPS73433DRVT | ACTIVE | WSON | DRV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CVX | Samples |
| TPS73433TDDCRQ1 | ACTIVE | SOT-23-THIN | DDC | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | PXTQ | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

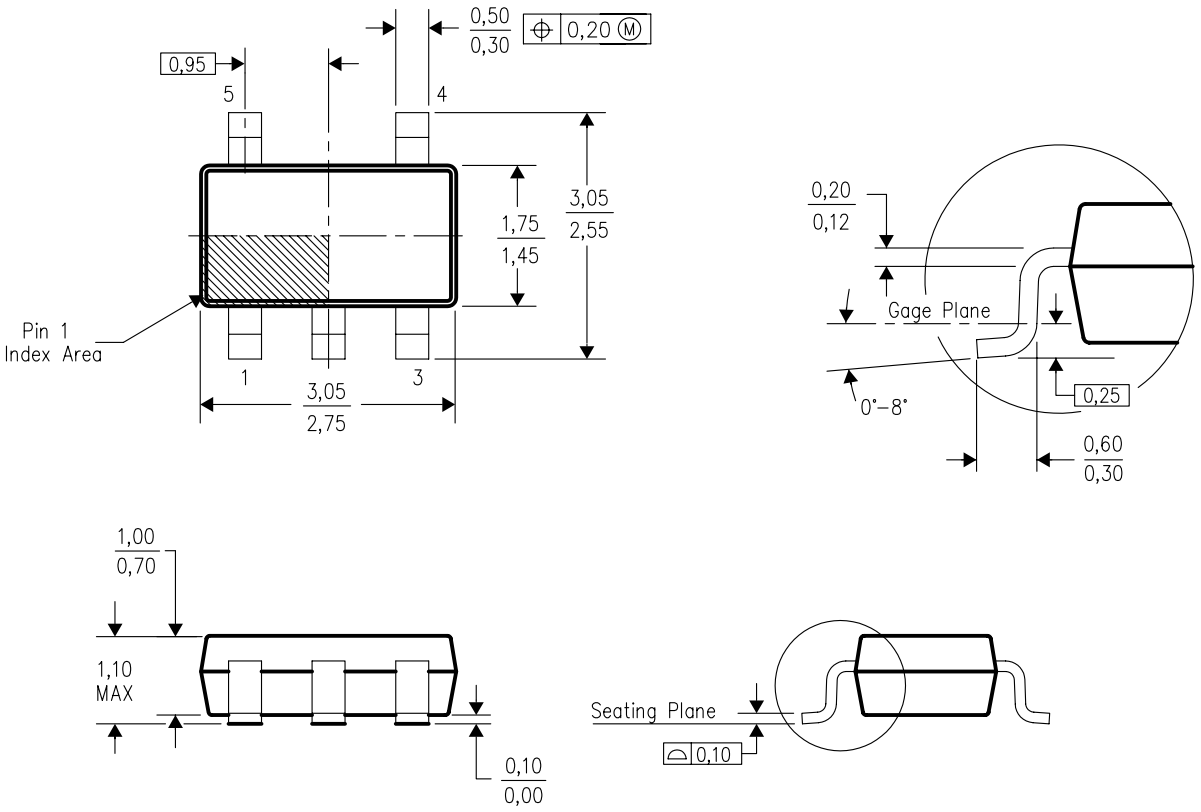
**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

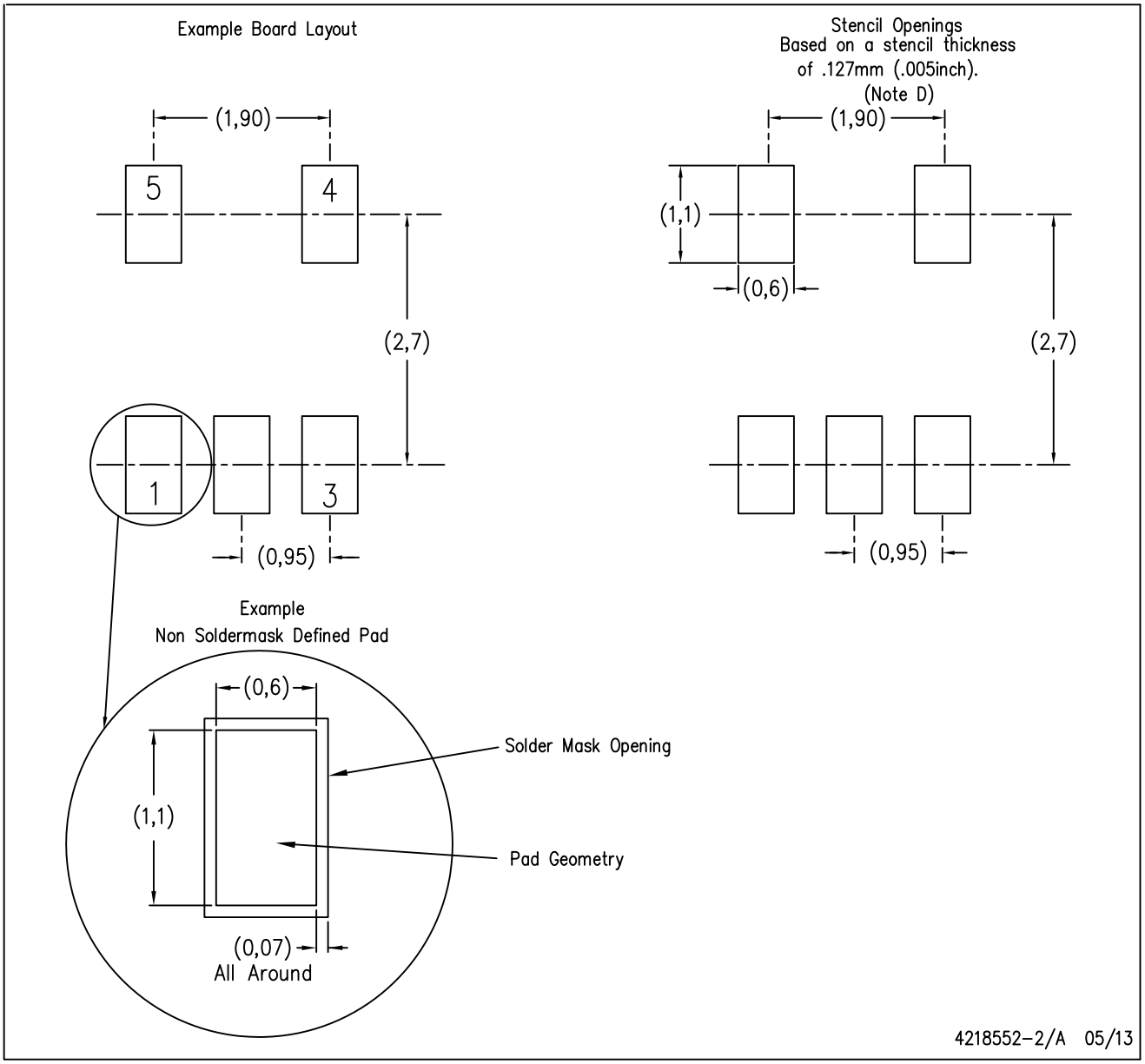
## DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE




4204403–2/E 06/05

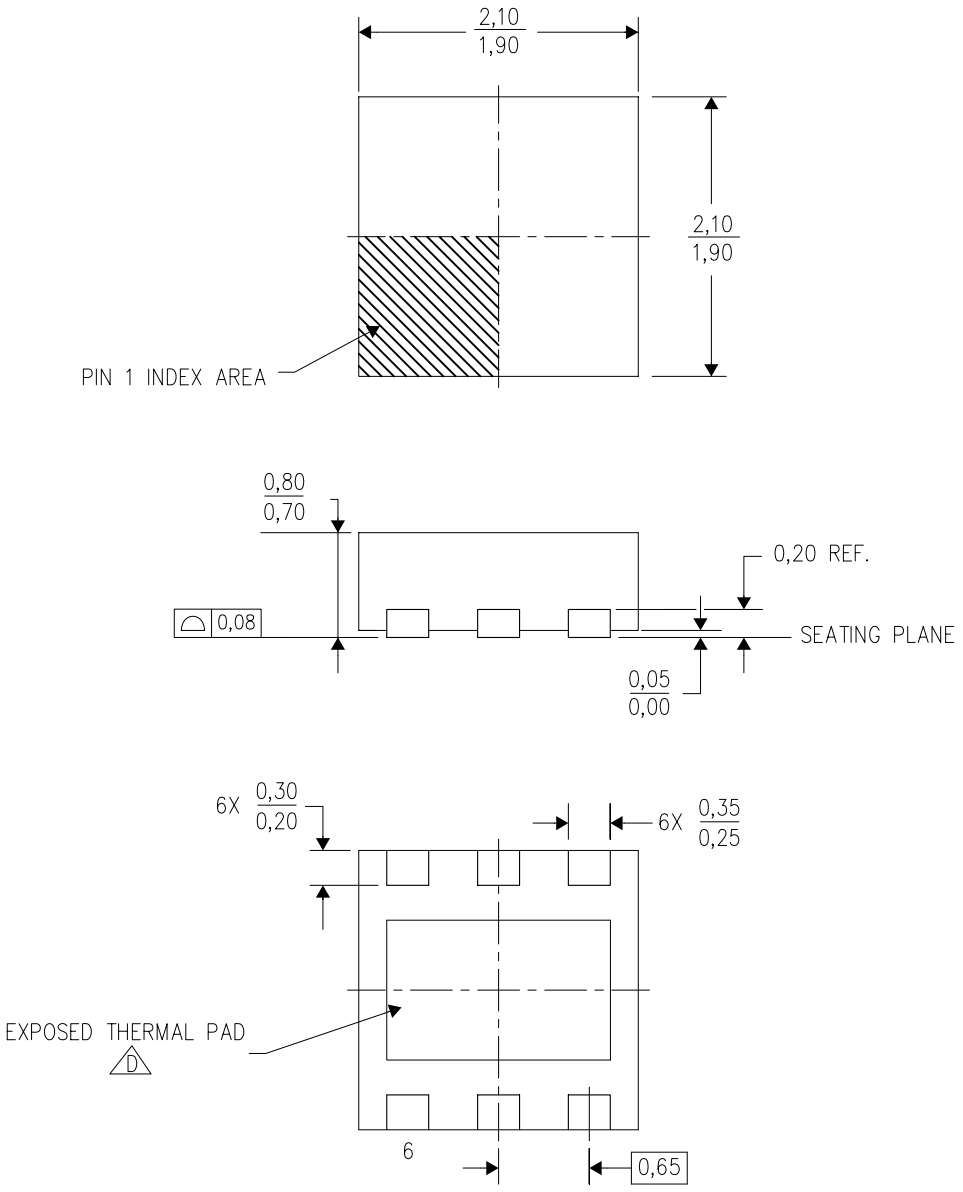
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AB (5 pin).

DDC (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

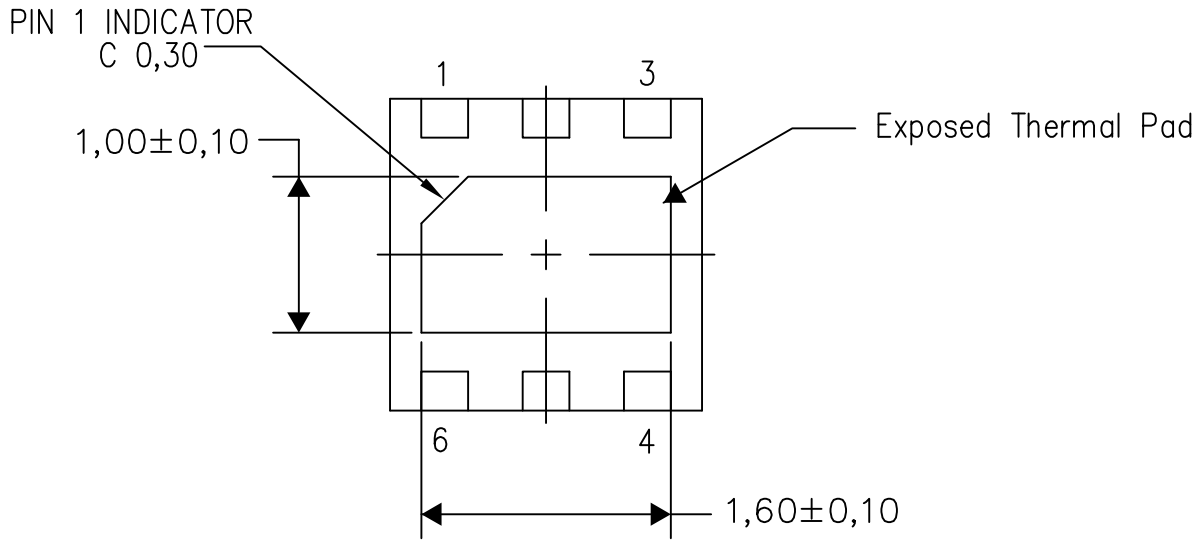
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



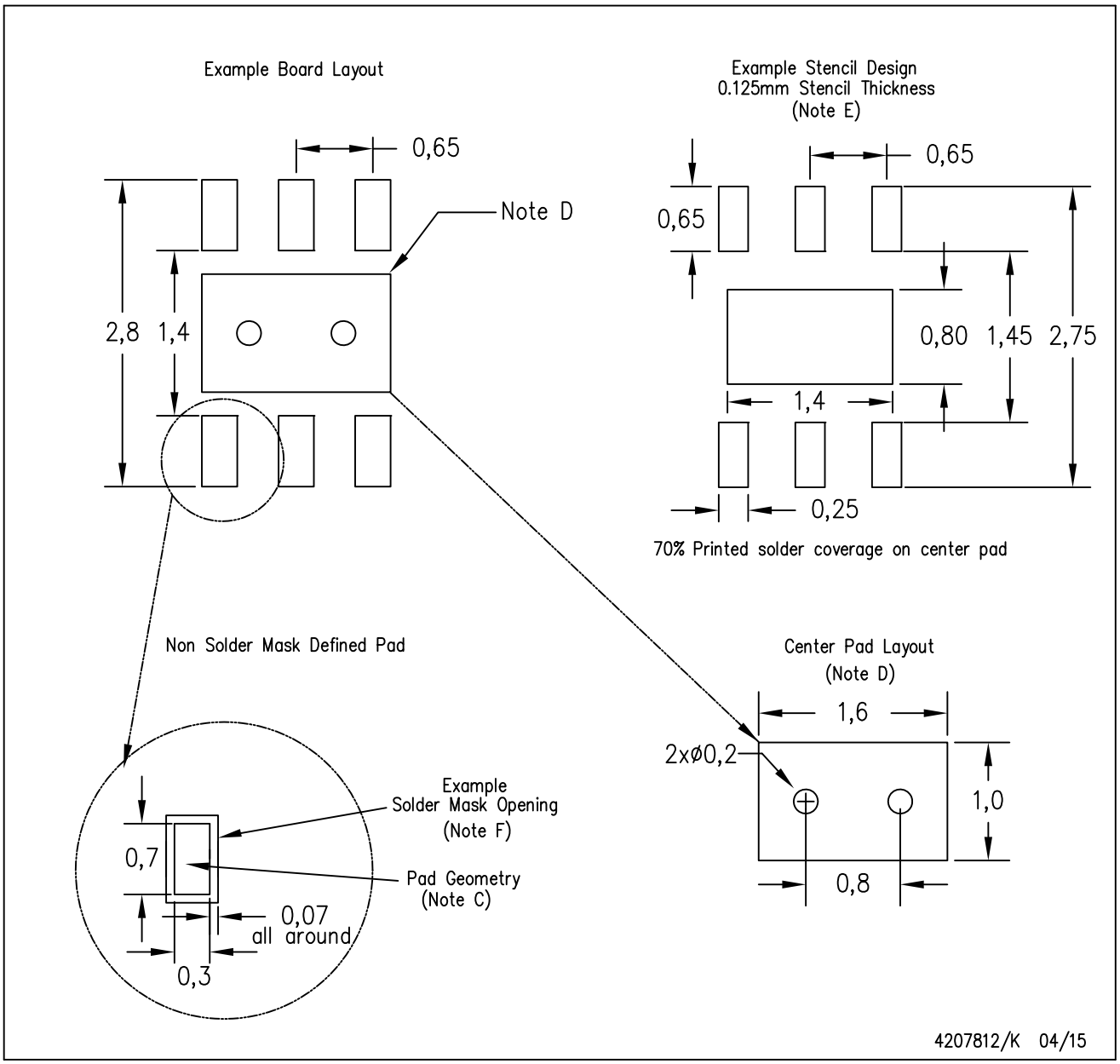

Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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