LMV611 单通道 / LMV612 双通道 / LMV614 四通道 1.4MHz，低功耗通用，1.8V 运算放大器

查询样品: LMV611, LMV612, LMV614

特性

- （典型 **1.8V** 电源值；除非另外注明）
- 保证了 **1.8V**，**2.7V** 和 **5V** 技术规格
- 输出摆幅
  - **w/600Ω** 负载时，电源轨摆幅 **80mV**
  - **w/2kΩ** 负载时，电源轨摆幅 **30mV**
- V_{CM}超过电源轨 **200mW**
- 电源电流（每个通道）**100μA**
- 增益带宽产品 **1.4MHz**
- 最大 V_{OS}**4.0mV**
- 温度范围 **-40°C** 至 **125°C**

应用范围

- 消费类通信产品
- 消费类计算产品
- 掌上电脑 **(PDA)**
- 音频预放大器
- 便携式/电池供电类设备
- 电源电流监控
- 电池监控

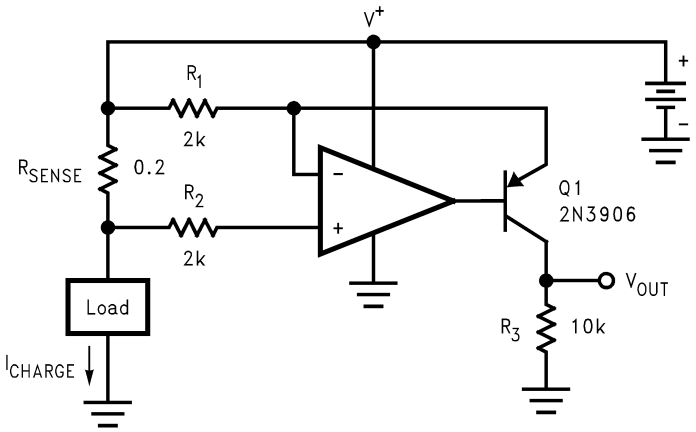
说明

LMV611/LMV612/LMV614 是单通道、双通道和四通道低压、低功率运算放大器。 它们专门针对低压通用应用而设计。 其它重要特点有，轨到轨输入/输出，1.8V 的低电源电压以及宽温度范围。 LMV611/LMV612/LMV614 输入共模扩展至电源以上 200mV，并且此输出可在无负载时轨到轨摆动，并在由 1.8V 电源供电，且负载为 2kΩ 时，输出在 30mV 以内。 LMV611/2/4 在汲取的静态电流为 100uA（典型值）时，可实现 1.4MHz 的增益带宽。

-40°C 至 125°C 的工业增强型温度范围使得 LMV611/LMV612/LMV614 能够适应广泛的扩展环境应用。

LMV611 采用微型 5 引脚 SC70 封装，LMV612 采用节省空间的 8 引脚超薄型小外形尺寸封装 (VSSOP) 和小外形尺寸集成电路封装 (SOIC)，而 LMV614 采用 14 引脚薄型小外形尺寸封装 (TSSOP) 和 SOIC 封装。 这些小型封装放大器为需要最小印刷电路板 (PCB) 封装尺寸的应用提供了理想的解决方案。 有空间受限 PC 电路板要求的应用包含便携式和电池供电类电子元器件。

典型应用



$$V_{OUT} = \frac{R_{SENSE} \bullet R_3}{R_1} \bullet I_{Charge} = 1\Omega \bullet I_{Charge}$$

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

ESD Tolerance(3)	Machine Model	200V
	Human Body Model	2000V
Supply Voltage (V^+–V^-)		6V
Differential Input Voltage		± Supply Voltage
Voltage at Input/Output Pins		V^++0.3V, V^- -0.3V
Storage Temperature Range		−65°C to 150°C
Junction Temperature(4)		150°C
For soldering specifications see product folder at www.ti.com and SNOA549		

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Operating Ratings(1)

Supply Voltage Range		1.8V to 5.5V
Temperature Range		−40°C to 125°C
Thermal Resistance (θ_{JA})	5-Pin SC70	414°C/W
	5-Pin SOT-23	265°C/W
	8-Pin VSSOP	235°C/W
	8-Pin SOIC	175°C/W
	14-Pin TSSOP	155°C/W
	14-Pin SOIC	127°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.

1.8V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 1.8V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes. See(1)

Symbol	Parameter	Condition		Min(2)	Typ(3)	Max(2)	Units
V_{OS}	Input Offset Voltage	LMV611 (Single)			1	4	mV
		LMV612 (Dual) LMV614 (Quad)			1	5.5	mV
TCV_{OS}	Input Offset Voltage Average Drift				5.5		µV/°C
I_B	Input Bias Current				15		nA
I_{OS}	Input Offset Current				13		nA
I_S	Supply Current (per channel)				103	185	µA
CMRR	Common Mode Rejection Ratio	LMV611, 0 ≤ V_{CM} ≤ 0.6V 1.4V ≤ V_{CM} ≤ 1.8V(4)		60	78		dB
		LMV612 and LMV614 0 ≤ V_{CM} ≤ 0.6V 1.4V ≤ V_{CM} ≤ 1.8V(4)		55	76		
		−0.2V ≤ V_{CM} ≤ 0V 1.8V ≤ V_{CM} ≤ 2.0V		50	72		
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V			100		dB
CMVR	Input Common-Mode Voltage Range	For CMRR Range ≥ 50dB	T_A = 25°C	V^- −0.2	−0.2 to 2.1	V^+ +0.2	V
			T_A −40°C to 85°C	V^-		V^+	
			T_A = 125°C	V^- +0.2		V^+ −0.2	
A_V	Large Signal Voltage Gain LMV611 (Single)	R_L = 600Ω to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V		77	101		dB
		R_L = 2kΩ to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V		80	105		
	Large Signal Voltage Gain LMV612 (Dual) LMV614 (Quad)	R_L = 600Ω to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V		75	90		dB
		R_L = 2kΩ to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V		78	100		
V_O	Output Swing	R_L = 600Ω to 0.9V V_{IN} = ±100mV		1.65	1.72		V
					0.077	0.105	
		R_L = 2kΩ to 0.9V V_{IN} = ±100mV		1.75	1.77		
					0.024	0.035	
I_O	Output Short Circuit Current(5)	Sourcing, V_O = 0V V_{IN} = 100mV			8		mA
		Sinking, V_O = 1.8V V_{IN} = −100mV			9		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See Applications section for information of temperature derating of the device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) For specified temperature ranges, see Input Common-Mode Voltage Range specifications.
(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45mA over long term may adversely affect reliability.

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 1.8V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes. See (1)

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
SR	Slew Rate	See (4)		0.35		V/µs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			67		deg
G_m	Gain Margin			7		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 0.5V		60		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		pA/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_{IN} = 1 V_{PP}		0.023		%
	Amp-to-Amp Isolation	See (5)		123		dB

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See Applications section for information of temperature derating of the device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(5) Input referred, R_L = 100kΩ connected to V^+/2. Each amp excited in turn with 1kHz to produce V_O = 3V_{PP} (For Supply Voltages <3V, V_O = V^+).

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes. See (1)

Symbol	Parameter	Condition	Min (2)	Typ (3)	Max (2)	Units
V_{OS}	Input Offset Voltage	LMV611 (Single)		1	4	mV
		LMV612 (Dual) LMV614 (Quad)		1	5.5	mV
TCV_{OS}	Input Offset Voltage Average Drift			5.5		µV/°C
I_B	Input Bias Current			15		nA
I_{OS}	Input Offset Current			8		nA
I_S	Supply Current (per channel)			105	190	µA
CMRR	Common Mode Rejection Ratio	LMV611, 0 ≤ V_{CM} ≤ 1.5V 2.3V ≤ V_{CM} ≤ 2.7V (4)	60	81		dB
		LMV612 and LMV614 0 ≤ V_{CM} ≤ 1.5V 2.3V ≤ V_{CM} ≤ 2.7V (4)	55	80		
		−0.2V ≤ V_{CM} ≤ 0V 2.7V ≤ V_{CM} ≤ 2.9V	50	74		
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V V_{CM} = 0.5V		100		dB

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See Applications section for information of temperature derating of the device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) For specified temperature ranges, see Input Common-Mode Voltage Range specifications.

2.7V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes. See(1)

Symbol	Parameter	Condition		Min(2)	Typ(3)	Max(2)	Units
V_{CM}	Input Common-Mode Voltage Range	For CMRR Range ≥ 50dB	T_A = 25°C	V^- −0.2	−0.2 to 3.0	V^+ +0.2	V
			T_A = −40°C to 85°C	V^-		V^+	
			T_A = 125°C	V^- +0.2		V^+ −0.2	
A_V	Large Signal Voltage Gain LMV611 (Single)	R_L = 600Ω to 1.35V, V_O = 0.2V to 2.5V		87	104		dB
		R_L = 2kΩ to 1.35V, V_O = 0.2V to 2.5V		92	110		
	Large Signal Voltage Gain LMV612 (Dual) LMV614 (Quad)	R_L = 600Ω to 1.35V, V_O = 0.2V to 2.5V		78	90		dB
		R_L = 2kΩ to 1.35V, V_O = 0.2V to 2.5V		81	100		
V_O	Output Swing	R_L = 600Ω to 1.35V V_{IN} = ±100mV		2.55	2.62		V
					0.083	0.110	
		R_L = 2kΩ to 1.35V V_{IN} = ±100mV		2.65	2.675		
					0.025	0.04	
I_O	Output Short Circuit Current(5)	Sourcing, V_O = 0V V_{IN} = 100mV			30		mA
		Sinking, V_O = 0V V_{IN} = −100mV			25		

(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45mA over long term may adversely affect reliability.

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes. See(1)

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
SR	Slew Rate	See(4)		0.4		V/µs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			70		deg
G_m	Gain Margin			7.5		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 0.5V		57		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		pA/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_{IN} = $1V_{PP}$		0.022		%
	Amp-to-Amp Isolation	See(5)		123		dB

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. See Applications section for information of temperature derating of the device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(5) Input referred, R_L = 100kΩ connected to V^+/2. Each amp excited in turn with 1kHz to produce V_O = $3V_{PP}$ (For Supply Voltages <3V, V_O = V^+).

5V DC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 5V, V^- = 0V, $V_{CM} = V^+/2$, $V_O = V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes. See(1)

Symbol	Parameter	Condition		Min(2)	Typ(3)	Max(2)	Units
V_{OS}	Input Offset Voltage	LMV611 (Single)			1	4	mV
		LMV612 (Dual) LMV614 (Quad)			1	5.5	mV
TCV_{OS}	Input Offset Voltage Average Drift				5.5		µV/°C
I_B	Input Bias Current				14	35	nA
I_{OS}	Input Offset Current				9		nA
I_S	Supply Current (per channel)				116	210	µA
CMRR	Common Mode Rejection Ratio	$0 \le V_{CM} \le 3.8V$ $4.6V \le V_{CM} \le 5.0V$(4)		60	86		dB
		$-0.2V \le V_{CM} \le 0V$ $5.0V \le V_{CM} \le 5.2V$		50	78		
PSRR	Power Supply Rejection Ratio	$1.8V \le V^+ \le 5V$ V_{CM} = 0.5V			100		dB
CMVR	Input Common-Mode Voltage Range	For CMRR Range ≥ 50dB	T_A = 25°C	V^- −0.2	−0.2 to 5.3	V^+ +0.2	V
			T_A = −40°C to 85°C	V^-		V^+	
			T_A = 125°C	V^- +0.3		V^+ −0.3	
A_V	Large Signal Voltage Gain LMV611 (Single)	R_L = 600Ω to 2.5V, V_O = 0.2V to 4.8V		88	102		dB
		R_L = 2kΩ to 2.5V, V_O = 0.2V to 4.8V		94	113		
	Large Signal Voltage Gain LMV612 (Dual) LMV614 (Quad)	R_L = 600Ω to 2.5V, V_O = 0.2V to 4.8V		81	90		dB
		R_L = 2kΩ to 2.5V, V_O = 0.2V to 4.8V		85	100		
V_O	Output Swing	R_L = 600Ω to 2.5V V_{IN} = ±100mV		4.855	4.890		V
					0.120	0.160	
		R_L = 2kΩ to 2.5V V_{IN} = ±100mV		4.945	4.967		
					0.037	0.065	
I_O	Output Short Circuit Current(5)	LMV611, Sourcing, V_O = 0V V_{IN} = 100mV			100		mA
		Sinking, V_O = 5V V_{IN} = −100mV			65		

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. See Applications section for information of temperature derating of the device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

(2) All limits are specified by testing or statistical analysis.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

(4) For specified temperature ranges, see Input Common-Mode Voltage Range specifications.

(5) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45mA over long term may adversely affect reliability.

5V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C. V^+ = 5V, V^- = 0V, $V_{CM} = V^+/2$, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes. See(1)

Symbol	Parameter	Conditions	Min(2)	Typ(3)	Max(2)	Units
SR	Slew Rate	See(4)		0.42		V/µs
GBW	Gain-Bandwidth Product			1.5		MHz
Φ_m	Phase Margin			71		deg
G_m	Gain Margin			8		dB
e_n	Input-Referred Voltage Noise	f = 10 kHz, V_{CM} = 1V		50		nV/√Hz
i_n	Input-Referred Current Noise	f = 10 kHz		0.08		pA/√Hz
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_O = 1V_{PP}		0.022		%
	Amp-to-Amp Isolation	See(5)		123		dB

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No assurance of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. See Applications section for information of temperature derating of the device. Absolute Maximum Ratings indicated junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) All limits are specified by testing or statistical analysis.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Connected as voltage follower with input step from V^- to V^+. Number specified is the slower of the positive and negative slew rates.
(5) Input referred, R_L = 100kΩ connected to $V^+/2$. Each amp excited in turn with 1kHz to produce $V_O = 3V_{PP}$ (For Supply Voltages <3V, $V_O = V^+$).

Connection Diagrams

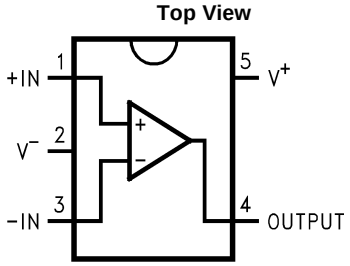


Figure 1. 5-Pin SC70/SOT-23 (LMV611)
See Package Numbers DCK and DBV

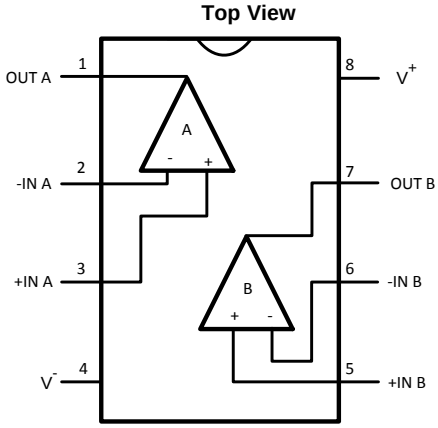


Figure 2. 8-Pin VSSOP/SOIC (LMV612)
See Package Numbers DGK and D

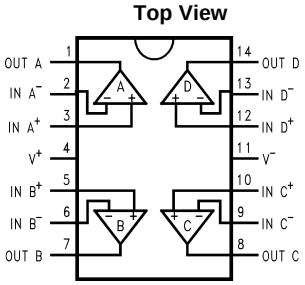


Figure 3. 14-Pin TSSOP/SOIC (LMV614)
See Package Numbers PW and D

Typical Performance Characteristics

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Supply Current vs. Supply Voltage (LMV611)

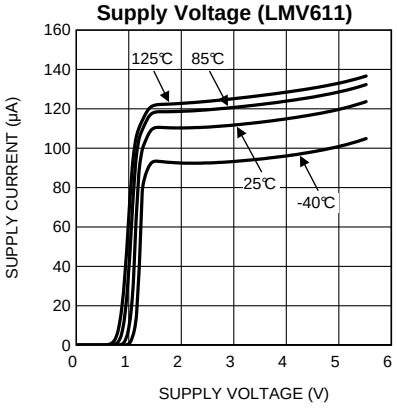


Figure 4.

Sourcing Current vs. Output Voltage

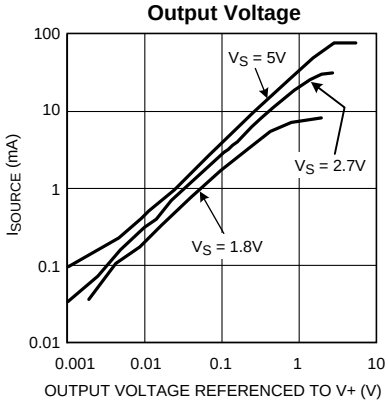


Figure 5.

Sinking Current vs. Output Voltage

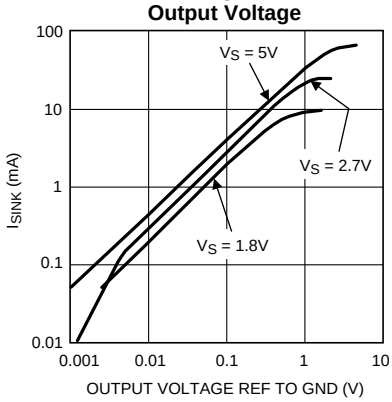


Figure 6.

Output Voltage Swing vs. Supply Voltage

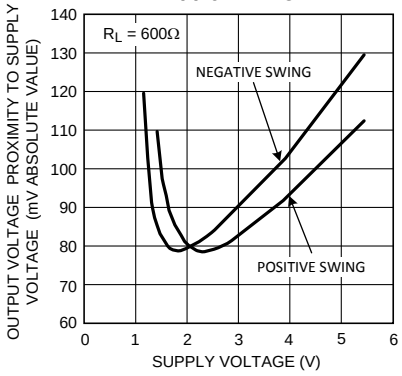


Figure 7.

Output Voltage Swing vs. Supply Voltage

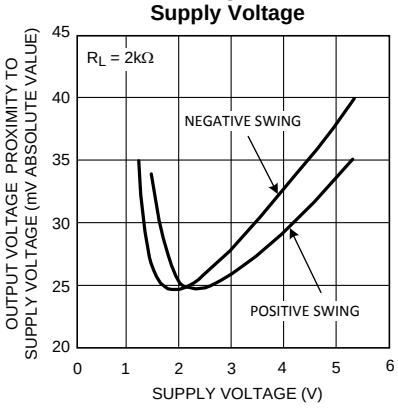


Figure 8.

Gain and Phase vs. Frequency

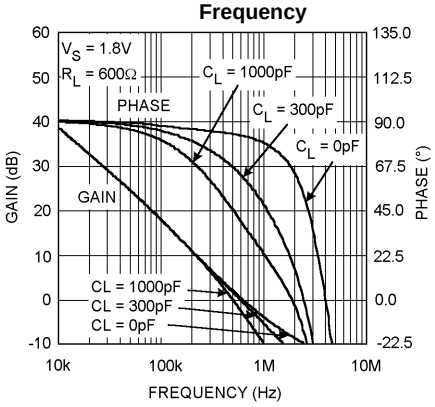


Figure 9.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Gain and Phase vs. Frequency

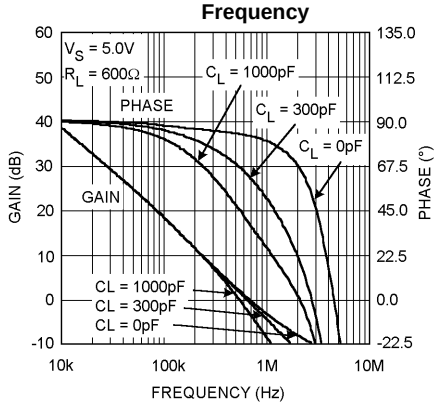


Figure 10.

Gain and Phase vs. Frequency

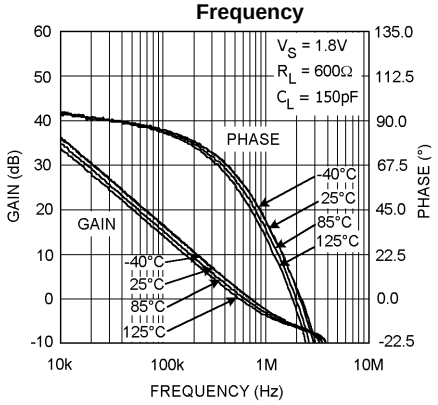


Figure 11.

Gain and Phase vs. Frequency

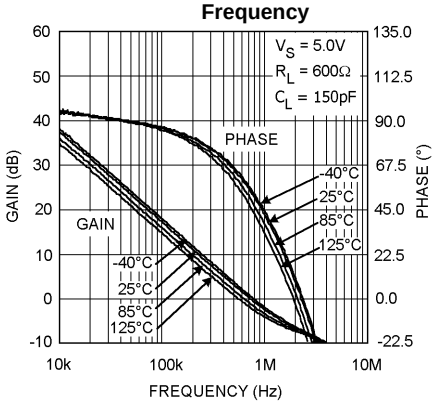


Figure 12.

CMRR vs. Frequency

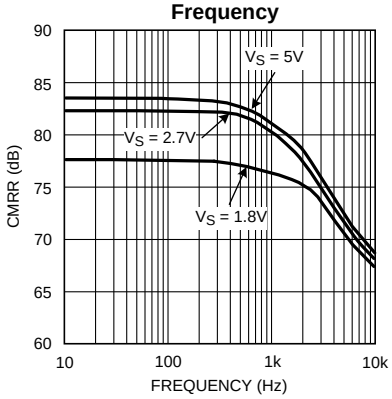


Figure 13.

PSRR vs. Frequency

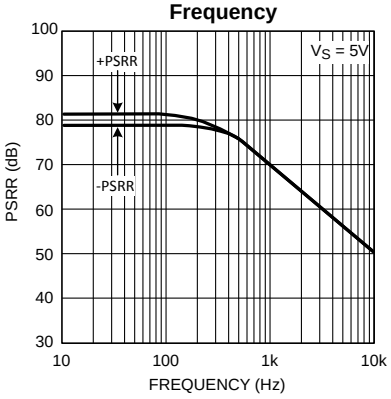


Figure 14.

Input Voltage Noise vs. Frequency

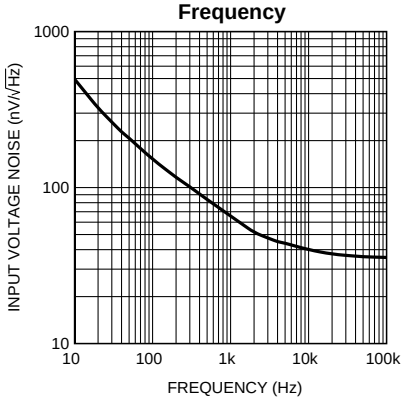


Figure 15.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Input Current Noise vs. Frequency

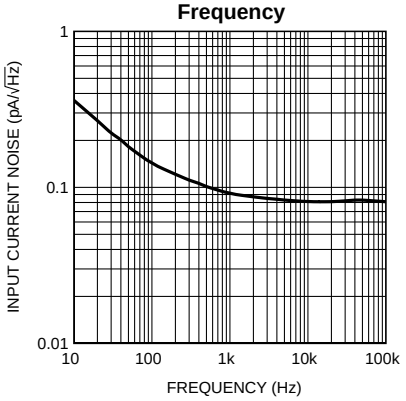


Figure 16.

THD vs. Frequency

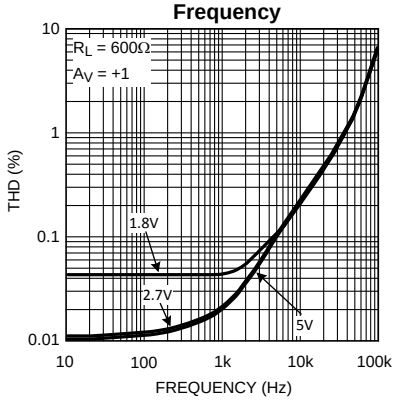


Figure 17.

THD vs. Frequency

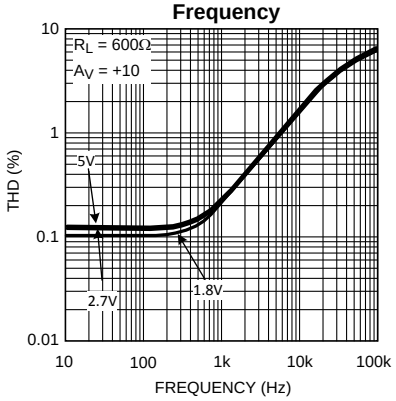


Figure 18.

Slew Rate vs. Supply Voltage

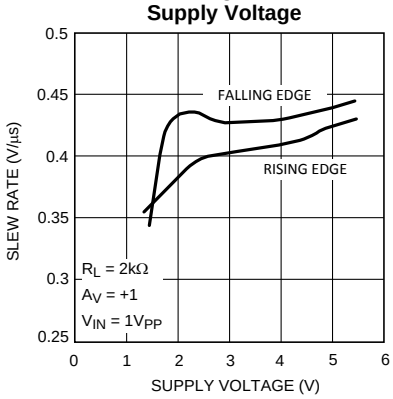


Figure 19.

Small Signal Non-Inverting Response

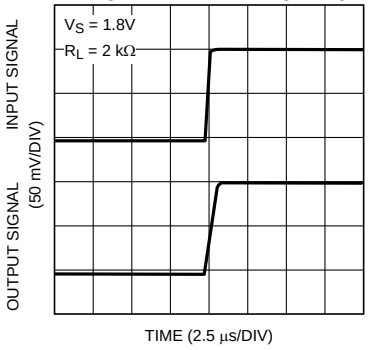


Figure 20.

Small Signal Non-Inverting Response

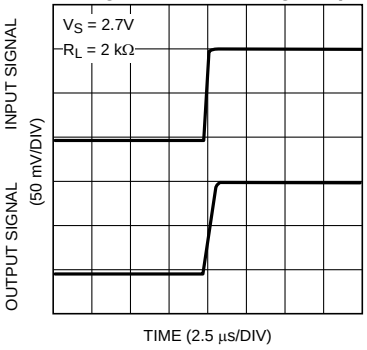


Figure 21.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Small Signal Non-Inverting Response

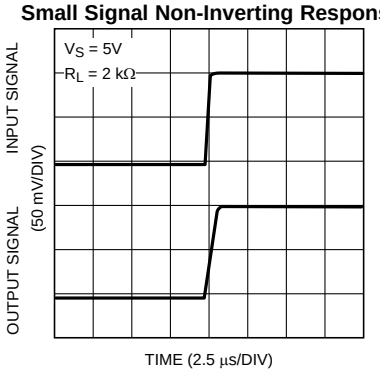


Figure 22.

Large Signal Non-Inverting Response

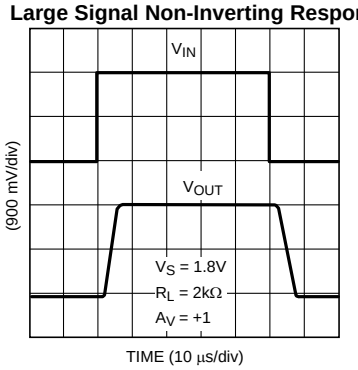


Figure 23.

Large Signal Non-Inverting Response

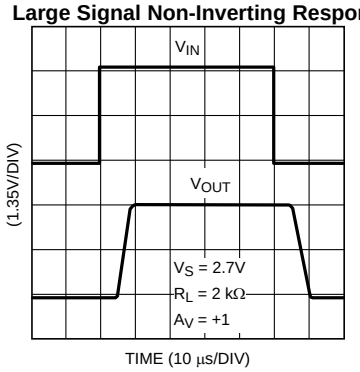


Figure 24.

Large Signal Non-Inverting Response

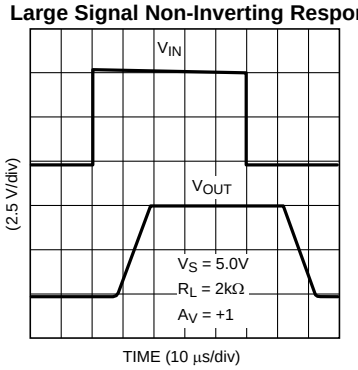


Figure 25.

Short Circuit Current vs. Temperature (Sinking)

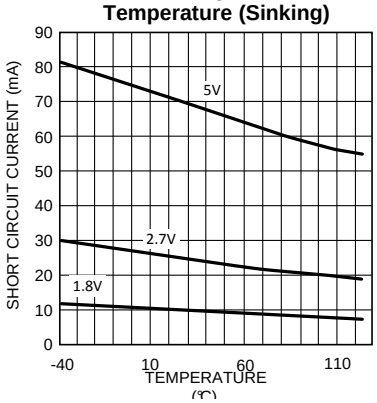


Figure 26.

Short Circuit Current vs. Temperature (Sourcing)

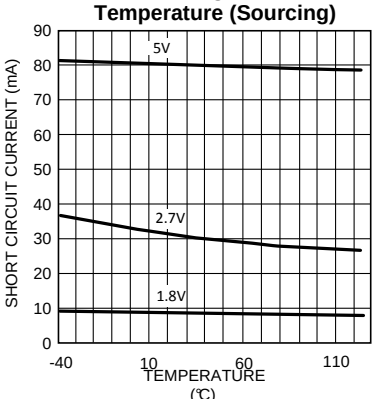


Figure 27.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_S = +5V, single supply, T_A = 25°C.

Offset Voltage vs. Common Mode Range

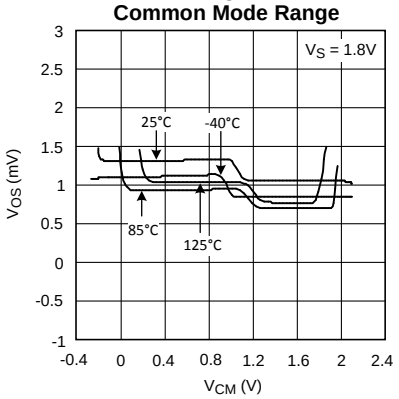


Figure 28.

Offset Voltage vs. Common Mode Range

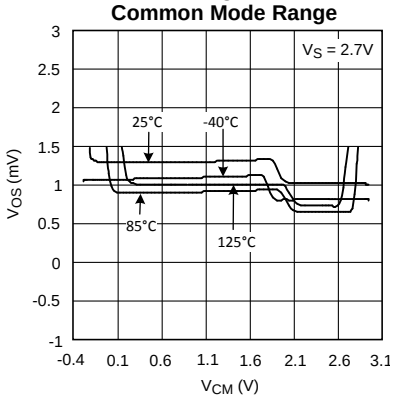


Figure 29.

Offset Voltage vs. Common Mode Range

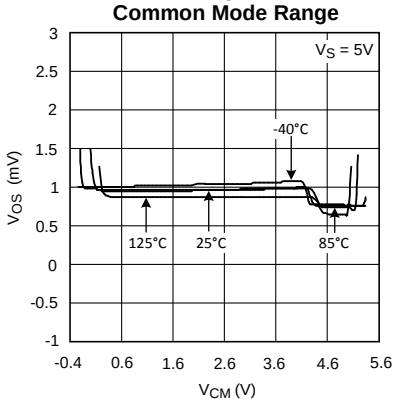


Figure 30.

APPLICATION NOTE

INPUT AND OUTPUT STAGE

The rail-to-rail input stage of this family provides more flexibility for the designer. The LMV611/LMV612/LMV614 use a complimentary PNP and NPN input stage in which the PNP stage senses common mode voltage near V^- and the NPN stage senses common mode voltage near V^+. The transition from the PNP stage to NPN stage occurs 1V below V^+. Since both input stages have their own offset voltage, the offset of the amplifier becomes a function of the input common mode voltage and has a crossover point at 1V below V^+.

This V_{OS} crossover point can create problems for both DC and AC coupled signals if proper care is not taken. Large input signals that include the V_{OS} crossover point will cause distortion in the output signal. One way to avoid such distortion is to keep the signal away from the crossover. For example, in a unity gain buffer configuration and with V_S = 5V, a 5V peak-to-peak signal will contain input-crossover distortion while a 3V peak-to-peak signal centered at 1.5V will not contain input-crossover distortion as it avoids the crossover point. Another way to avoid large signal distortion is to use a gain of −1 circuit which avoids any voltage excursions at the input terminals of the amplifier. In that circuit, the common mode DC voltage can be set at a level away from the V_{OS} cross-over point. For small signals, this transition in V_{OS} shows up as a V_{CM} dependent spurious signal in series with the input signal and can effectively degrade small signal parameters such as gain and common mode rejection ratio. To resolve this problem, the small signal should be placed such that it avoids the V_{OS} crossover point. In addition to the rail-to-rail performance, the output stage can provide enough output current to drive 600Ω loads. Because of the high current capability, care should be taken not to exceed the 150°C maximum junction temperature specification.

INPUT BIAS CURRENT CONSIDERATION

The LMV611/LMV612/LMV614 family has a complementary bipolar input stage. The typical input bias current (I_B) is 15nA. The input bias current can develop a significant offset voltage. This offset is primarily due to I_B flowing through the negative feedback resistor, R_F. For example, if I_B is 50nA and R_F is 100kΩ, then an offset voltage of 5mV will develop ($V_{OS} = I_B \times R_F$). Using a compensation resistor (R_C), as shown in Figure 31, cancels this effect. But the input offset current (I_{OS}) will still contribute to an offset voltage in the same manner.

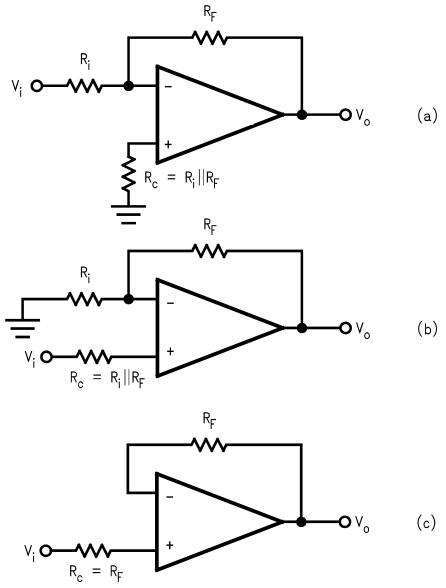


Figure 31. Canceling the Offset Voltage due to Input Bias Current

Typical Applications

HIGH SIDE CURRENT SENSING

The high side current sensing circuit (Figure 32) is commonly used in a battery charger to monitor charging current to prevent over charging. A sense resistor R_{SENSE} is connected to the battery directly. This system requires an op amp with rail-to-rail input. The LMV611/LMV612/LMV614 are ideal for this application because its common mode input range goes up to the rail.

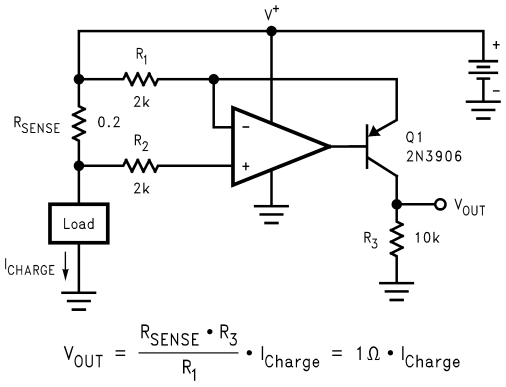


Figure 32. High Side Current Sensing

HALF-WAVE RECTIFIER WITH RAIL-TO-GROUND OUTPUT SWING

Since the LMV611/LMV612/LMV614 input common mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction is an easy task. All that is needed are two external resistors; there is no need for diodes or matched resistors. The half wave rectifier can have either positive or negative going outputs, depending on the way the circuit is arranged.

In Figure 33 the circuit is referenced to ground, while in Figure 34 the circuit is biased to the positive supply. These configurations implement the half wave rectifier since the LMV611/LMV612/LMV614 can not respond to one-half of the incoming waveform. It can not respond to one-half of the incoming because the amplifier can not swing the output beyond either rail therefore the output disengages during this half cycle. During the other half cycle, however, the amplifier achieves a half wave that can have a peak equal to the total supply voltage. R_I should be large enough not to load the LMV611/LMV612/LMV614.

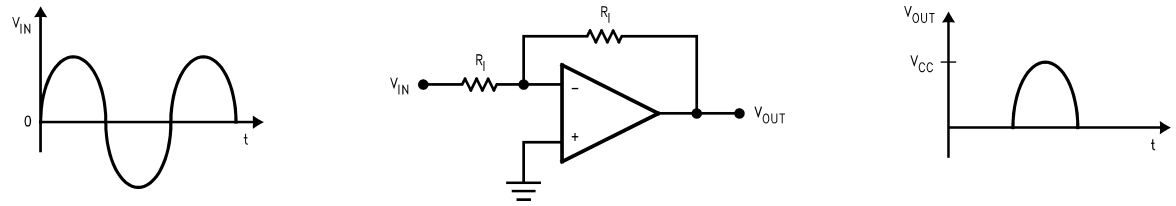


Figure 33. Half-Wave Rectifier with Rail-To-Ground Output Swing Referenced to Ground

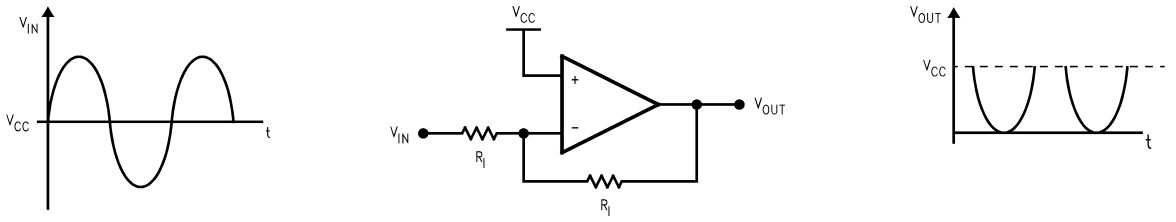


Figure 34. Half-Wave Rectifier with Negative-Going Output Referenced to V_{CC}

INSTRUMENTATION AMPLIFIER WITH RAIL-TO-RAIL INPUT AND OUTPUT

Some manufactures make a non-“rail-to-rail”-op amp rail-to-rail by using a resistive divider on the inputs. The resistors divide the input voltage to get a rail-to-rail input range. The problem with this method is that it also divides the signal, so in order to get the obtained gain, the amplifier must have a higher closed loop gain. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMRR as well. The LMV611/LMV612/LMV614 is rail-to-rail and therefore doesn't have these disadvantages.

Using three of the LMV611/LMV612/LMV614 amplifiers, an instrumentation amplifier with rail-to-rail inputs and outputs can be made as shown in Figure 35.

In this example, amplifiers on the left side act as buffers to the differential stage. These buffers assure that the input impedance is very high and require no precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMRR set by the matching R_1-R_2 with R_3-R_4. The gain is set by the ratio of R_2/R_1 and R_3 should equal R_1 and R_4 equal R_2. With both rail-to-rail input and output ranges, the input and output are only limited by the supply voltages. Remember that even with rail-to-rail outputs, the output can not swing past the supplies so the combined common mode voltages plus the signal should not be greater that the supplies or limiting will occur. For additional applications, see the following TI application reports:

- AN-29 Application Report (SNOA624)
- AN-31 Application Report (SNLA140)
- AN-71 Application Report (SNOA652)
- AN-127 Application Report (SNVA516)

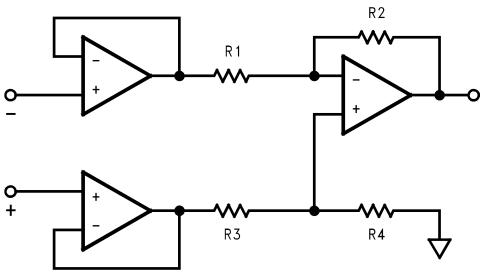
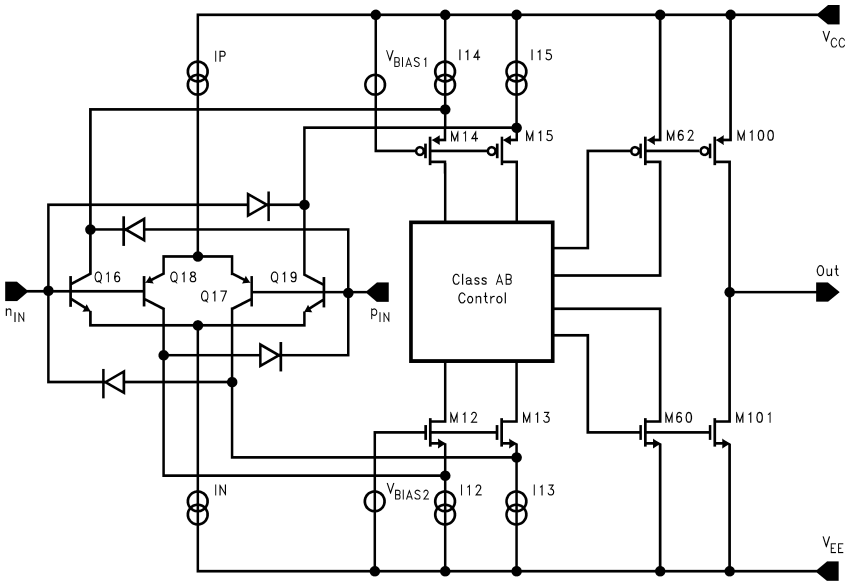


Figure 35. Rail-to-rail Instrumentation Amplifier

Simplified Schematic



REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV611MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AE9A	Samples
LMV611MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AE9A	Samples
LMV611MG/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AVA	Samples
LMV611MGX/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AVA	Samples
LMV612MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV6 12MA	Samples
LMV612MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV6 12MA	Samples
LMV612MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAUAG | CU SN	Level-1-260C-UNLIM	-40 to 125	AD9A	Samples
LMV612MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU NIPDAUAG | CU SN	Level-1-260C-UNLIM	-40 to 125	AD9A	Samples
LMV614MA/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV614MA	Samples
LMV614MAX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMV614MA	Samples
LMV614MT/NOPB	ACTIVE	TSSOP	PW	14	94	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LMV61 4MT	Samples
LMV614MTX/NOPB	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LMV61 4MT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

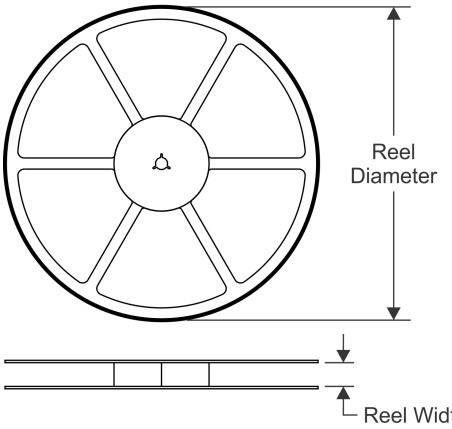
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

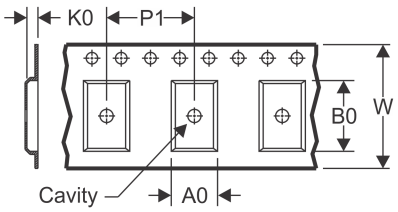
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

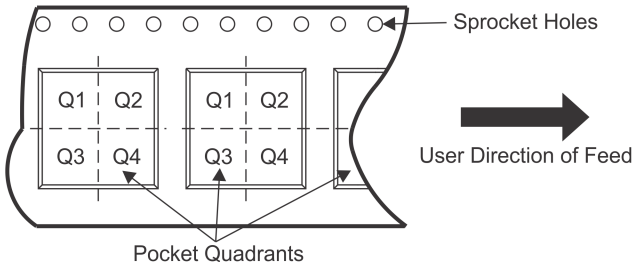


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

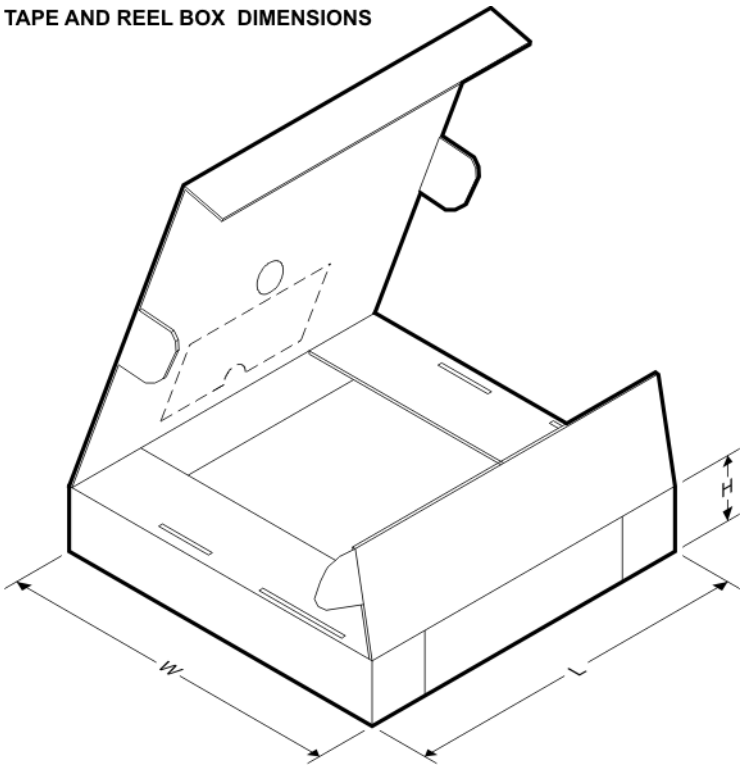
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV611MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV611MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV611MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV611MGX/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV612MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV612MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV612MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV614MAX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LMV614MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
LMV614MTX/NOPB	TSSOP	PW	14	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

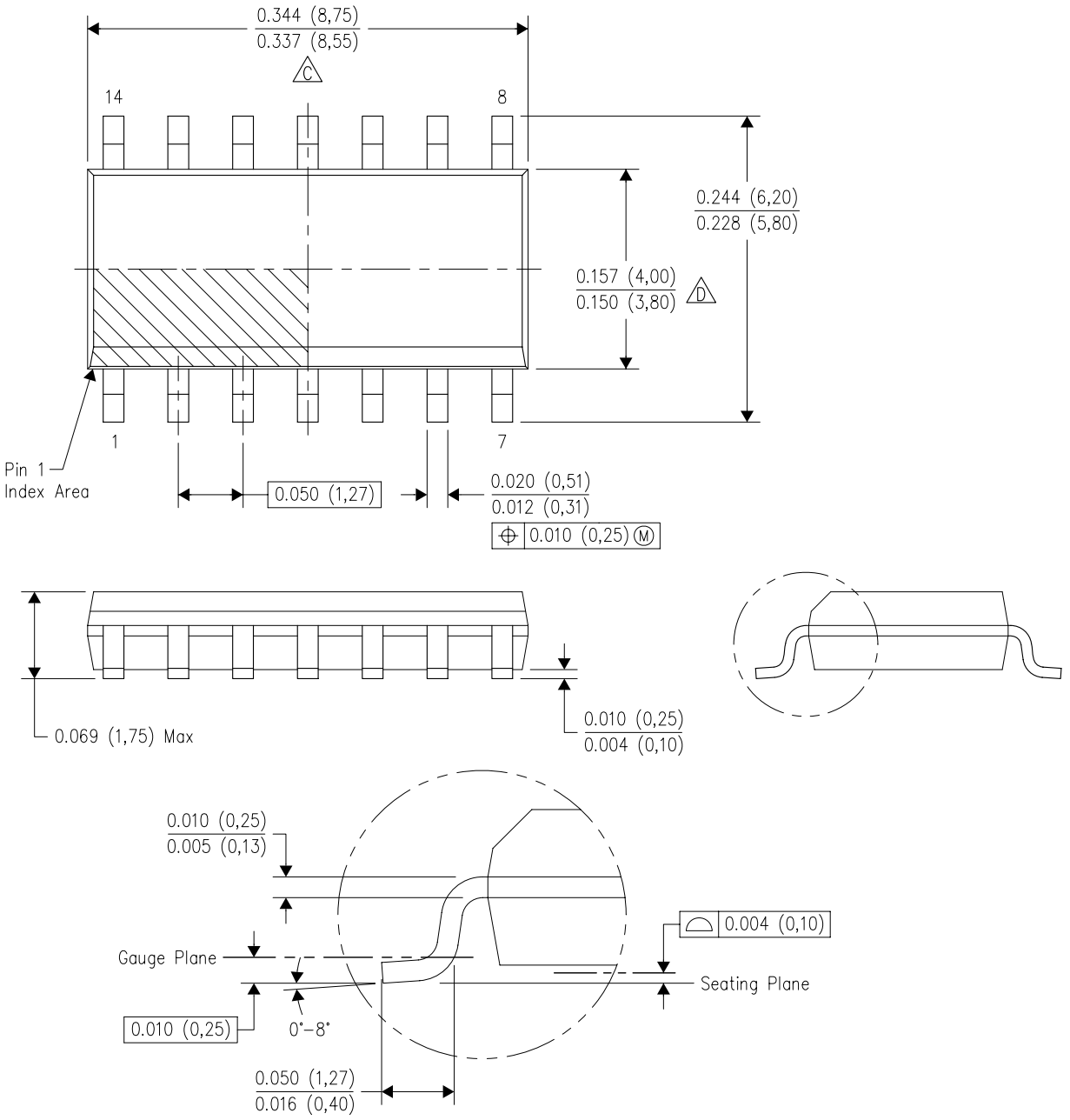
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV611MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV611MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV611MG/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV611MGX/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV612MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMV612MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV612MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV614MAX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LMV614MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0
LMV614MTX/NOPB	TSSOP	PW	14	2500	367.0	367.0	35.0

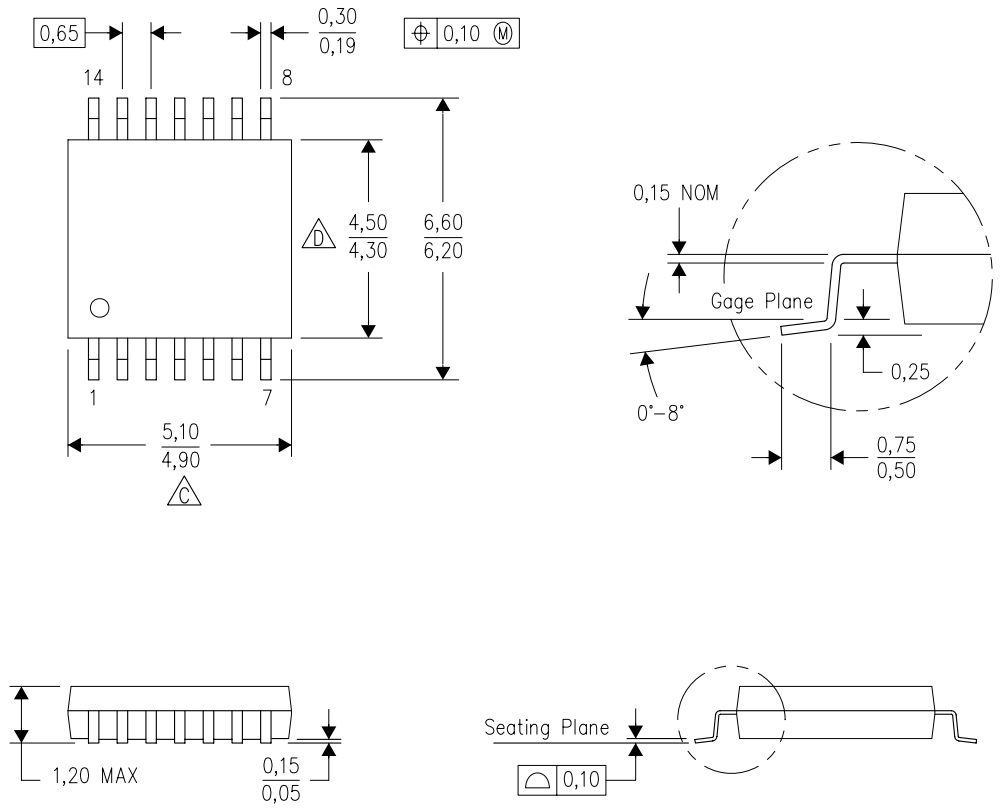
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

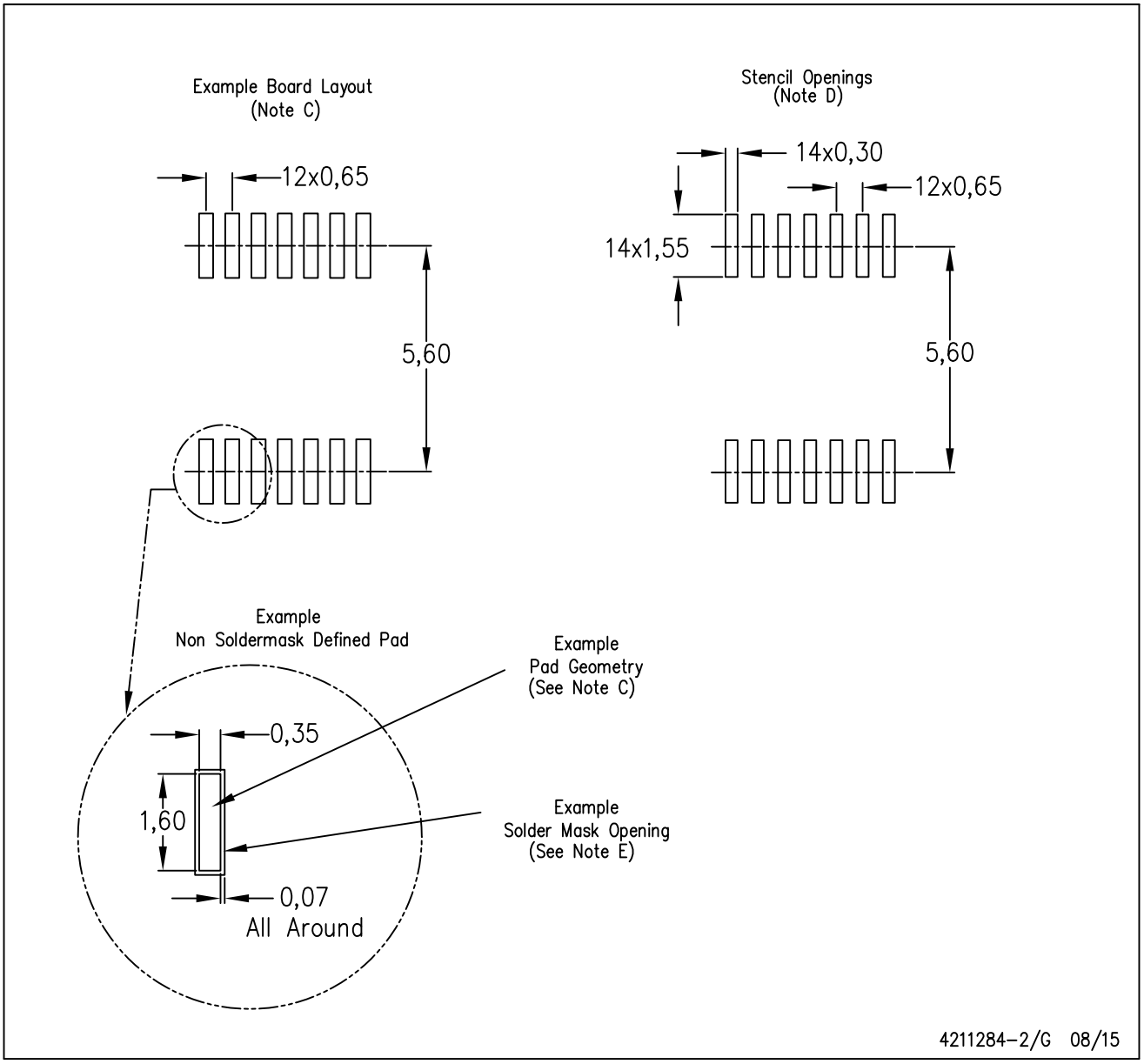
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

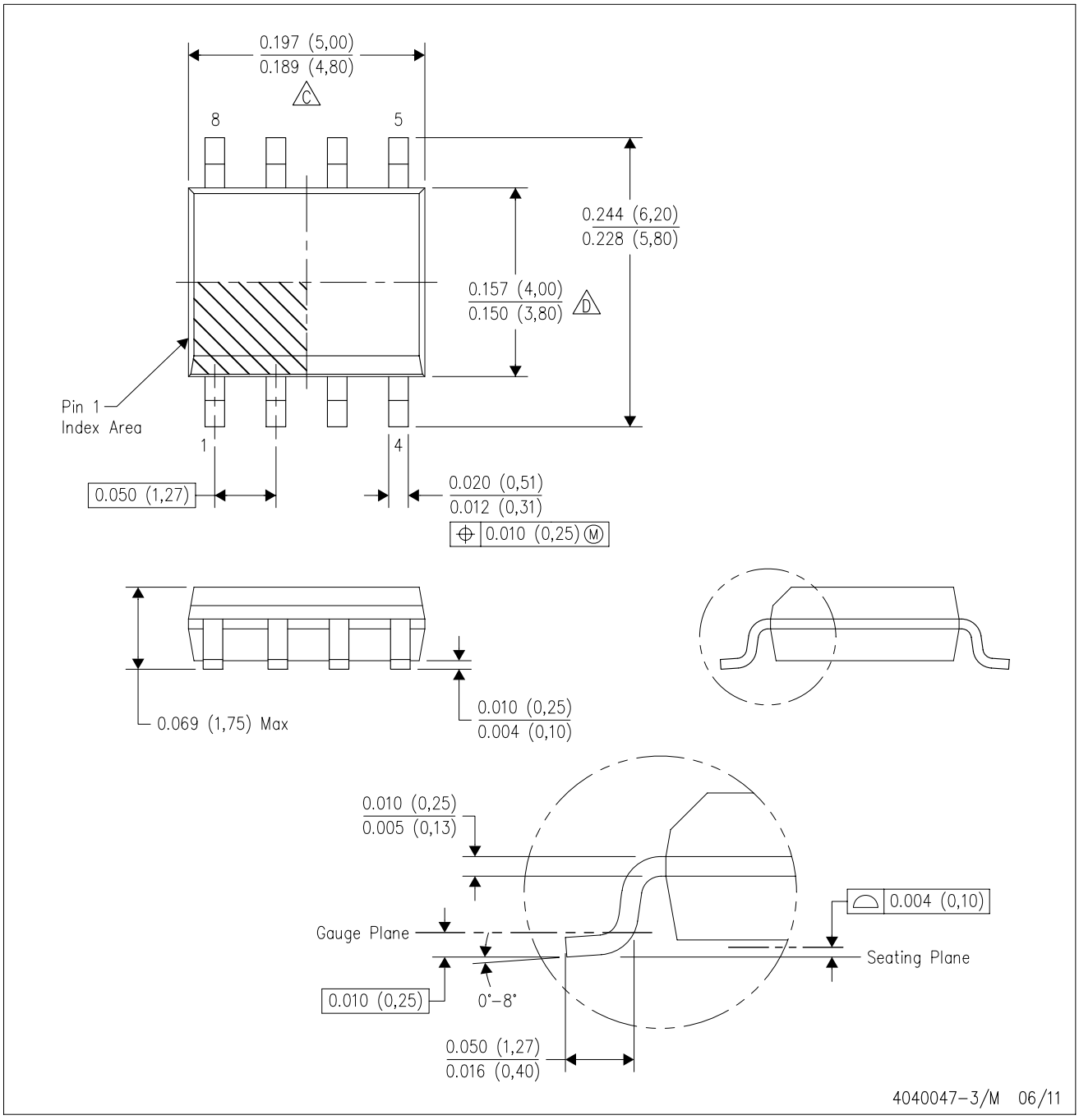
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



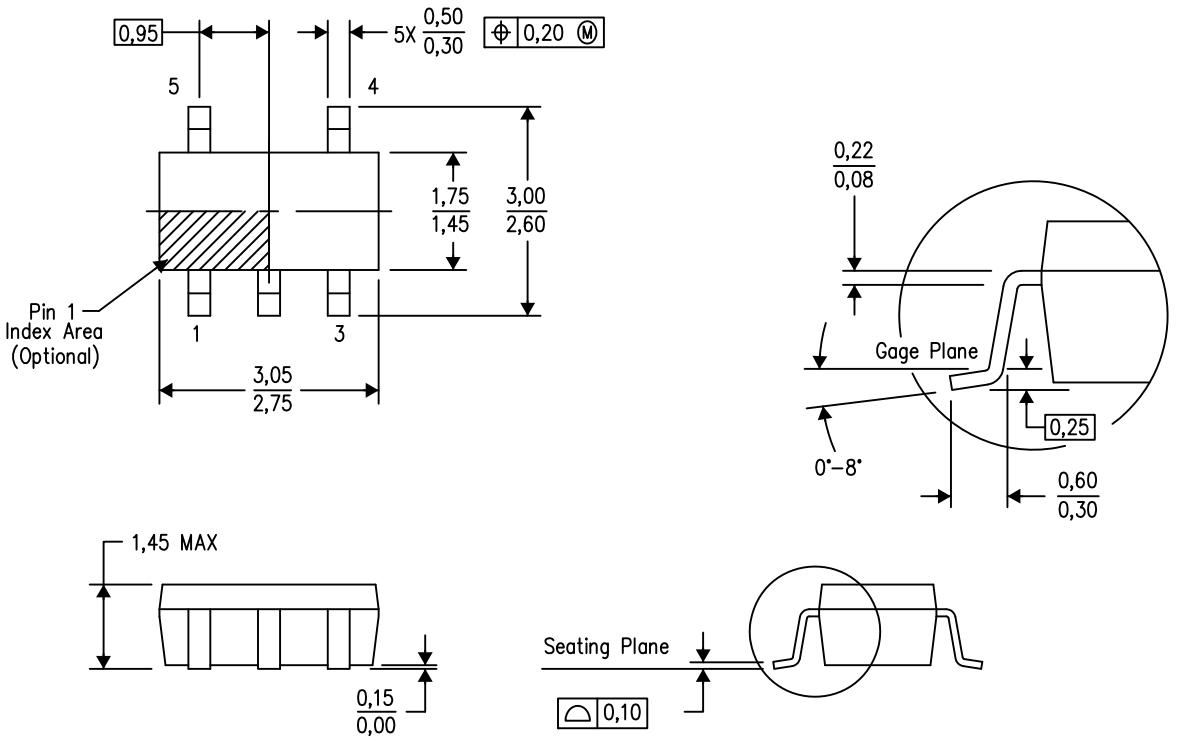
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

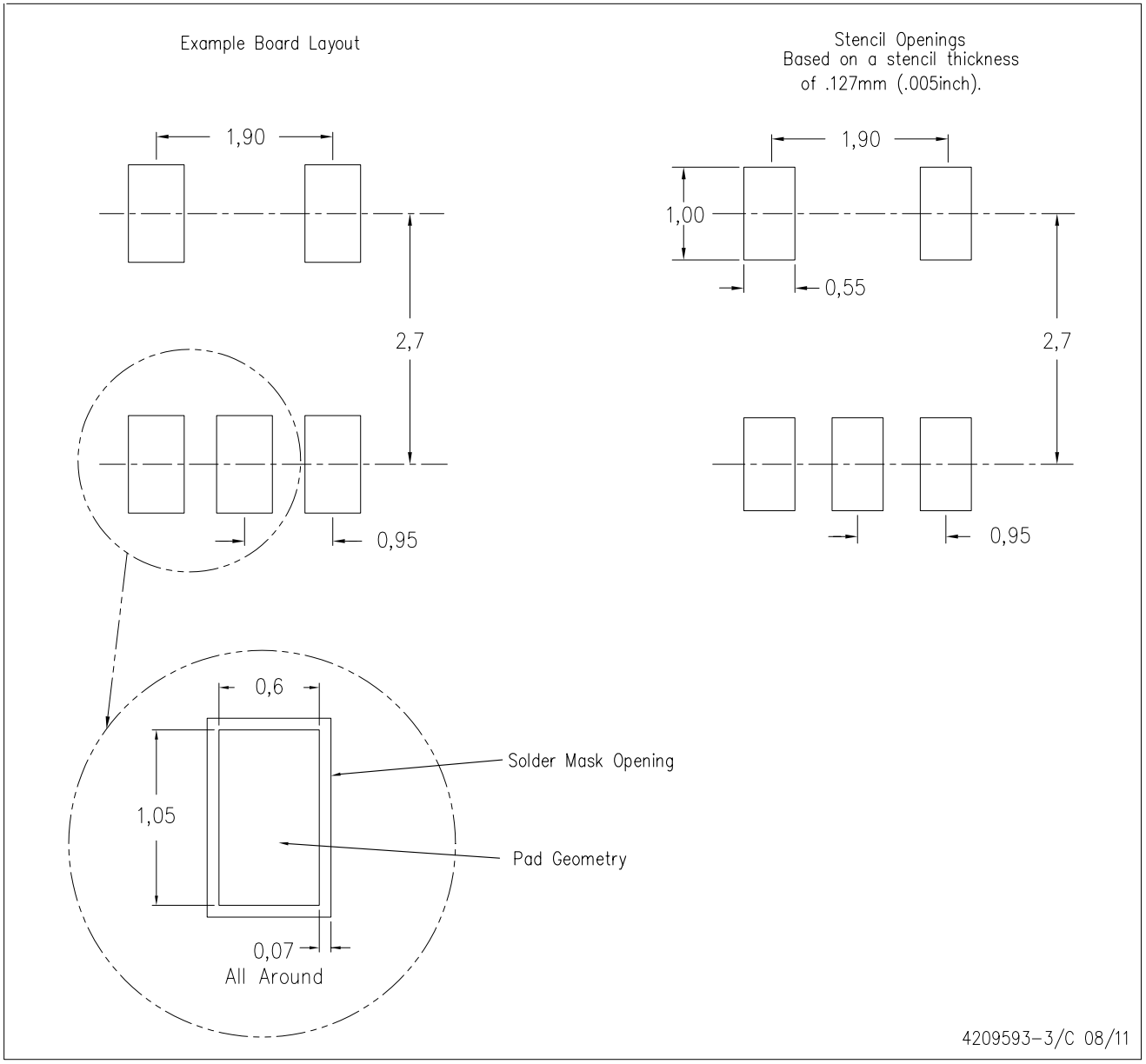
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

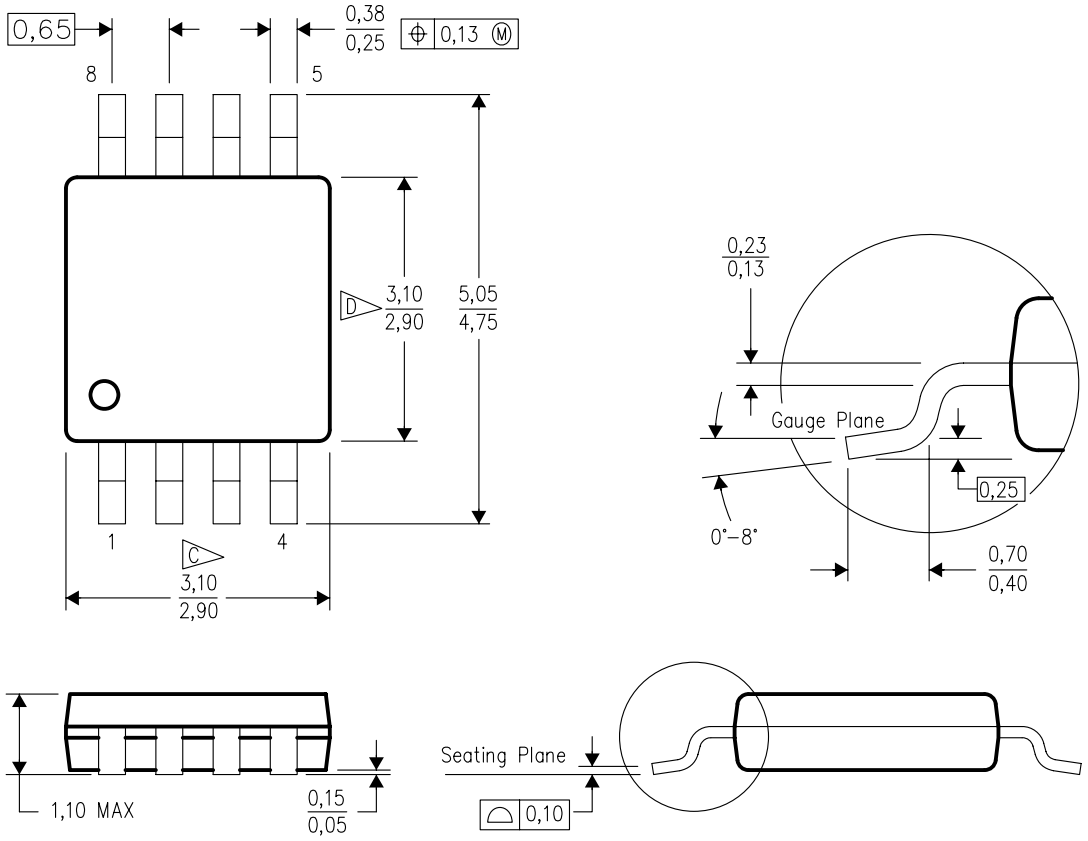
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

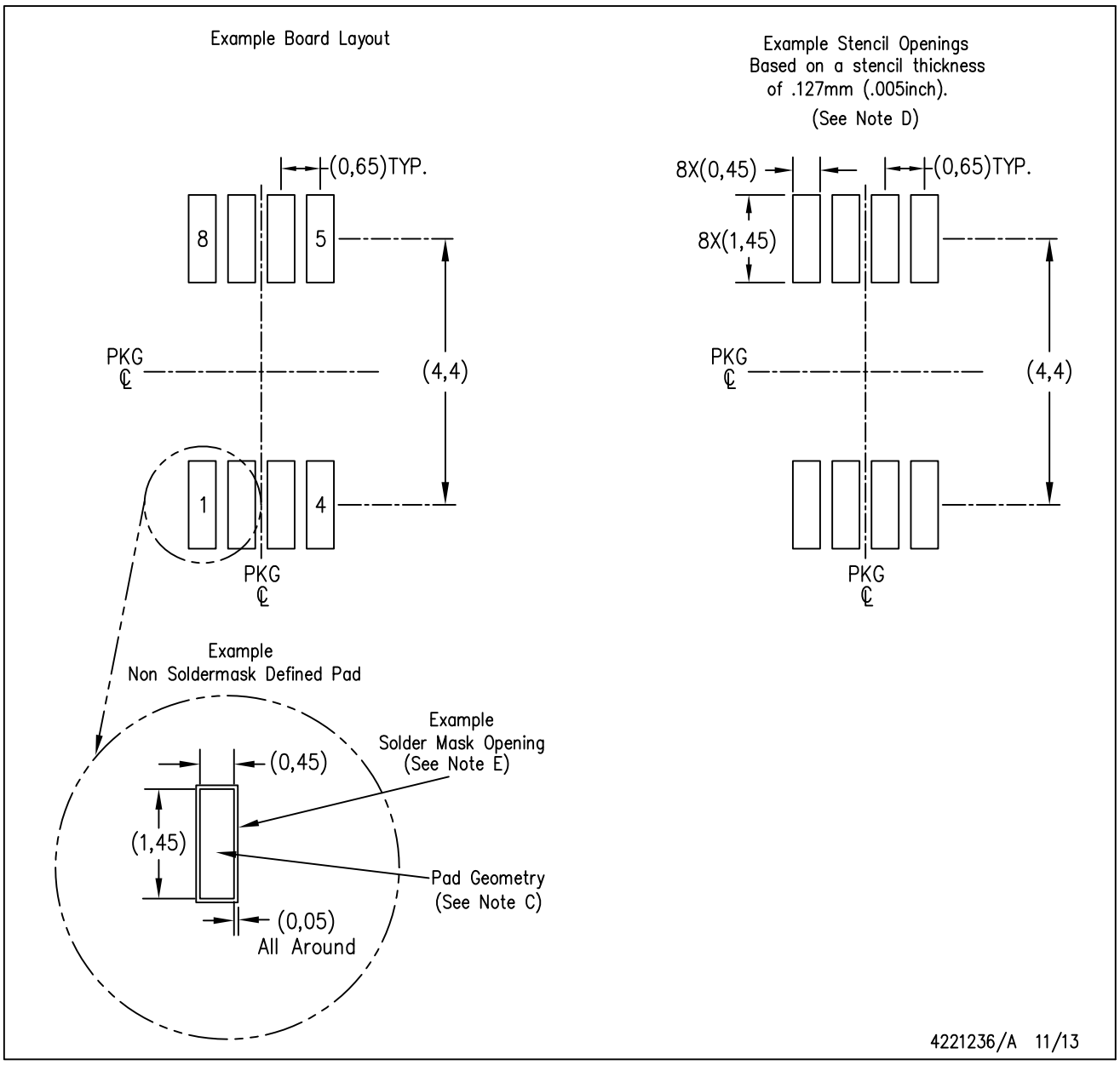
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

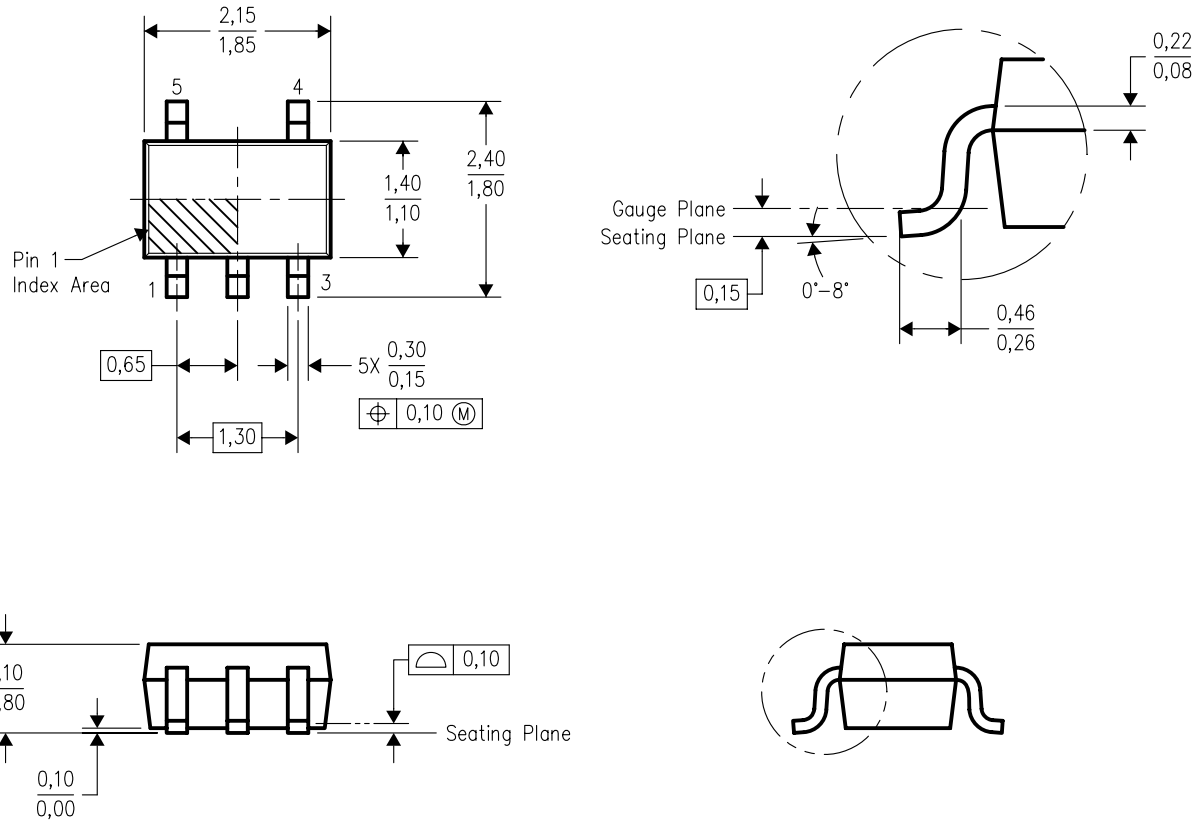
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

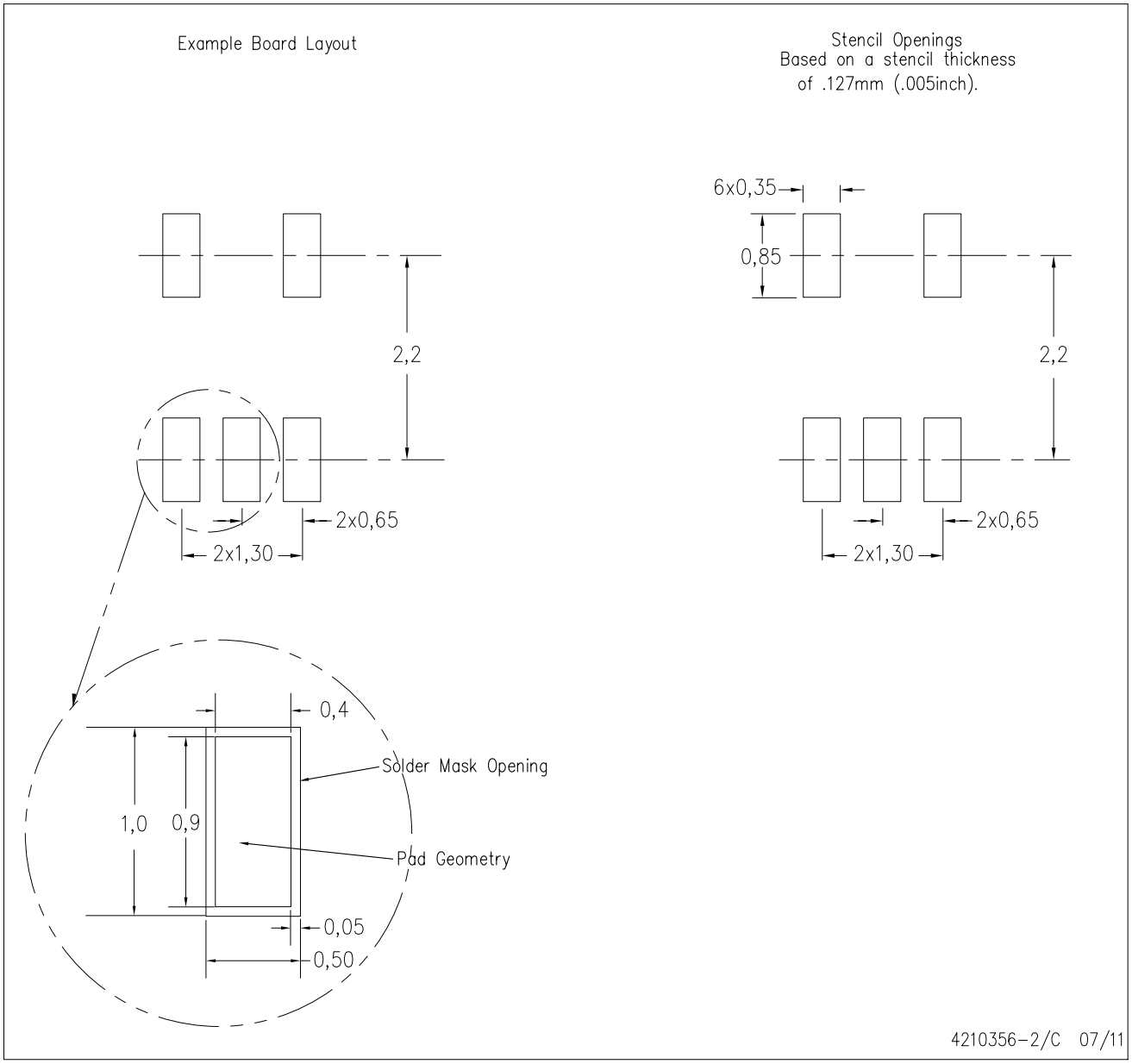
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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