TPS6115x Dual-Output Boost WLED Driver Using Single Inductor

1 Features

- 2.5-V to 6-V Input Voltage Range
- Two Outputs Each up to 27 V
- 0.7-A Integrated Switch
- Built-In Power Diode
- 1.2-MHz Fixed PWM Frequency
- Individually Programmable Output Current
- Input-to-Output Isolation
- Built-In Soft Start
- Overvoltage Protection
- Up to 83% Efficiency
- Up to 30-kHz PWM Dimming Frequency

2 Applications

- Sub- and Main-Display Backlight in Clamshell Phones
- Display and Keypad Backlight
- Up to 14-WLED Driver

3 Description

The TPS6115x is a high-frequency boost converter with two regulated current outputs for driving WLEDs. Each current output can be individually programmed through external resistors. There is a dedicated selection pin for each output so the two outputs can be turned on separately or simultaneously. The output current can be reduced by a pulse width modulation (PWM) signal on SEL pins or an analog voltage on the ISET pins, resulting in PWM dimming of the WLEDs. The boost regulator runs at a 1.2-MHz fixed switching frequency to reduce output ripple and avoid audible noises associated with pulse frequency modulation (PFM) control.

The two current outputs are ideal for driving WLED backlights for the sub and main displays in clamshell phones. The two outputs can also be used for driving display and keypad backlights. When used together, the two outputs can drive up to 14 WLEDs for one large display.

In addition to the small inductor, small capacitor, and 3-mm × 3-mm VSON package, the built-in MOSFET and diode eliminate the need for any external power devices. Overall, the device provides an extremely compact solution with high efficiency and plenty of flexibility.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61150 TPS61151	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

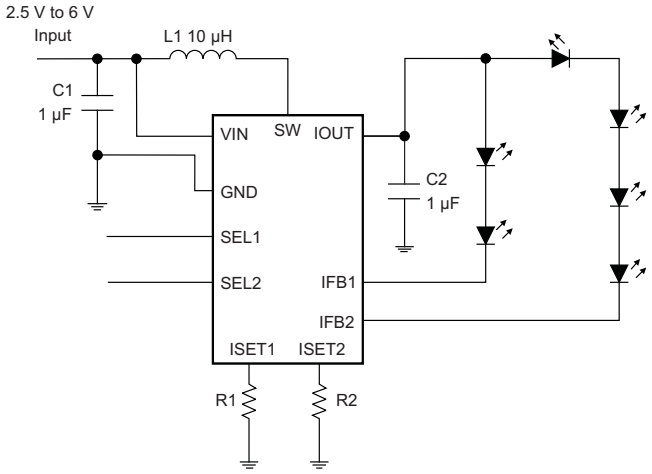

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Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2009) to Revision E — **Page**

- Changed "QFN" package to "VSON" throughout document ... 1
- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* and *Thermal Information* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Deleted obsolete *Dissipation Ratings* table ... 5

Changes from Revision C (November 2008) to Revision D — **Page**

- Deleted *Lead temperature* specification from *Absolute Maximum Ratings* table ... 4
- Corrected FET error in Figure 9 ... 11

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5 Device Comparison Tables

Table 1. OVP Options

T_A	PACKAGE(1)	OVP (TYPICAL)	PACKAGE MARKING
–40 to +85°C	TPS61150DRCR	28 V	BCQ
–40 to +85°C	TPS61151DRCR	22 V	BRH
–40 to +85°C	TPS61150DRCT	28 V	BCQ
–40 to +85°C	TPS61151DRCT	22 V	BRH

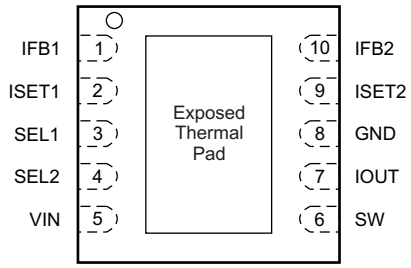
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

Table 2. TPS6115x Mode Selection

SEL1	SEL2	IFB1	IFB2
H	L	Enable	Disable
L	H	Disable	Enable
H	H	Enable	Enable
L	L	Device shutdown	

6 Pin Configuration and Functions

DRC Package
10-Pin VSON With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1, 10	IFB1, IFB2	I	The return path for the I_{OUT} regulation. Current regulator is connected to this pin, and it can be disabled to open the current path.
2, 9	ISET1, ISET2	I	Output current programming pins. The resistor connected to the pin programs its corresponding output current.
3, 4	SEL1, SEL2	I	Mode selection pins. See Table 2 for details.
5	VIN	I	The input pin to the device. It provides the current to the boost power stage and also powers the device circuit. When V_{IN} is below the undervoltage lockout threshold, the device turns off and disables outputs, thus disconnecting the WLEDs from the input.
6	SW	I	This is the switching node of the device.
7	IOUT	O	The output of the constant current supply. It is directly connected to the boost converter output.
8	GND	O	The ground of the device. Connect the input and output capacitors very close to this pin.
—	Thermal Pad	—	The thermal pad should be soldered to the analog ground. If possible, use thermal via to connect to ground plane for ideal power dissipation.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Supply voltages on pin VIN(2)	–0.3		V
Voltages on pins SEL1, SEL2, ISET1 and ISET2(2)	–0.3		V
Voltage on pin IOUT, SW, IFB1 and IFB2(2)		30	V
Operating junction temperature	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_I	Input voltage	2.5		6	V
V_O	Output voltage	V_{IN}		27	V
L	Inductor(1)		10		µH
C_{IN}	Input capacitor(1)	1			µF
C_O	Output capacitor(1)	1			µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) See the *Application and Implementation* section for further information.

7.4 Thermal Information

THERMAL METRIC(1)		TPS6115x DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

At V_I = 3.6 V, SELx = V_{IN}, R_{SET} = 80 kΩ, V_{IO} = 15 V, and T_A = –40°C to +85°C. Typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage range		2.5		6	V
I_Q	Operating quiescent current into V_{IN}	Device PWM switching no load			2	mA
I_{SD}	Shutdown current	SELx = GND			1.5	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		1.65	1.8	V
V_{hys}	Undervoltage lockout hysterisis			70		mV
ENABLE AND SOFT START						
$V_{(selh)}$	SEL logic high voltage	V_{IN} = 2.7 V to 6 V	1.2			V
$V_{(sell)}$	SEL logic low voltage	V_{IN} = 2.7 V to 6 V			0.4	V
$R_{(en)}$	SEL pulldown resistor		300	700		kΩ
T_{off}	SEL pulse width to disable	SELx high to low	40			ms
K_{ss}	IFB soft start current steps			16		
T_{ss}	Soft start time step	Measured as clock divider		64		
T_{ss_en}	Soft start enable time	Time between falling and rising of two adjacent SELx pulses	40			ms
CURRENT FEEDBACK						
$V_{(ISET)}$	ISET pin voltage		1.204	1.229	1.254	V
$K_{(ISET)}$	Current multiplier	I_{OUT}/I_{SET}	820	900	990	
K_M	Current matching	In reference to the average of two output current	–6%		6%	
$V_{(IFB)}$	IFB regulation voltage		300	330	360	mV
$V_{(IFB\_L)}$	IFB low threshold hysteresis			60		mV
TI_{sink}	Current sink settle time measured from SELx rising edge (1)				6	µs
I_{lkg}	IFB pin leakage current	I_{FB} voltage = 25 V			1	µA
POWER SWITCH AND DIODE						
$r_{DS(on)}$	N-channel MOSFET on-resistance	V_{IN} = V_{GS} = 3.6 V		0.6	0.9	Ω
$I_{(LN\_NFET)}$	N-channel leakage current	V_{DS} = 25 V			1	µA
V_F	Power diode forward voltage	I_D = 0.7 A		0.83	1	V
OC AND OVP						
I_{LIM}	N-Channel MOSFET current limit	Dual output, I_{OUT} = 15 V, D = 76%	0.75	1	1.25	A
		Single output , I_{OUT} = 15 V, D = 76%	0.40	0.55	0.7	
$I_{(IFB\_MAX)}$	Current sink max output current	I_{FB} = 330 mV	35			mA
V_{OVP}	Overvoltage threshold	TPS61150	27	28	29	V
		TPS61151	21	22	23	
$V_{OVP(hys)}$	Overvoltage hysteresis	TPS61150		550		mV
		TPS61151		440		
PWM AND PFM CONTROL						
f_S	Oscillator frequency		1	1.2	1.5	MHz
D_{max}	Maximum duty cycle	V_{FB} = 1 V	90%	93%		
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
T_{hys}	Thermal shutdown threshold hysteresis			15		°C

(1) This specification determines the minimum on time required for PWM dimming for desirable linearity. The maximum PWM dimming frequency can be calculated from the minimum duty cycle required in the application.

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7.6 Typical Characteristics

Data for all characteristic graphs were taken using the *Typical Application* with inductor = 10 µH (VLCF4018T-100MR74-2), R1 = R2 = 56 kΩ, unless otherwise noted.

Table 3. Table Of Graphs

		FIGURE
Overcurrent limit	V_{IN} = 3 V, 3.6 V, and 4 V, Single and dual output	Figure 1, Figure 2
K value over current	V_{IN} = 3.6 V, I_{LOAD} = 2 mA to 25 mA	Figure 3
PWM dimming linearity	Frequency = 20 kHz and 30 kHz	Figure 4
Single output PWM dimming waveform		Figure 5
Multiplexed PWM dimming waveform		Figure 6
Start-up waveform		Figure 7

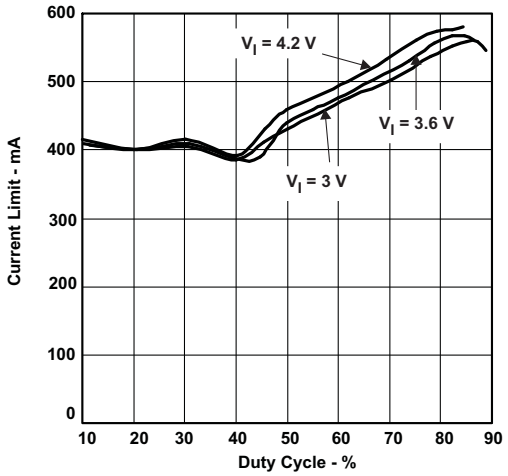

Figure 1. Overcurrent Limit (Single Output) vs Duty Cycle

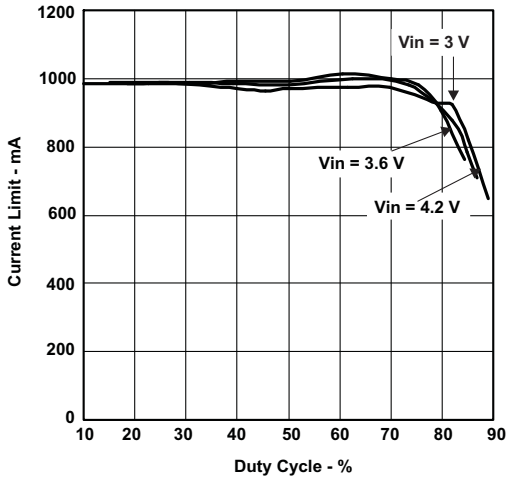

Figure 2. Overcurrent Limit (Dual Output) vs Duty Cycle

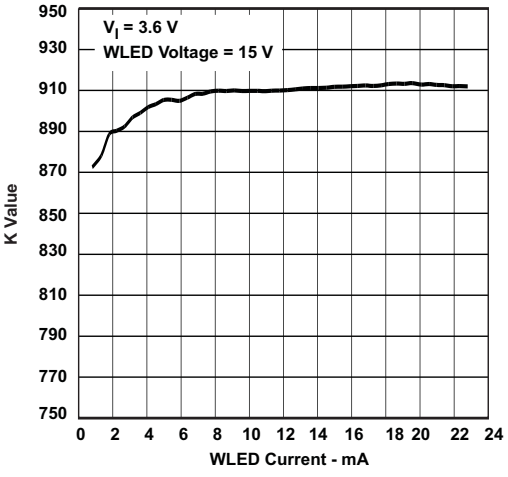

Figure 3. K Value vs WLED Current

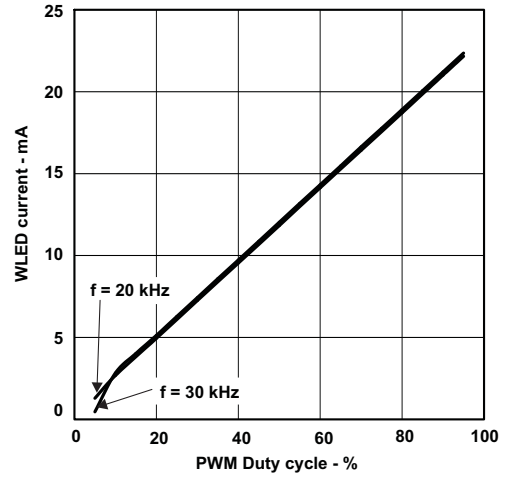

Figure 4. WLED Brightness Dimming Linearity

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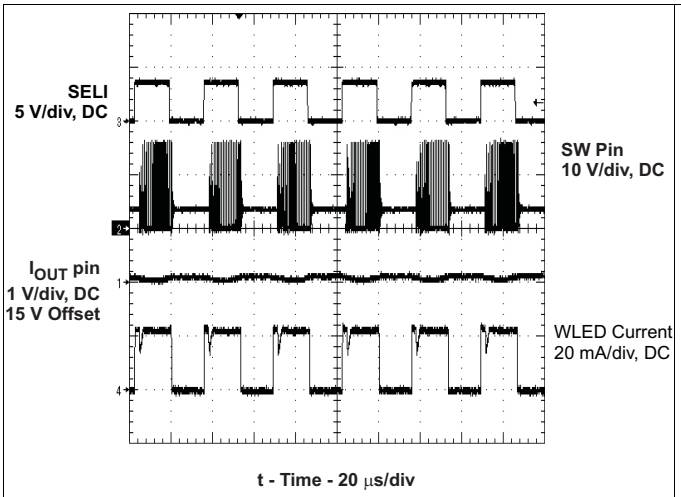
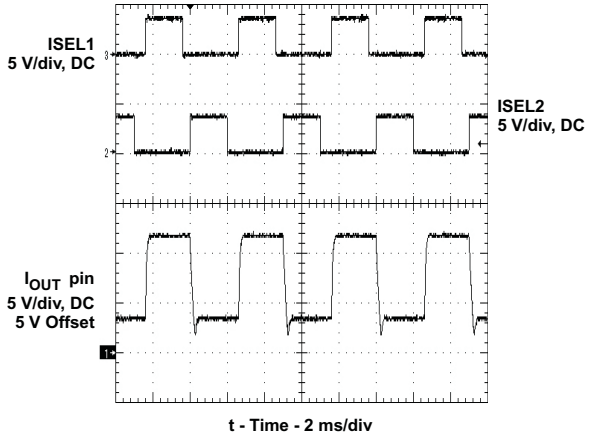


Figure 5. Single Output WLED PWM Brightness Dimming



ISEL1: 4 WLED ISEL2: 2 WLED

Figure 6. Multiplexed PWM Dimming

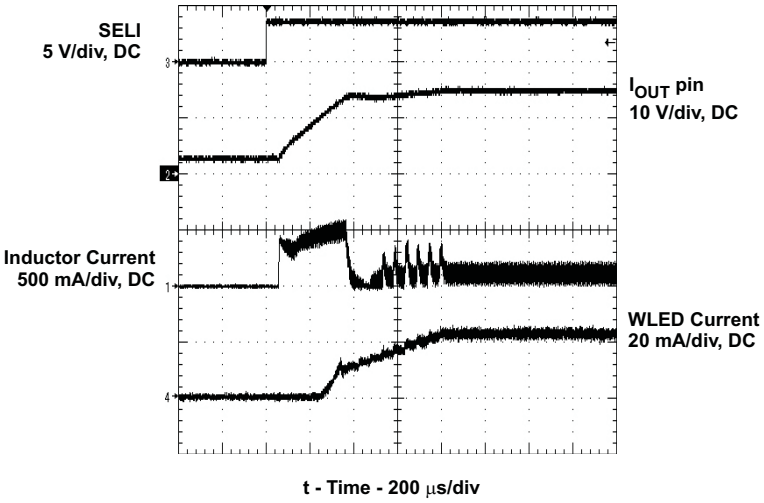


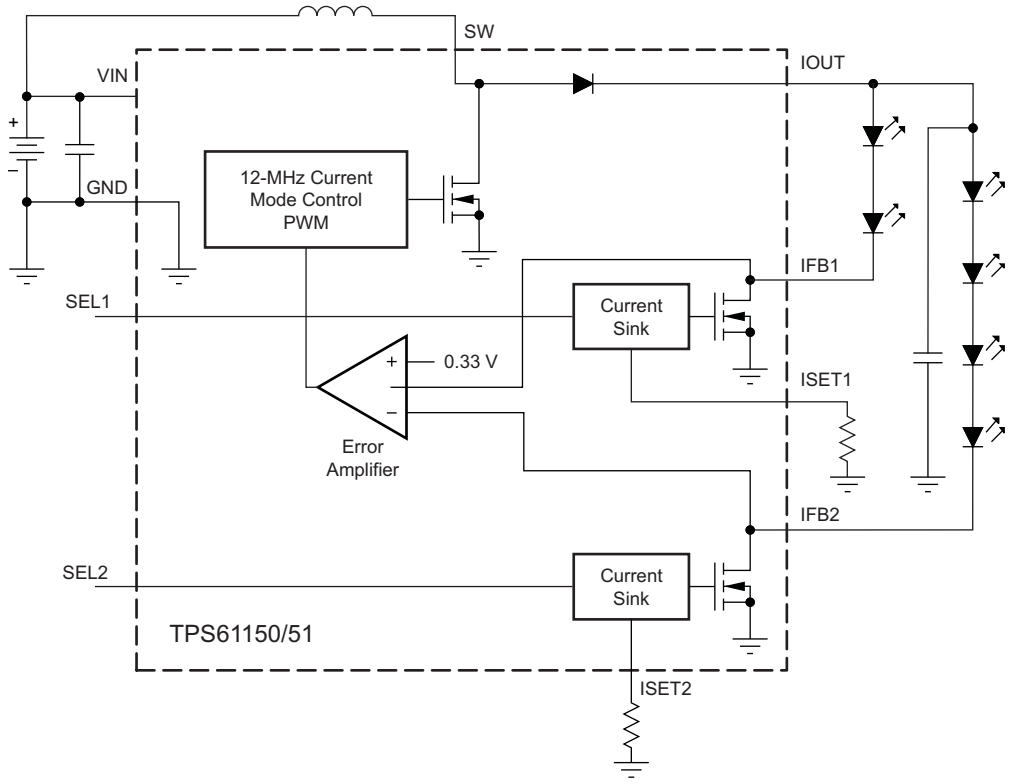
Figure 7. WLED Start-Up

8 Detailed Description

8.1 Overview

The TPS6115x is a two-channel WLED driver with an integrated inductive boost converter. The boost converter generates the bias voltage for the LED string while the two integrated low-side current sinks independently regulate the current in LED strings from V_{IN} to 29 V. Independent LED string dimming is provided via a PWM input at the SEL1 and SEL2 inputs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Start-Up

During start-up, both the boost converter and the current sink circuitry ramp up simultaneously to establish a steady state. The current sink circuitry ramps up current in 16 steps with each step taking 64 clock cycles. This period ensures that the current sink loop is slower than the boost converter response during start-up. Therefore, the boost converter output comes up slowly as current sink circuitry ramps up the current. This configuration ensures a smooth start-up and minimizes in-rush current.

8.3.2 Overvoltage Protection (OVP)

To prevent the boost output runaway as the result of WLED disconnection, there is an overvoltage protection circuit that stops the boost converter from switching as soon as its output exceeds the OVP threshold. When the voltage falls below the OVP threshold, the converter resumes switching.

The two OVP options offer the choices to prevent a 25-V rated output capacitor or the internal 30-V FET from breaking down.

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Feature Description (continued)

8.3.3 Undervoltage Lockout

An undervoltage lockout prevents device malfunction at input voltages below 1.65 V (typical). When the input voltage is below the undervoltage threshold, the device remains off, and both the boost converter and current sink circuit are turned off, providing isolation between input and output.

8.3.4 Thermal Shutdown

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The thermal shutdown has a hysteresis of typically 15°C.

8.3.5 Enable

Pulling either the SEL1 or SEL2 pin low turns off the corresponding output. If both SEL1 and SEL2 are low for more than 40 ms, the device shuts down and consumes less than 1 µA current. The SEL pin can also be used for PWM brightness dimming. To improve PWM dimming linearity, soft start is disabled if the time from the falling and rising edges of two adjacent SELx pulses is less than 40 ms. See the *Application and Implementation* section for details.

Each SEL input pin has an internal pulldown resistor to disable the device when the pin is floating.

8.4 Device Functional Modes

8.4.1 Current Regulation

The TPS6115x uses a single boost regulator to drive two WLED strings, each with independently programmable current. The boost converter adopts PWM control which is ideal for high output current and low output ripple noises. The feedback loop regulates the IFB pins to a threshold voltage (330 mV typical), giving the current sink circuit just enough headroom to operate.

The regulation current is set by the resistor on the ISET pin based on Equation 1.

$$I_O = \frac{V_{ISET}}{R_{SET}} \times K_{ISET} \quad (1)$$

Where:

- I_O = output current
- V_{ISET} = ISET pin voltage (1.229 V typical)
- R_{SET} = ISET pin resistor value
- K_{ISET} = current multiplier (900 typical)

When both outputs are enabled, the boost converter provides enough power to provide the demanded current through IFB1 and IFB2 while keeping the voltage at IOUT high enough to meet the forward voltage drops of the WLEDs. Specifically, at start-up, the boost converter increases its output power, and therefore the output voltage, from I_{OUT} until IFB1 reaches its regulated voltage. Once IFB1 is within regulation, the device looks to the IFB2 voltage and may increase $V_{(IOUT)}$ further to get IFB2 in regulation. After both IFB pins reach regulation, the feedback path dynamically switches to whichever IFB pin drops more than the IFB low hysteresis voltage (60 mV typical) below its regulation voltage. This architecture ensures proper current regulation for both IFB1 pins; however, the voltage at one IFB pin is higher than the minimum required regulation voltage. The overall efficiency when both strings are on depends on the voltage difference between the IFB1 and IFB2 pins. A large difference reduces the efficiency as a result of power losses across the current sink circuit of the IFB pin with the higher drop.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The standard application circuit is shown in Figure 8. Typical V_{IN} range is from a single cell Li+ battery. LED strings voltages can be as high as 28 V (TPS61150) or 22 V (TPS61151). LED string voltage mismatch is allowed due to the adaptive feedback headroom voltage which dynamically looks for and regulates the highest voltage string.

9.2 Typical Application

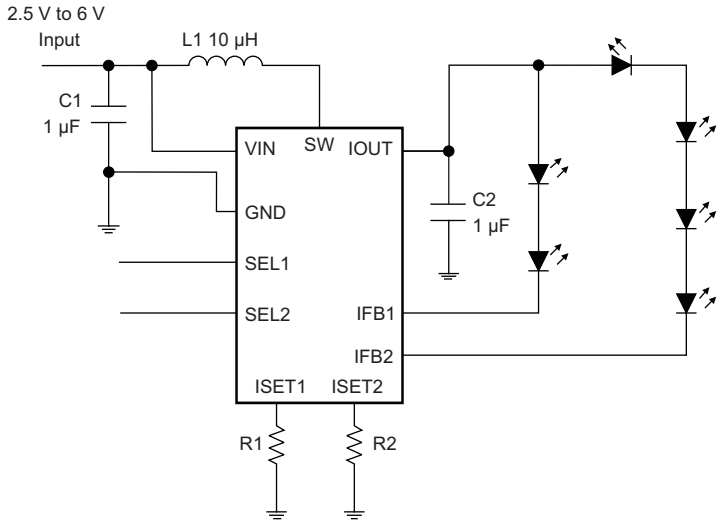

Figure 8. TPS6115x Typical Application

9.2.1 Design Requirements

For typical dual output boost WLED driver applications, use the parameters listed in Table 4.

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.5 V
Minimum output voltage	V_{IN}
Output current	up to 35 mA/string
Fixed switching frequency	1.2 MHz

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9.2.2 Detailed Design Procedure

9.2.2.1 Maximum Output Current

The overcurrent limit in a boost converter limits the maximum input current (and thus the maximum input power) for a given input voltage. Maximum output power is less than the maximum input power because of power conversion losses. Therefore, the current limit, input voltage, output voltage, and efficiency can all change maximum current output. Because current limit clamps peak inductor current, ripple must be subtracted to derive the maximum DC current. The ripple current is a function of switching frequency, inductor value, and duty cycle. Equation 2 and Equation 3 take all of the above factors into account for maximum output current calculation.

$$I_P = \frac{1}{\left[L \times \left(\frac{1}{V_{IOUT} + V_F - V_{IN}} + \frac{1}{V_{IN}}\right) \times F_S\right]} \quad (2)$$

Where:

- I_P = inductor peak to peak ripple
- L = inductor value
- V_F = power diode forward voltage
- F_S = switching frequency
- V_{IOUT} = boost output voltage. It is equal to 330 mV + voltage drop across WLED.

$$I_{OUT\_MAX} = \frac{V_{IN} \times \left(I_{LIM} - \frac{I_P}{2}\right) \times \eta}{V_{IOUT}} \quad (3)$$

Where:

- I_{OUT_MAX} = maximum output current of the boost converter
- I_{LIM} = overcurrent limit
- η = efficiency

To keep a tight range on the overcurrent limit, the TPS6115x uses the VIN and IOUT pin voltages to compensate for the overcurrent limit variation caused by the slope compensation. However, the current threshold still has a residual dependency on the VIN and IOUT voltages. Use Figure 1 and Figure 2 to identify the typical overcurrent limit in a specific application, and use a ±25% tolerance to account for temperature dependency and process variations.

The maximum output current can also be limited by the current capability of the current-sink circuitry. It is designed to provide a maximum 35-mA current regardless of the current capability of the boost converter.

9.2.2.2 WLED Brightness Dimming

There are three ways to change the output current *on the fly* for WLED dimming. The first method parallels an additional resistor with the ISET pin resistor as shown in Figure 9. The switch (Q1) can change the ISET pin resistance, and therefore modify the output current. This method is very simple, but can provide only limited dimming steps.

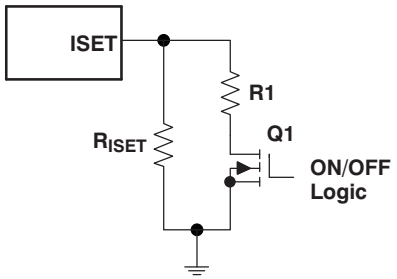

Figure 9. Switching In or Out With an Additional Resistor to Change Output Current

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Alternatively, a PWM dimming signal at the SEL pin can modulate the output current by the duty cycle of the signal. The logic high of the signal turns on the current sink circuit, while the logic low turns it off. This operation creates an averaged DC output current proportional to the duty cycle of the PWM signal. The frequency of the PWM signal must be high enough to avoid flashing of the WLEDs. The soft start of the current sink circuit is disabled during the PWM dimming to improve linearity.

The major concern of the PWM dimming is the creation of audible noises that can come from the inductor or output capacitor of the boost converter, or both. The audible noises on the output capacitor are created by the presence of voltage ripple in range of audible frequencies. The TPS6115x alleviates the problem by disconnecting the WLEDs from the output capacitor when the SEL pin is low. Therefore, the output capacitor is not discharged by the WLEDs, and thus reduces the voltage ripple during PWM dimming.

The audible noises can be eliminated by using a PWM dimming frequency above or below the audible frequency range. The maximum PWM dimming frequency of the TPS6115x is determined by the current settling time (T_{isink}), which is the time required for the sink circuit to reach a steady state after the SEL pin transitions from low to high. The maximum dimming frequency can be calculated by Equation 4:

$$F_{PWM\_MAX} = \frac{D_{MIN}}{T_{ISINK}} \quad (4)$$

Where:

- D_{MIN} = min duty cycle of the PWM dimming required in the application

For 20% D_{MIN}, a PWM dimming frequency up to 33 kHz is possible, putting the noise frequency above the audible range.

Because the TPS61150/1 dynamically regulates one IFB pin voltage, its output voltage can have a large ripple during PWM dimming as shown in Figure 6. This ripple may cause ceramic output capacitors to ring audibly. To reduce the output ripple, the configurations shown in Figure 16 and Figure 17 are recommended for PWM dimming. In Figure 16, both current strings have the same number of LEDs and the same PWM signal. In Figure 17, one string (in this case, string 2) is not PWM dimmed and has a greater total forward voltage drop than string 1, either because of having more LEDs than string 1 or because of adding a resistor in series with string 2. Therefore, IFB2 controls the regulation regardless of the PWM signal on IFB1, and the output ripple is significantly reduced when string 1 is dimmed. The circuit in Figure 17 could have been reconfigured with string 1 having the larger total forward drop.

The third method uses an external DC voltage and resistor as shown in Figure 10 to change the ISET pin current, and thus control the output current. The DC voltage can be the output of a filtered PWM signal. The formulas to calculate the output current is given by Equation 5 and Equation 6.

$$I_{WLED} = K_{ISET} \times \left(\frac{1.229}{R_{ISET}} + \frac{1.229 - V_{DC}}{R_1} \right) \text{ for DC voltage input} \quad (5)$$

$$I_{WLED} = K_{ISET} \times \left(\frac{1.229}{R_{ISET}} + \frac{1.229 - V_{DC}}{R_1 + 10K} \right) \text{ for PWM signal input}$$

Where:

- K_{ISET} = current multiplier between the ISET pin current and the IFB pin current.
- V_{DC}= voltage of the DC voltage source or the DC voltage of the PWM signal. (6)

Figure 10. Analog Dimming Using an External Voltage Source to Control the Output Current

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9.2.2.3 Inductor Selection

Because the selection of the inductor affects the power supply steady-state operation, transient behavior, and loop stability, the inductor is the key component in power regulator design. Three specifications are the most important to the performance of the inductor: the inductor value, DC resistance (DCR), and saturation current. Considering the inductor value alone is not enough.

The inductor inductance value determines the inductor ripple current. It is generally recommended to set peak-to-peak ripple current given by Equation 2 to betweeen 30% to 40% of DC current. It is a good compromise of power loss and inductor size. For this reason, 10-µH inductors are recommended for the TPS6115x. Inductor DC current can be calculated as Equation 7.

$$I_{L\_DC} = \frac{V_{IOUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (7)$$

Use the maximum load current and minimum V_{in} for calculation.

The internal loop compensation for PWM control is optimized for the external component shown in the Figure 8 with consideration of component tolerance. Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0-A value, depending on how the inductor vendor defines saturation. Using an inductor with a smaller inductance value forces discontinuous PWM in which the inductor current ramps down to zero before the end of each switching cycle, reduces the boost converter maximum output current, and causes large input voltage ripple. An inductor with larger inductance reduces the gain and phase margin of the feedback loop, possibly resulting in instability.

Regulator efficiency depends on the resistance of its high current path and switching losses associated with the PWM switch and power diode. Although the TPS6115x has optimized the internal switches, the overall efficiency still relies on inductor DCR; lower DCR improves efficiency. However, there is a trade-off between DCR and inductor size, and shielded inductors typically have higher DCR than unshielded ones. A DCR in range of 150 mΩ to 350 mΩ is suitable for applications that require *both on* mode. A DCR is the range of 250 mΩ to 450 mΩ is a good choice for single output applications. Table 5 and Table 6 list some recommended inductor models.

Table 5. Recommended Inductors for Single Output

	L (µH)	DCR TYPICAL(mΩ)	I_{SAT} (A)	SIZE (L × W × H mm)
TDK				
VLF3012AT-100MR49	10	360	0.49	2.8 × 3 × 1.2
VLCF4018T-100MR74-2	10	163	0.74	4 × 4 × 1.8
Sumida				
CDRH2D11/HP	10	447	0.52	3.2 × 3.2 × 1.2
CDRH3D16/HP	10	230	0.84	4 × 4 × 1.8

Table 6. Recommended Inductors for Dual Output

	L (µH)	DCR TYPICAL (mΩ)	I_{SAT} (A)	SIZE (L × W × H mm)
TDK				
VLCF4018T-100MR74-2	10	163	0.74	4 × 4 × 1.8
VLF4012AT-100MR79	10	300	0.85	3.5 × 3.7 × 1 .2
Sumida				
CDRH3D16/HP	10	230	0.84	4 × 4 × 1.8
CDRH4D11/HP	10	340	0.85	4.8 × 4.8 × 1.2

9.2.2.4 Input and Output Capacitor Selection

The output capacitor is primarily selected for the output ripple of the converter. This ripple voltage is the sum of the ripple caused by the capacitor capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by Equation 8.

$$C_{OUT} = \frac{(V_{IOUT} - V_{IN}) I_{OUT}}{V_{IOUT} \times F_S \times V_{RIPPLE}}$$

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Where:

- V_{RIPPLE} = peak-to-peak output ripple (8)

For V_{IN} = 3.6 V, V_{IOUT} = 20 V, and F_S = 1.2 MHz, 0.1% ripple (20 mV) would require a 1-µF capacitor. For this value, ceramic capacitors are the best choice for size, cost, and availability.

The additional output ripple component caused by ESR is calculated using Equation 9:

$$V_{ripple\_ESR} = I_{out} \times R_{ESR} \quad (9)$$

As a result of its low ESR, V_{ripple_ESR} can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

During a load transient, the capacitor at the output of the boost converter must supply or absorb additional current before the inductor current ramps up the steady-state value. Larger capacitors always help to reduce the voltage over- and undershoot during a load transient. A larger capacitor also helps loop stability.

Care must be taken when evaluating ceramic capacitor derating because of the applied DC voltage, aging, and frequency response. For example, larger form-factor capacitors (in size 1206) have self-resonant frequencies in the range of the TPS6115x switching frequency. Therefore, the effective capacitance is significantly lower for these capacitors. As a result, it may be necessary to use small capacitors in parallel instead of one large capacitor.

Table 7 lists some recommended input and output ceramic capacitors. Two popular vendors for high-value ceramic capacitors are:

TDK (http://www.component.tdk.com/components.php)

Murata (http://www.murata.com/cap/index.html)

Table 7. Recommended Input and Output Capacitors

	CAPACITANCE (µF)	VOLTAGE (V)	CASE
TDK			
C3216X5R1E475K	4.7	25	1206
C2012X5R1E105K	1	25	0805
C1005X5R0J105K	1	6.3	0402
Murata			
GRM319R61E475KA12D	4.7	25	1206
GRM216R61E105KA12D	1	25	0805
GRM155R60J105KE19D	1	6.3	0402

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9.2.3 Application Curves

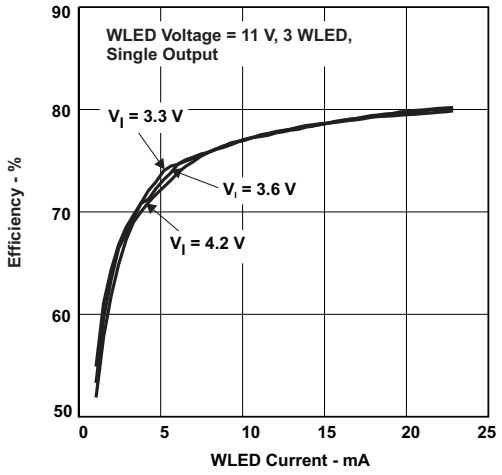

Figure 11. Efficiency vs Load Current

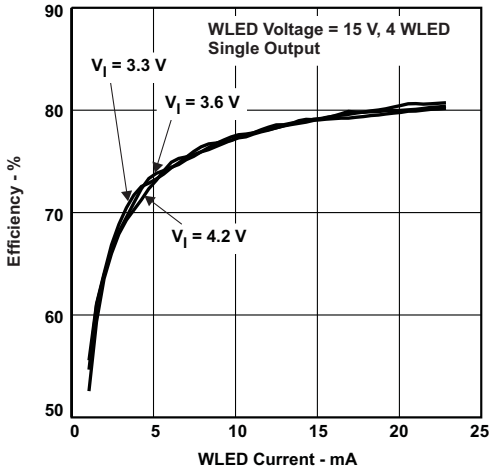

Figure 12. Efficiency vs Load Current

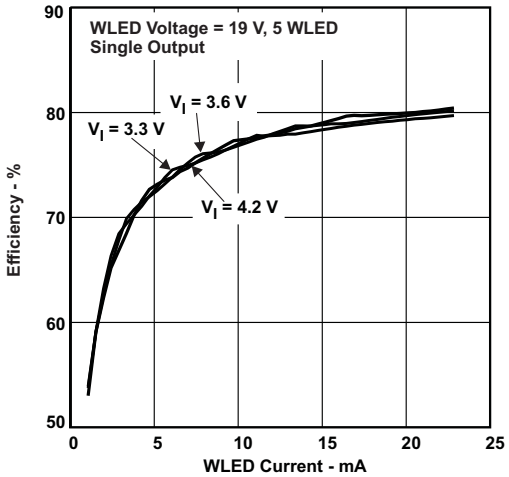

Figure 13. Efficiency vs Load Current

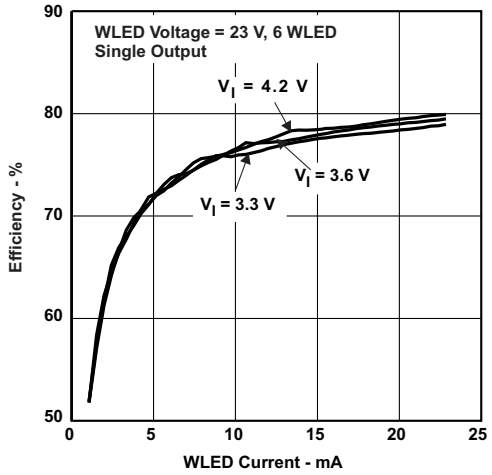

Figure 14. Efficiency vs Load Current

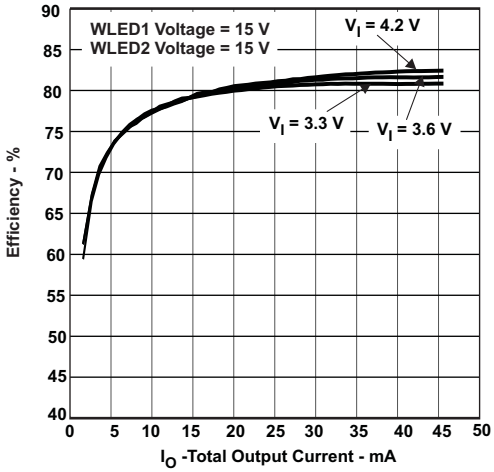

Figure 15. Both on Efficiency vs Total Output Current

9.3 Additional Application Circuits

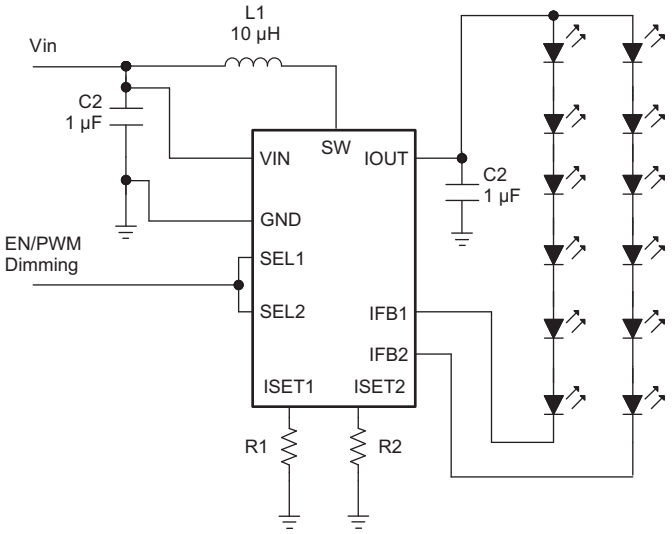

Figure 16. Driving up to 12 WLEDs With One LCD Backlight

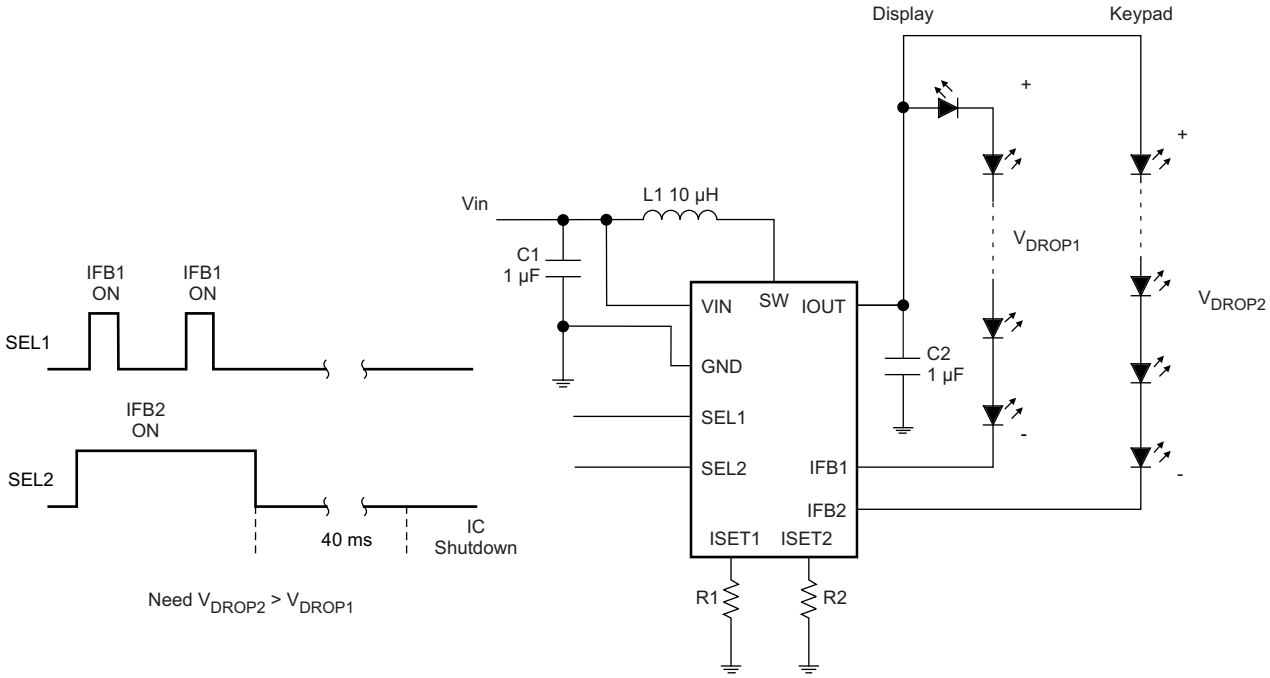

Figure 17. Driving A Keypad and LCD Backlight, Applying PWM Signal to the SEL1 Pin

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10 Power Supply Recommendations

Apply an input voltage between 2.5 V and 6 V. Bypass IN with a ceramic capacitor as close to the VIN pin and GND pin as possible in order to filter switching noise.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, especially those providing high current and using high switching frequencies, printed circuit board (PCB) layout is an important design step. If layout is not carefully done, the regulator could show instability as well as electromagnetic interference (EMI) problems. Therefore, use wide and short traces for high current paths. The input capacitor must not only be close to the VIN pin, but also to the GND pin in order to reduce the input ripple seen by the device. The VIN and SW pins are conveniently located on the edges of the device; therefore, the inductor can be placed close to the device. The output capacitor must be placed near the load to minimize ripple and maximize transient performance.

It is also beneficial to have the ground of the output capacitor close to the GND pin because there will be a large ground return current flowing between these two connections. When laying out the signal ground, use short traces separated from power ground traces, and connect them together at a single point on the PCB.

11.2 Layout Example

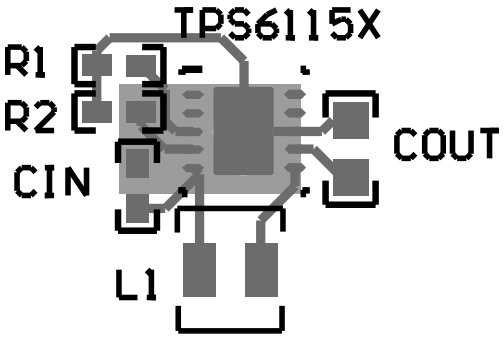

Figure 18. TPS61150 Layout Example

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Related Links

Table 8 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61150	Click here	Click here	Click here	Click here	Click here
TPS61151	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61150DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BCQ	Samples
TPS61150DRCRG4	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BCQ	Samples
TPS61150DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		BCQ	Samples
TPS61150DRCTG4	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		BCQ	Samples
TPS61151DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRH	Samples
TPS61151DRCRG4	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRH	Samples
TPS61151DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRH	Samples
TPS61151DRCTG4	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BRH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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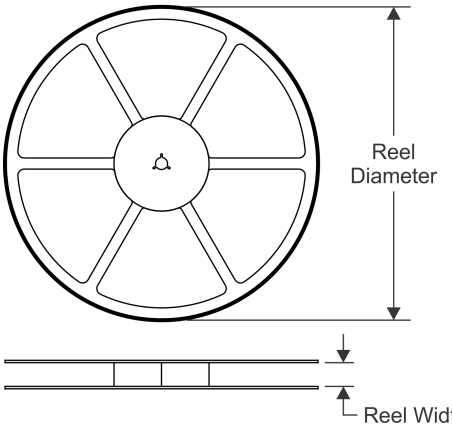
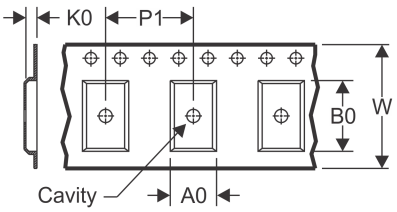
TAPE AND REEL INFORMATION

REEL DIMENSIONS

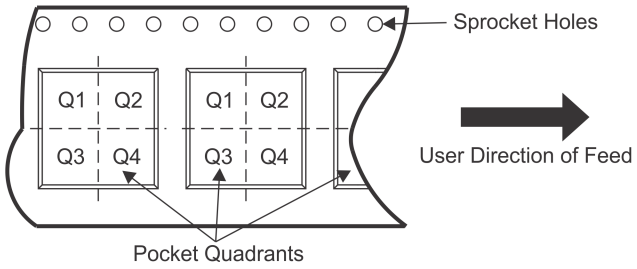


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

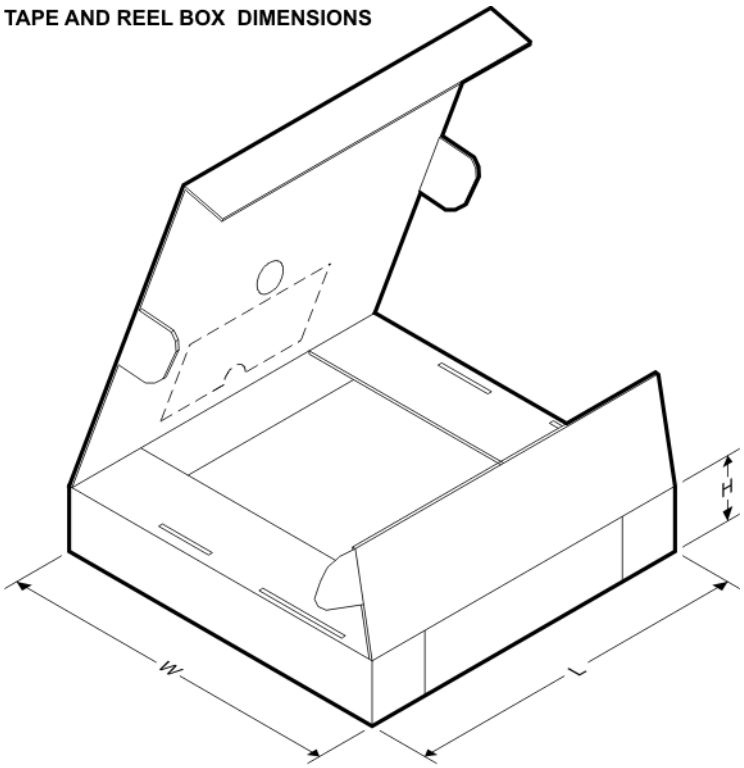
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61150DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61150DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61151DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61151DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

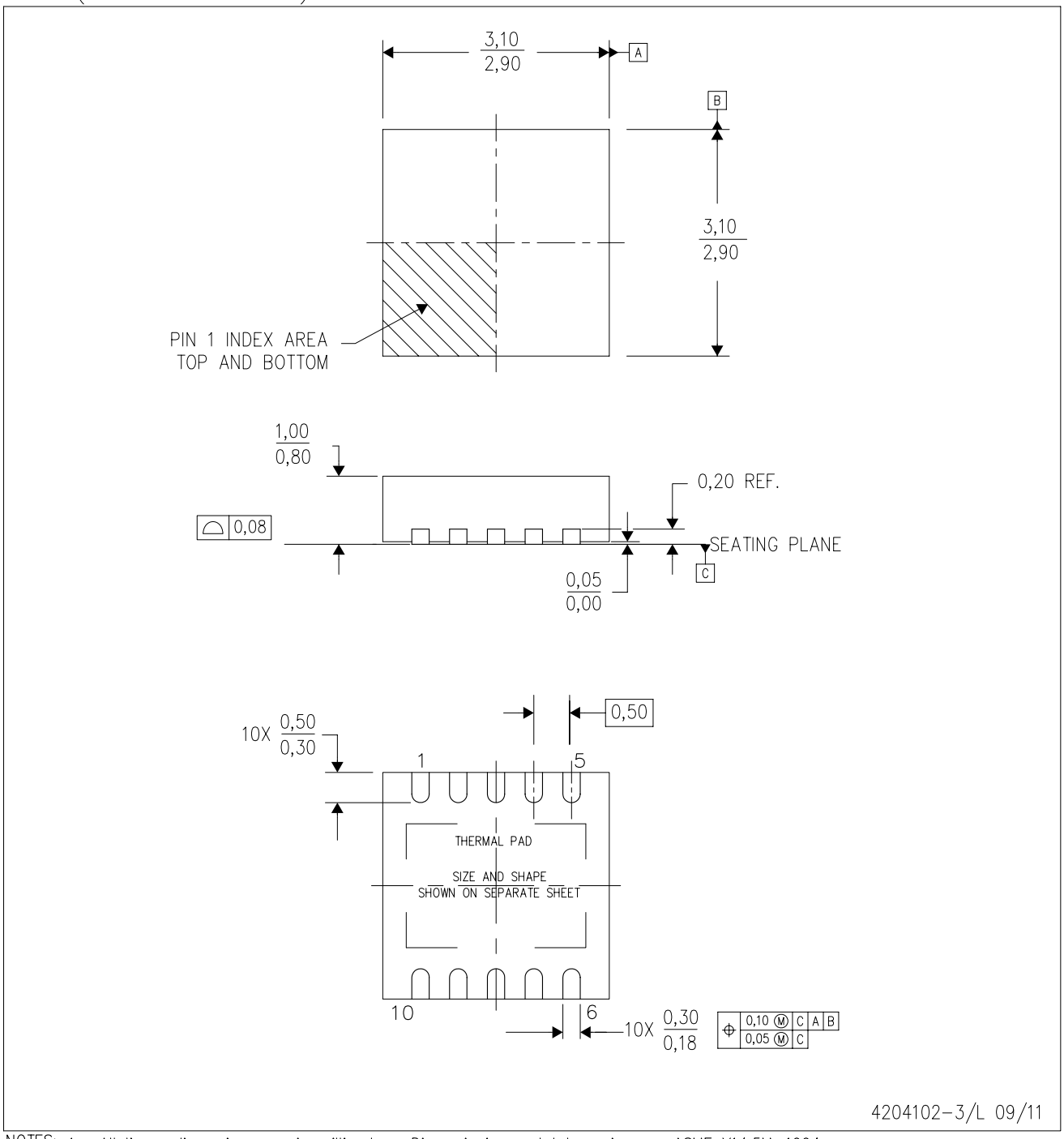
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61150DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS61150DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS61151DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS61151DRCT	VSON	DRC	10	250	210.0	185.0	35.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

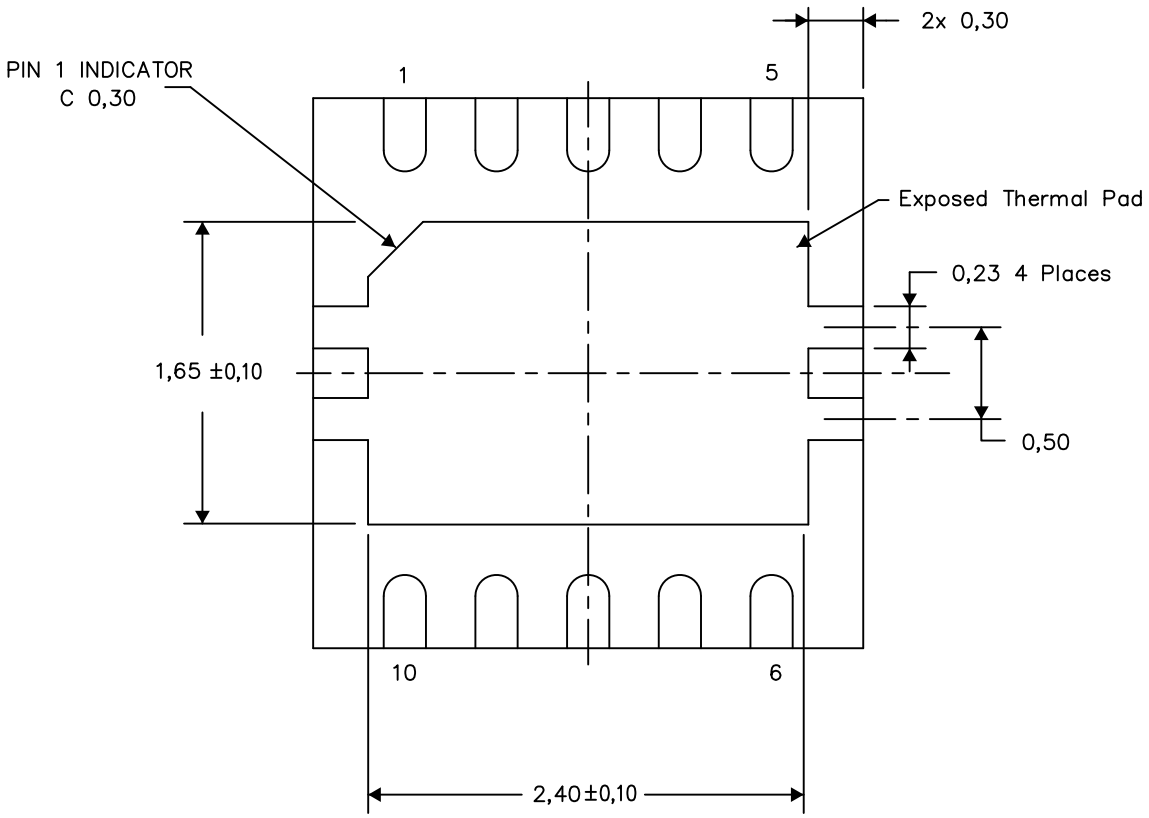
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



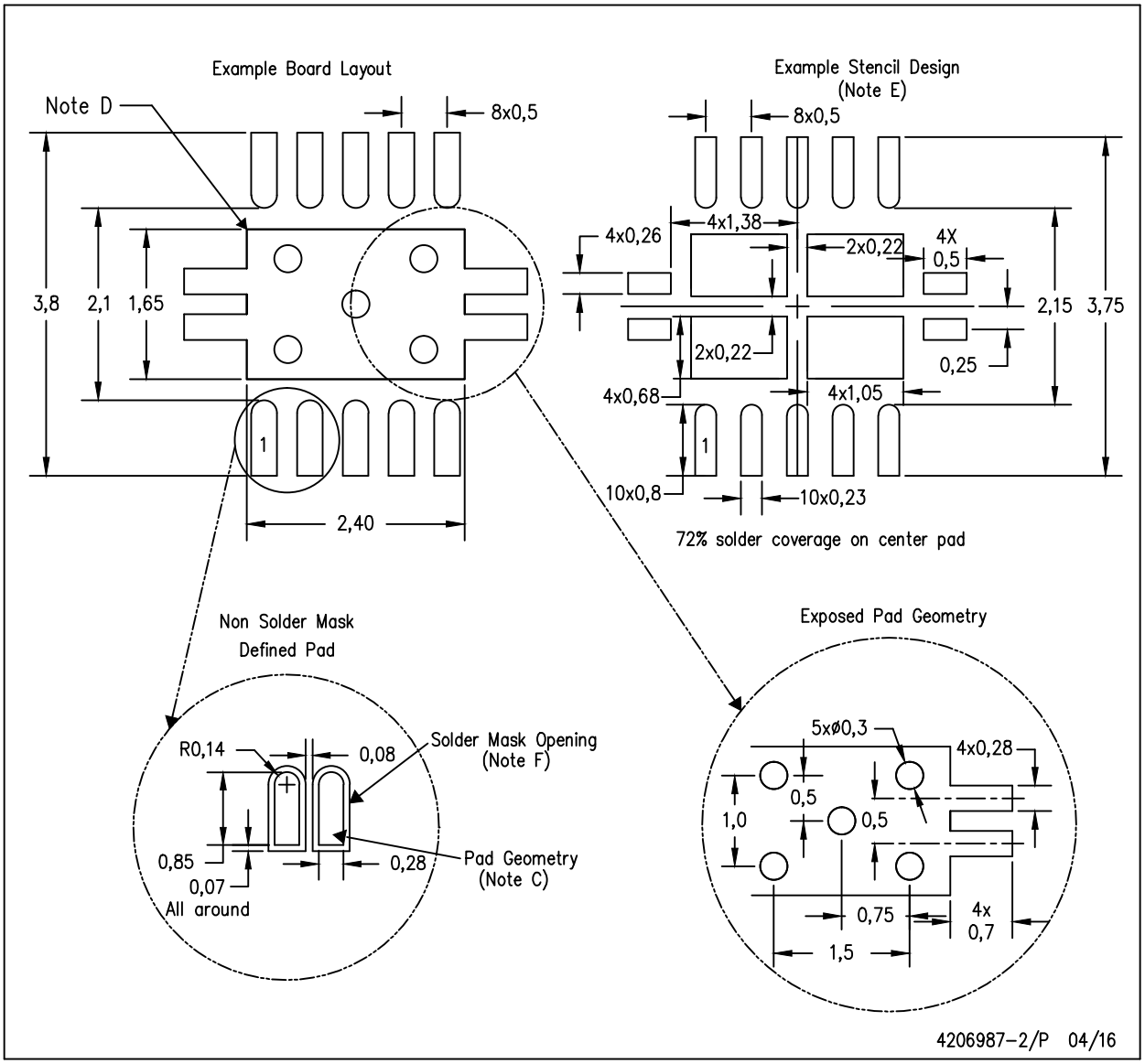
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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