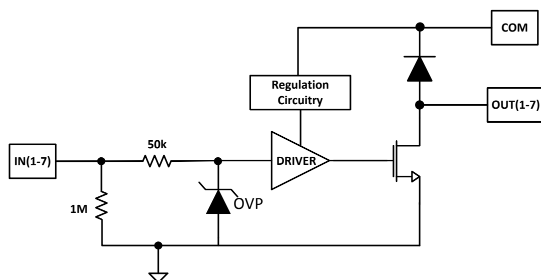
TPL7407L 40V 7 通道低侧驱动器

查询样片: **TPL7407L**

特性

- **600mA** 额定漏极电流（每通道）
- **7** 通道达灵顿 **(Darlington)** 阵列（例如 **ULN2003A**）的 **CMOS** 引脚到引脚改进
- 功耗（极低 V_{OL}）
  - 电流为 **100mA** 时，V_{OL} 低于达灵顿 **(Darlington)** 阵列的四分之一
- 每通道小于 **10nA** 的极低输出泄露
- 扩展环境温度范围：T_A = **-40°C** 至 **125°C**
- 高压输出 **40V**
- 与 **1.8V** 至 **5.0V** 微控制器和逻辑接口兼容
- 用于感应反冲保护的内部自振荡二极管
- 输入下拉电阻器可实现三态输入驱动器
- 用来消除嘈杂环境中寄生运行的输入电阻电容 **(RC)** 缓冲器
- 电感负载驱动器应用
- 静电放电 **(ESD)** 保护性能超过 **JESD 22** 规范要求
  - **2kV** 人体模型 **(HBM)**，**500V** 充电器件模型 **(CDM)**
- 采用 **16** 引脚小外形尺寸集成电路 **(SOIC)** 和薄型小外形尺寸 **(TSSOP)** 封装

简化电路原理图



应用范围

- 电感负载
  - 继电器
  - 单极步进 **&** 有刷直流电机
  - 螺线管 **&** 阀门
- 发光二极管 **(LED)**
- 逻辑电平位移
- 栅极 **&** 绝缘栅双极型晶体管 **(IGBT)** 驱动

说明

TPL7407L 是一款高压、高电流 NMOS 晶体管阵列。这个器件包含 7 个特有高压输出的 NMOS 晶体管，这些晶体管具有针对开关电感负载的共阴极钳位二极管。一个单个 NMOS 通道的最大漏极电流额定值为 600mA。 增加的全新稳压和驱动电路在整个通用输入输出 (GPIO) 范围内 (1.8V-5.0V) 提供最大驱动强度。可将这些晶体管并联以实现更高的电流能力。

TPL7407L 的主要优势是其经提升的效率以及低于双极达灵顿 (Darlington) 器件的泄露值。 借助于较低的 V_{OL}，功率耗散比传统中继驱动器少一半，每通道的电流少于 250mA。

器件信息

订货编号	封装（引脚）	封装尺寸
TPL7407L	SOIC (16)	9.9mm x 3.91mm
TPL7407L	TSSOP (16)	5.0mm x 4.4mm

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

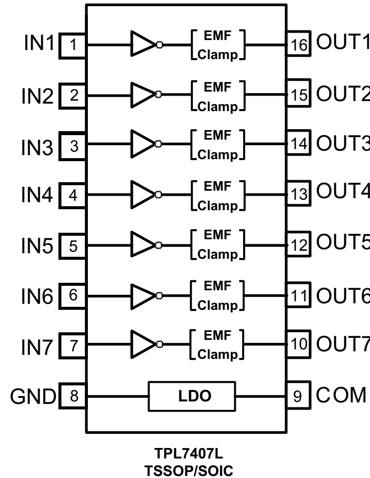
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2014, Texas Instruments Incorporated

English Data Sheet: SLRS066

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TERMINAL CONFIGURATION AND FUNCTIONS



Terminal Functions

TERMINAL		DESCRIPTION
NAME	NUMBER	
IN(X)	1, 2, 3, 4, 5, 6, 7	GPIO inputs that will drive the outputs "low" (or sinnk current) when driven "high"
OUT(X)	16, 15, 14, 13, 12, 11, 10	Driver output that sinks currents after input is driven "high"
COM	9	Supply PIn that should be tied to 8.5V or higher for proper operation
GND	8	Ground pin

Specifications

Absolute Maximum Ratings(1)

at 25°C free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
V_{OUT}	Pins OUT1-OUT7 to GND voltage	-0.3	42	V
V_{OK}	Ouput Clamp diode reverse voltage(2)	-0.3	42	V
V_{COM}	COM pin voltage(2)	-0.3	42	V
V_{IN}	Pins IN1-IN7 to GND voltage (2)	-0.3	30	V
I_{DS}	Continuous drain current per channel(3) (4)		600	mA
I_{OK}	Output clamp current		500	mA
I_{GND}	Total continuous GND-terminal current		–2	A
T_A	Operating free-air temperature range	–40	125	°C
T_J	Operating virtual junction temperature	-40	150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND/substrate terminal, unless otherwise noted.
(3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Copyright © 2014, Texas Instruments Incorporated

Thermal Information

THERMAL METRIC[1]		TPL7407L SOIC (D) 16 PINS	TPL7407L TSSOP (PW) 16 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	91.9	115.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	50.1	49.5	°C/W
θ_{JB}	Junction-to-board thermal resistance	49.4	60.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.6	8.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.1	60.2	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Recommended Operating Conditions

Over operating temperature range

		MIN	NOM	MAX	UNIT
V_{OUT}	OUT1- OUT7 pin voltage for recommended operation	0		40	V
V_{COM}	COM pin voltage range for full output drive	8.5		40	V
V_{IL}	IN1- IN7 input low voltage ("Off" high impedance output)			0.9	V
V_{IH}	IN1- IN7 input high voltage ("Full Drive" low impedance output)	1.5			V
T_J	Operating virtual junction temperature	-40		125	°C
I_{DS}	Continuous drain current	0		500	mA

Electrical Characteristics

T_J= –40°C to 125°C; Typical Values at T_A=T_J= 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL} (V_{DS})	OUT1- OUT7 low-level output voltage	V_{IN} ≥ 1.5V	I_D = 100 mA		200	320	mV
			I_D = 200 mA		420	650	
$I_{OUT(OFF)}$ (I_{DS_OFF})	OUT1- OUT7 OFF-state leakage current	V_{OUT} = 24V,	V_{IN} ≤ 1.0V		10	500	nA
V_F	Clamp forward voltage	I_F = 200 mA				1.4	V
$I_{IN(off)}$	IN1- IN7 Off-state input current	V_{INX}= 0V	V_{OUT}=40V			500	nA
$I_{IN(ON)}$	IN1- IN7 ON state input current	V_{INX}=1.5V-5.0V				10	μA
I_{COM}	Static current flowing through COM pin	V_{COM}=8.5V-40V			15	25	μA

Switching Characteristics

Typical Values at T_A=T_J= 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{INX} ≥1.65V, Vpullup=24V, Rpull-up = 48Ω		350		ns
t_{PHL}	Propagation delay time, high- to low-level output	V_{INX} ≥1.65V, Vpullup=24V, Rpull-up = 48Ω		350		ns
C_i	Input capacitance	V_I = 0, f = 100KHz		5		pF

Typical Characteristics

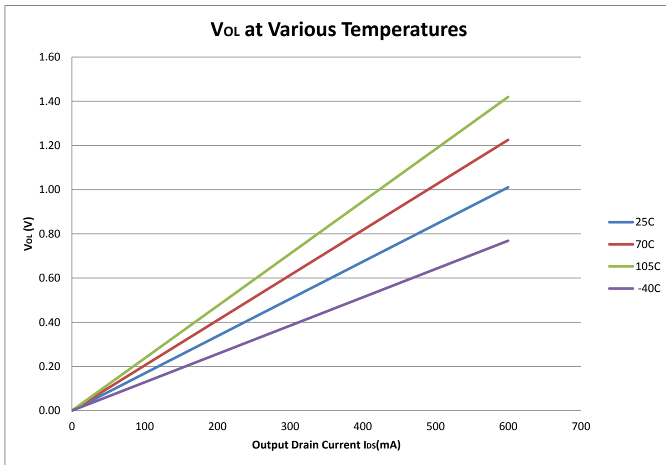


Figure 1. V_{OL} (V_{DS})

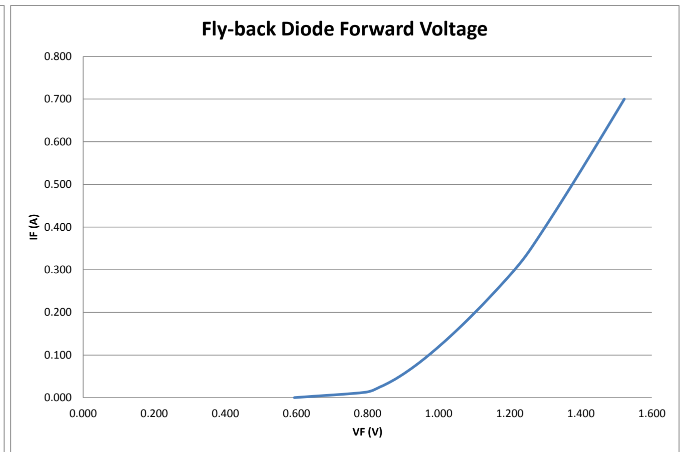


Figure 2. Flyback Diode Forward Voltage

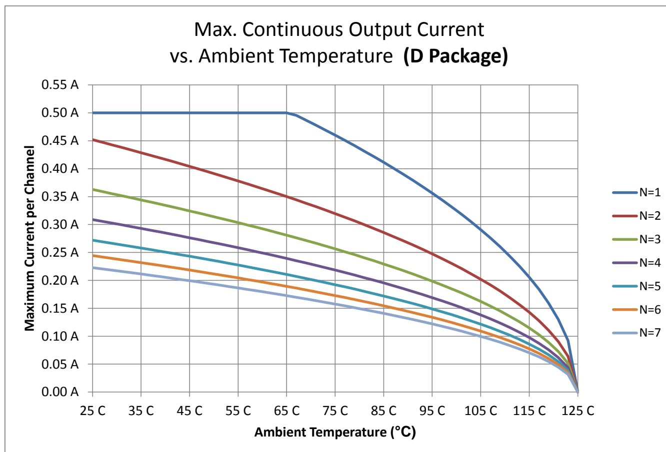


Figure 3. Maximum Output Current vs. Temperature (SOIC)

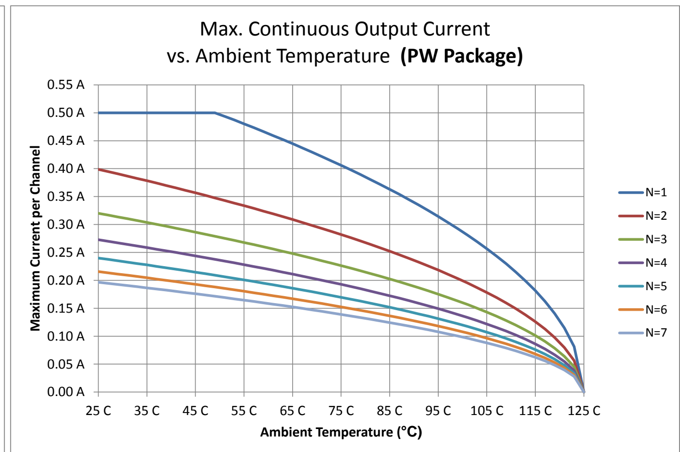


Figure 4. Maximum Output Current vs. Temperature (TSSOP)

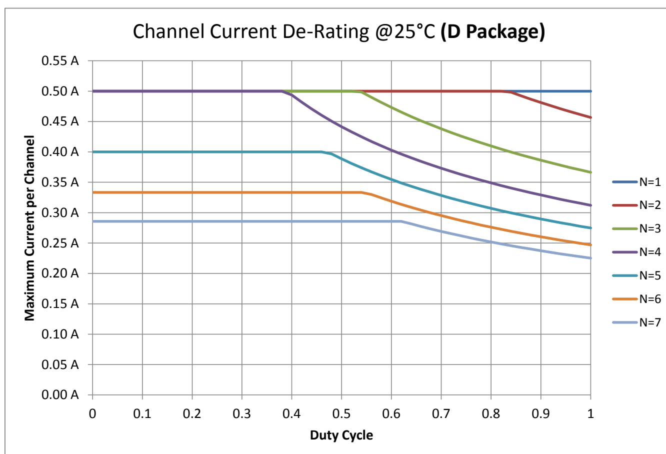


Figure 5. D Package Maximum Collector Current Vs. Duty Cycle at 25°C

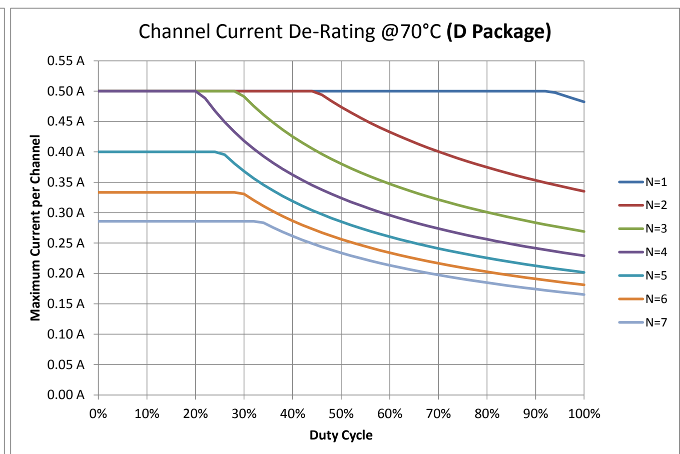


Figure 6. D Package Maximum Collector Current Vs. Duty Cycle at 70°C

Copyright © 2014, Texas Instruments Incorporated

Typical Characteristics (continued)

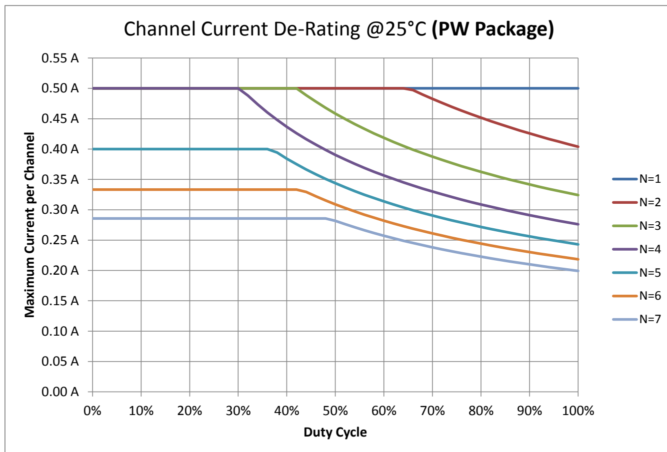


Figure 7. PW Package Maximum Collector Current Vs. Duty Cycle at 25°C

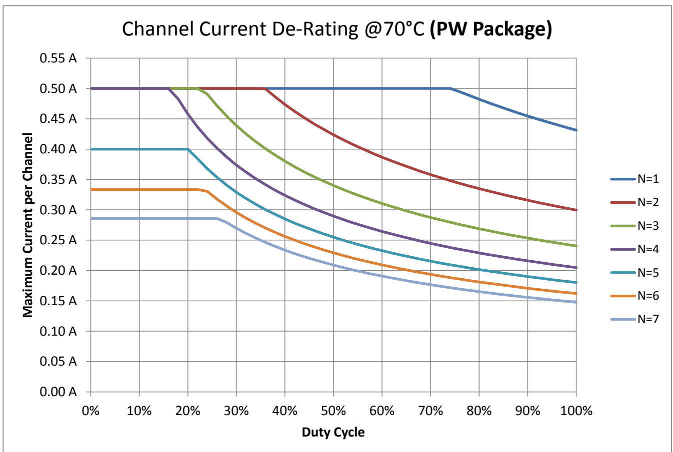


Figure 8. PW Package Maximum Collector Current Vs. Duty Cycle at 70°C

Copyright © 2014, Texas Instruments Incorporated

APPLICATION AND IMPLEMENTATION

TTL and other Logic Inputs

TPL7407L input interface is specified for standard 1.8V and 5V CMOS logic interface and can tolerate up to 30V. At any input voltage the output drivers will be driven at it's maximum when Vcom is greater than or equal to 8.5V.

Input RC Snubber

TPL7407L features an input RC snubber that helps prevent spurious switching in noisy environment. Connect an external 1kΩ to 5kΩ resistor in series with the input to further enhance TPL7407L's noise tolerance.

High-impedance Input Drivers

TPL7407L features a 1MΩ input pull-down resistor. The presence of this resistor allows the input drivers to be tri-stated. When a high-impedance driver is connected to a channel input the TPL7407L detects the channel input as a low level input and remains in the OFF position. The input RC snubber helps improve noise tolerance when input drivers are in the high-impedance state.

On-chip Power Dissipation

Use the below equation to calculate TPL7407L on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li}$$

Where:

N is the number of channels active together.

V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. (1)

Thermal Reliability

It is recommended to limit TPL7407L IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation. Use the following equation to calculate the maximum allowable on-chip power dissipation for a target IC junction temperature:

$$PD_{(MAX)} = \left(T_{J(MAX)} - T_A\right) / \theta_{JA}$$

Where:

$T_{J(MAX)}$ is the target maximum junction temperature.

T_A is the operating ambient temperature.

θ_{JA} is the package junction to ambient thermal resistance. (2)

Improving Package Thermal Performance

θ_{JA} value depends on the PC board layout. An external heat sink and/or a cooling mechanism, like a cold air fan, can help reduce θ_{JA} and thus improve device thermal capabilities. Refer to TI's design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.

Copyright © 2014, Texas Instruments Incorporated

Application Examples

Unipolar Stepper Motor Driver

Figure 9 shows an implementation of TPL7407L for driving a uniploar stepper motor. The unconnected input channels can be used for other functions. When an input pin is left open the internal 1MΩ pull down resistor pulls the respective input pin to GND potential. For higher noise immunity use an external short across an unconnected input and GND pins. The COM pin must be tied to the supply of whichever inductive load is being driven for the driver to be protected by the free-wheeling diode.

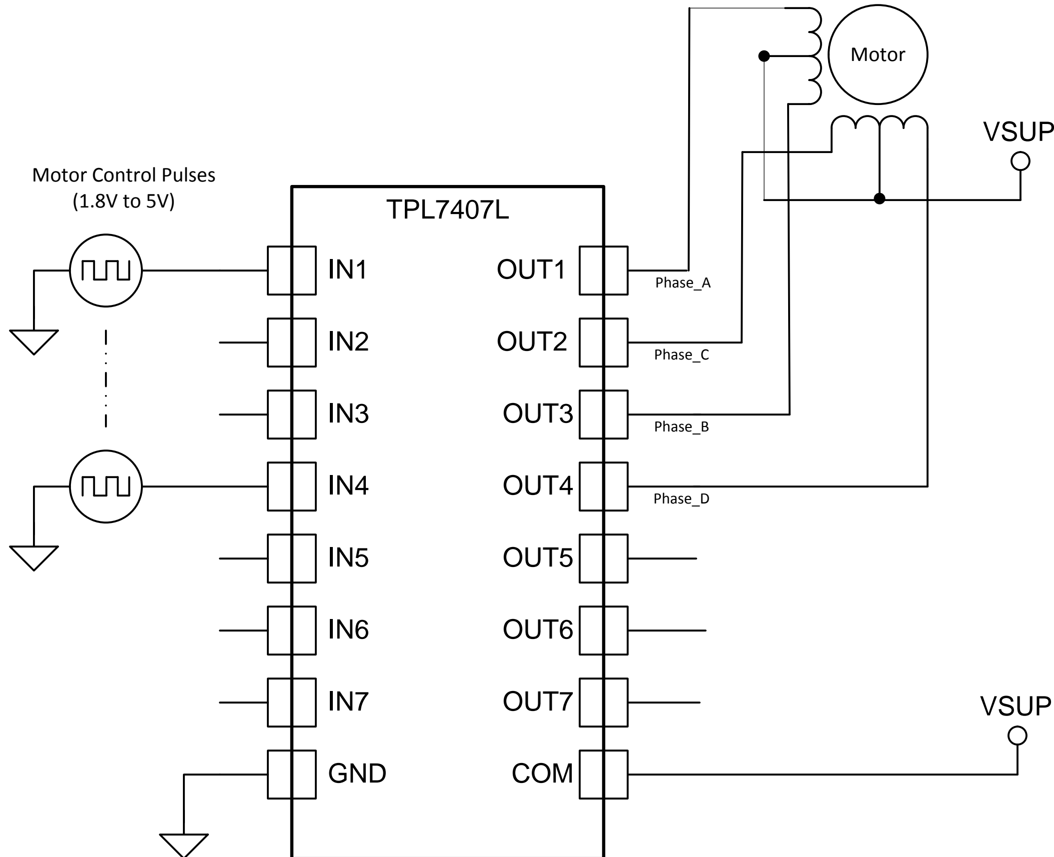


Figure 9. TPL7407L as a Stepper Motor Driver

Multi-Purpose Sink Driver

When configured as per Figure 10 TPL7407L can be used as a multi-purpose driver. The output channels can be tied together to sink more current. TPL7407L can easily drive motors, relays & LEDs with little power dissipation. COM must be tied to highest load voltage, which may or may not be same as inductive load supply.

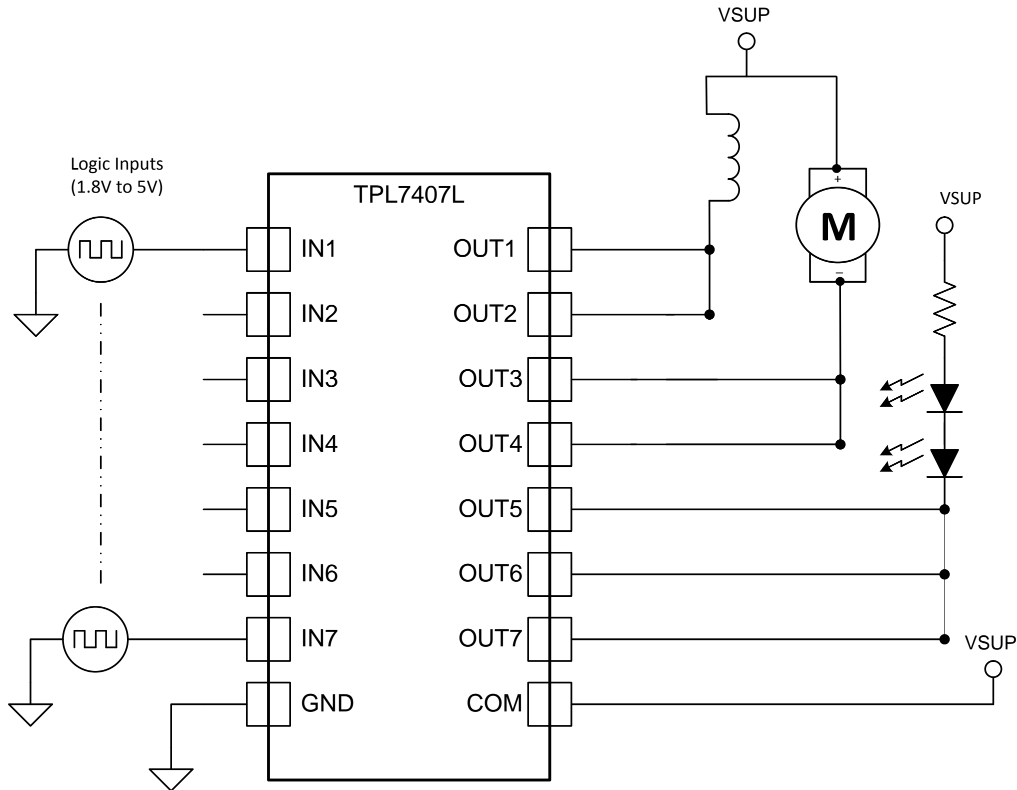


Figure 10. TPL7407L Multi-Purpose Sink Driver Application

Copyright © 2014, Texas Instruments Incorporated

24V Relay Driver

To drive lower resistance relays, like <48Ω , connect two or more adjacent channels in parallel as shown in Figure 11. Connecting several channels in parallel lowers the channel output resistance and increases the drive current. TPL7407L can be used for driving 12V, 24V & 36V relays with similar a implementation.

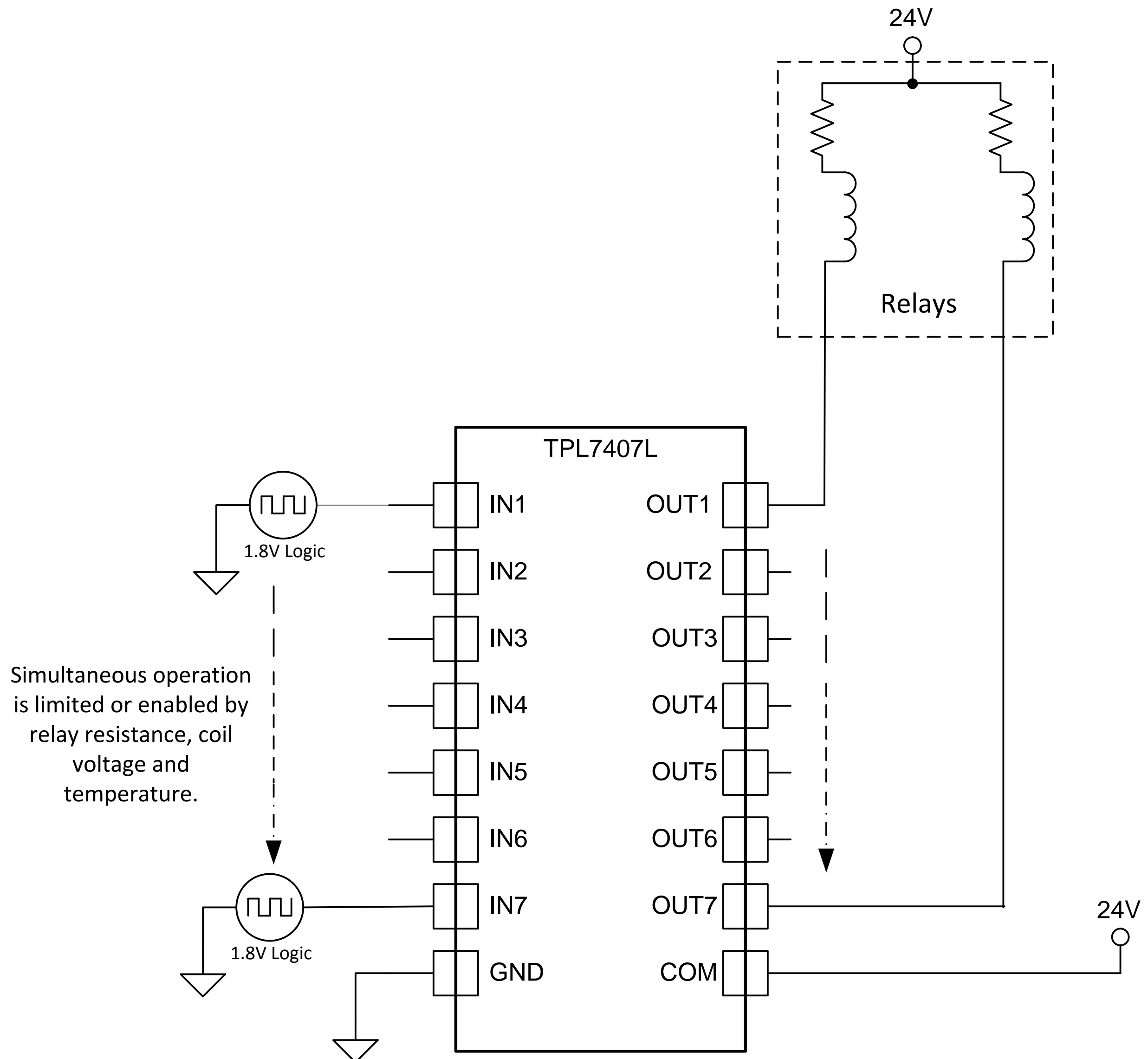


Figure 11. TPL7407L Driving 24V Relays

Copyright © 2014, Texas Instruments Incorporated

REVISION HISTORY

Changes from Original (January 2014) to Revision A **Page**

- 初次发布完整版本。 1

Copyright © 2014, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPL7407LDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	TPL7407L	Samples
TPL7407LPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	TPL7407L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

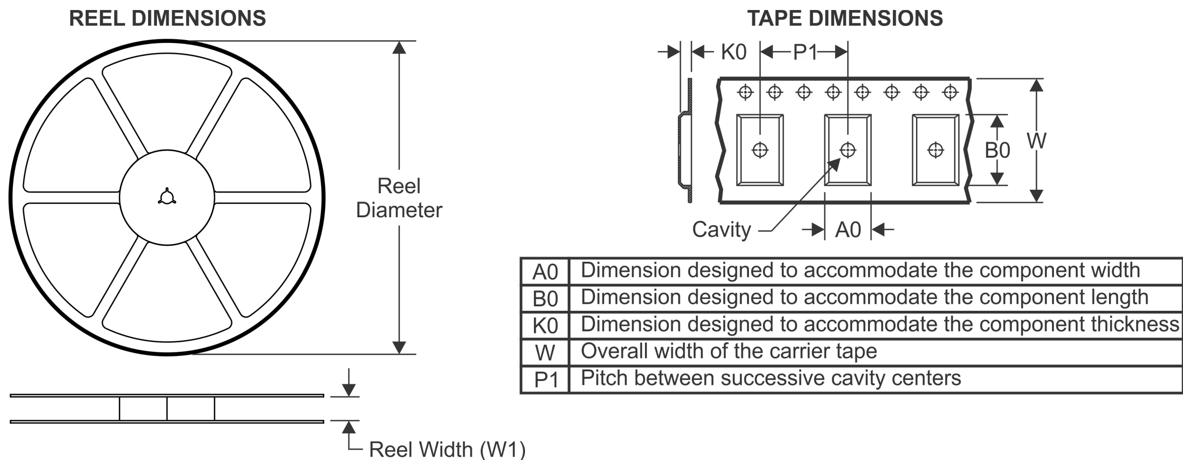
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

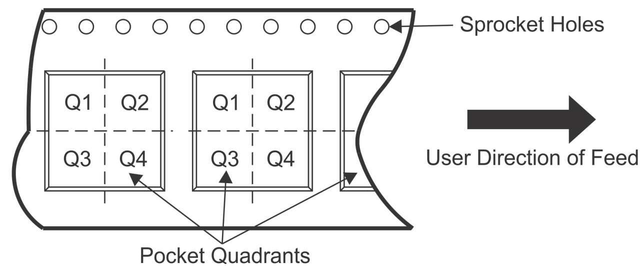
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

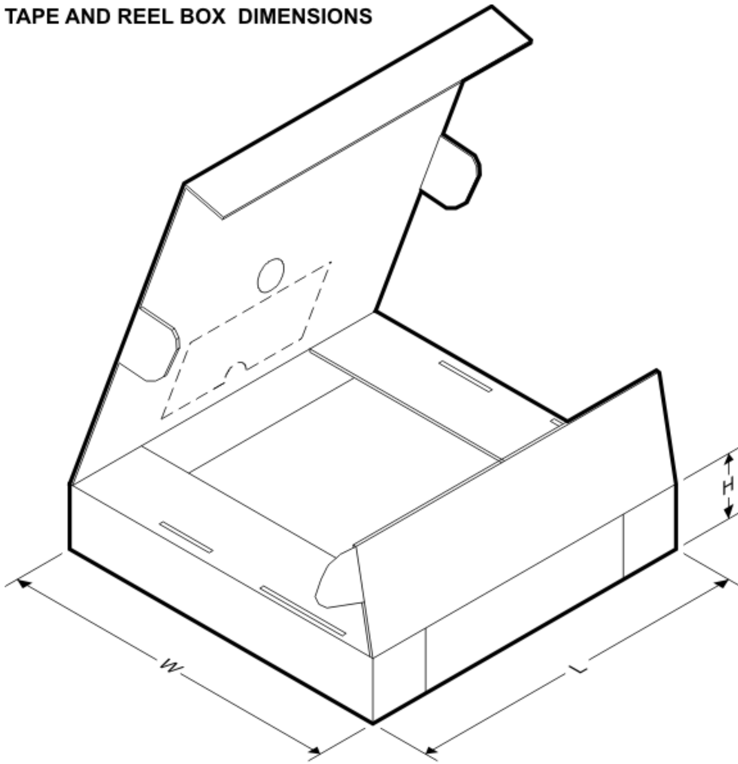
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL7407LDR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
TPL7407LPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

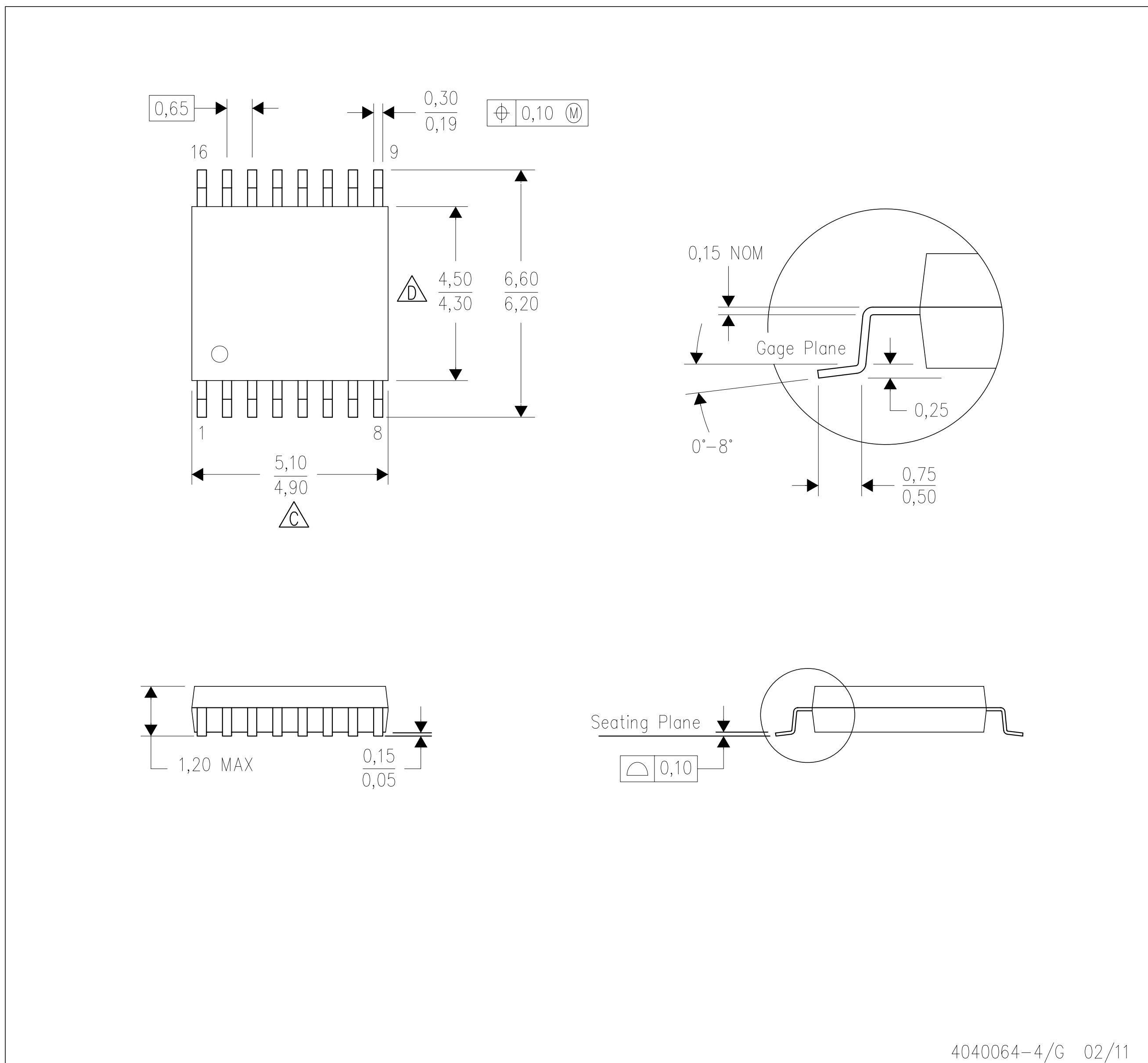
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

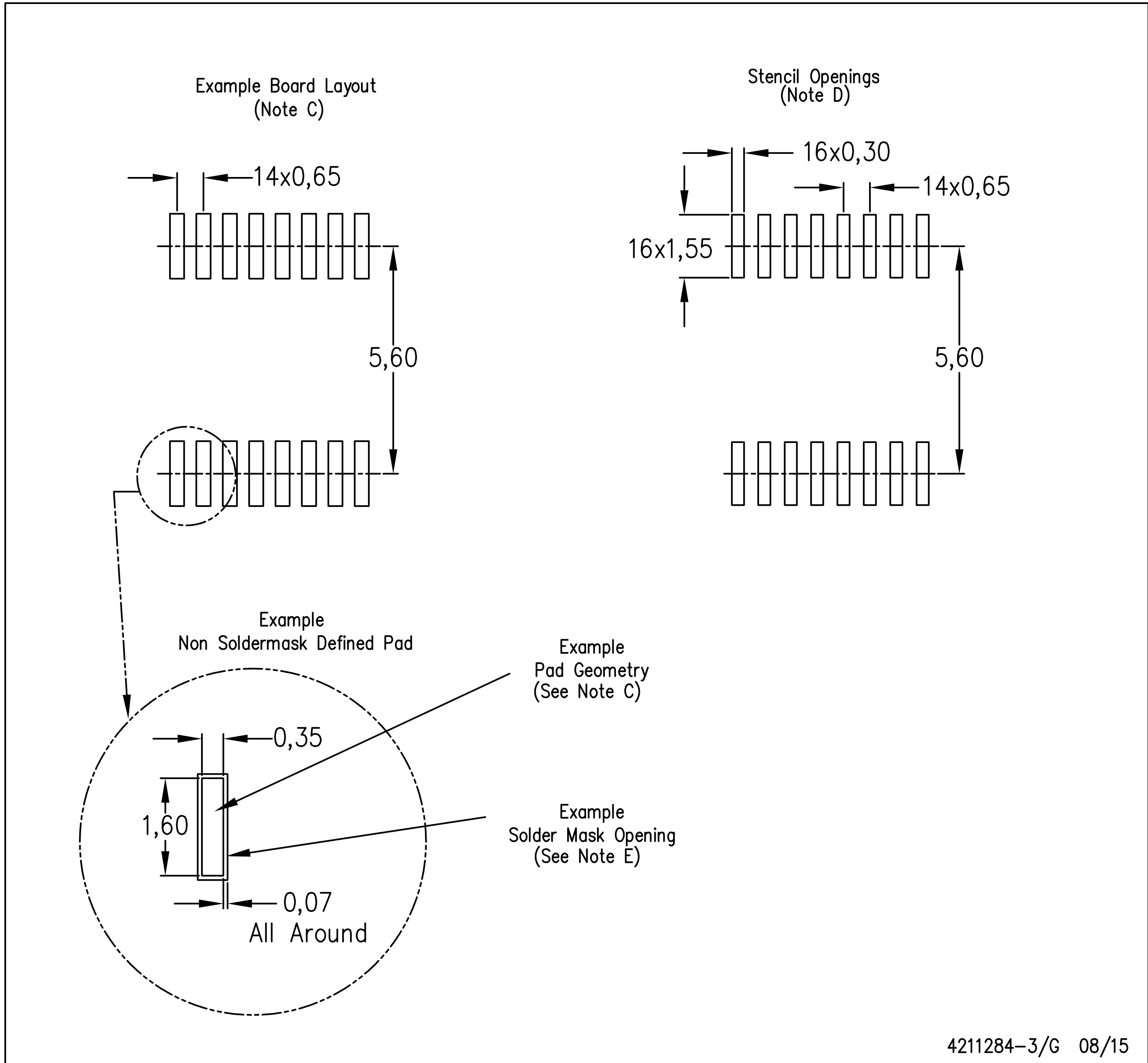
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL7407LDR	SOIC	D	16	2500	364.0	364.0	27.0
TPL7407LPWR	TSSOP	PW	16	2000	364.0	364.0	27.0

PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



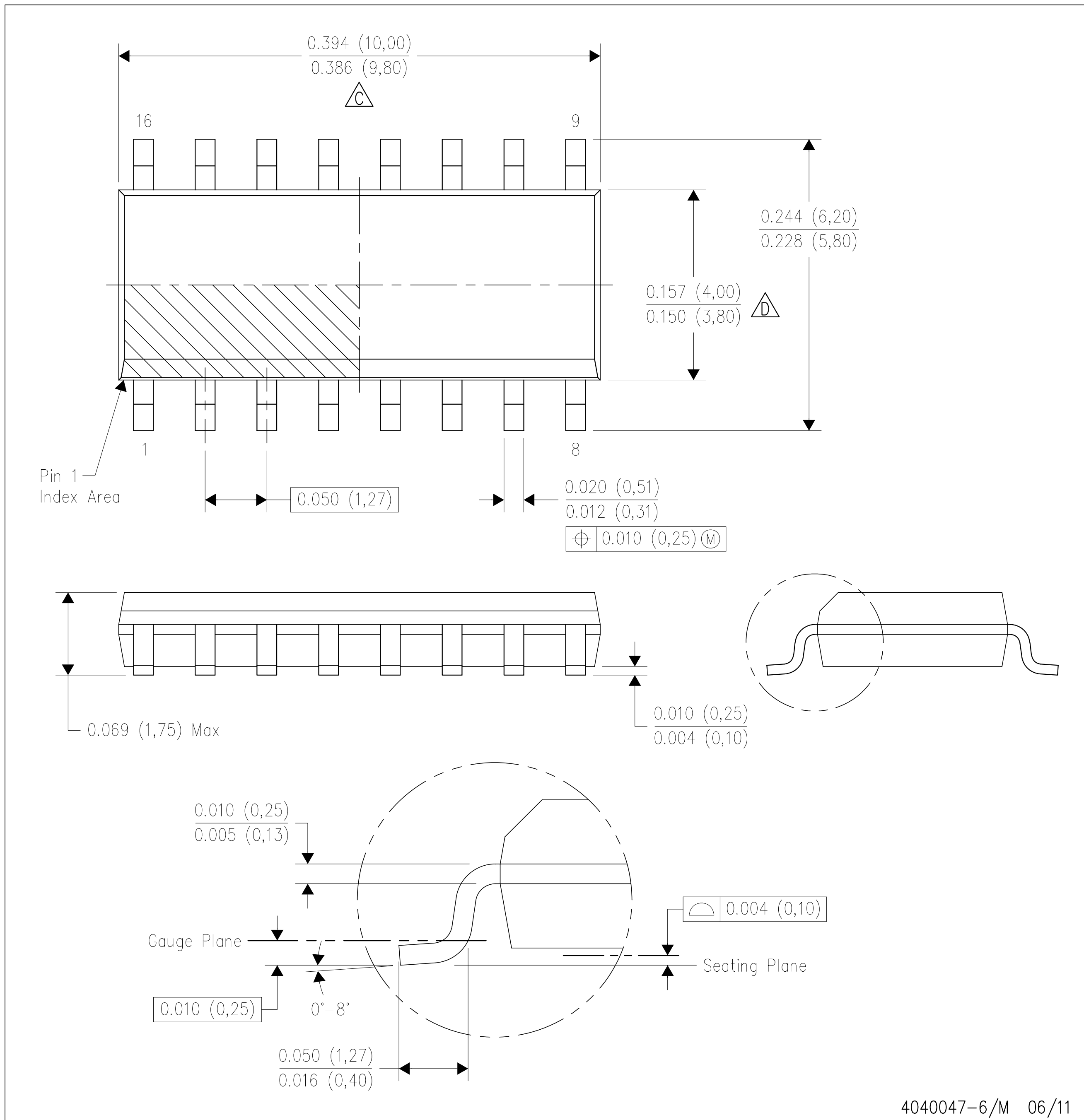
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



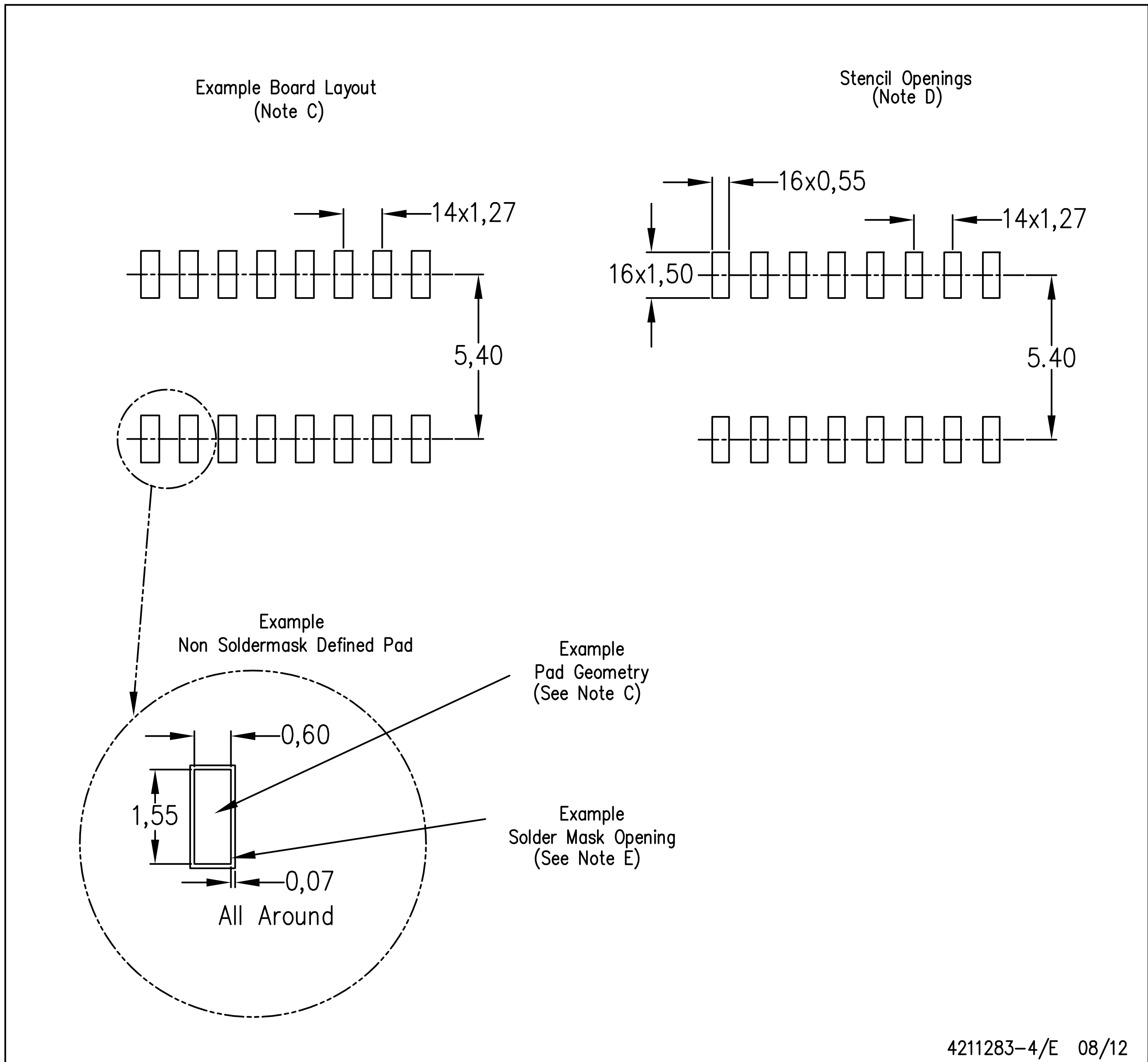
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (http://www.ti.com/sc/docs/stdterms.htm) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称"设计人员"）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权 负责并确保 应用的安全性， 及设计人员的 应用 （包括应用中使用的所有 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的 应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何 应用前， 将彻底测试该等 应用和 该等应用中所用 TI 产品的 功能。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称"TI 资源"），旨在帮助设计人员开发整合了 TI 产品的 应用， 如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的 应用时， 才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法理授予您任何TI知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等产权包括但不限于任何专利权、版权、屏蔽作品权或与使用TI产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系"按原样"提供。TI 兹免除对资源及其使用作出所有其他明确或默认的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的 符合 相关功能安全标准和要求的应用。在应用内使用产品的行为本身不会 配有 任何安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和 标准。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的 产品， 并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2017 德州仪器半导体技术（上海）有限公司