ME2323D/ME2323D-G

P-Channel 20-V (D-S) MOSFET，ESD Protection

GENERAL DESCRIPTION

The ME2323D(-G) is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦50mΩ@V_{GS}=-4.5V
- $R_{DS(ON)}$ ≦65mΩ@V_{GS}=-2.5V
- $R_{DS(ON)}$ ≦75mΩ@V_{GS}=-1.8V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

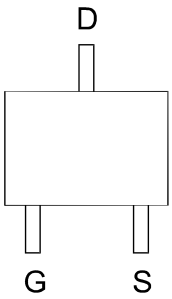
APPLICATIONS

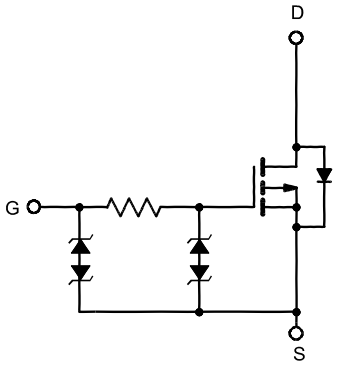
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION

(SOT-23)

Top View





P - Channel

Ordering Information: ME2323D (Pb-free)

ME2323D-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain	T_A=25℃	I_D	-4.2	A
	T_A=70℃		-3.3	
Pulsed Drain Current		I_{DM}	-17	A
Maximum Power Dissipation	T_A=25℃	P_D	1.4	W
	T_A=70℃		0.9	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	90	℃/W

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-0.25	-0.5	-1	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±4.5V			±5	μA
		V_{DS}=0V, V_{GS}=±8V			±10	
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-16V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance[a]	V_{GS}=-4.5V, I_D= -4.0A		45	50	mΩ
		V_{GS}=-2.5V, I_D= -3.0A		52	65	
		V_{GS}=-1.8V, I_D= -2.0A		60	75	
V_{SD}	Diode Forward Voltage	I_S=-1.0A, V_{GS}=0V		-0.78	-1	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=-10V, V_{GS}=-4.5V, I_D=-4A		10.5		nC
Qgs	Gate-Source Charge			0.5		
Qgd	Gate-Drain Charge			3		
Ciss	Input Capacitance	V_{DS}=-10V, V_{GS}=0V, f=1MHz		220		pF
Coss	Output Capacitance			95		
Crss	Reverse Transfer Capacitance			30		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-10V, R_L=2.5Ω, R_{GEN}=3Ω, V_{GS}=-4.5V		560		ns
t_r	Turn-On Rise Time			4000		
$t_{d(off)}$	Turn-Off Delay Time			400		
t_f	Turn-Off Fall Time			4000		

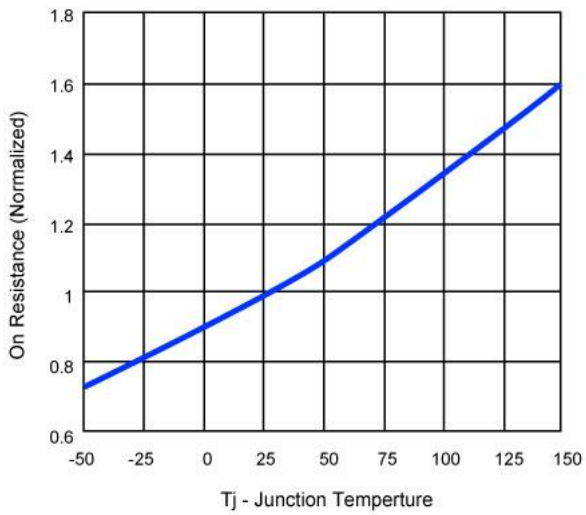
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

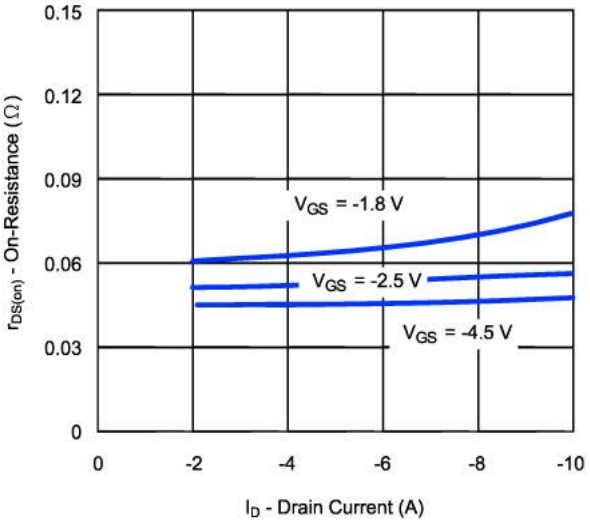
P-Channel 20-V (D-S) MOSFET，ESD Protection

Typical Characteristics (T_J =25℃ Noted)

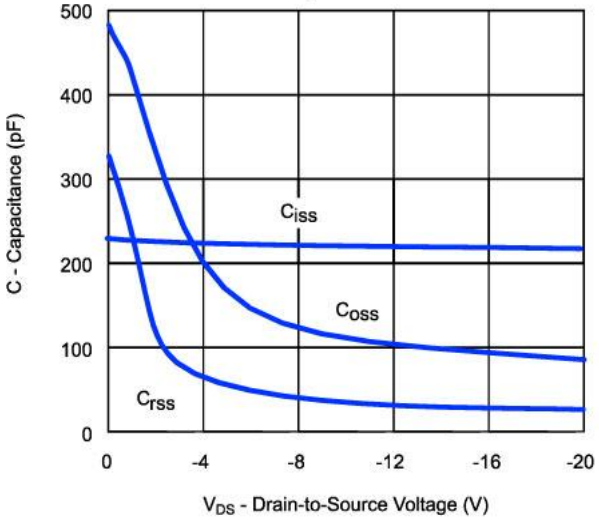
On Resistance vs. Junction Temperture



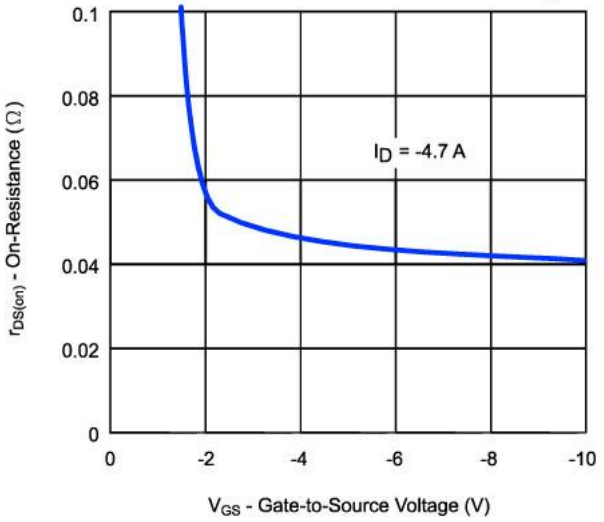
On-Resistance vs. Drain Current



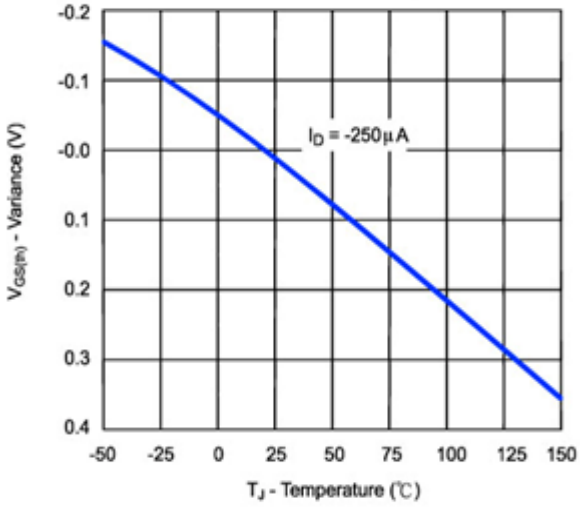
Capacitance



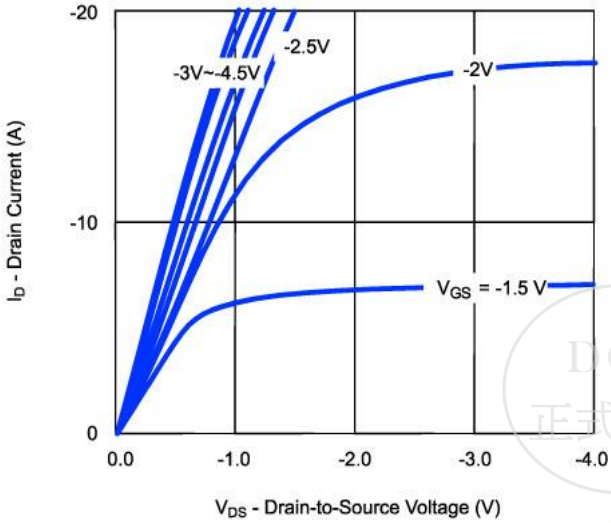
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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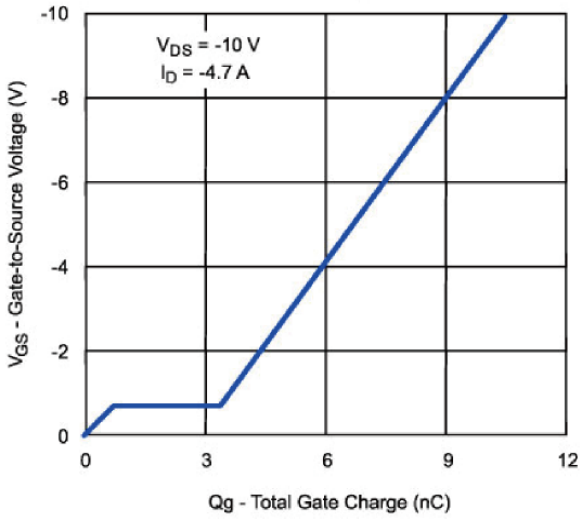
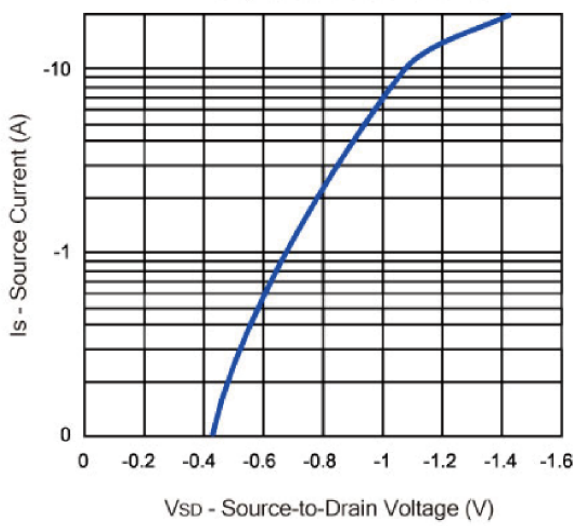
Typical Characteristics (T_J =25℃ Noted)

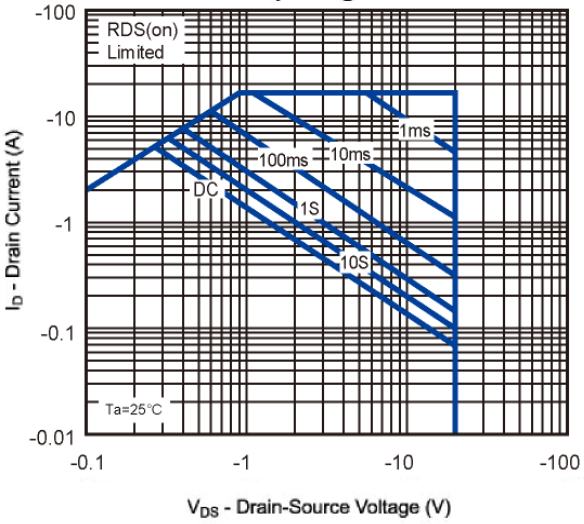
Gate Charge



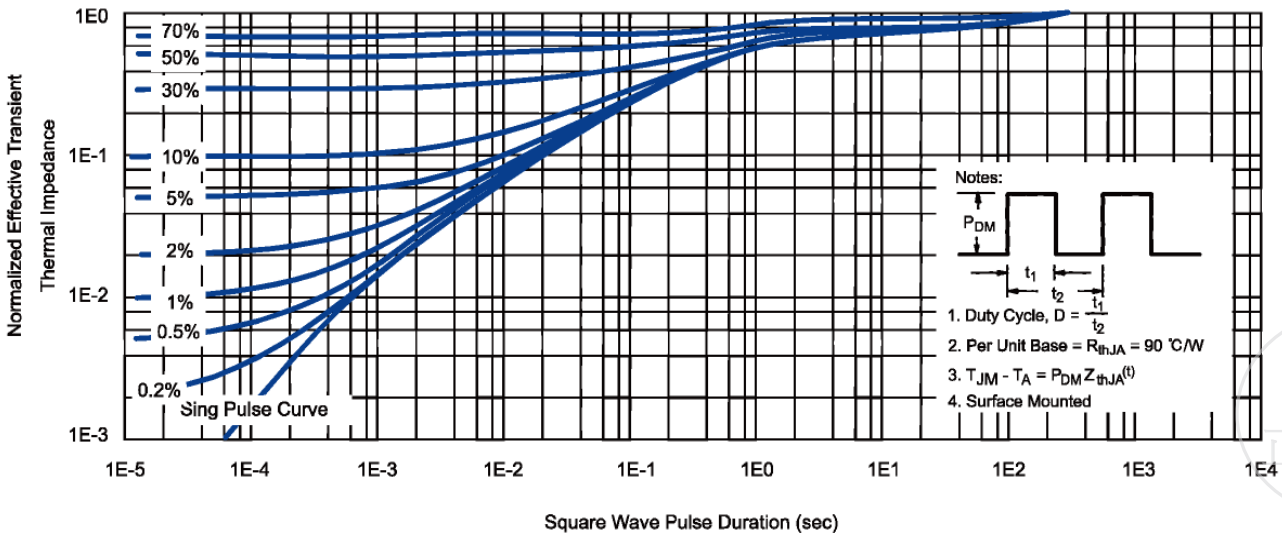
Body-diode characteristics



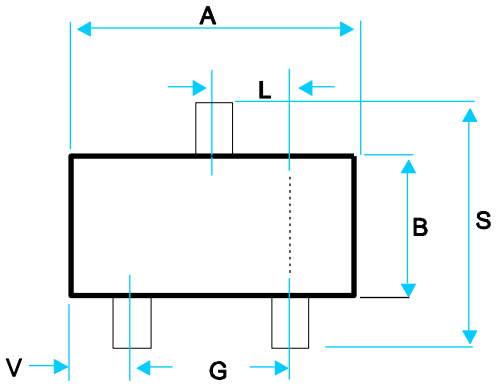
Maximum Forward Biased Safe Operating Area

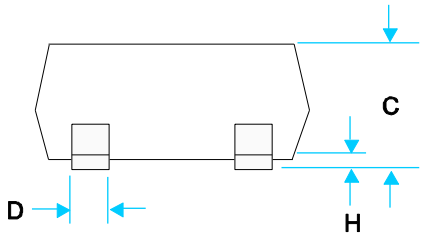


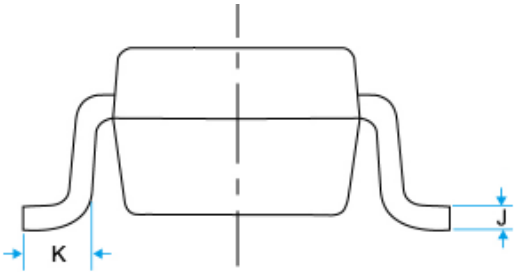
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60