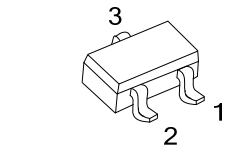
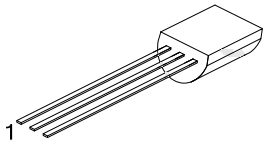
XL/ML1225

SCR

MEDIUM POWER LOW VOLTAGE TRANSISTOR



SOT-23



TO-92

■ DESCRIPTION

The **XL1225/ML1225** silicon controlled rectifiers are high performance planner diffused PNPN devices. These parts are intended for low cost high volume applications.

■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
-	XL1225G-xx-AE3-R	SOT-23	G	K	A	Tape Reel
XL1225L-xx-T92-B	XL1225G-xx-T92-B	TO-92	K	G	A	Tape Box
XL1225L-xx-T92-K	XL1225G-xx-T92-K	TO-92	K	G	A	Bulk
-	ML1225G-xx-AE3-R	SOT-23	G	K	A	Tape Reel
ML1225L-xx-T92-B	ML1225G-xx-T92-B	TO-92	K	G	A	Tape Box
ML1225L-xx-T92-K	ML1225G-xx-T92-K	TO-92	K	G	A	Bulk

Note: Pin Assignment : G: Gate K: Cathode A: Anode

XL1225G-xx-AE3-R (1)Packing Type (2)Package Type (3)Rank (4)Green Package (5) Peak Voltage	(1) B: Tape Box, K: Bulk, R: Tape Reel (2) AE3: SOT-23, T92: TO-92 (3) Refer to CLASSIFICATION OF I_{GT} (4) G: Halogen Free and Lead Free, L: Lead Free (5) XL : 400V , ML: 300V

■ MARKING

Package	MARKING	
	XL1225	ML1225
SOT-23	X25G	L25G
TO-92	UTC XL1225□ □□□ L: Lead Free G: Halogen Free Date Code 1	UTC ML1225□ □□□ L: Lead Free G: Halogen Free Date Code 1

■ ABSOLUATE MAXIUM RATINGS (Ta= 25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Repetitive Peak Off-State Voltage (T_J =40 ~ 125°C, R_{GK} =1kΩ)	XL1225	V_{DRM}	400	V
	ML1225		300	
On-State Current (Tc=40°C)		$I_{T(RMS)}$	0.8	A
Average On-State Current (Half Cycle=180,Tc=40°C)		$I_{T(AV)}$	0.5	A
Peak Reverse Gate Voltage (IGR=10μA)		V_{GRM}	1	V
Peak Gate Current (10μs Max.)		I_{GM}	0.1	A
Gate Dissipation (20ms Max.)		$P_{G(AV)}$	150	mW
Junction Temperature		T_J	+125	°C
Storage Temperature		T_{STG}	-40 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The device is guaranteed to meet performance specification within 0℃~70℃ operating temperature range and assured by design from –20°C ~85°C.

■ ELECTRICAL CHARACTERISTICS (Ta= 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Off State Leakage Current	I_{DRM}	V_{DRM}(R_{GK}=1KΩ), T_J =125°C			0.1	mA
Off State Leakage Current	I_{DRM}	V_{DRM}(R_{GK}=1KΩ), T_J =25°C			1.0	μA
On State Voltage	V_T	AT I_T=0.4A			1.4	V
		AT I_T=0.8A			2.2	
On State Threshold Voltage	$V_{T(TO)}$	T_J =125°C			0.95	V
On State Slops Resistance	Rt	T_J =125°C			600	m
Gate Trigger Current	I_{GT}	V_D=7V			200	μA
Gate Trigger Voltage	V_{GT}	V_D=7V			0.8	V
Holding Current	I_H	R_{GK}=1KΩ			5	mA
Latching Current	I_L	R_{GK}=1KΩ			6	mA
Critical Rate of Voltage Rise	DV/DT	V_D=0.67×V_{DRM}(R_{GK}=1KΩ),T_J =125°C				V/μs
Critical Rate of Current Rise	DV/DT	I_G=10mA, dI_G/dt=0.1A/μs,T_J =125°C				A/μs
Gate Controlled Delay Time	T_{GD}	I_G=10mA, dI_G/dt=0.1A/μs			2.2	μs
Commutated Turn-off Time	TG	T_J =85°C, V_D=0.67*V_{DRM}, V_R=35V, I_T=$I_{T(AV)}$			200	μs

■ CLASSIFICATION OF I_{GT}

RANK	B	C	AA	AB	AC	AD
RANGE	50-100	100-200	8-15	15-20	20-25	25-50

■ TYPICAL CHARACTERICS

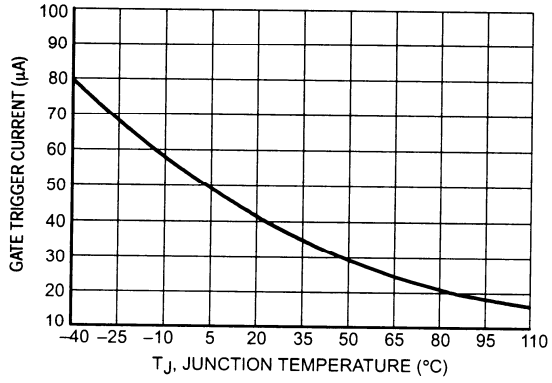


Figure 1. Typical Gate Trigger Current versus Junction Temperature

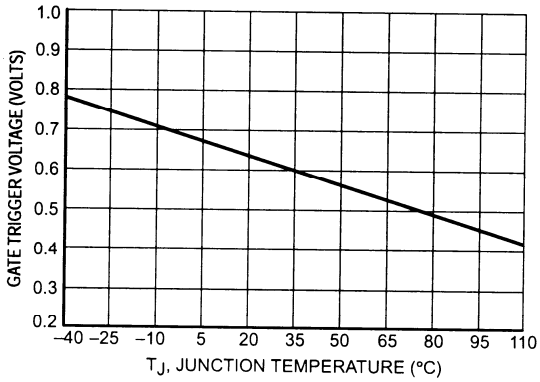


Figure 2. Typical Gate Trigger Voltage versus Junction Temperature

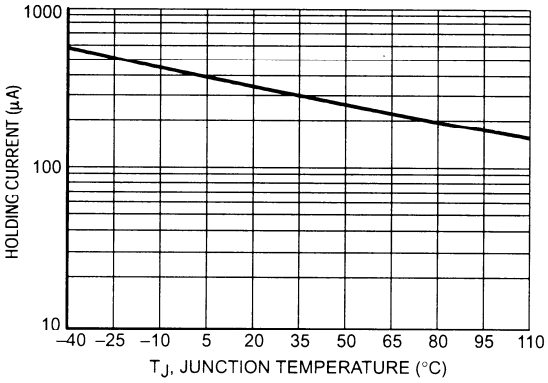


Figure 3. Typical Holding Current versus Junction Temperature

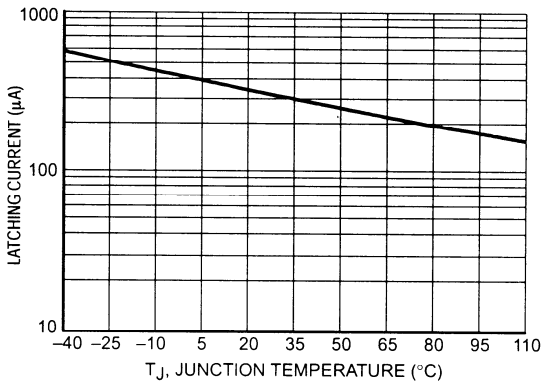


Figure 4. Typical Latching Current versus Junction Temperature

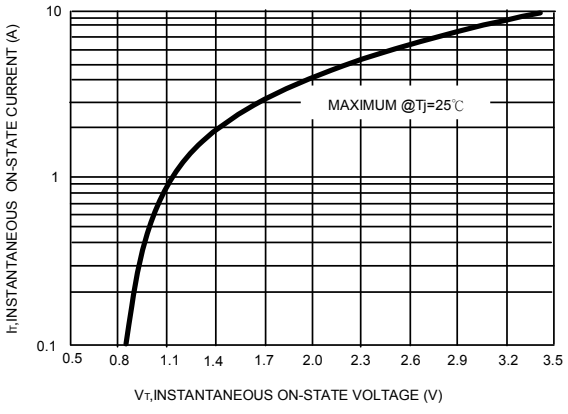


Figure 5. Typical On-State Characteristics