



UF830K

Preliminary

Power MOSFET

4.5A, 500V, 1.5Ω, N-CHANNEL POWER MOSFET

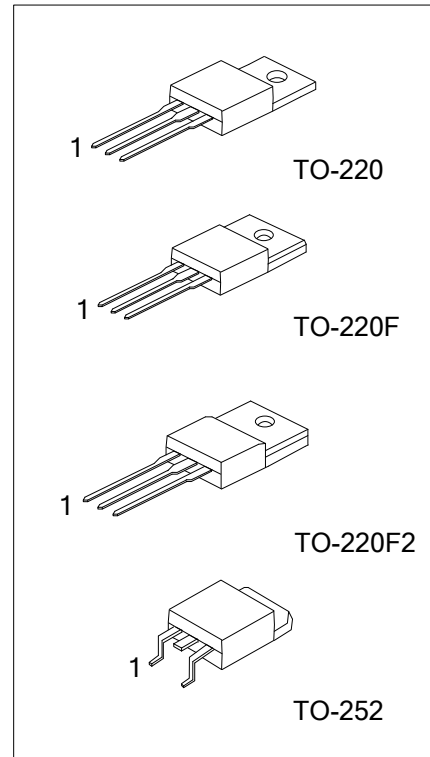
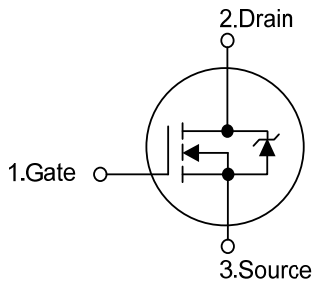
■ **DESCRIPTION**

The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

■ **FEATURES**

- * $R_{DS(ON)} < 1.5\Omega @ I_D = 2.5A$
- * Single Pulse Avalanche Energy Rated
- * Rugged- SOA is Power Dissipation Limited
- * Fast Switching Speeds
- * Linear Transfer Characteristics
- * High Input Impedance

■ **SYMBOL**



■ **ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UF830KL-TA3-T	UF830KG-TA3-T	TO-220	G	D	S	Tube
UF830KL-TF3-T	UF830KG-TF3-T	TO-220F	G	D	S	Tube
UF830KL-TF2-T	UF830KG-TF2-T	TO-220F2	G	D	S	Tube
UF830KL-TN3-R	UF830KG-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UF830KL-TA3-T</p> <p>(1) Packing Type (2) Package Type (3) Lead Free</p>	<p>(1) T: Tube, R: Tape Reel (2) TA3: TO-220, TF3: TO-220F, TF2: TO-220F2, TN3: TO-252 (3) L: Lead Free, G: Halogen Free</p>
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■ **MARKING INFORMATION**

PACKAGE	MARKING
TO-220 TO-220F TO-220F2 TO-252	<p>Lot Code ← UTC UF830K L: Lead Free G: Halogen Free Data Code</p>

■ ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, Unless Otherwise Specified.)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage (T _J =25°C ~125°C)		V _{DS}	500	V
Drain to Gate Voltage (R _{GS} =20kΩ, T _J =25°C ~125°C)		V _{DGR}	500	V
Gate to Source Voltage		V _{GS}	±30	V
Drain Current	Continuous	I _D	4.5	A
	Pulsed	I _{DM}	18	A
Power Dissipation (T _C = 25°C)	TO-220	P _D	73	W
	TO-220F		38	W
	TO-220F2		40	W
	TO-252		50	W
Single Pulse Avalanche Energy Rating (Note 2)		E _{AS}	300	mJ
Junction Temperature		T _J	+150	°C
Storage Temperature		T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. V_{DD}=50V, starting T_J=25°C, L=25mH, R_G=25Ω, peak I_{AS}=4.5A

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	TO-220/TO-220F	θ _{JA}	62.5	°C/W
	TO-220F2			
	TO-252			
Junction to Case	TO-220	θ _{Jc}	1.71	°C/W
	TO-220F		3.31	
	TO-220F2		3.125	
	TO-252		2.5	°C/W

■ ELECTRICAL SPECIFICATIONS (T_A =25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	500			V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} =V _{DS} , I _D =250μA	2.0		4.0	V
On-State Drain Current (Note 1)	I _{D(ON)}	V _{DS} >I _{D(ON)} ×R _{DS(ON)MAX} , V _{GS} =10V	4.5			A
Drain-Source Leakage Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} =0V			25	μA
		V _{DS} =0.8×Rated BV _{DSS} V _{GS} =0V, T _J = 125°C			250	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V			±100	nA
Static Drain-Source On-State Resistance	R _{DS(ON)}	I _D =2.5A, V _{GS} =10V (Note 2)		1.23	1.5	Ω
Forward Transconductance (Note 1)	g _{FS}	V _{DS} ≥10V, I _D =2.7A	2.5	4.2		S
Turn-On Delay Time	t _{D(ON)}	V _{DD} =30V, I _D ≈0.5A R _{GS} =12Ω, R _L =54Ω (Note 2)		48	60	ns
Turn-On Rise Time	t _R			48	60	ns
Turn-Off Delay Time	t _{D(OFF)}			40	53	ns
Turn-Off Fall Time	t _F			44	60	ns
Total Gate Charge	Q _G		V _{GS} =10V, I _D =1.3A		14	32
Gate-Source Charge	Q _{GS}	V _{DS} =50V		5.4		nC
Gate-Drain Charge	Q _{GD}	I _{G(REF)} =100μA (Note 3)		6		nC
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		590		pF
Output Capacitance	C _{OSS}			80		pF
Reverse Transfer Capacitance	C _{RSS}			15		pF

Notes: 1. Pulse Test: Pulse width≤300μs, Duty Cycle≤2%.

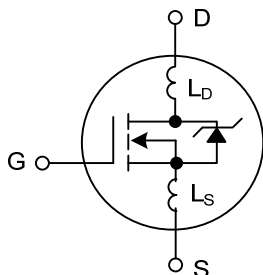
2. MOSFET Switching Times are Essentially Independent of Operating Temperature.

3. Gate Charge is Essentially Independent of Operating Temperature.

INTERNAL PACKAGE INDUCTANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Internal Drain Inductance					
Measured from the contact screw on tab to center of die	L_D		3.5		nH
Measured from the drain lead(6mm from package) to center of die			4.5		nH
Internal Source Inductance					
Measured from the source lead(6mm from header) to source bond pad	L_S		7.5		nH

Remark: Modified MOSFET symbol showing the internal devices inductances as below.

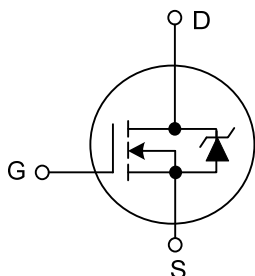


SOURCE TO DRAIN DIODE SPECIFICATIONS

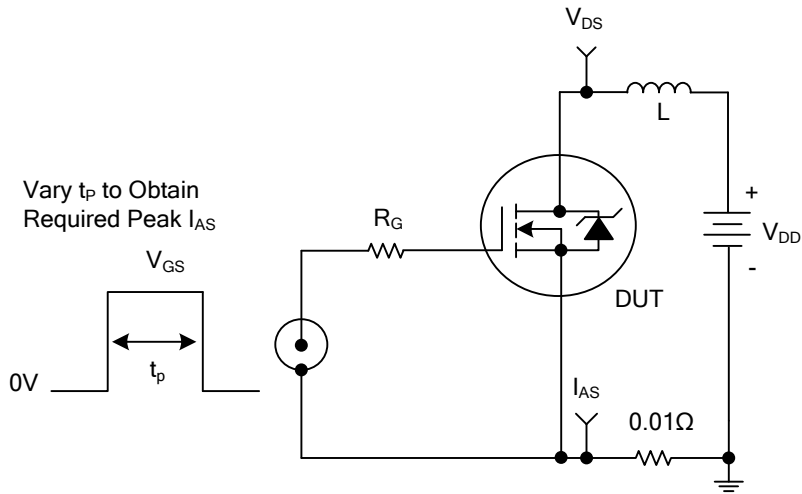
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Source to Drain Diode Voltage	V_{SD}	$T_J=25^{\circ}\text{C}, I_{SD}=4.5\text{A}, V_{GS}=0\text{V}$ (Note 1)			1.6	V
Continuous Source to Drain Current	I_{SD}	(Note 2)			5.5	A
Pulse Source to Drain Current	I_{SDM}				18	A
Reverse Recovery Time	t_{rr}	$T_J=25^{\circ}\text{C}, I_{SD}=4.5\text{A}, dI/dt=100\text{A}/\mu\text{s}$	180	350	760	ns
Reverse Recovery Charge	Q_{RR}	$T_J=25^{\circ}\text{C}, I_{SD}=4.5\text{A}, dI/dt=100\text{A}/\mu\text{s}$	0.96	2.2	4.3	μC

Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

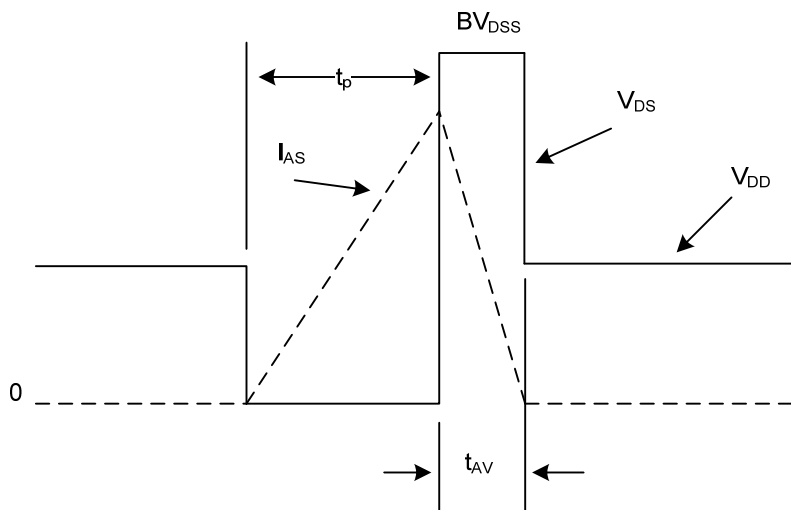
2. Modified MOSFET symbol showing the integral reverse P-N junction diode as below.



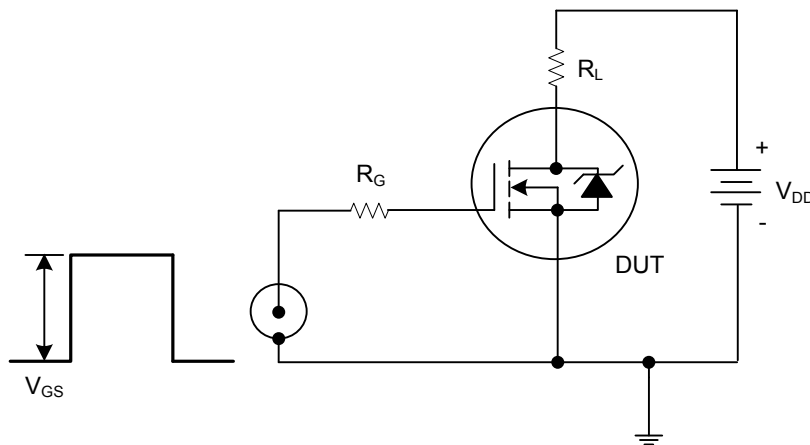
■ TEST CIRCUITS AND WAVEFORMS



Unclamped Energy Test Circuit

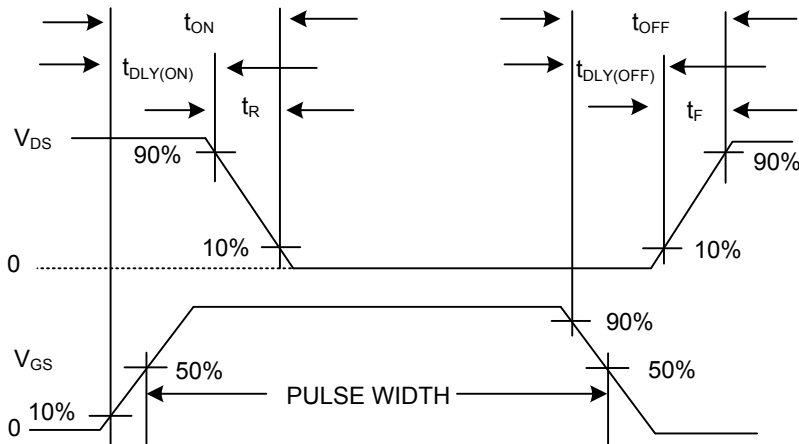


Unclamped Energy Waveforms

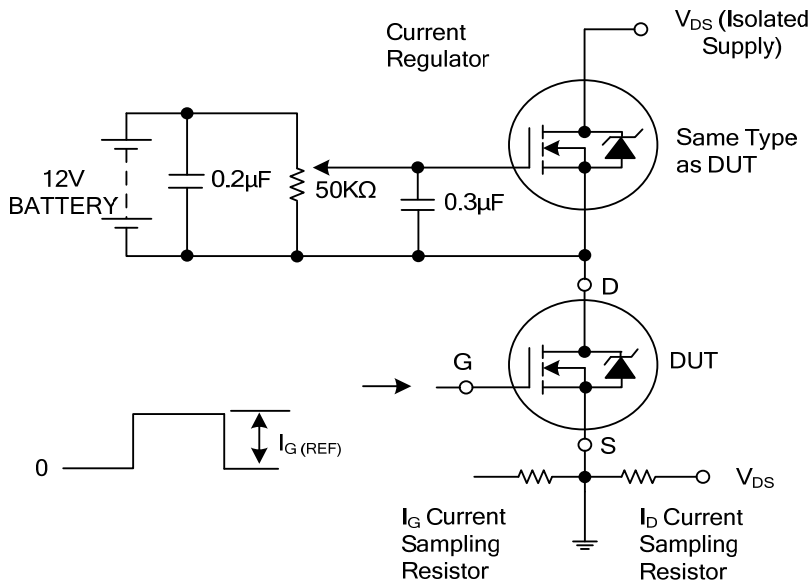


Switching Time Test Circuit

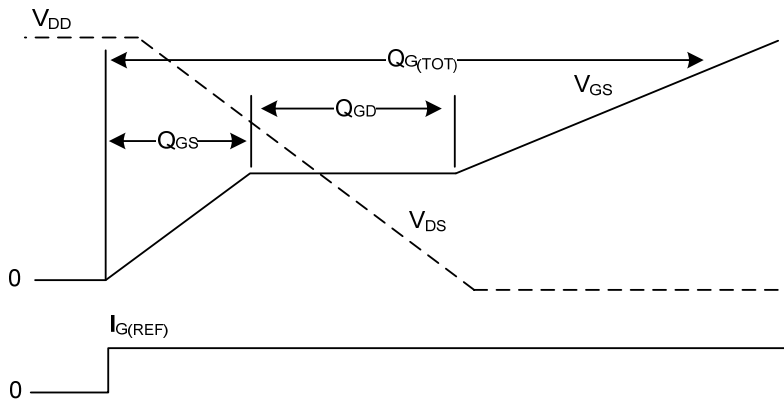
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



Resistive Switching Waveforms



Gate Charge Test Circuit



Gate Charge Waveforms

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