P-Channel 30V (D-S) MOSFET

GENERAL DESCRIPTION

The ME2307 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦70mΩ@V_{GS}=-10V
- $R_{DS(ON)}$ ≦95mΩ@V_{GS}=-4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$

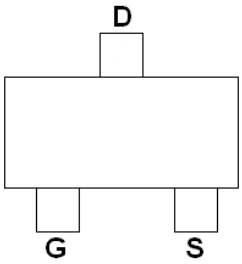
APPLICATIONS

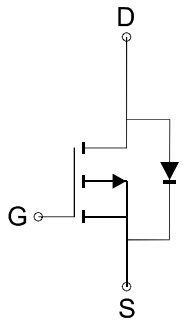
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION

(SOT-23)

Top View





P-Channel MOSFET

Ordering Information:ME2307 (Pb-free)

ME2307-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current *	T_A=25℃	I_D	-3.5	A
	T_A=70℃		-2.8	
Pulsed Drain Current		I_{DM}	-14	A
Maximum Power Dissipation	T_A=25℃	P_D	1.4	W
	T_A=70℃		0.9	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	90	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1		-3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance [a]	V_{GS}=-10V, I_D= -3.2A		58	70	mΩ
		V_{GS}=-4.5V, I_D= -2.5A		75	95	
V_{SD}	Diode Forward Voltage	I_S=-1A, V_{GS}=0V		-0.8	-1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=-15V,V_{GS}=-10V,I_D=-1.7A		14	18	nC
Qg	Total Gate Charge	V_{DS}=-15V, V_{GS}=-4.5V, I_D=-1.7A		6.8		
Qgs	Gate-Source Charge			2.8		
Qgd	Gate-Drain Charge			2.3		
Rg	Gate resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		3.5	4.5	Ω
Ciss	Input Capacitance	V_{DS}=-15V, V_{GS}=0V, f=1MHz		460	540	pF
Coss	Output Capacitance			74		
Crss	Reverse Transfer Capacitance			23		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-15V, R_L =15Ω R_{GEN}=6Ω, V_{GS}=-10V		33	43	ns
t_r	Turn-On Rise Time			17	22	
$t_{d(off)}$	Turn-Off Delay Time			39	52	
t_f	Turn-Off Fall time			5	6.5	

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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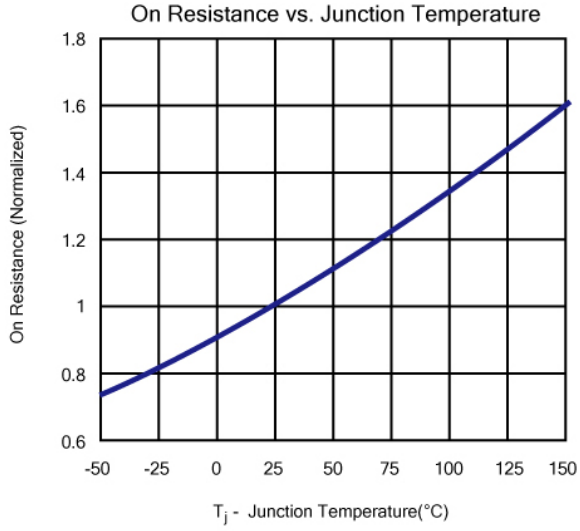
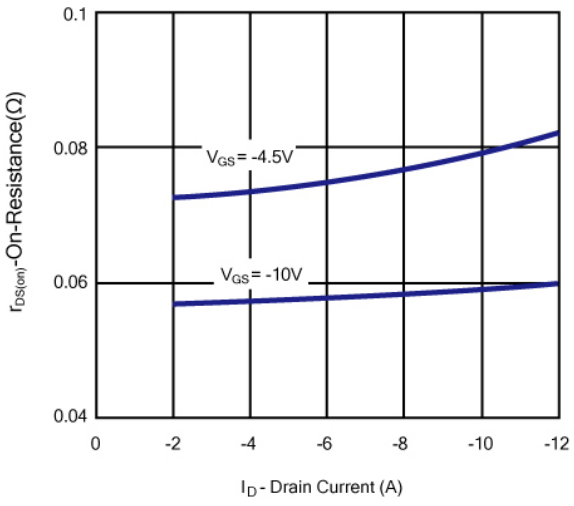
Typical Characteristics (T_J =25℃ Noted)

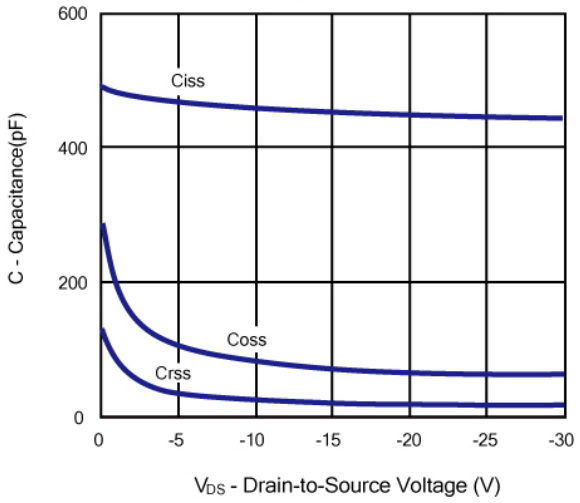
On Resistance vs. Junction Temperature



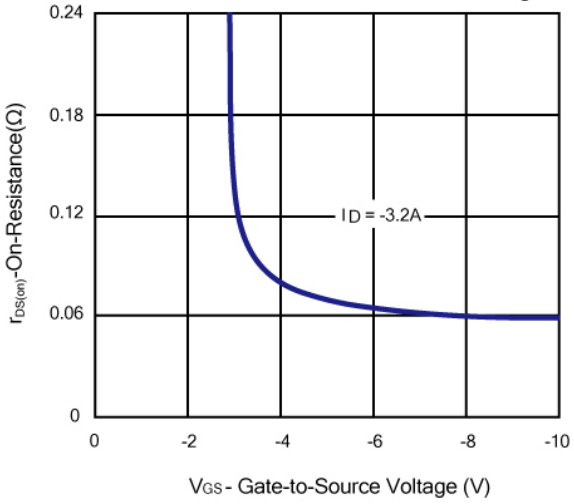
On-Resistance vs. Drain Current



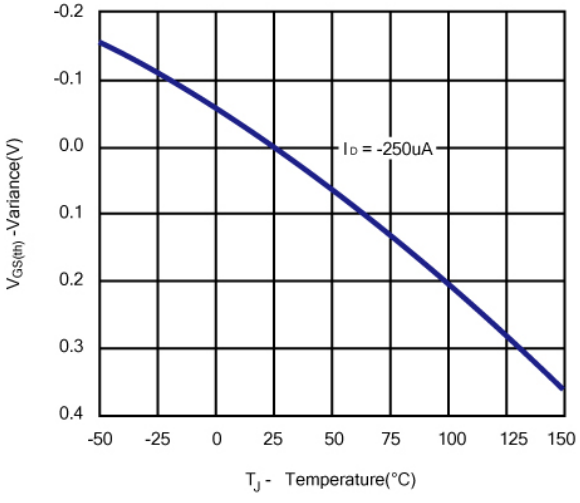
Capacitance



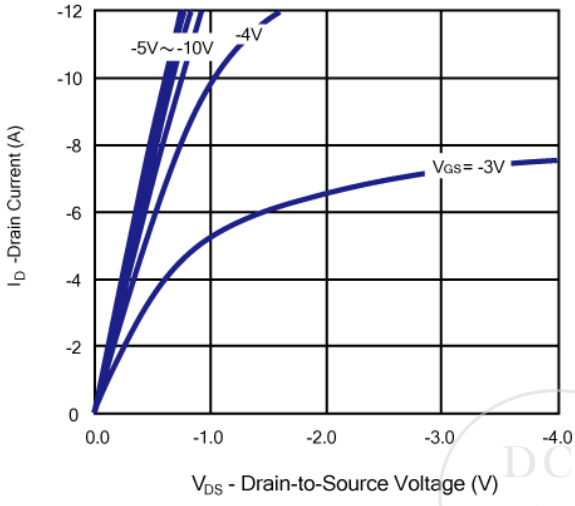
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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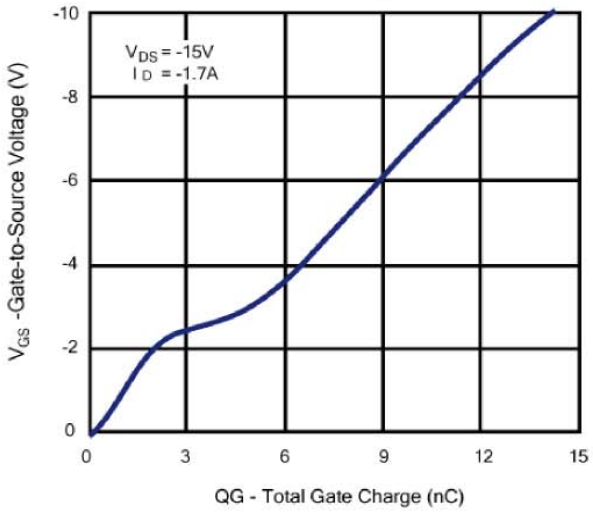
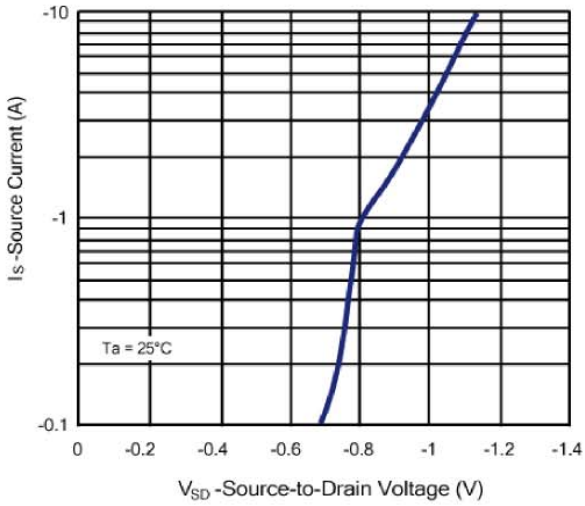
Typical Characteristics (T_J =25℃ Noted)

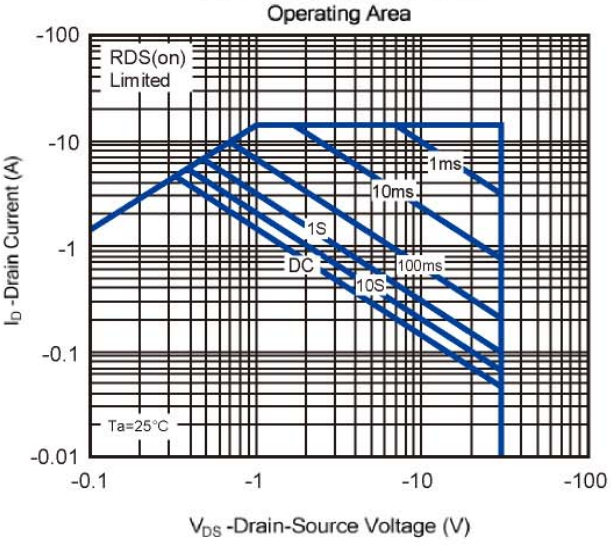
Gate Charge



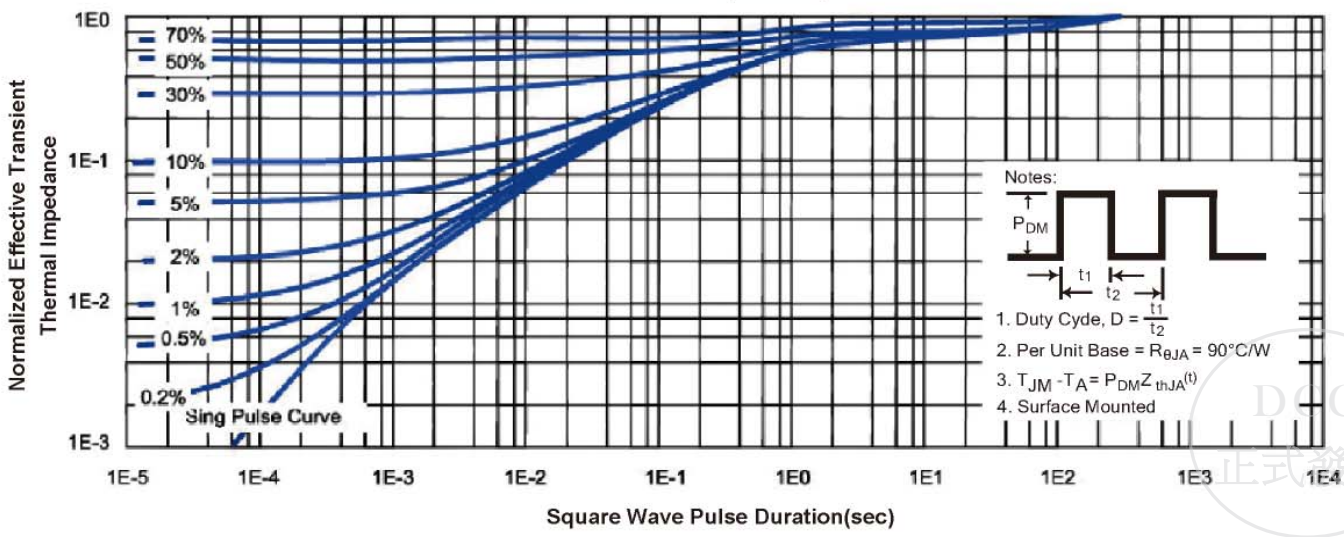
Body-diode characteristics



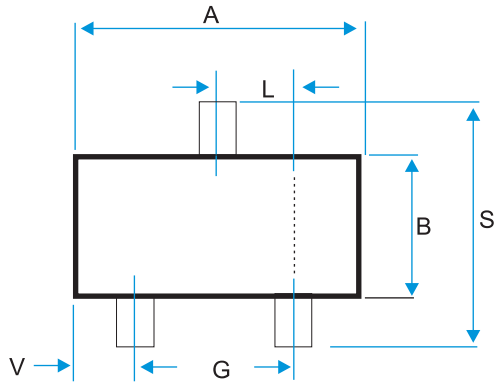
Maximum Forward Biased Safe Operating Area

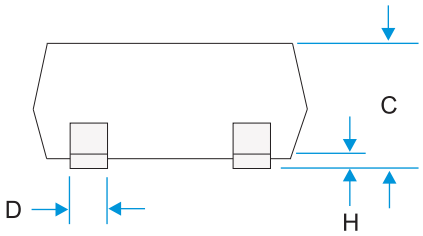


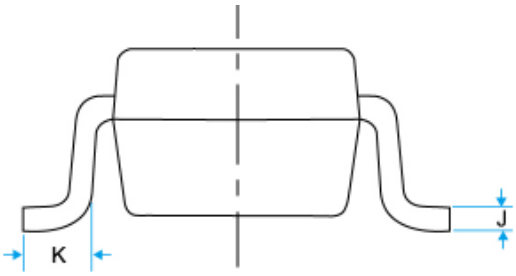
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60