

P- Channel 30V (D-S) MOSFET

GENERAL DESCRIPTION

The ME85P03 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where switching, and low in-line power loss are needed in a very small outline surface mount package.

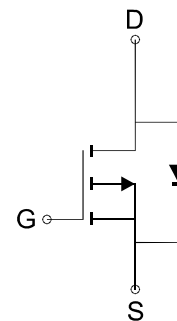
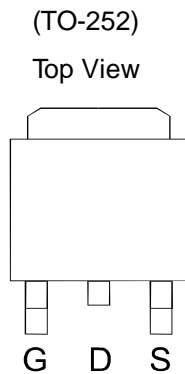
FEATURES

- $R_{DS(ON)} \leq 8m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 11m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION



P-Channel MOSFET

Ordering Information: ME85P03 (Pb-free)

ME85P03-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_A = 25^\circ C$ Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current*	I_D	$T_C = 25^\circ C$	-80
		$T_C = 70^\circ C$	-65
Pulsed Drain Current (Package limited)	I_{DM}	-200	A
Maximum Power Dissipation*	P_D	$T_C = 25^\circ C$	83
		$T_C = 70^\circ C$	53
Operating Junction Temperature	T_J	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Case*	$R_{\theta JC}$	1.5	

*The device mounted on 1in² FR4 board with 2 oz copper



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Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μA	-30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-1		-3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V			-1	μA
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =-10V, I _D = -20A		6.7	8	mΩ
		V _{GS} =-4.5V, I _D = -20A		8.4	11	
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.7	-1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _D =-20A		88		nC
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-4.5V, I _D =-20A		44		
Q _{gs}	Gate-Source Charge			12.5		
Q _{gd}	Gate-Drain Charge			19.5		
C _{iss}	Input capacitance	V _{DS} =-15V, V _{GS} =0V, F=1MHz		3887		pF
C _{oss}	Output Capacitance			432		
C _{rss}	Reverse Transfer Capacitance			372		
t _{d(on)}	Turn-On Delay Time	V _{DS} =-15V, R _L =15Ω V _{GS} =-10V, R _G =6Ω I _D =-1A		48		ns
t _r	Turn-On Rise Time			20		
t _{d(off)}	Turn-Off Delay Time			170		
t _f	Turn-Off Fall Time			54		

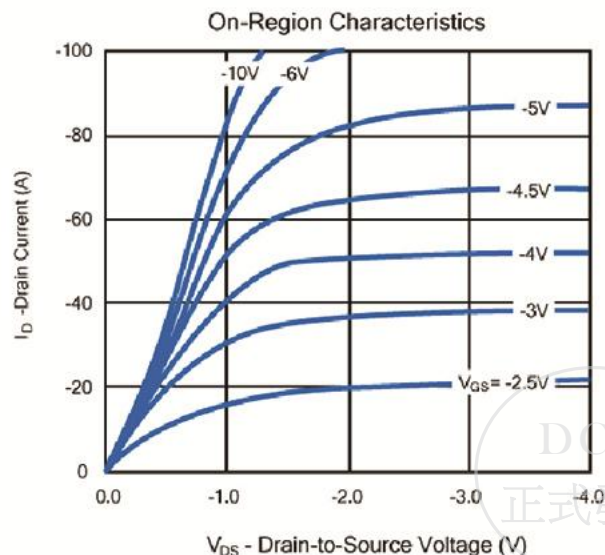
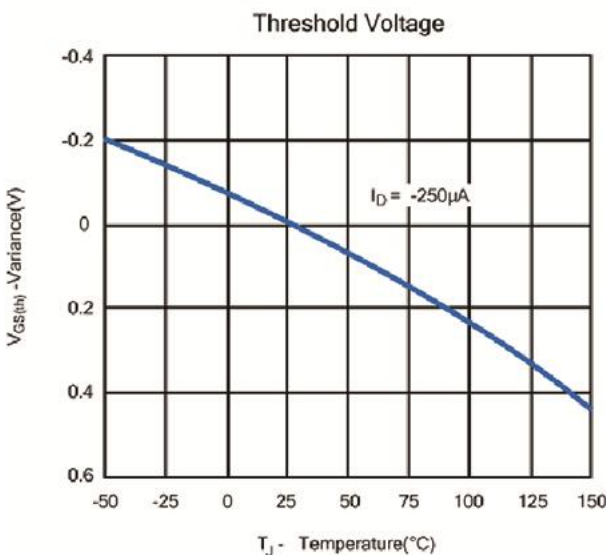
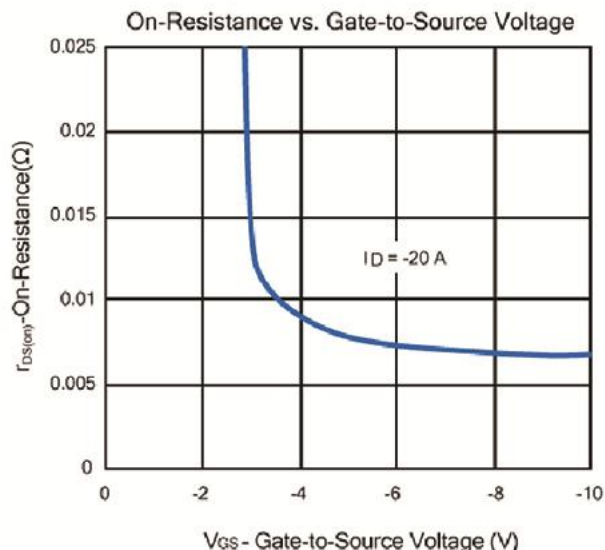
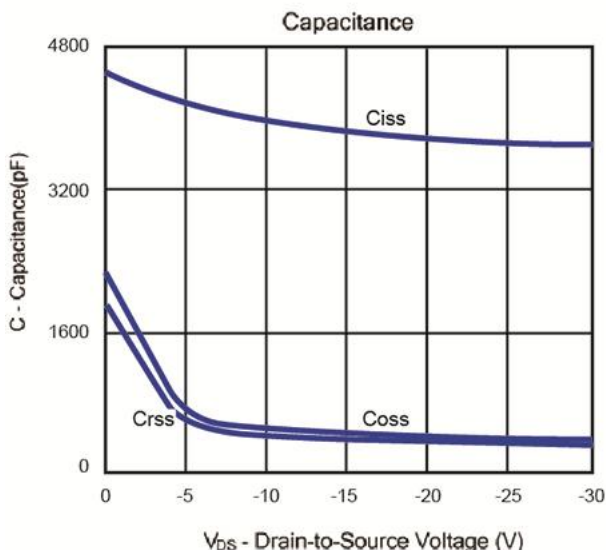
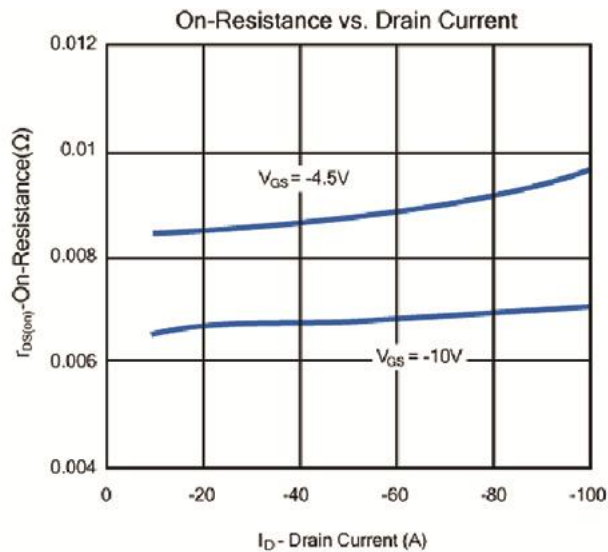
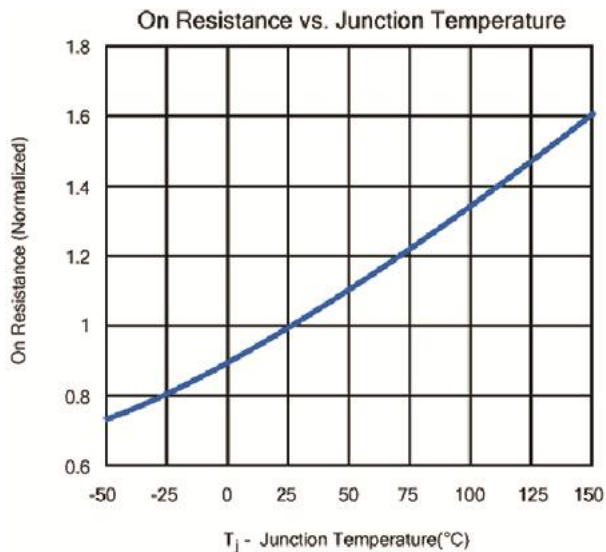
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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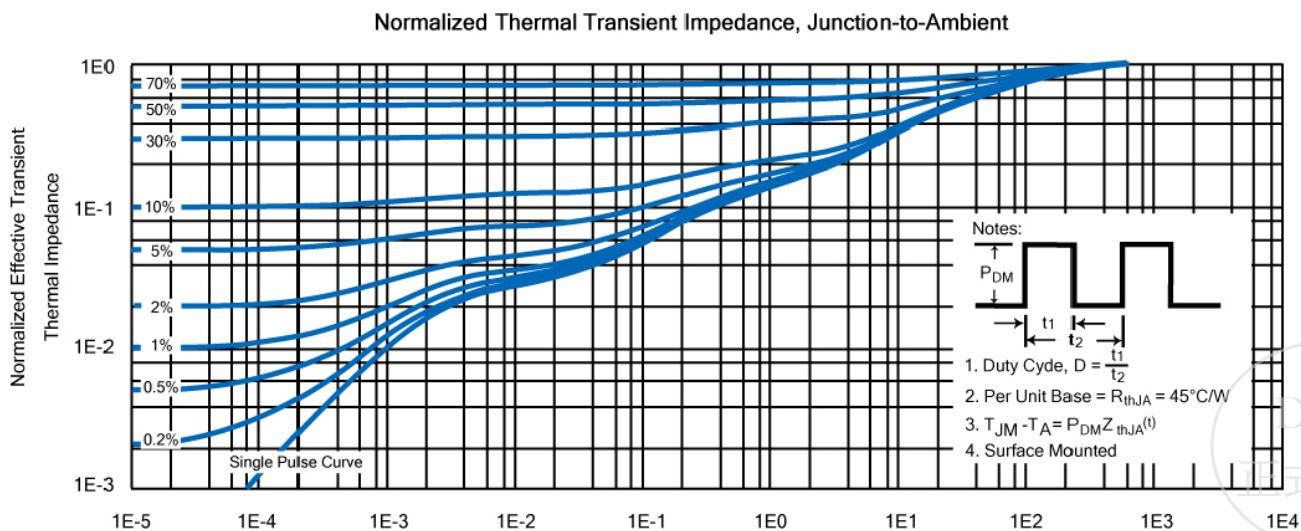
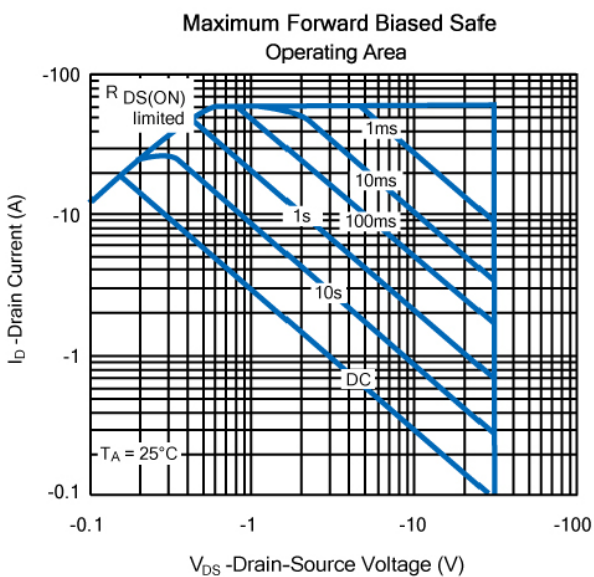
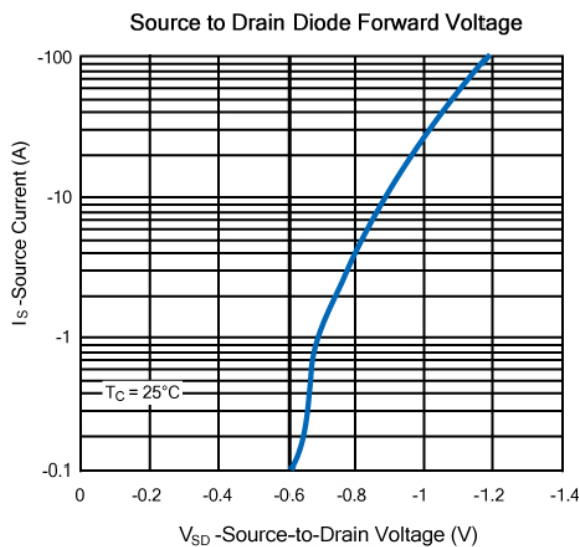
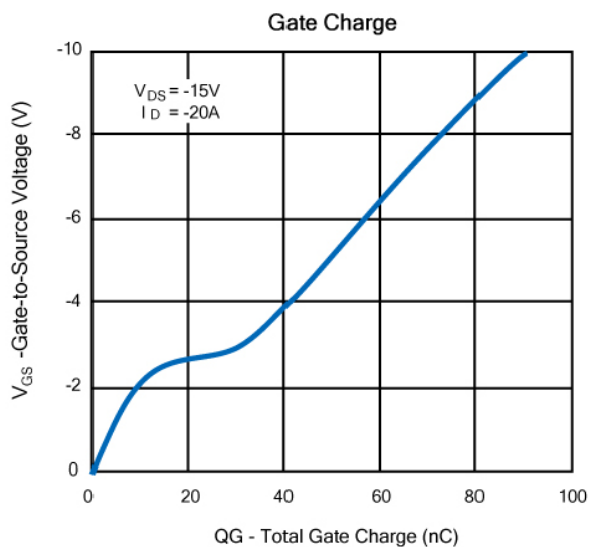
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Typical Characteristics (T_J = 25°C Noted)

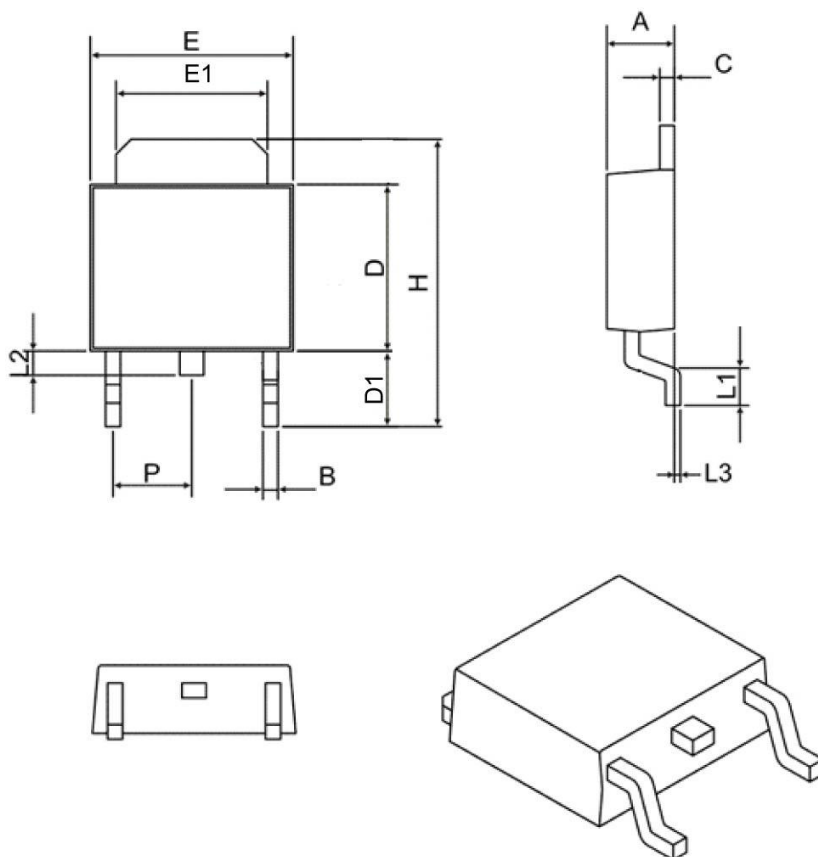


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Typical Characteristics (T_J = 25°C Noted)



TO-252 Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	

