

**N-Channel 60-V (D-S) MOSFET**

**GENERAL DESCRIPTION**

The ME25N06 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

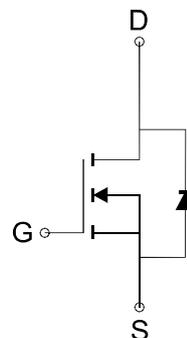
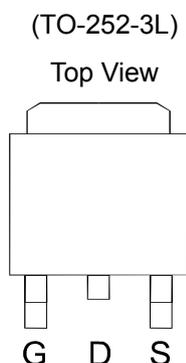
**FEATURES**

- $R_{DS(ON)} \leq 62m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 86m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

**APPLICATIONS**

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

**PIN CONFIGURATION**



Ordering Information: ME25N06 (Pb-free)

ME25N06-G (Green product-Halogen free)

**Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)**

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Continuous Drain Current	$I_D$	$T_C=25^\circ C$	16
		$T_C=70^\circ C$	13
Pulsed Drain Current	$I_{DM}$	65	A
Maximum Power Dissipation	$P_D$	$T_C=25^\circ C$	25
		$T_C=70^\circ C$	16
Operating Junction Temperature	$T_J$	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Case*	$R_{\theta JC}$	5	$^\circ C/W$

\* The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper



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Electrical Characteristics ( $T_J = 25^\circ\text{C}$  Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\ \mu A$	60			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\ \mu A$	1		3	V
$I_{GSS}$	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 25V$			$\pm 100$	nA
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=60V, V_{GS}=0V$			1	$\mu A$
$R_{DS(on)}$	Drain-Source On-Resistance <sup>a</sup>	$V_{GS}=10V, I_D=15A$		52	62	m $\Omega$
		$V_{GS}=4.5V, I_D=10A$		70	86	
$V_{SD}$	Diode Forward Voltage	$I_S=15A, V_{GS}=0V$		1	1.2	V
<b>DYNAMIC</b>						
$Q_g$	Total Gate Charge	$V_{DS}=48V, V_{GS}=10V, I_D=16A$		17		nC
$Q_{gs}$	Gate-Source Charge			4.2		
$Q_{gd}$	Gate-Drain Charge			5		
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$		0.6		$\Omega$
$C_{iss}$	Input Capacitance	$V_{DS}=30V, V_{GS}=0V, f=1MHz$		523		pF
$C_{oss}$	Output Capacitance			47		
$C_{rss}$	Reverse Transfer Capacitance			14		
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=30V, R_L=15\ \Omega$ $V_{GEN}=10V, R_G=3\ \Omega$		11		ns
$t_r$	Turn-On Rise Time			13		
$t_{d(off)}$	Turn-Off Delay Time			34		
$t_f$	Turn-Off Fall Time			4		

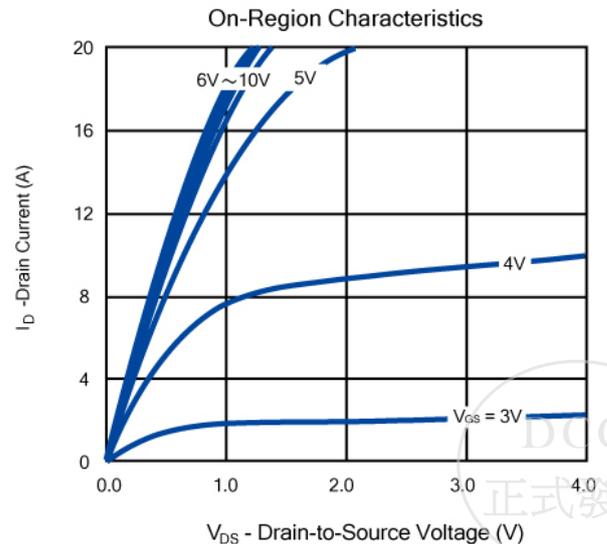
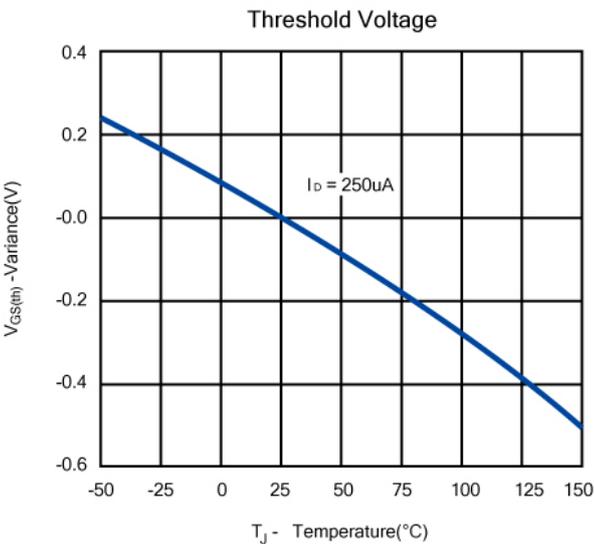
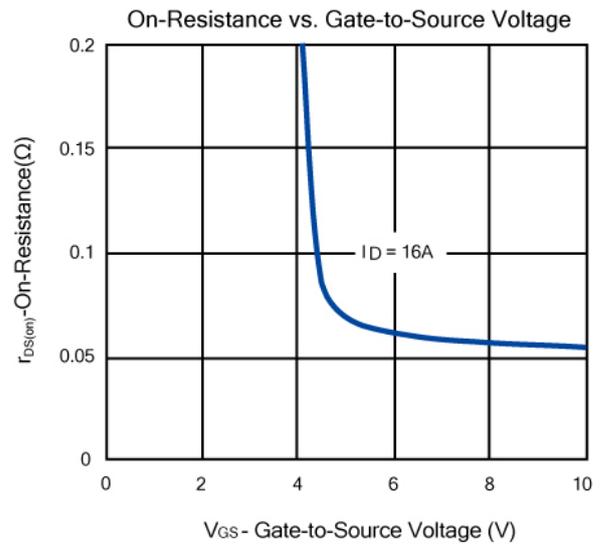
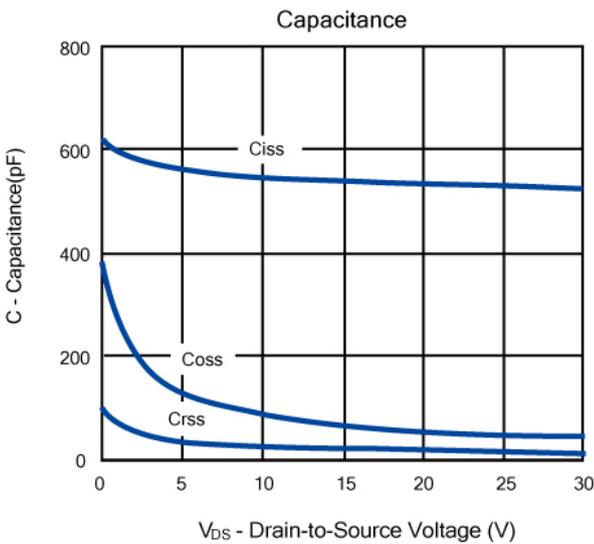
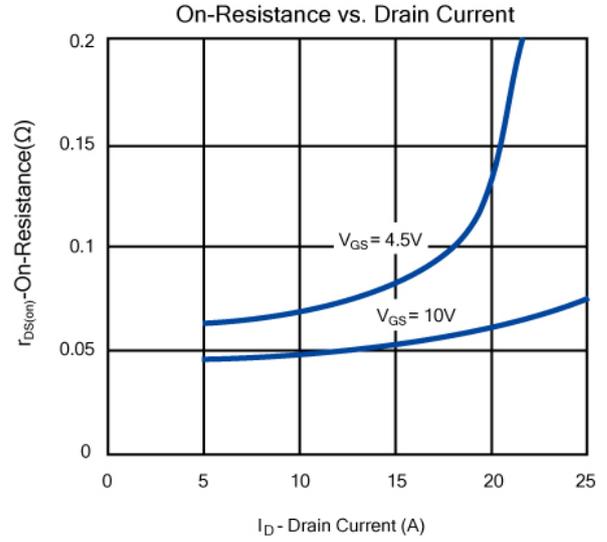
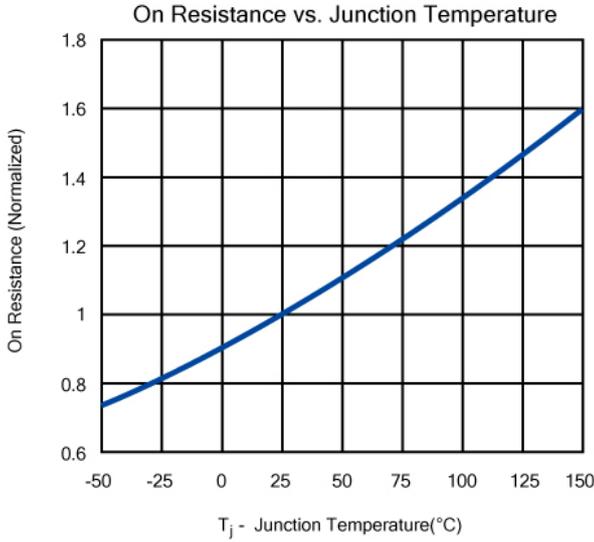
Notes: a. pulse test: pulse width  $\leq 300\ \mu s$ , duty cycle  $\leq 2\%$ , Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



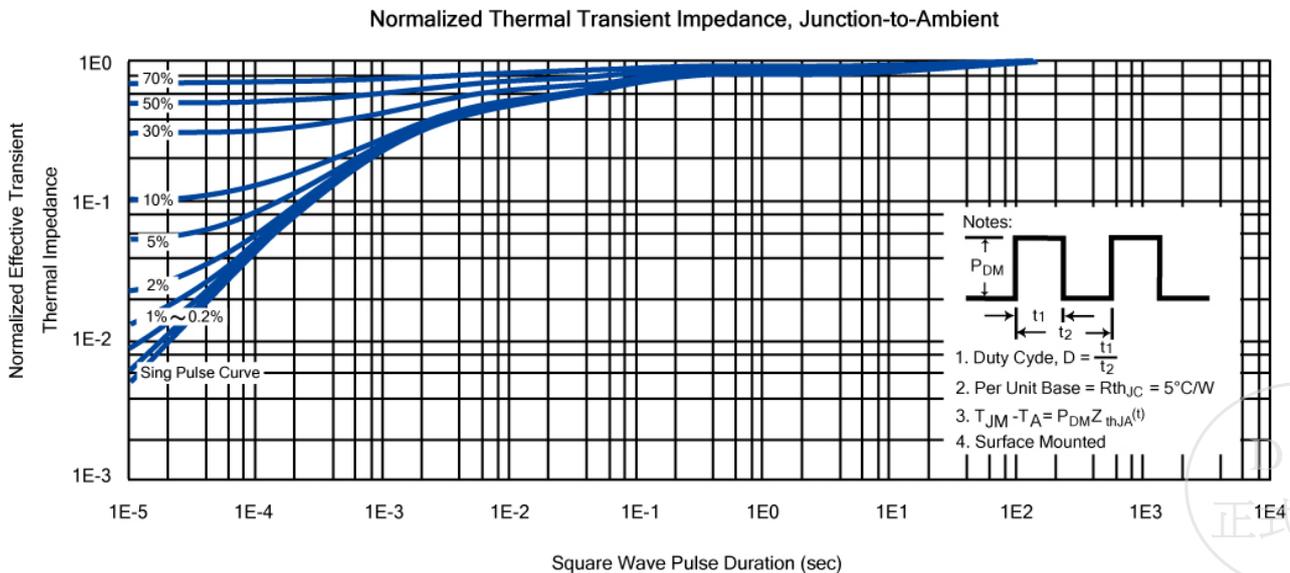
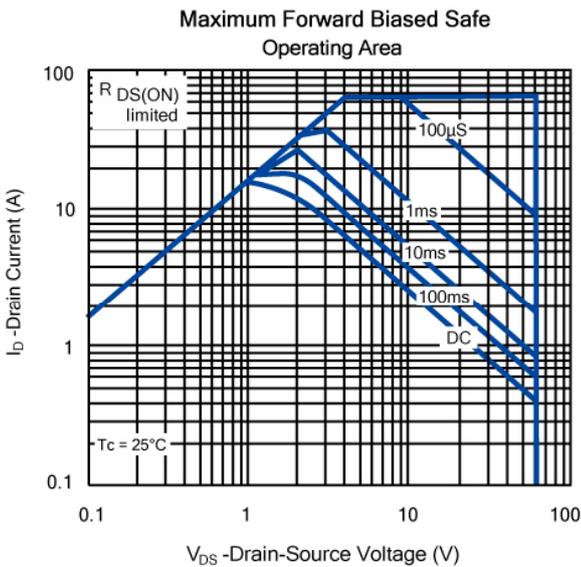
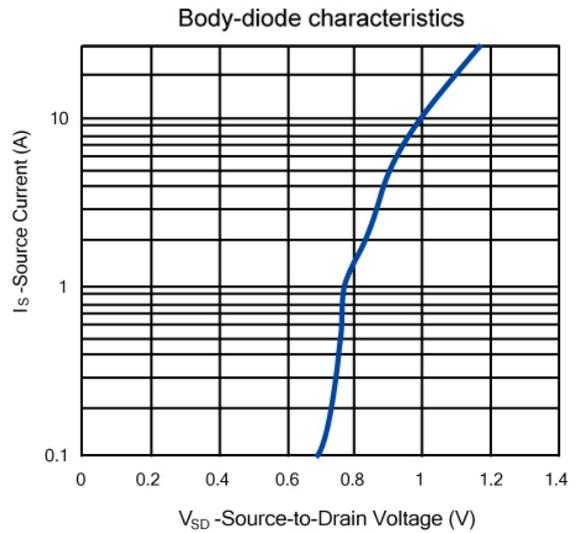
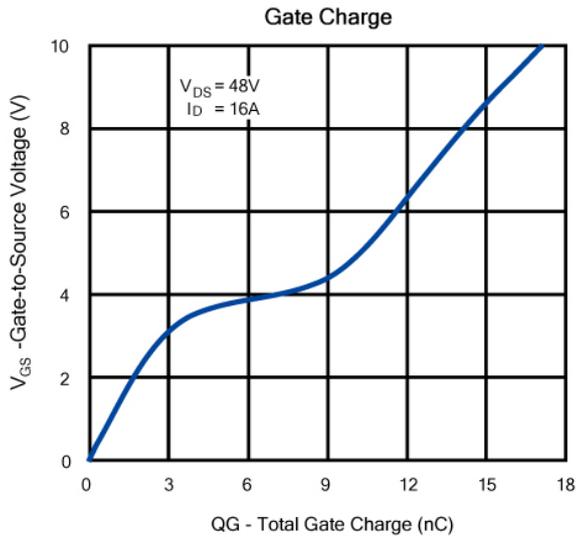
**N-Channel 60-V (D-S) MOSFET**

**Typical Characteristics (T<sub>J</sub> = 25°C Noted)**

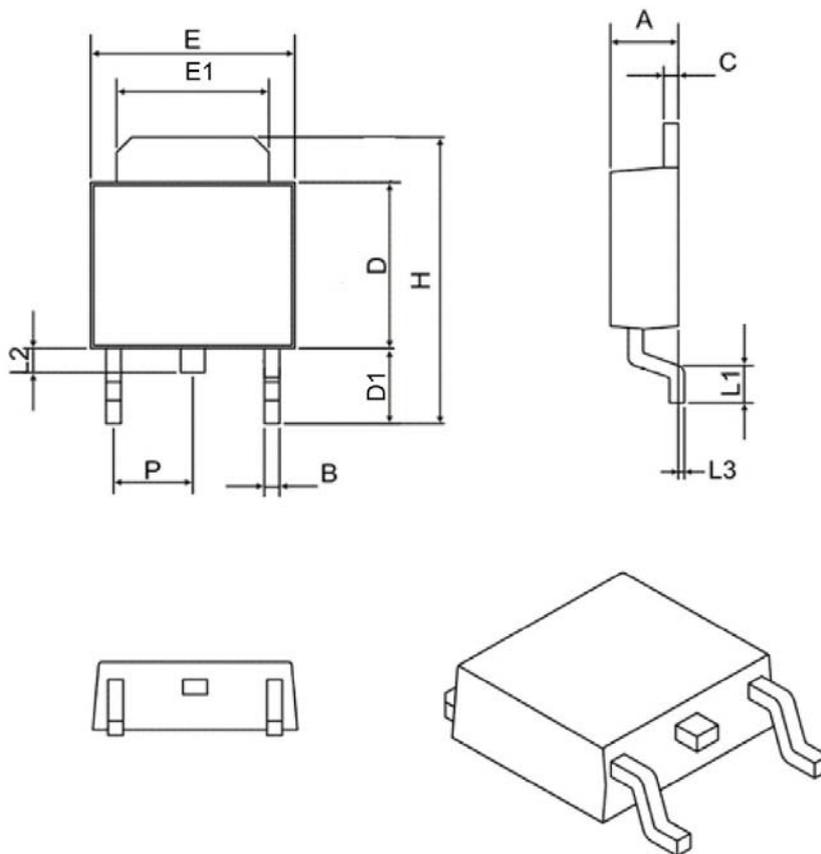


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**TO252-3L Package Outline**



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	

