

N and P- Channel 30-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4542 is the N and P Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

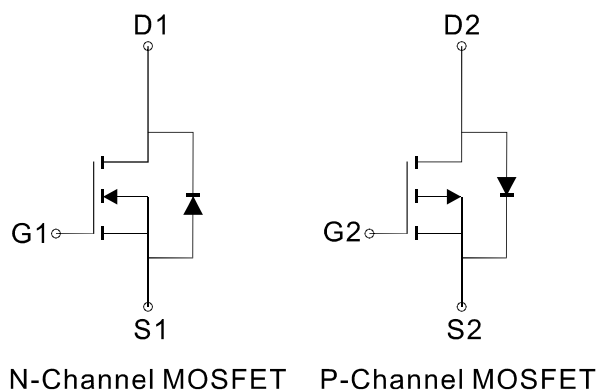
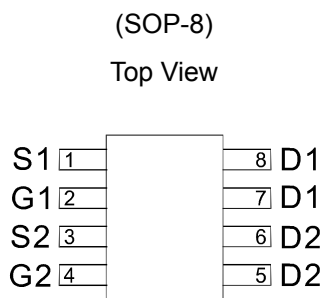
FEATURES

- R_{DS(ON)} 25mΩ@V_{GS}=10V (N-Ch)
- R_{DS(ON)} 40mΩ@V_{GS}=4.5V (N-Ch)
- R_{DS(ON)} 35mΩ@V_{GS}=-10V (P-Ch)
- R_{DS(ON)} 58mΩ@V_{GS}=-4.5V (P-Ch)
- Super high density cell design for extremely low R_{DS(ON)}
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter
- LCD Display inverter

PIN CONFIGURATION



Ordering Information: ME4542 (Pb-free)
ME4542-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25 Unless Otherwise Noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
		Maximum Ratings	Maximum Ratings	
Drain-Source Voltage	V _{DS}	30	-30	V
Gate-Source Voltage	V _{GS}	±20	±20	
Continuous Drain Current	I _D	T _A =25	-6	A
		T _A =70	-4.8	
Pulsed Drain Current	I _{DM}	28	-24	
Maximum Power Dissipation	P _D	T _A =25	2	W
		T _A =70	1.3	
Operating Junction Temperature	T _J	-55 to 150		
Thermal Resistance-Junction to Ambient *	R _{θJA}	62.5	62.5	/W

*The device mounted on 1in2 FR4 board with 2 oz copper

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Electrical Characteristics (TA=25 Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA V _{GS} =0V, I _D =-250 μA	N-Ch P-Ch	30 -30		V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA V _{DS} =V _{GS} , I _D =-250 μA	N-Ch P-Ch	1.0 -1.0	3.0 -3.0	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V	N-Ch P-Ch		±100 ±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V V _{DS} =-30V, V _{GS} =0V	N-Ch P-Ch		1 -1	μA
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D = 6.7A V _{GS} =-10V, I _D = -6.1A	N-Ch P-Ch	21 30	25 35	m
		V _{GS} =4.5V, I _D = 5.0A V _{GS} =-4.5V, I _D = -5.0A	N-Ch P-Ch	32 48	40 58	
V _{SD}	Diode Forward Voltage	I _S =1.7A, V _{GS} =0V I _S =-1.7A, V _{GS} =0V	N-Ch P-Ch	0.8 -0.8	1.2 -1.2	V
DYNAMIC						
Q _g	Total Gate Charge	N-Channel V _{DS} =15V, V _{GS} =10V, I _D =6.7A P-Channel V _{DS} =-15V, V _{GS} =-10V, I _D =-6.1A	N-Ch P-Ch	12 21		nC
Q _{gs}	Gate-Source Charge		N-Ch P-Ch	2 4		
Q _{gd}	Gate-Drain Charge		N-Ch P-Ch	2.5 6		
C _{iss}	Input Capacitance	N-Channel V _{DS} =15V, V _{GS} =0V, f=1MHz P-Channel V _{DS} =15V, V _{GS} =0V, f=1MHz	N-Ch P-Ch	360 840		pF
C _{oss}	Output Capacitance		N-Ch P-Ch	70 120		
C _{rss}	Reverse Transfer Capacitance		N-Ch P-Ch	17 32		
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	N-Ch P-Ch	0.5 5.5		
t _{d(on)}	Turn-On Delay Time	N-Channel V _{DD} =15V, R _L =15 I _D =1A, V _{GEN} =10V, R _G =6 P-Channel V _{DD} =-15V, R _L =15 I _D =-1A, V _{GEN} =-10V, R _G =6	N-Ch P-Ch	9.3 32		ns
t _r	Turn-On Rise Time		N-Ch P-Ch	14 13		
t _{d(off)}	Turn-Off Delay Time		N-Ch P-Ch	32 58		
t _f	Turn-Off Fall Time		N-Ch P-Ch	3.2 6.8		

Notes: a. Pulse test; pulse width 300us, duty cycle 2%

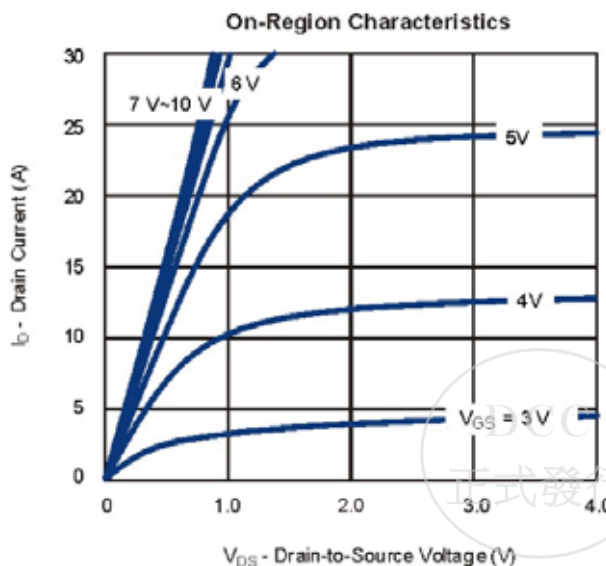
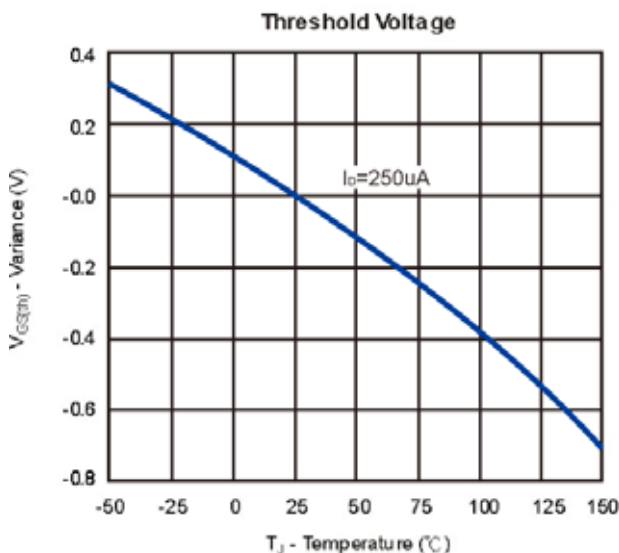
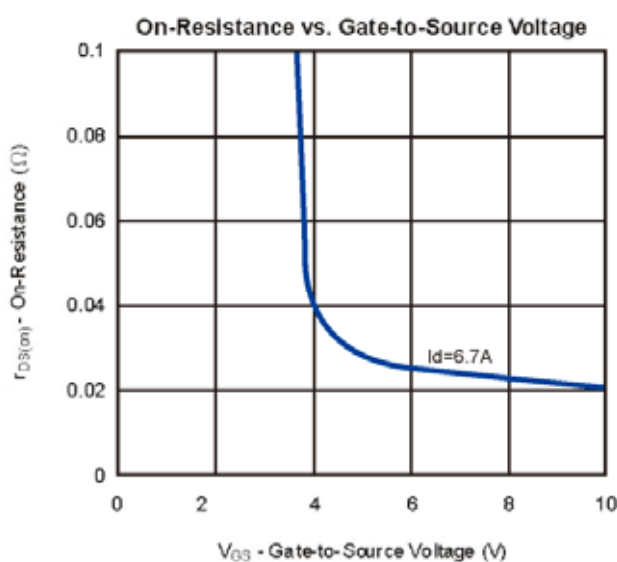
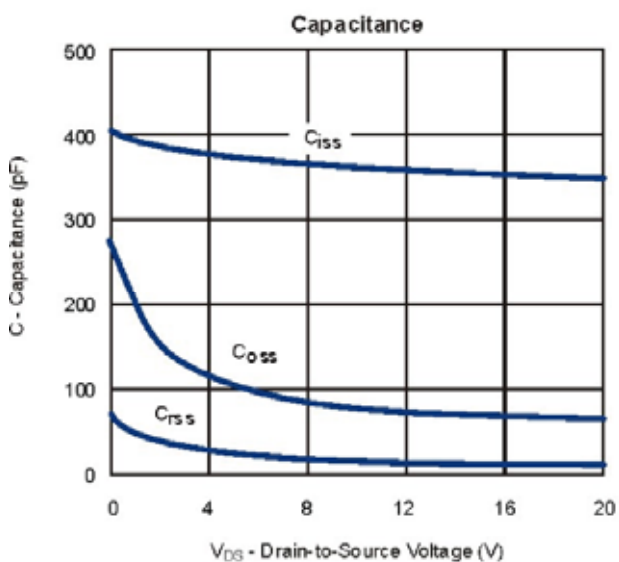
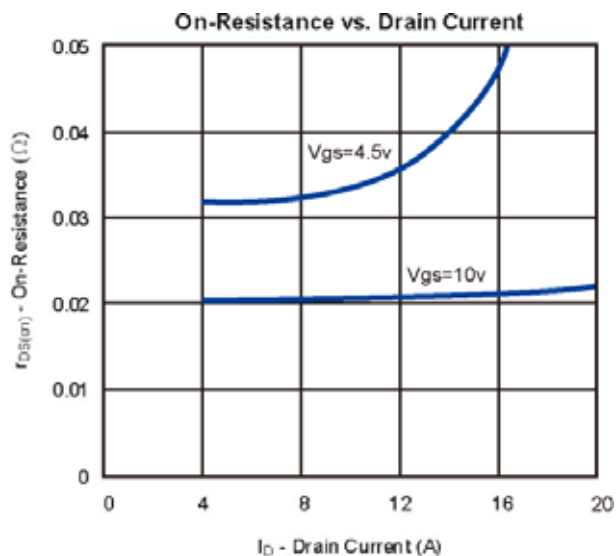
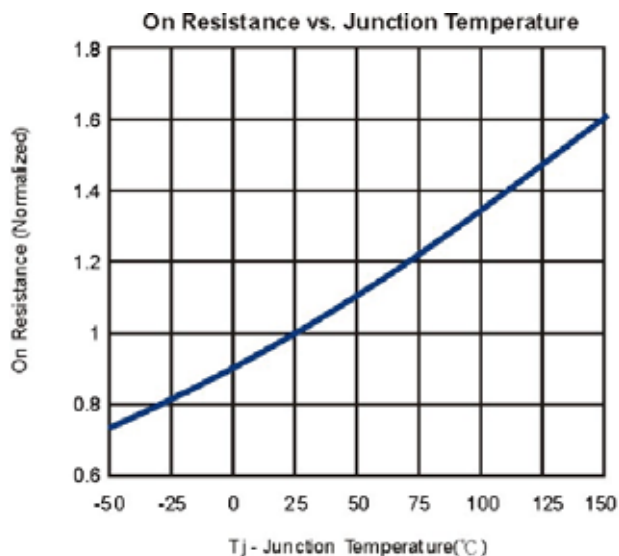
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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Typical Characteristics (T_J =25 Noted)

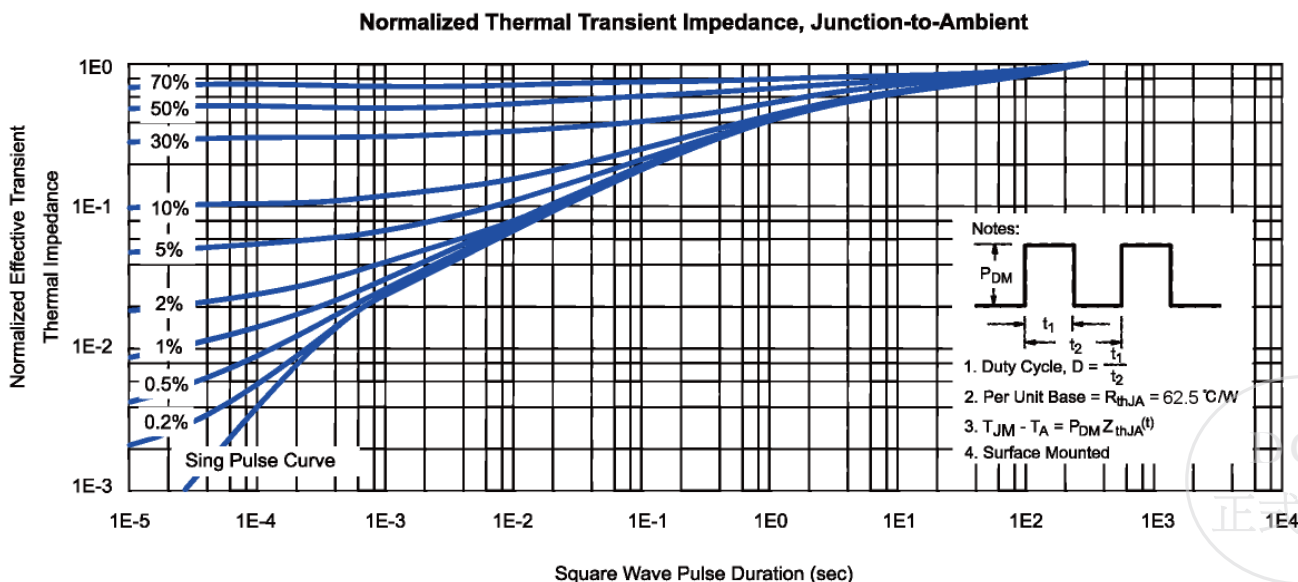
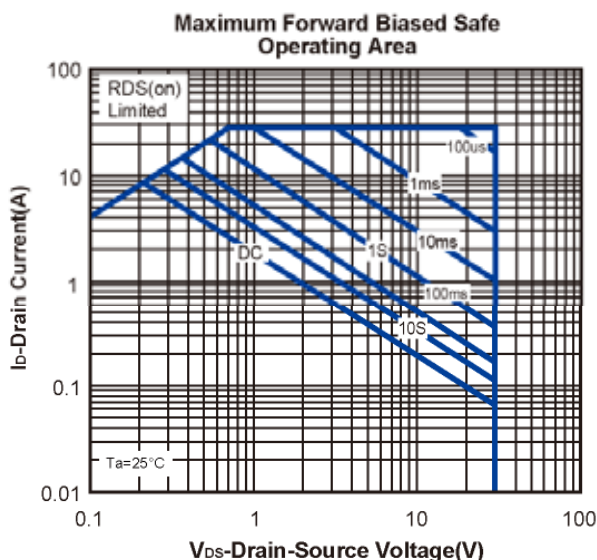
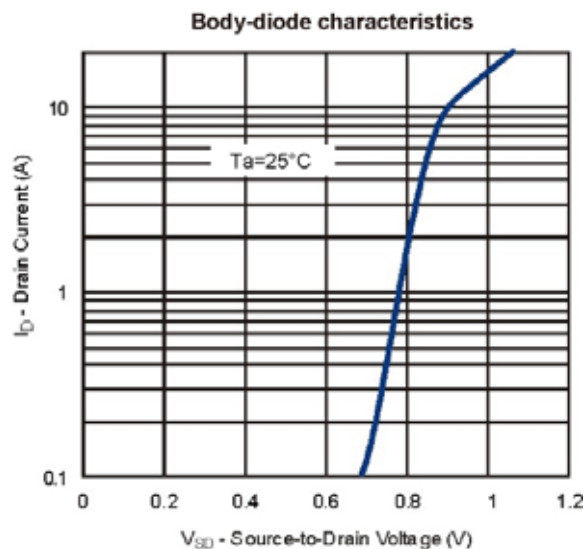
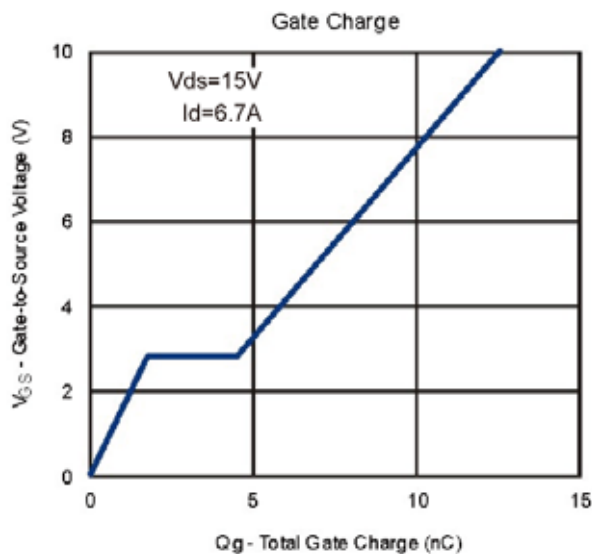
N-CHANNEL



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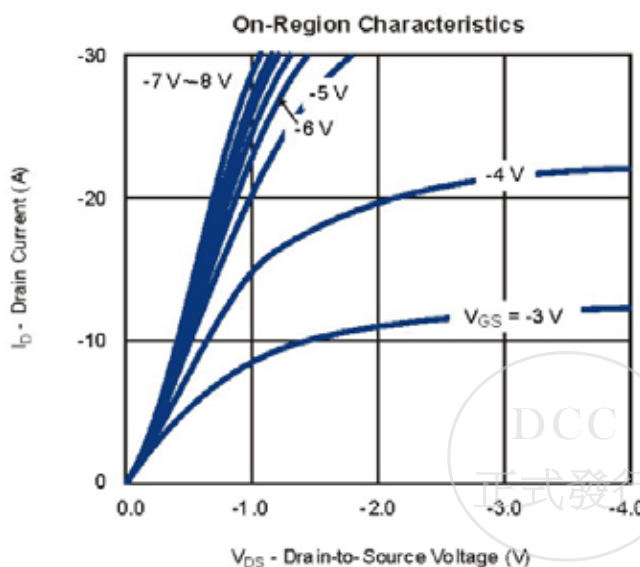
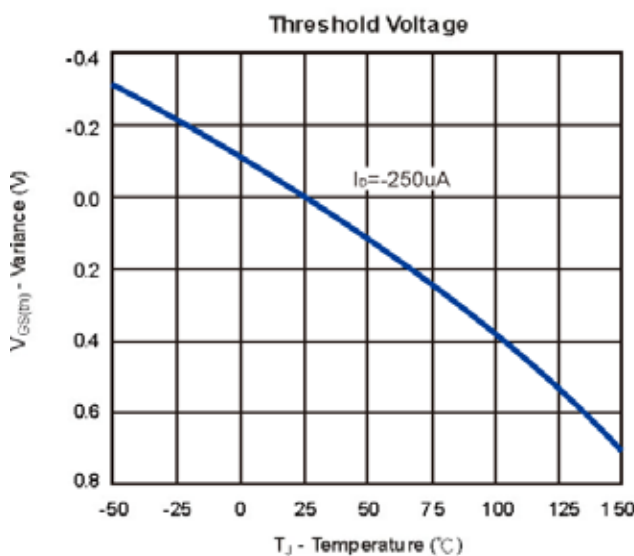
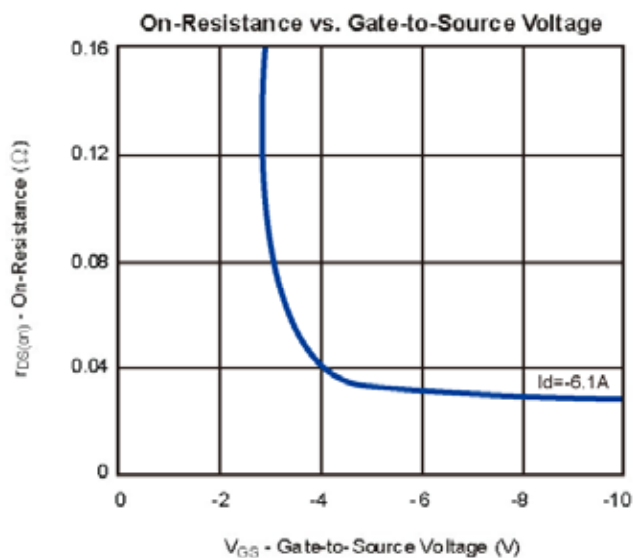
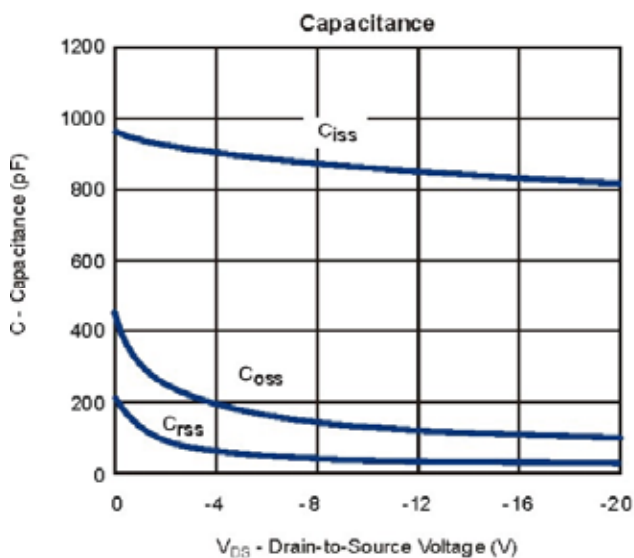
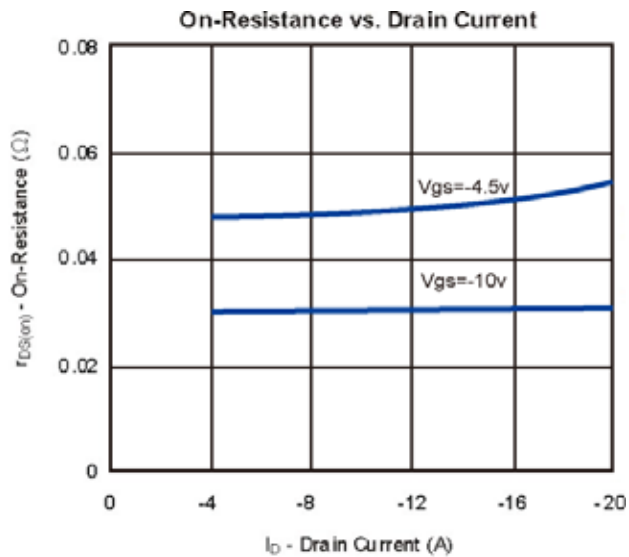
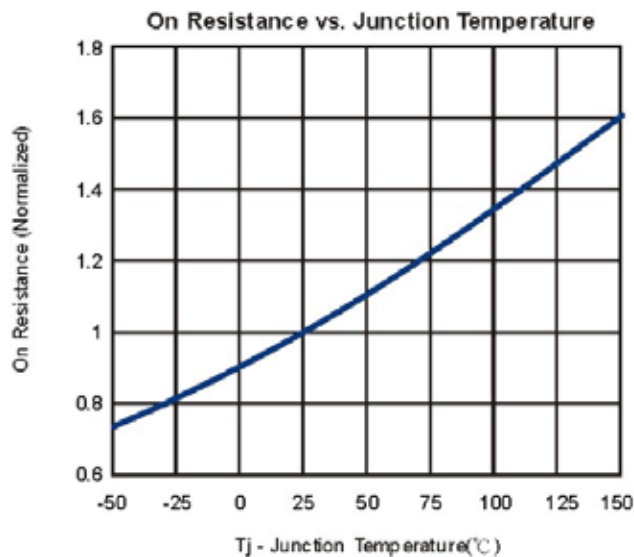
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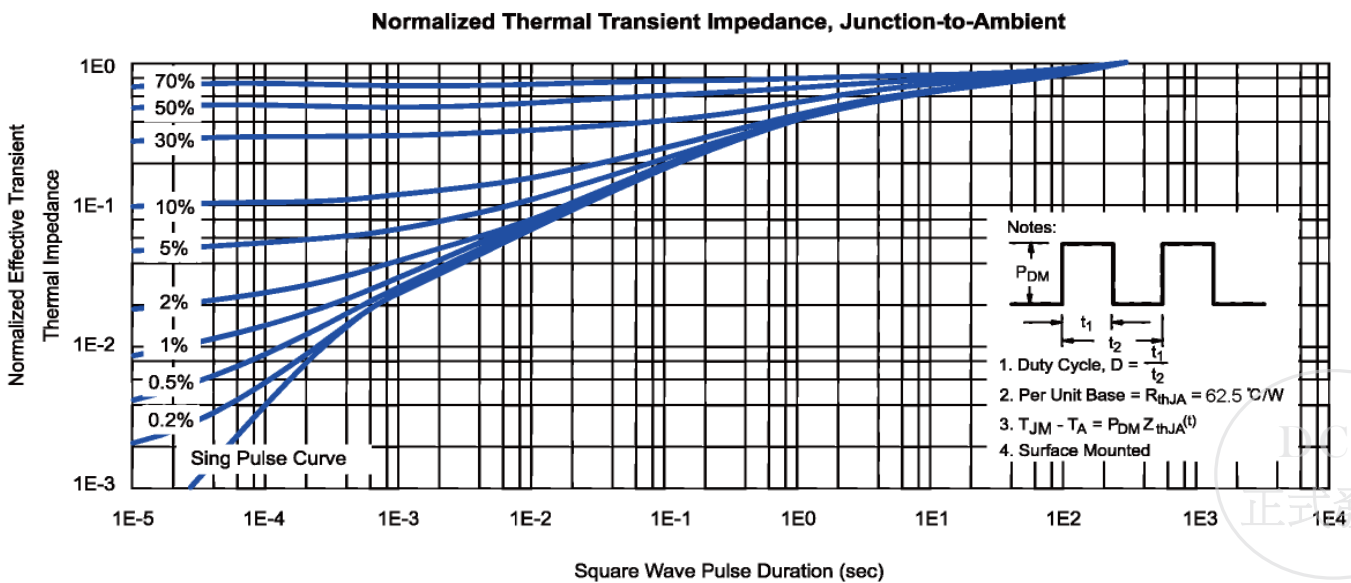
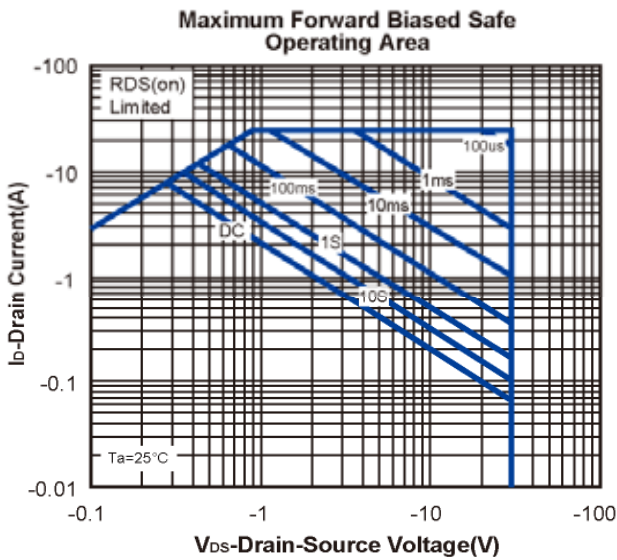
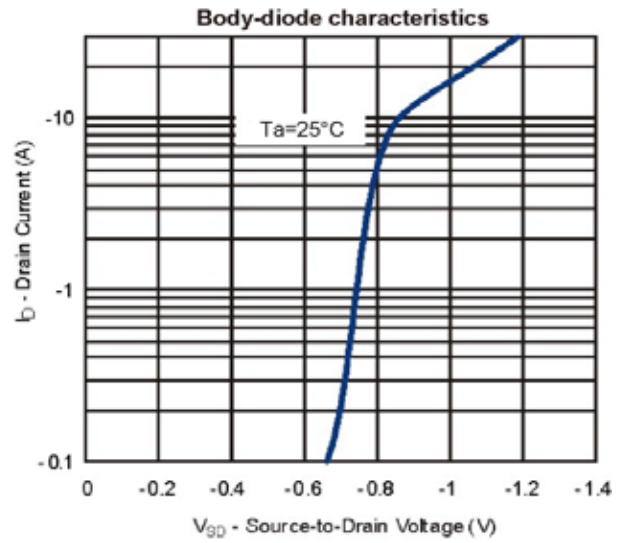
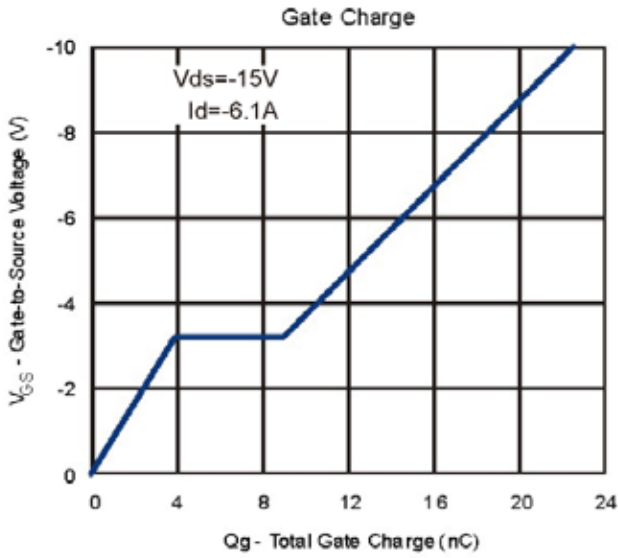
P-CHANNEL



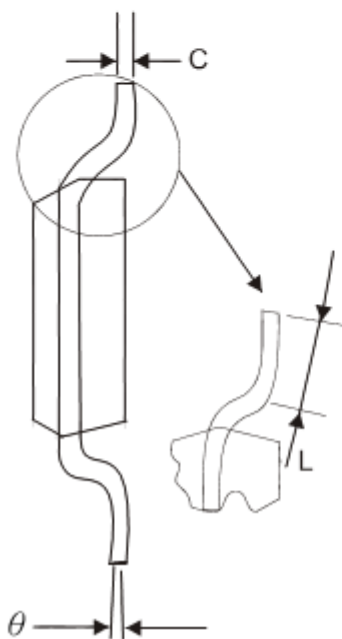
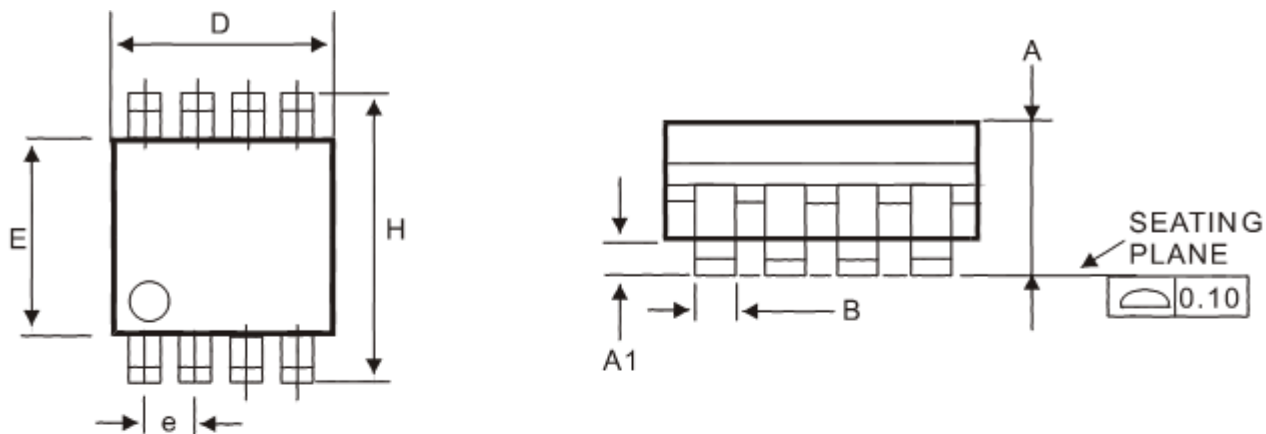
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Typical Characteristics (T_J =25 Noted)

P-CHANNEL



SOP-8 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

